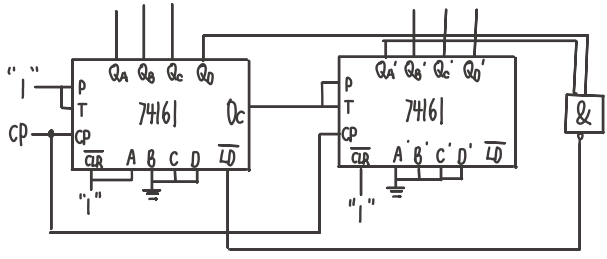
数字电子技术第九次作业

5.16 使用两片 74161 芯片级联，分别使用 $Q_D'\sim Q_A'$，$Q_D\sim Q_A$ 生成从高位到低位的二进制数

∴ $\overline{LD}=\overline{Q_A'Q_D}$，得电路图如下



5.17 解：容易发现该电路由两块同步置位的 74161 芯片串联而成，当代表高4位的 74161 芯片输出进位信号时两块芯片被同时置数

易得预置值应该为十进制数 256-M 的二进制原码表示

∴ M=100 时，$I_7\sim I_0$ 预置值为 $[156]_{10}=[10011100]_2$

M=200 时，$I_7\sim I_0$ 预置值为 $[56]_{10}=[00111000]_2$

当 $I_7\sim I_0$ = 01101000　　M = 256 - $[01101000]_2$ = 152

5.18 解：序列信号为 11010001011，故将 74161 改造为模10计数器，$Q_D\sim Q_A$=1001，同步预置信号激活多路选择器使用 CC4512 芯片

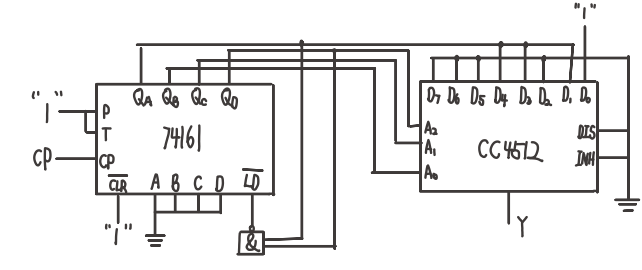
电路状态表如下

Q_D	Q_C	Q_B	Q_A	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1

→ ∴ 令 $A_2=Q_D$　$A_1=Q_C$　$A_0=Q_B$　$\overline{LD}=\overline{Q_AQ_D}$

∴ $D_0=1$　$D_2=0$　$D_1=D_3=D_4=Q_A$　$D_5=D_6=D_7=0$

给出如下电路图

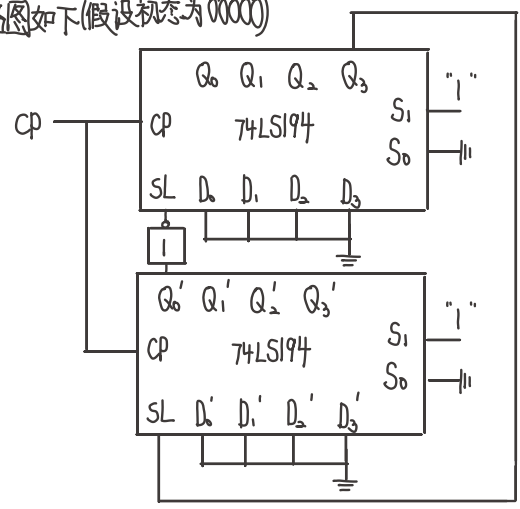


5.19 解 使用2片74LS194芯片级联实现模10位移计数器(生成格雷码)

使 Q_0' 和 $Q_3 \sim Q_0$ 作为计数输出端，数码映射如下

状态	$Q_0'Q_3Q_2Q_1Q_0$ 位表示
0	0 0 0 0 0
1	0 0 0 0 1
2	0 0 0 1 1
3	0 0 1 1 1
4	0 1 1 1 1
5	1 1 1 1 1
6	1 1 1 1 0
7	1 1 1 0 0
8	1 1 0 0 0
9	1 0 0 0 0

电路图如下(假设初态为00000)



(1-8)

5.20 解 使74161芯片构建8计数器和CC4512数据选择器生成序列码

状态表如下

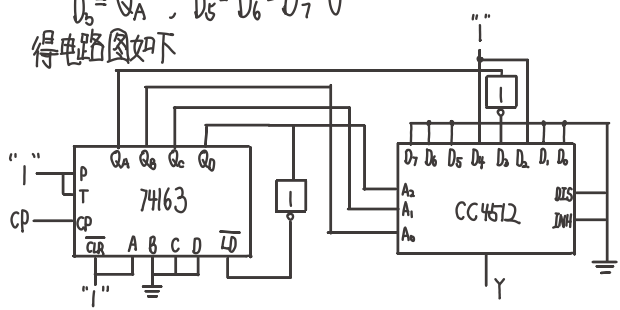
Q_D	Q_C	Q_B	Q_A	Y
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1

$\therefore$ 令 $A_2=Q_D$，$A_1=Q_C$，$A_0=Q_B$

$\therefore D_0=D_1=0$，$D_2=D_4=1$，$\overline{LD}=\overline{Q_D}$

$D_3=\overline{Q_A}$，$D_5=D_6=D_7=0$

得电路图如下



5.21 解：容易得到电路图需要4个JK触发器 Q_3-Q_0 代表BCD码的四位

状态转移表如下

Q_3^n	Q_2^n	Q_1^n	Q_0^n	Q_3^{n+1}	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	1	1	1	1
1	1	1	1	无	无	无	无

用卡诺图化简得

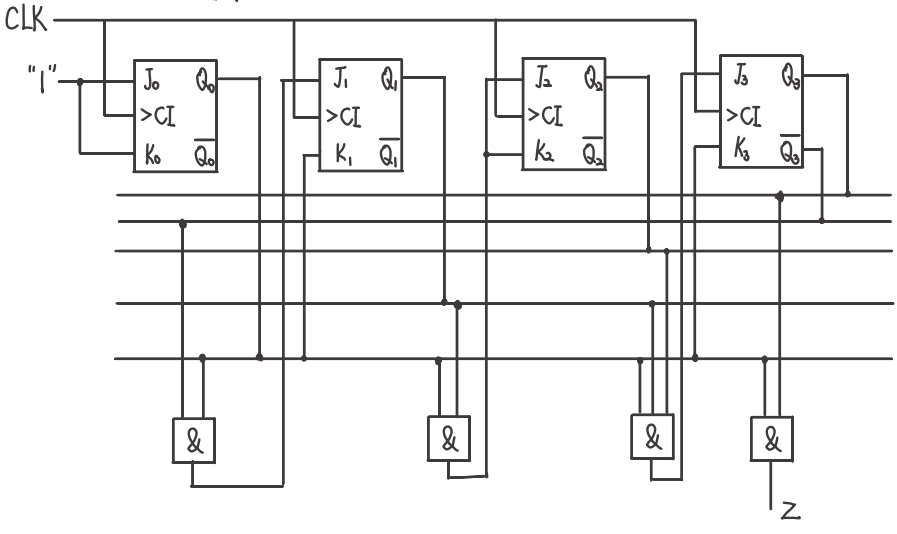
$Q_3^{n+1} = Q_3^n\overline{Q_2^n} + \overline{Q_3^n}Q_2^nQ_1^nQ_0^n$，故 $J_3 = Q_2^nQ_1^nQ_0^n$，$K_3 = Q_0^n$

$Q_2^{n+1} = \overline{Q_2^n}\,Q_1^nQ_0^n + Q_2^n(\overline{Q_1^n} + \overline{Q_0^n})$，故 $J_2 = Q_1^nQ_0^n$，$K_2 = Q_1^nQ_0^n$

$Q_1^{n+1} = \overline{Q_1^n}\,\overline{Q_3^n}\,Q_0^n + Q_1^n\overline{Q_0^n}$，故 $J_1 = \overline{Q_3^n}Q_0^n$，$K_1 = Q_0^n$

$Q_0^{n+1} = \overline{Q_0^n}$，故 $J_0 = 1$　$K_0 = 1$　　$Z = Q_3^nQ_0^n$（进位标志）

电路图如下



5.22 解：其原始状态表如下

S^{n+1}/Z^n / S^n	X	0	1
S0		S0/0	S1/0
S1		S2/0	S3/0
S2		S4/0	S5/1
S3		S6/1	S7/0
S4		S8/0	S9/0
S5		SA/0	SB/0
S6		SC/0	SD/1
S7		SE/0	SF/0

续

S^{n+1}/Z^n / S^n	X	0	1
S8		S0/0	S1/0
S9		S2/0	S3/0
SA		S4/0	S5/1
SB		S6/1	S7/0
SC		S8/0	S9/0
SD		SA/0	SB/0
SE		SC/1	SD/1
SF		SE/0	SF/0

5.23 (a) 作隐含表如下

B	X						
C	X	X					
D	X	X	X				
E	X	X	X	✓			
F	✓	X	X	X	X		
G	X	X	✓	X	X	X	
H	X	✓	X	X	X	X	X
I	X	X	X	X	X	X	X	X
	A	B	C	D	E	F	G	H

(b) 作隐含表如下

B	X						
C	X	✓					
D	X	X	X				
E	X	X	X	X			
F	✓	X	X	X	X		
G	X	X	X	X	X	X	
H	X	✓	✓	X	X	X	X
	A	B	C	D	E	F	G

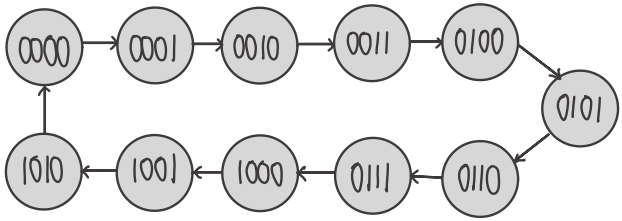
简化后状态表

	0	1
A	A/0	C/1
B	B/1	C/0
C	B/0	A/0
D	C/1	D/0
I	B/0	D/0

简化后状态表

	00	01	10	11
A	D/0	D/0	A/0	A/0
B	B/1	D/0	A/0	E/1
D	D/0	B/0	A/0	E/1
E	B/1	A/0	A/0	E/1
G	G/0	G/0	A/0	A/0

5.25 解 易得至少需要4个触发器，状态图如下



状态表如下

Q_3^n	Q_2^n	Q_1^n	Q_0^n	Q_3^{n+1}	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	0
1	0	1	0	0	0	0	0

续表

$$D_0 = \overline{Q_1^n}\,\overline{Q_0^n} + \overline{Q_3^n}\,\overline{Q_0^n} \qquad Z = Q_3^n Q_1^n \text{（进位输出）}$$

$$D_1 = \overline{Q_1^n} Q_0^n + \overline{Q_3^n} Q_1^n \overline{Q_0^n}$$

$$D_2 = Q_2^n\overline{Q_1^n} + \overline{Q_2^n} Q_1^n Q_0^n + Q_2^n\overline{Q_0^n}$$

$$D_3 = Q_3^n\overline{Q_1^n} + Q_2^n Q_1^n Q_0^n$$