# 数字电子技术第8次作业

55解 $J_1 = X \cdot \overline{Q_2^n}$　$K_1 = X \cdot Q_2^n$　$J_2 = \overline{X}\, Q_1^n$　$K_2 = \overline{X}\, \overline{Q_1^n}$

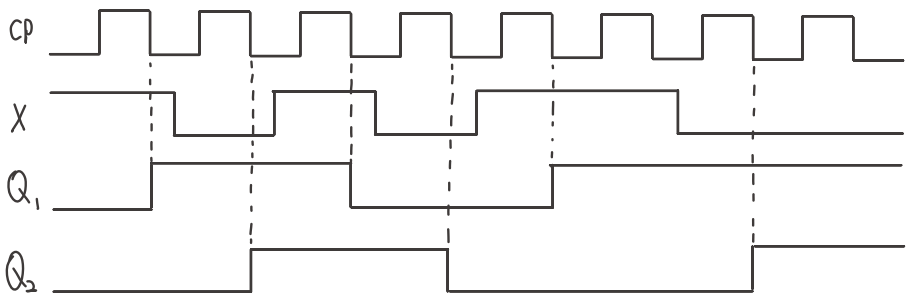
状态方程 $Q_1^{n+1} = X\,\overline{Q_2^n}\cdot\overline{Q_1^n} + \overline{X\,Q_2^n}\,Q_1^n = X\,\overline{Q_1^n}\,\overline{Q_2^n} + \overline{X}\,Q_1^n + \overline{Q_2^n}\,Q_1^n = \overline{X}\,Q_1^n + X\,\overline{Q_2^n}$

$Q_2^{n+1} = \overline{X}\,Q_1^n \cdot \overline{Q_2^n} + \overline{X}\,\overline{Q_1^n}\,Q_2^n = \overline{X}\,Q_1^n\,\overline{Q_2^n} + X\,Q_2^n + Q_1^n\,Q_2^n = X\,Q_2^n + \overline{X}\,Q_1^n$

状态转换表

| X | $Q_1^n$ | $Q_2^n$ | $Q_1^{n+1}$ | $Q_2^{n+1}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 |

时钟下降沿进行更新




56解 控制函数 $J_1 = \overline{Q_3^n}$　$K_1 = 1$　$J_2 = K_2 = Q_1^n$　$J_3 = Q_1^n\,Q_2^n$　$K_3 = 1$

输出函数 $Q_i^{n+1} = J_i\overline{Q_i^n} + \overline{K_i}\,Q_i^n$　$(i = 1, 2, 3)$　$C = Q_3^n$

∴ 得状态方程 $Q_1^{n+1} = \overline{Q_3^n}\cdot\overline{Q_1^n}$

$Q_2^{n+1} = Q_1^n\,\overline{Q_2^n} + \overline{Q_1^n}\,Q_2^n = Q_1^n \oplus Q_2^n$

$Q_3^{n+1} = Q_1^n\,Q_2^n\,\overline{Q_3^n}$

状态转移表如右：

| $Q_2^n$ | $Q_1^n$ | $Q_0^n$ | $Q_2^{n+1}$ | $Q_1^{n+1}$ | $Q_0^{n+1}$ | C |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |

易得电路为5进制转换器

57解 已知控制函数 $D_0 = Q_0 + \overline{X}Y\overline{Q_1}$

$D_1 = Q_1 + X\overline{YQ_0}$

输出函数 $L = Q_0^n$ ， $G = Q_1^n$ $E = \overline{Q_1^n + Q_0^n}$

状态方程 $Q_0^{n+1} = Q_0^n + \overline{X}Y\overline{Q_1^n}$

$Q_1^{n+1} = Q_1^n + X\overline{YQ_0^n}$

$X=1$ $Y=0$

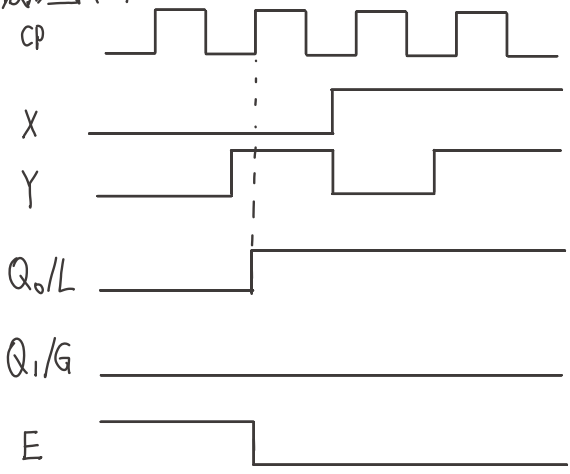
$Q_0^{n+1} = Q_0^n$

$Q_1^{n+1} = Q_1^n + \overline{Q_0^n}$

状态转换表如下

| X | Y | $Q_1^n$ | $Q_0^n$ | $Q_1^{n+1}$ | $Q_0^{n+1}$ | G | L | E |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

波形图如下




58解. 时钟方程 $CP_0 = CP_2 = CP$　　$CP_1 = Q_1$

控制方程 $J_1 = \overline{Q_3^n}$　　$J_2 = 1$　　$J_3 = Q_1^n Q_2^n$

$K_1 = 1$　　$K_2 = 1$　　$K_3 = 1$

∴状态方程为 $Q_1^{n+1} = J_1\overline{Q_1^n} + \overline{K_1}Q_1^n = \overline{Q_1^n}\cdot\overline{Q_3^n}$

$Q_2^{n+1} = J_2\overline{Q_2^n} + \overline{K_2}\cdot Q_2^n = \overline{Q_2^n}$

$Q_3^{n+1} = J_3\overline{Q_3^n} + \overline{K_3}\cdot Q_3^n = Q_1^n Q_2^n \overline{Q_3^n}$

状态转移真值表为

| $Q_3^n$ | $Q_2^n$ | $Q_1^n$ | $Q_3^{n+1}$ | $Q_2^{n+1}$ | $Q_1^{n+1}$ | $CP_3$ | $CP_2$ | $CP_1$ |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | ↓ | ↑ | ↓ |
| 0 | 0 | 1 | 0 | 1 | 0 | ↓ | ↓ | ↓ |
| 0 | 1 | 0 | 0 | 1 | 1 | ↓ | ↑ | ↓ |
| 0 | 1 | 1 | 1 | 0 | 0 | ↓ | ↓ | ↓ |
| 1 | 0 | 0 | 0 | 0 | 0 | ↓ | 0 | ↓ |
| 1 | 0 | 1 | 0 | 1 | 0 | ↓ | ↓ | ↓ |
| 1 | 1 | 0 | 0 | 1 | 0 | ↓ | 0 | ↓ |
| 1 | 1 | 1 | 0 | 0 | 0 | ↓ | ↓ | ↓ |

容易发现电路功能为异步五进制递增计数器，且有自启动能力

5.9 解 时钟方程 $CP_0 = CP$ $CP_1 = \overline{\overline{Q_0} \cdot \overline{Q_1 Q_2 CP}} = Q_0 + \overline{Q_1} + \overline{Q_2} + \overline{CP}$ $CP_2 = Q_1$

控制方程 $J_0 = \overline{Q_1^n Q_2^n}$ $K_0 = K_1 = K_2 = J_1 = J_2 = 1$

∴状态方程 $Q_0^{n+1} = J_0 \overline{Q_0^n} + \overline{K_0} Q_0^n = \overline{Q_2^n}\,\overline{Q_0^n} + \overline{Q_1^n}\,\overline{Q_0^n}$

$Q_1^{n+1} = J_1 \overline{Q_1^n} + \overline{K_1} \overline{Q_1^n} = \overline{Q_1^n}$ $Q_2^{n+1} = \overline{Q_2^n}$

| $Q_0$ \ $Q_2Q_1$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | 1 | | 1 |
| 1 | | | 1 | |

状态转移真值表

| $Q_2^n$ | $Q_1^n$ | $Q_0^n$ | $Q_2^{n+1}$ | $Q_1^{n+1}$ | $Q_0^{n+1}$ | $CP_2$ | $CP_1$ | $CP_0$ |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | ↑ | ↓ |
| 0 | 0 | 1 | 0 | 1 | 0 | ↑ | ↓ | ↓ |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | ↑ | ↓ |
| 0 | 1 | 1 | 1 | 0 | 0 | ↓ | ↓ | ↓ |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | ↑ | ↓ |
| 1 | 0 | 1 | 1 | 1 | 0 | ↑ | ↓ | ↓ |
| 1 | 1 | 0 | 0 | 0 | 0 | ↓ | ↓ | ↓ |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | ↑ | ↓ |

容易发现电路为 7 进制递增计数器，且有自启动功能

5.10 解 时钟方程 $CP_0 = CP_2 = CP$ $CP_1 = \overline{Q_0}$

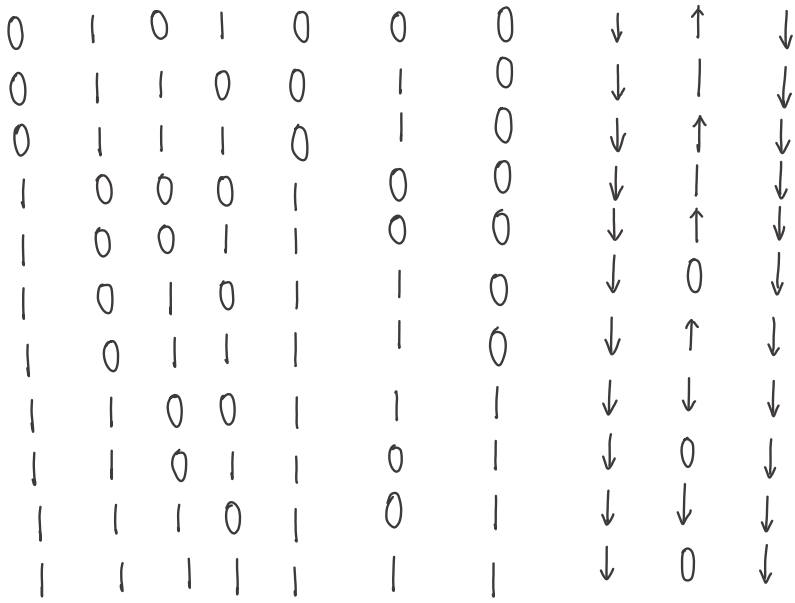
控制方程 $D_0 = A Q_2^n$ $D_1 = \overline{Q_1^n}$ $D_2^n = A + \overline{Q_2^n}$

∴状态方程 $Q_0^{n+1} = A Q_2^n$ $Q_2^{n+1} = A + \overline{Q_2^n}$

$Q_1^{n+1} = \overline{Q_1^n}$

状态转移真值表

| A | $Q_2^n$ | $Q_1^n$ | $Q_0^n$ | $Q_2^{n+1}$ | $Q_1^{n+1}$ | $Q_0^{n+1}$ | $CP_2$ | $CP_1$ | $CP_0$ |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | ↓ | ↓ | ↓ |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | ↓ | ↑ | ↓ |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | ↓ | ↓ | ↓ |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | ↓ | ↑ | ↓ |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | ↓ | ↓ | ↓ |



状态转换表

| $Q_2^nQ_1^nQ_0^n$ / $Q_2^{n+1}Q_1^{n+1}Q_0^{n+1}$ A | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
|---|---|---|---|---|---|---|---|---|
| 0 | 100 | 100 | 110 | 110 | 000 | 000 | 010 | 010 |
| 1 | 100 | 100 | 110 | 110 | 111 | 101 | 101 | 111 |

5.11 解 已知 74163 是同步清零同步置数的四位二进制计数器

取 $Q_2 \sim Q_0$ 为电路中状态码乘载位，$S_0 \sim S_6$ 状态分别对应 $Q_2 \sim Q_0$ 构成的 3 位二进制数 0~6 的位表示，容易发现当且仅当 $X_1^n = X_0^n = 0$ 且状态为 $S_0, S_3, S_6$ 时输出为 0

$\therefore Z = X_1 + X_0 + \overline{Q_2}\overline{Q_1}\overline{Q_0} + \overline{Q_2}Q_1\overline{Q_0} + Q_2\overline{Q_1}\overline{Q_0}$ 使用置数端和 $Q_2 \sim Q_0$ 控制芯片进行输出

($\overline{LD}$ 低电平进行置数
$\overline{LD}$ 高电平计数器 +1)

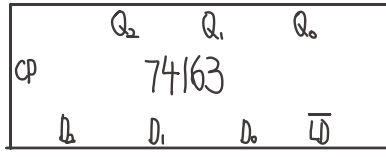
| $D_2D_1D_0/\overline{LD}$ / $Q_2^nQ_1^nQ_0^n$ | $X_1X_0$ 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 0 0 | 000/0 | 100/0 | Φ | Φ/1 |
| 0 0 1 | Φ/1 | Φ | Φ | 001/0 |
| 0 1 1 | 000/0 | 011/0 | Φ | Φ |
| 0 1 0 | 010/0 | Φ/1 | Φ | Φ |

| | | | | |
|---|---|---|---|---|
| 1 1 0 | 000/0 | Φ/1 | Φ | 110/0 |
| 1 1 1 | Φ | Φ | Φ | Φ |
| 1 0 1 | 101/0 | Φ/1 | Φ | Φ/1 |
| 1 0 0 | Φ/1 | 100/0 | Φ | Φ |

$\overline{LD} = Q_2^n \overline{Q_1^n} \overline{Q_0^n} X_0 + \overline{Q_1^n} \overline{Q_0^n} X_1 + \overline{Q_2^n} Q_1^n Q_0^n \overline{X_1} + Q_2^n \overline{Q_1^n} X_1$

$D_2 = Q_2^n \overline{Q_1^n} + Q_2^n X_1 + \overline{Q_1^n} X_0 \quad D_1 = \overline{Q_2^n} Q_1^n \overline{Q_0^n} + Q_1^n X_0 + Q_1^n X_1$

$D_0 = Q_2^n \overline{Q_1^n} Q_0^n + Q_0^n X_1 + Q_0^n X_0 \quad D_3 = 0$




(74163芯片要使用的引脚一览)

按照上述逻辑表达式连接电路即可，电路详图由于逻辑表达式过于冗长略去

5.12 解：引脚作用 ENP：高电平下可计数 ENT 高电平下可计数 CO：进位输出

$\overline{CLR}$ 低电平下清零 $\overline{LD}$：低电平下进入置数模式

假设两芯片状态输出的进制数均为0

图片使用两片74161芯片进行级联

对于每一片芯片 $Q_C - Q_A$ 的输出构成四进制计数器，$Q_D$的输出为一个二进制计数器，当 $Q_C \sim Q_A$ 输0x4时自动激活 $\overline{LD}$ 引脚反转 $Q_D$ 并将 $Q_C \sim Q_A$ 重新置零，因此二者又级联形成一个八进制计数器

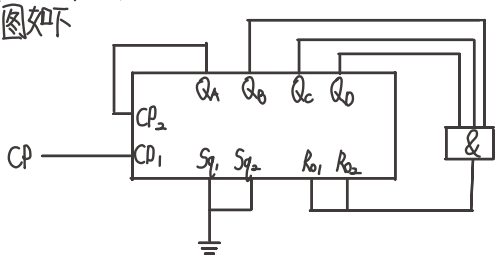
两片芯片本身又进行级联，当低位芯片输出 QxC 后会激活高位芯片的ENP引脚，使其开始计数并+1，之后低端芯片又被置为初态。

两块芯片级联构成一个64进制计数器

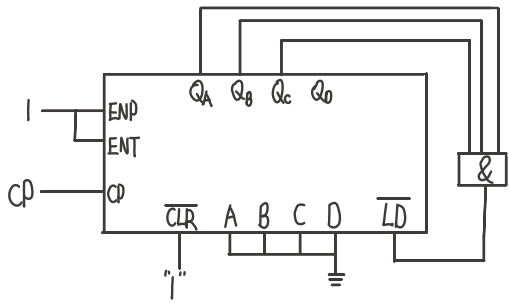
(输出引脚为$Q_A$) (输出引脚为$Q_D$)

5.13解：74LS90是二/五进制计数器，因此我们首先将其二进制计数器和五进制计数器级联，得到十进制计数器，每次输出的位表示为0111时进行清零

电路简图如下




5.14解：基本思路和5-13一致，区别是74161芯片本身是四位的，因此不用做扩展




5.15解：使用两片74LS90芯片级联得到100进制计数器，然后当计数达到40时置零