Half-Duplex Amplifier Network

USRP Interface

J1
0732511153
PA
PA.SchDoc
RF_IN
RF_OUT
GND

J2
0732511153
LNA
LNA.SchDoc
RF_OUT
RF_IN
GND

TX/RX Switch
Switch.SchDoc
RF1
RF2
SW_CTRL
RFC
N1
ArrayFeed

SPI Test Points

SCK TP6 5000
MOSI TP8 5000
MISO TP10 5000
TP12 5000
GND
CS1 TP7 5000
CS2 TP9 5000
CS3 TP11 5000
CS4 TP13 5000

Phase Shifters

Phaseshift11
PhaseShifterA.SchDoc
Phaseshift12
PhaseShifterB.SchDoc
Phaseshift21
PhaseShifterA.SchDoc
Phaseshift22
PhaseShifterB.SchDoc
RF_IN
RF_OUT
SCK
MOSI
MISO
CS1
CS2
CS3
CS4
SCK/CLK
MOSI/SER_IN
MISO/SER_OUT
CS/LE

Antennas

ANT1
ANT2
ANT3
ANT4
ArrayPatch

MH1 4-40 Mounting Hole
MH2 4-40 Mounting Hole
MH3 4-40 Mounting Hole
MH4 4-40 Mounting Hole

RX/TX Swtich

5V
R1 10k
R4 22k
SW2
SW1
R2 0
R3 0
R10 R
CL-SB-12C-01
CL-SB-12C-01
J3
1881558
D4
APG1005CGC-T
Green
GND

USRP breakout has no documentation. Generic 2pin header for signal.

3.4V high signal, 0V low signal

RPi Header

J4
Adafruit_1993
MOSI
MISO
SCK
CS1
CS2
CS3
CS4
GND

Power Connectors

J5
1881561
5V
C19 0805 1uF
C20 100nF
GND

J6
1881561
5VP_PS
5VN_PS
C1 0805 1uF
C2 100nF
C3 0805 1uF
C4 100nF

5V and 5VP_PS are tied to the same external power supply

Power Test Points

5VP_PS TP14 5000
5VN_PS TP16 5000
TP18 5000
5V TP15 5000
TP17 5000
GND

Power LEDs

5V R7 150 D1 APG1005CGC-T Green
5VP_PS R8 150 D2 APG1005CGC-T Green
5VN_PS R9 150 D3 APG1005CGC-T Green
GND

Schematic error: Flip D3 polarity during assembly

Project: EECS430PhasedArray.PrjPcb
Sheet Title: EECS430PhasedArray.SchDoc

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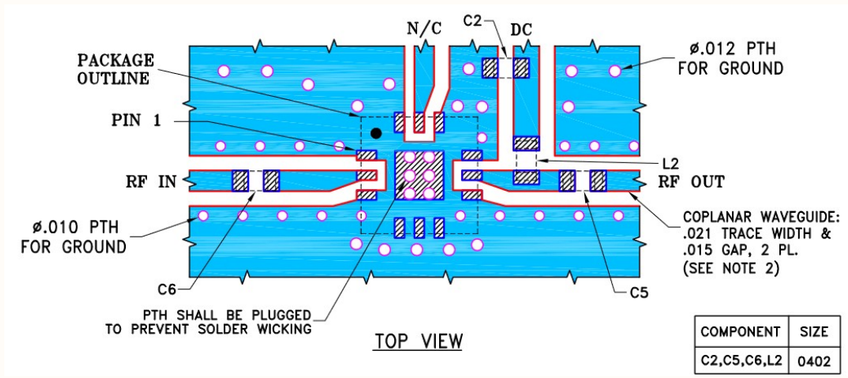
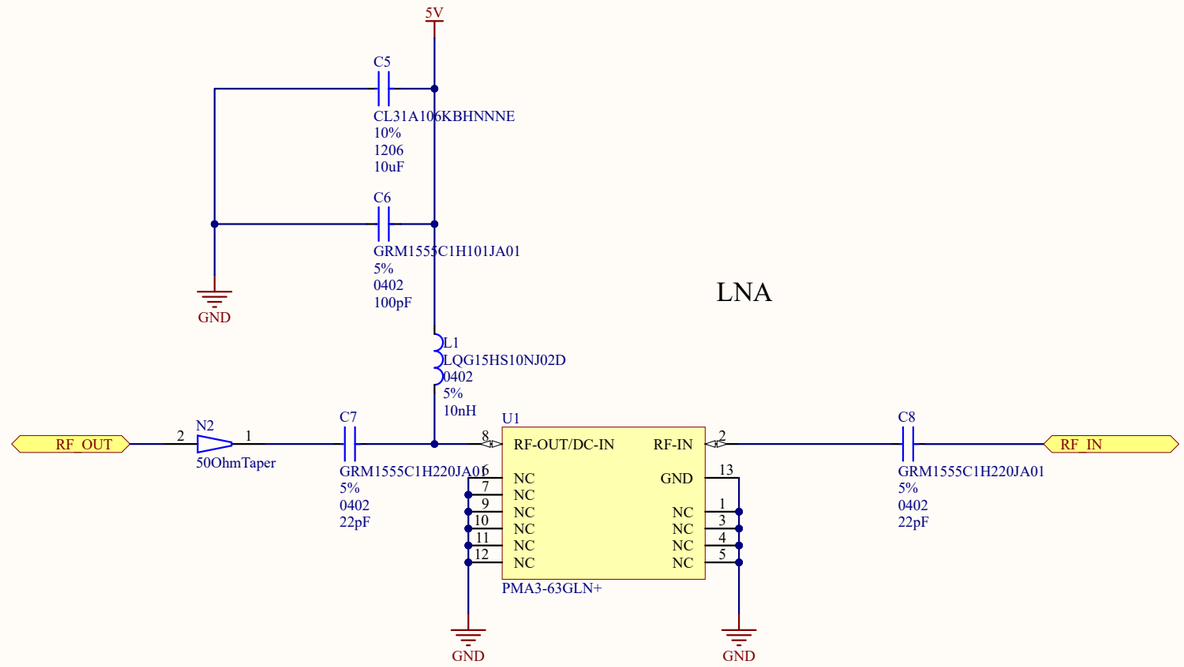


COMPONENT	SIZE
C2,C5,C6,L2	0402



LNA

RECOMMENDED APPLICATION AND CHARACTERIZATION TEST CIRCUIT

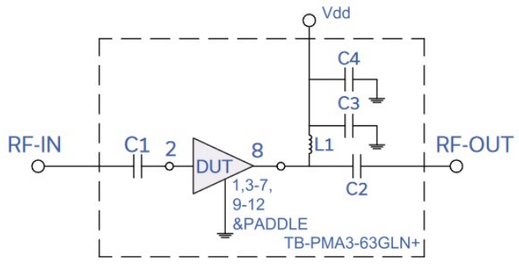


Fig 1. Application and Characterization Circuit
Note: This block diagram is used for characterization. (DUT soldered on Mini-Circuits Characterization test board TB-PMA3-63GLN+)
Gain, Return loss, Output power at 1dB compression (P1 dB), output IP3 (OIP3) and noise figure measured using Agilent's N5242A PNA-X microwave network analyzer.

Conditions:
1. Gain and Return loss: Pin= -35dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, 0 dBm/tone at output.

Component	Size	Value	P/N	Manufacturer
C1	0402	22pF	GRM1555C1H220JA01	Murata
C2	0402	22pF	GRM1555C1H220JA01	Murata
C3	0402	100pF	GRM1555C1H101JA01	Murata
C4	1206	22uF	GRM31CR61H106KA12	Murata
L1	0402	10nH	LQG15HSlONJD2	Murata

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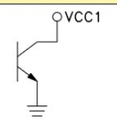
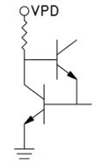
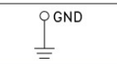
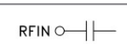
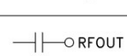
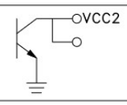
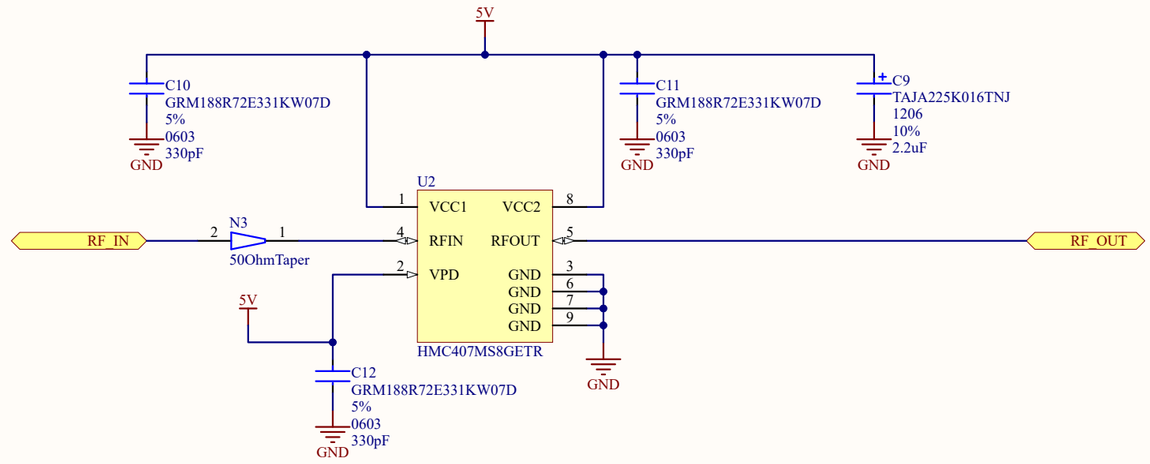
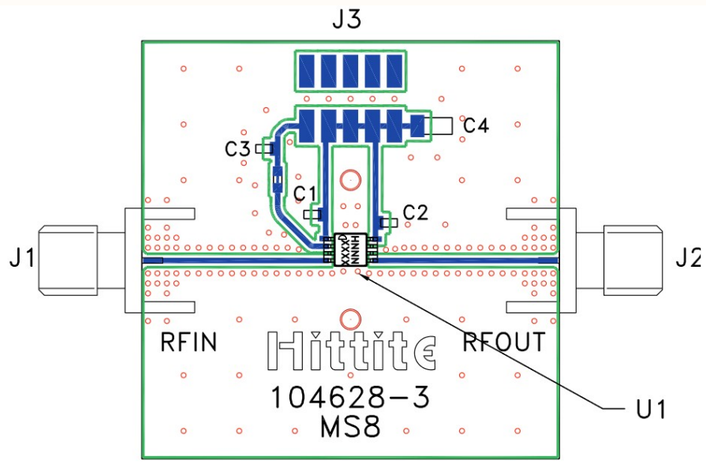
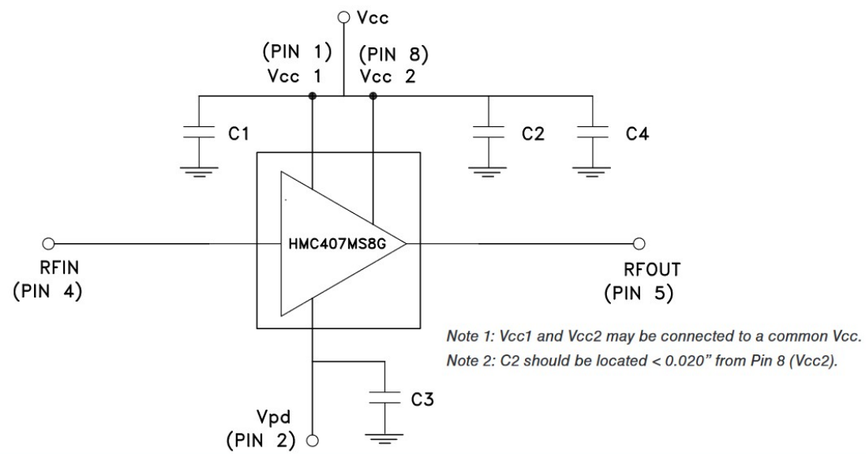
Pin Number	Function	Description	Interface Schematic
1	Vcc1	Power supply voltage for the first amplifier stage. An external bypass capacitor of 330 pF is required as shown in the application schematic.	
2	Vpd	Power control pin. For maximum power, this pin should be connected to 5V. A higher voltage is not recommended. For lower die current, this voltage can be reduced.	
3, 6, 7	GND	Ground: Backside of package has exposed metal ground slug that must be connected to ground thru a short path. Vias under the device are required.	
4	RFIN	This pin is AC coupled and matched to 50 Ohms.	
5	RFOUT	This pin is AC coupled and matched to 50 Ohms.	
8	Vcc2	Power supply voltage for the output amplifier stage. An external bypass capacitor of 330 pF is required. This capacitor should be placed no more than 20 mils form package lead.	





Application Circuit



Note 1: Vcc1 and Vcc2 may be connected to a common Vcc.
Note 2: C2 should be located < 0.020" from Pin 8 (Vcc2).

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Analog Devices, upon request.

Item	Description
J1 - J2	PCB Mount SMA RF Connector
J3	2 mm DC Header
C1 - C3	330 pF Capacitor, 0603 Pkg.
C4	2.2 µF Capacitor, Tantalum
U1	HMC407MS8G / HMC407MS8GE Amplifier
PCB [2]	104628 Eval Board

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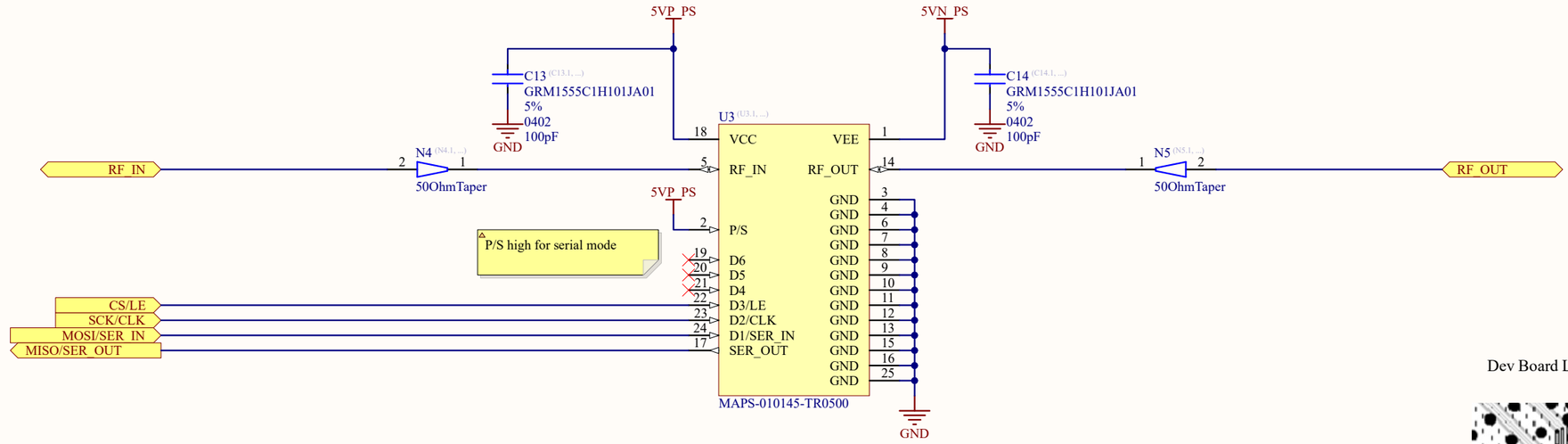
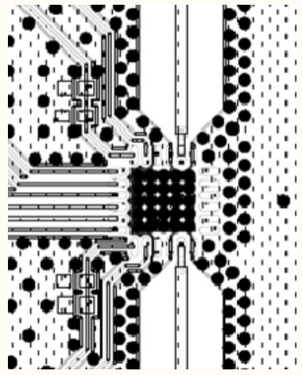


Dev Board Layout



Dev Board BOM

COUNT	ITEM_NUMBER	COMPANY PART NO.	DESCRIPTION	REFERENCE
1	1			
2	2	1000012822-2DFK103	cap, CAP,0.01uF,10%,25V,0402,X7R,RoHS,SMT	C1 C2
2	3	1000012822-2EAJ101	cap, CAP,100pF,5%,50V,0402,COG,RoHS,SMT	C3 C4
4	4	1000041706-0000000	1000041706-0000000, CONNECTOR,RT ANGLE JACK,MIXED	J2 J3 J4 J5
1	5	MAPS-010145-0000000	MAPS-010145-0000000, PHASE SHIFTER,C BAND,3.5-8.0GHz,4 BIT,SMT	U1
1	6	TSM-110-01-S-DV	TSM-110-01-S-DV, CONN, TERMSTRIP, 20P_2R, .230 POST HT, SMT	J1

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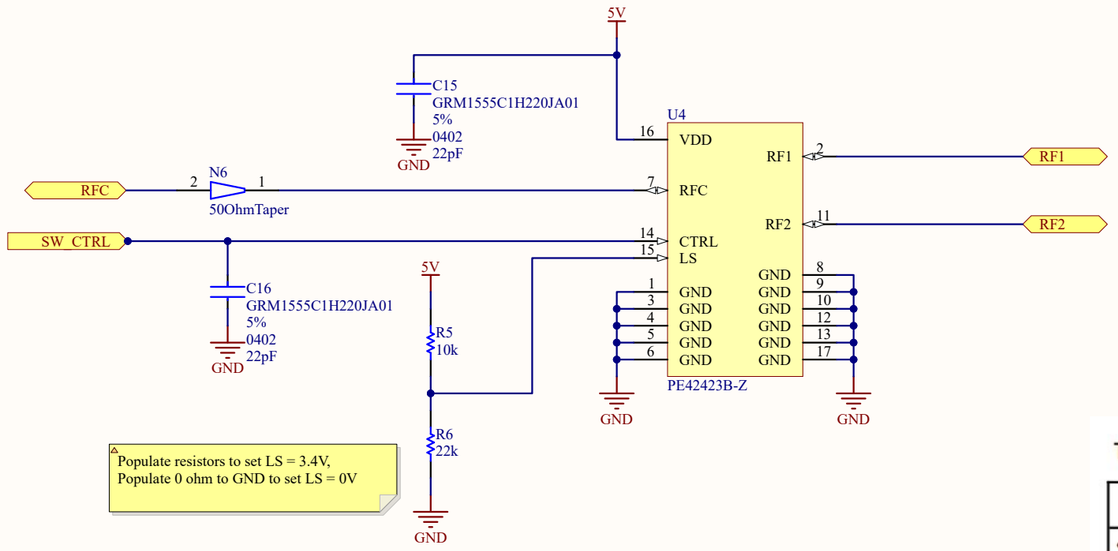


Figure 16. Evaluation Board Schematic

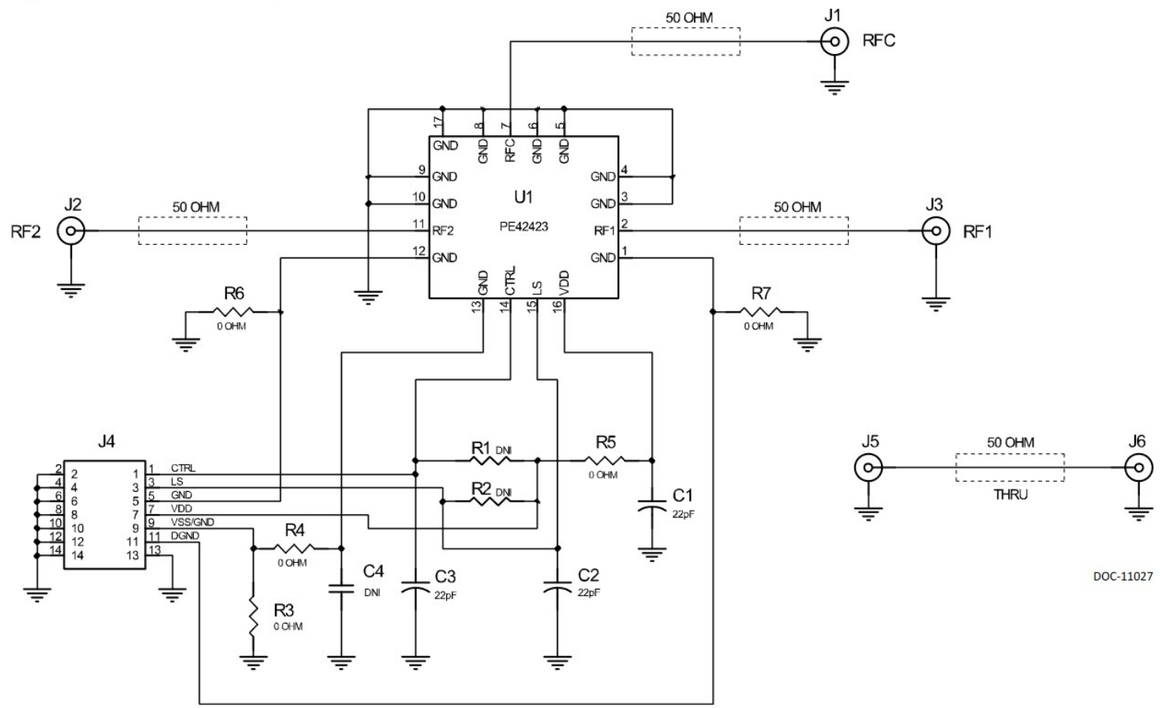
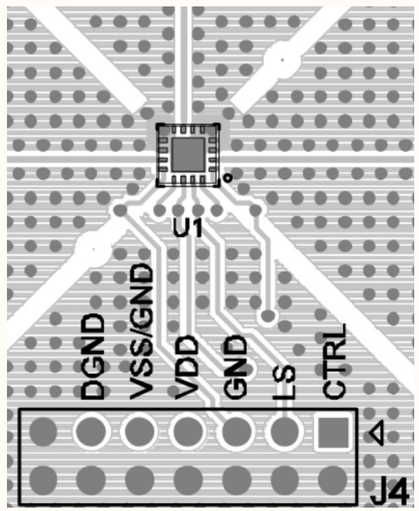


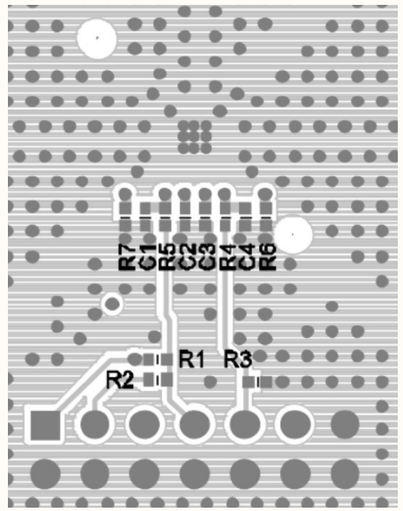
Table 6. Control Logic Truth Table

LS	CTRL	RFC-RF1	RFC-RF2
0	0	off	on
0	1	on	off
1	0	on	off
1	1	off	on

Table 5. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Digital input voltage (CTRL)	V_{CTRL}	-0.3	3.6	V
LS input voltage	V_{LS}	-0.3	3.6	V





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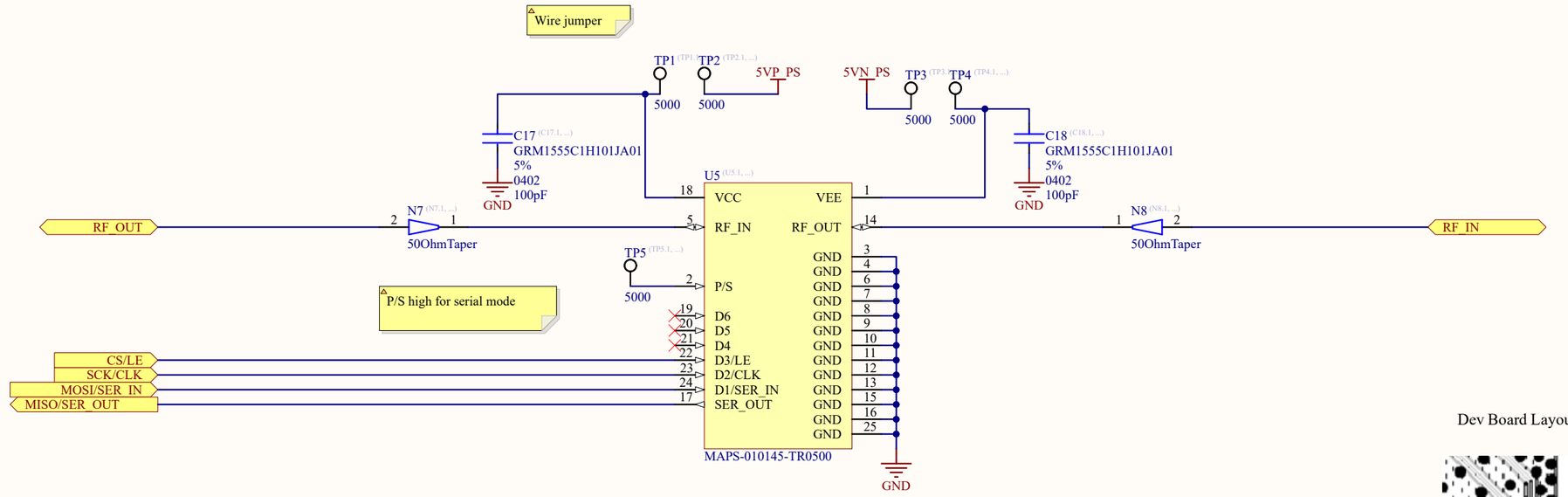
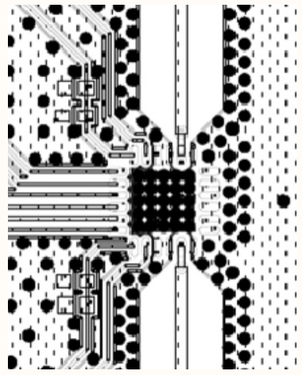


Dev Board Layout



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