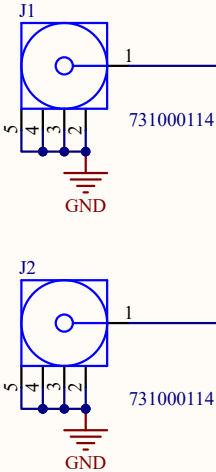


USRP Interface

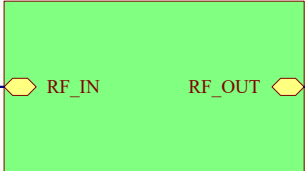
Alternatively: add another switch and only have 1 SMA connector



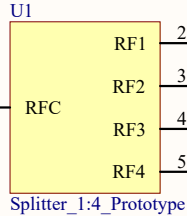
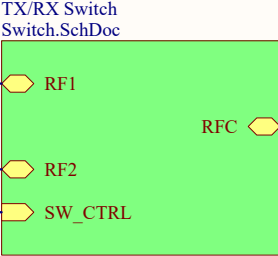
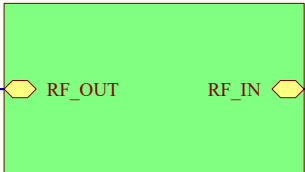
TODO: switch this to a different SMA connector

Half-Duplex Amplifier Network

PA
PA.SchDoc

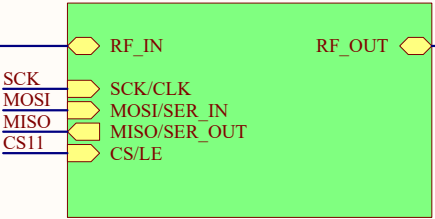


LNA
LNA.SchDoc



Phase Shifters

Phaseshift11
PhaseShifter.SchDoc

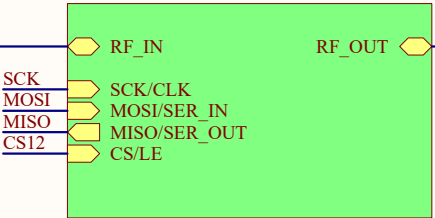


ANT1

PatchAntenna_Prototype

Insert patch here

Phaseshift12
PhaseShifter.SchDoc

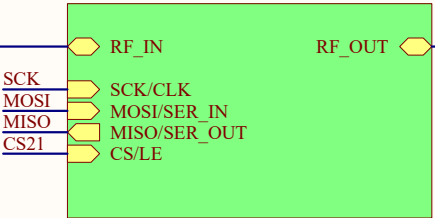


ANT2

PatchAntenna_Prototype

Insert patch here

Phaseshift21
PhaseShifter.SchDoc

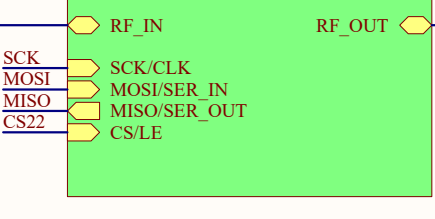


ANT3

PatchAntenna_Prototype

Insert patch here

Phaseshift22
PhaseShifter.SchDoc

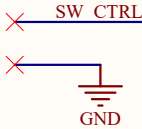


ANT4

PatchAntenna_Prototype

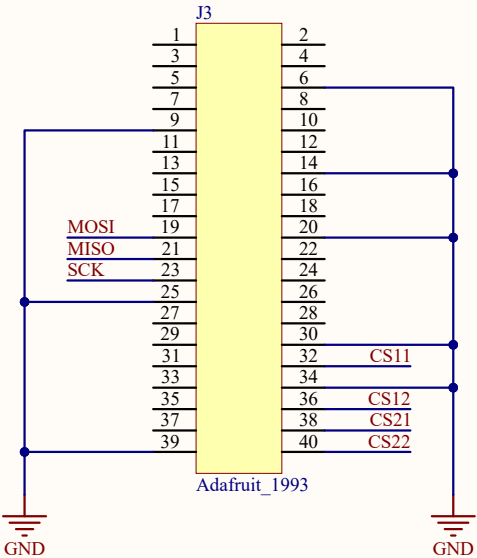
Insert patch here

USRP RX/TX Signal



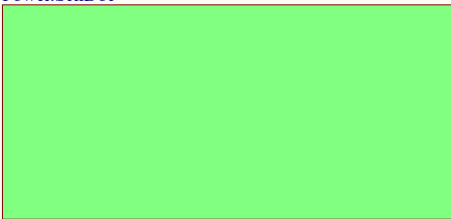
TODO: add USRP breakout

RPi Header



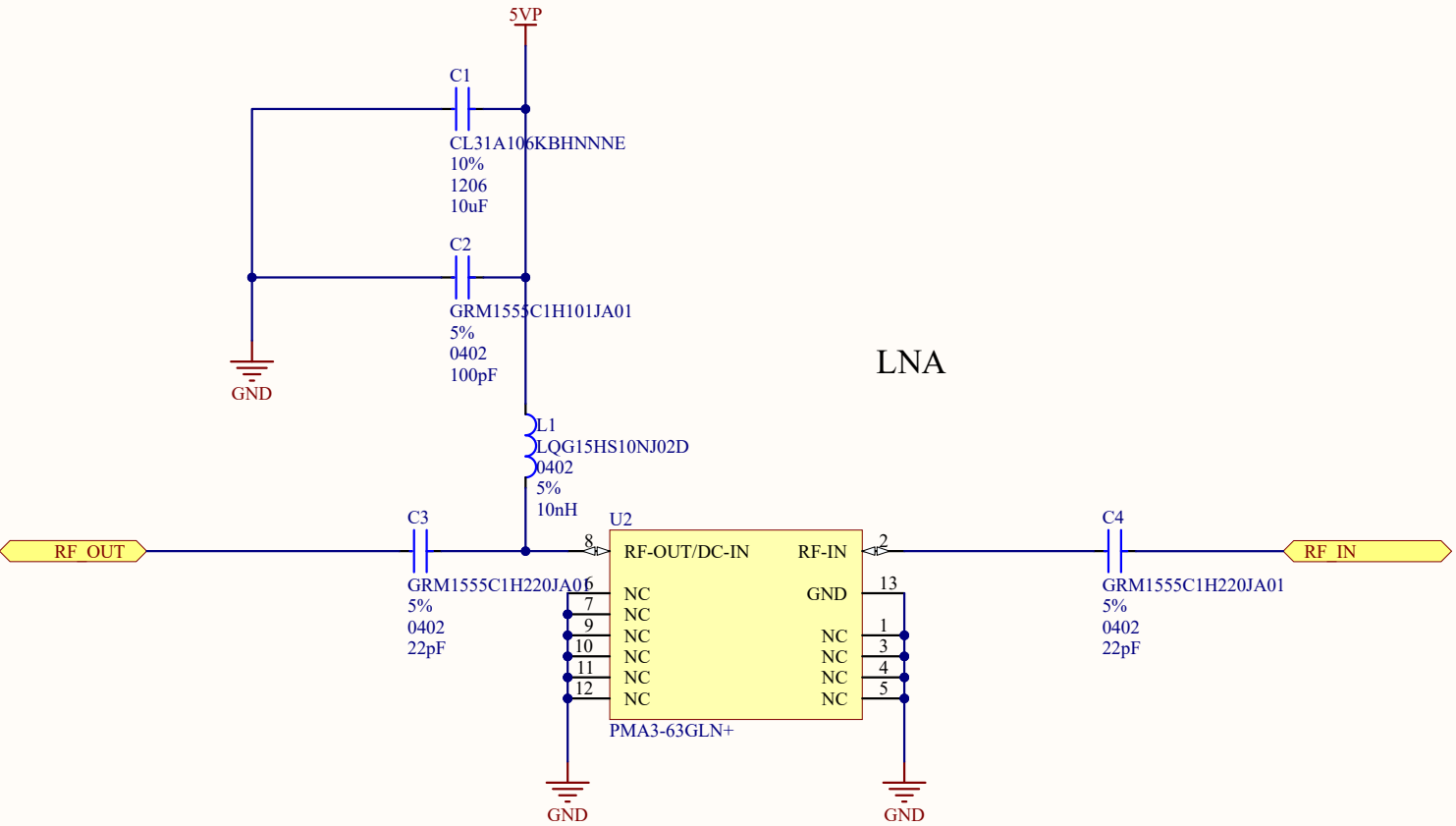
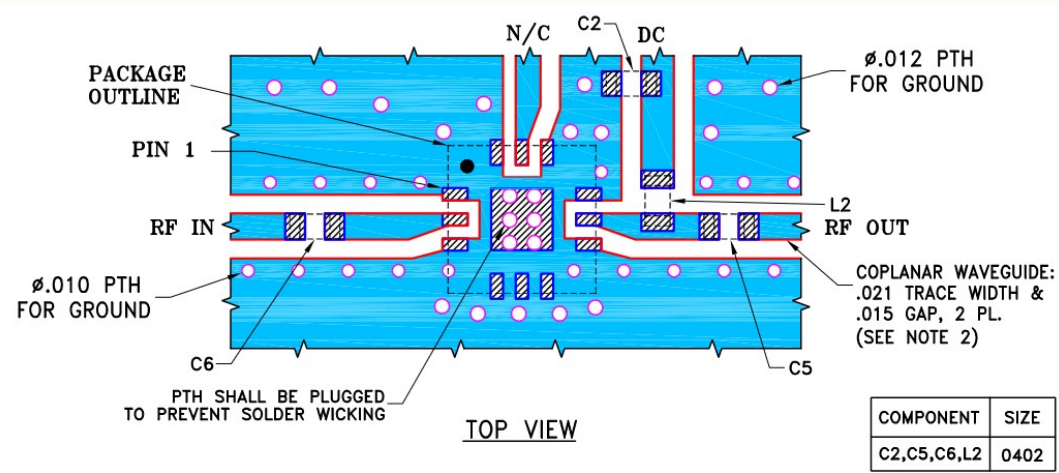
Connectors: 5VP, 5VN, 12VP

Power
Power.SchDoc



Project: EECS430PhasedArray.PrfPcb
Sheet Title: EECS430PhasedArray.SchDoc

Author:		Reviewer:	
Date Modified: 3/26/2024	Revision: A	Size: B	Sheet 1 of 6



RECOMMENDED APPLICATION AND CHARACTERIZATION TEST CIRCUIT

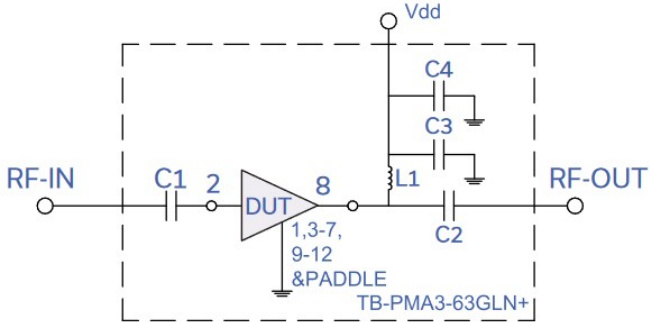


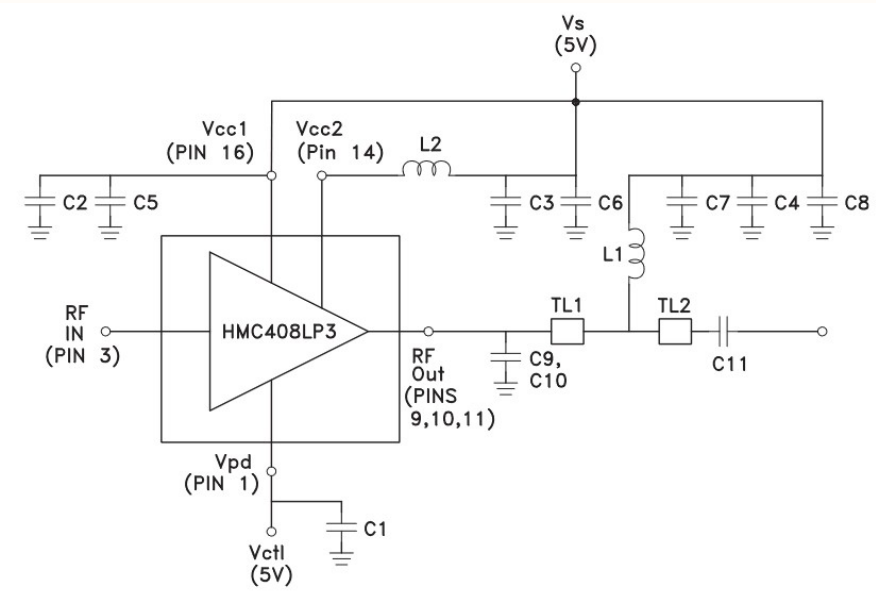
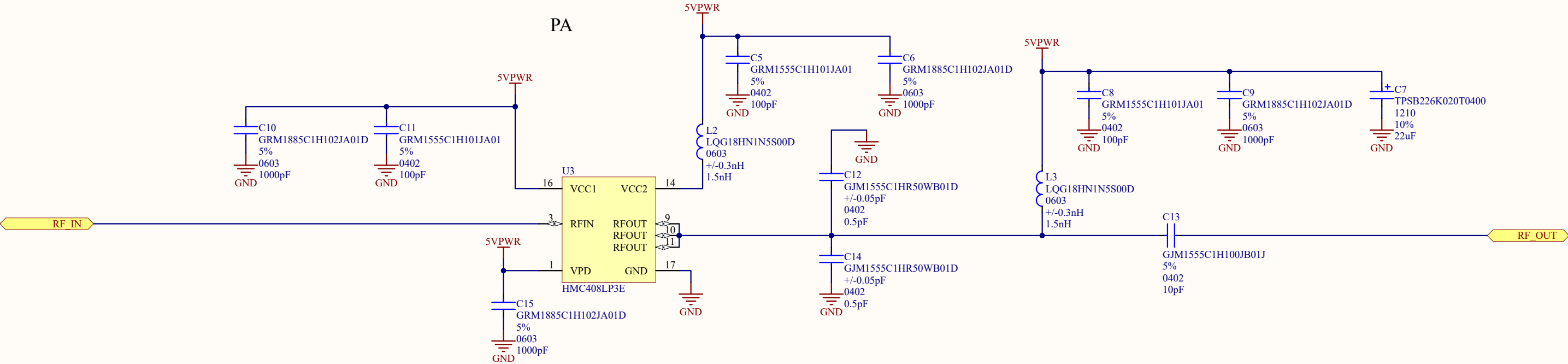
Fig 1. Application and Characterization Circuit

Note: This block diagram is used for characterization. (DUT soldered on Mini-Circuits Characterization test board TB-PMA3-63GLN+)

Gain, Return loss, Output power at 1dB compression (P1 dB), output IP3 (OIP3) and noise figure measured using Agilent's N5242A PNA-X microwave network analyzer.

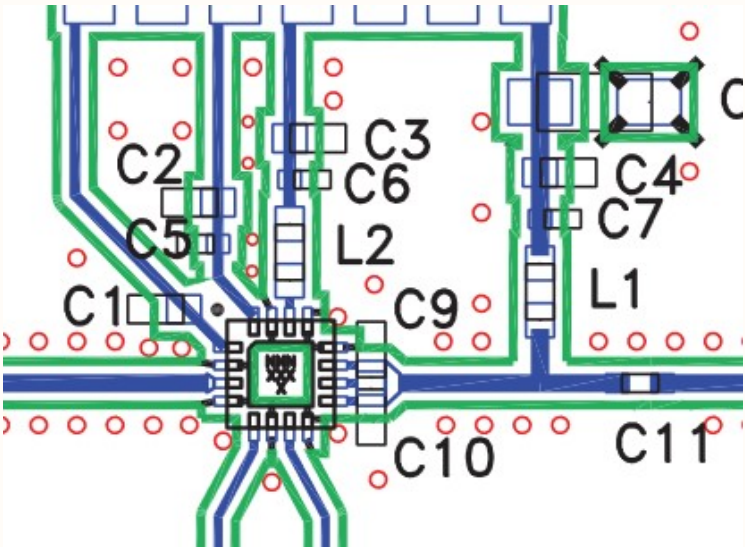
- Conditions:
- Gain and Return loss: Pin= -35dBm
 - Output IP3 (OIP3): Two tones, spaced 1 MHz apart, 0 dBm/tone at output.

Component	Size	Value	P/N	Manufacturer
C1	0402	22pF	GRM1555C1H220JA01	Murata
C2	0402	22pF	GRM1555C1H220JA01	Murata
C3	0402	100pF	GRM1555C1H101JA01	Murata
C4	1206	22uF	GRM31CR61H106KA12	Murata
L1	0402	10nH	LQG15HS10NJ02D	Murata



Item	Description
J1 - J2	PCB Mount SMA RF Connector
J3	2 mm DC Header
C1 - C4	1,000 pF Capacitor, 0603 Pkg.
C5 - C7	100 pF Capacitor, 0402 Pkg.
C8	2.2 μ F Tantalum Capacitor
C9 - C10	0.5 pF Capacitor, 0603 Pkg.
C11	10 pF Capacitor, 0402 Pkg.
L1 - L2	1.6 nH Inductor, 0603 Pkg.
U1	HMC408LP3 / HMC408LP3E Amplifier
PCB [2]	104629 Eval Board

[1] Reference this number when ordering complete evaluation PCB
[2] Circuit Board Material: Rogers 4350



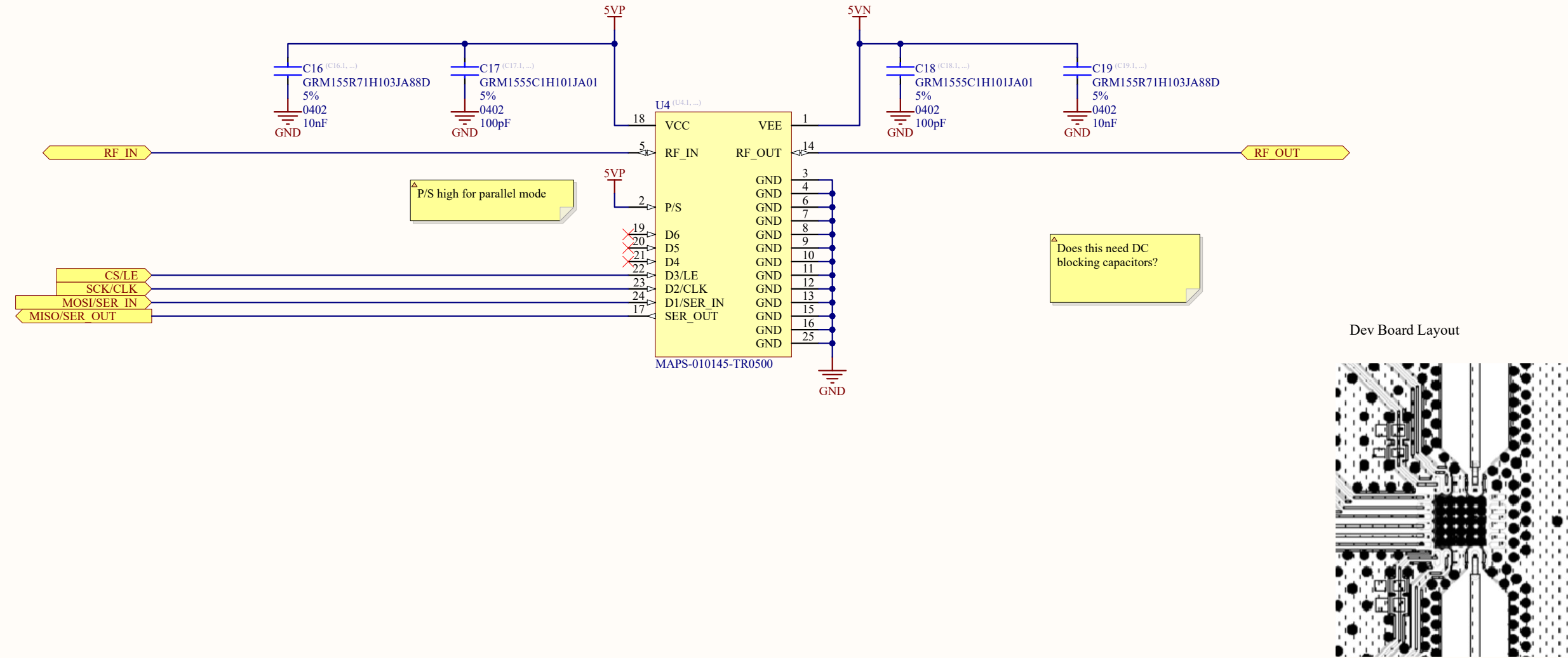
The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.

Note 1: C9, C10 should be located $< 0.020"$ from pins 9, 10, & 11.
Note 2: Application circuit values shown are optimized for 5.7 - 5.9 GHz operation.
Contact our Applications Engineers for optimization of output match for other frequencies.

	TL1	TL2
Impedance	50 Ohm	50 Ohm
Length	0.200"	0.100"

Project: EECS430PhasedArray.PrjPcb
Sheet Title: PA.SchDoc

Author:	Reviewer:
Date Modified: 3/26/2024	Revision: A
Size: B	Sheet 3 of 6



Dev Board BOM

COUNT	ITEM_NUMBER	COMPANY PART NO.	DESCRIPTION	REFERENCE
1	1			
2	2	1000012822-2DFK103	cap, CAP,0.01uF,10%,25V,0402,X7R,RoHS,SMT	C1 C2
2	3	1000012822-2EAJ101	cap, CAP,100pF,5%,50V,0402,COG,RoHS,SMT	C3 C4
4	4	1000041706-0000000	1000041706-0000000, CONNECTOR,RT ANGLE JACK,MIXED	J2 J3 J4 J5
1	5	MAPS-010145-0000000	MAPS-010145-0000000, PHASE SHIFTER,C BAND,3.5-8.0GHz,4 BIT,SMT	U1
1	6	TSM-110-01-S-DV	TSM-110-01-S-DV, CONN, TERMSTRIP, 20P_2R, .230 POST HT, SMT	J1

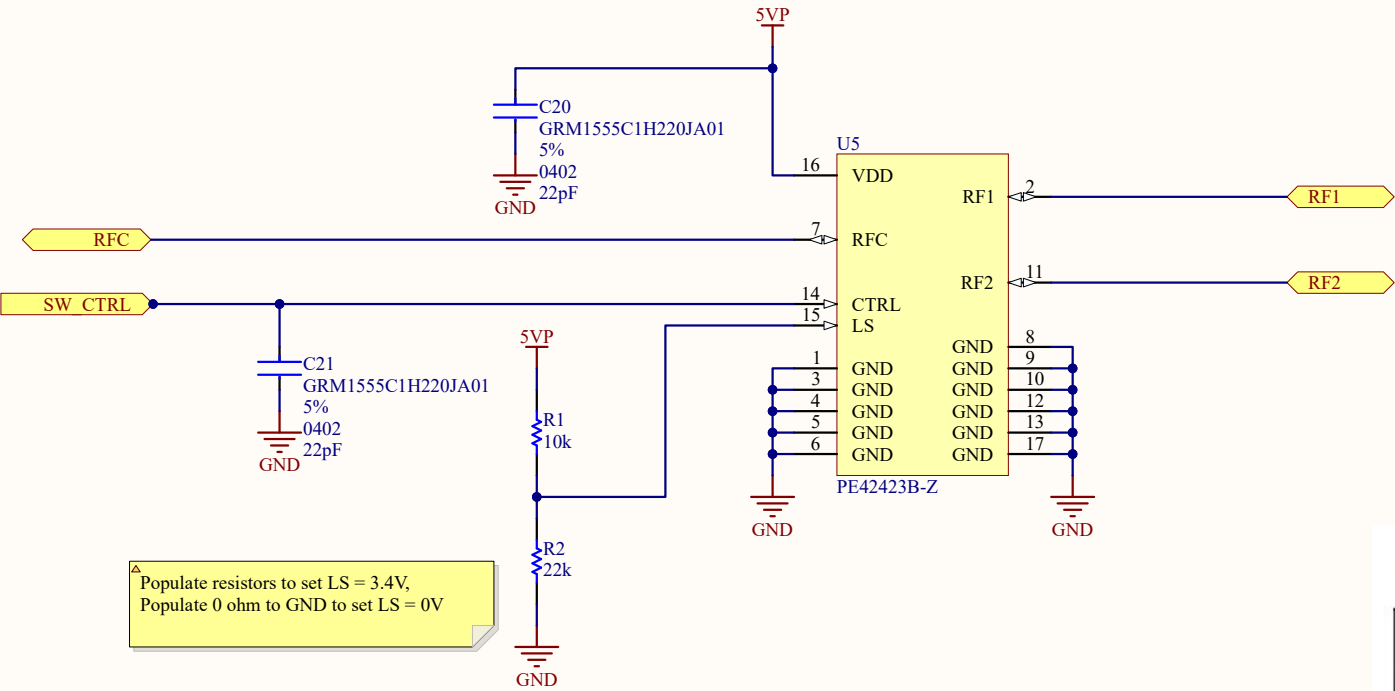


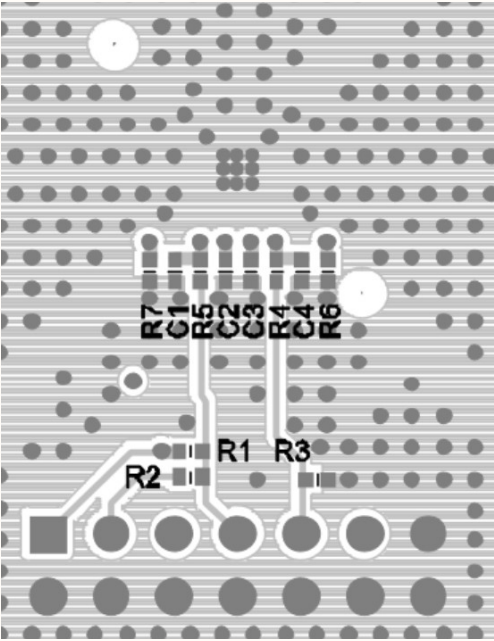
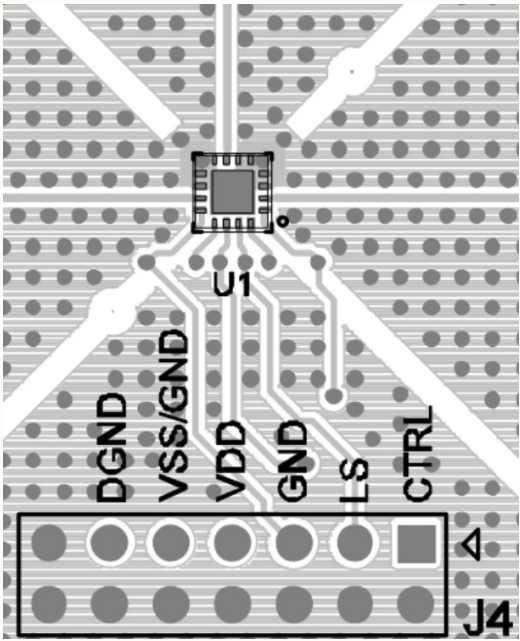
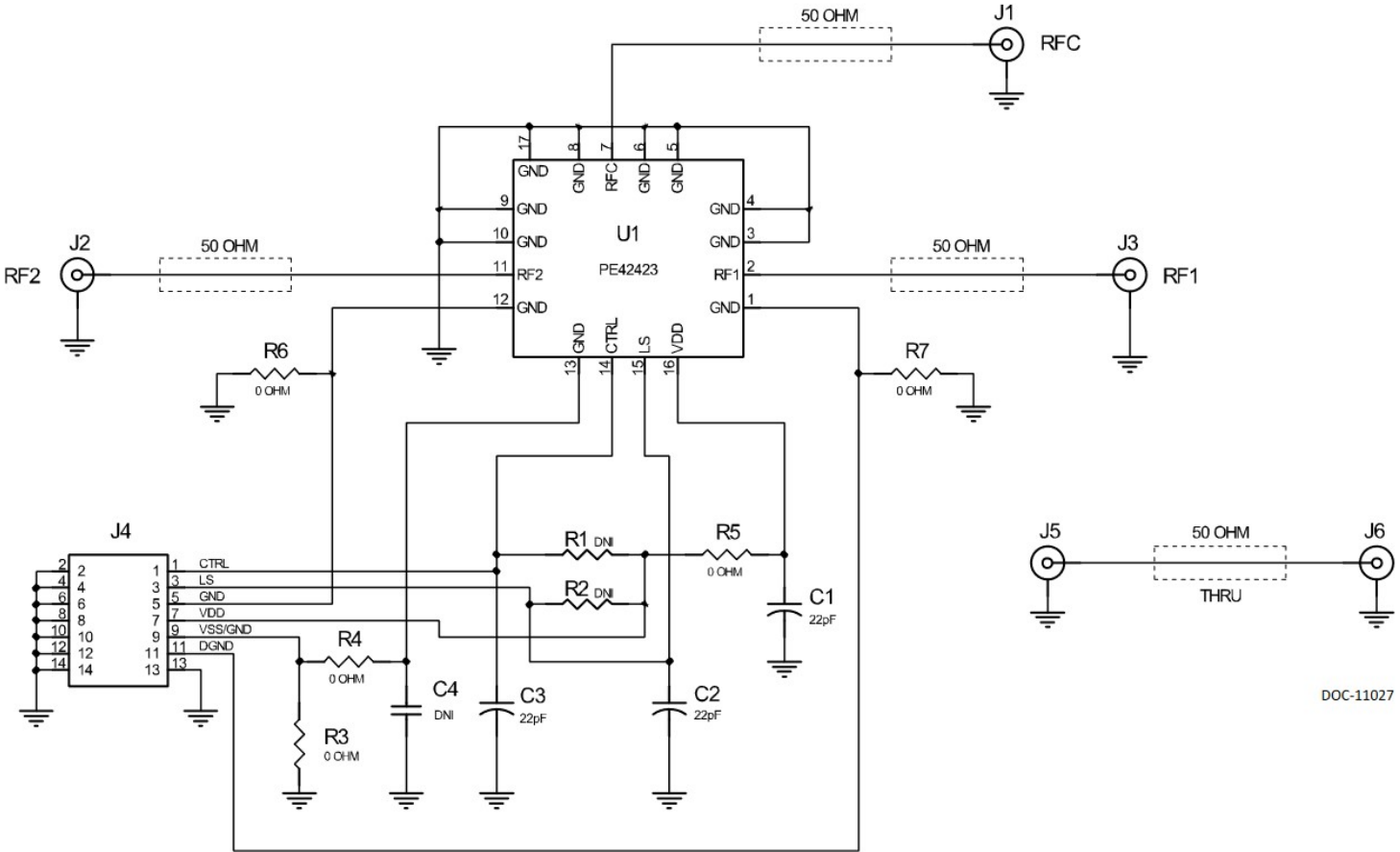
Table 6. Control Logic Truth Table

LS	CTRL	RFC-RF1	RFC-RF2
0	0	off	on
0	1	on	off
1	0	on	off
1	1	off	on

Table 5. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Digital input voltage (CTRL)	V_{CTRL}	-0.3	3.6	V
LS input voltage	V_{LS}	-0.3	3.6	V

Figure 16. Evaluation Board Schematic



Project: EECS430PhasedArray.PrjPeb
Sheet Title: Switch.SchDoc

Author:	Reviewer:
Date Modified: 3/26/2024	Revision: A
Size: B	Sheet 5 of 6

