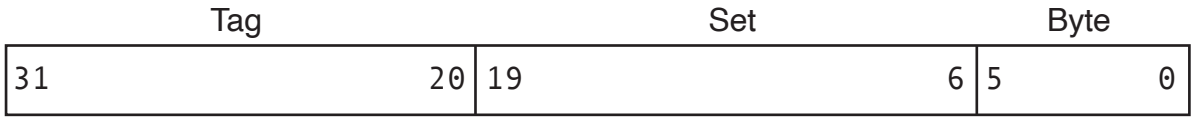
Cache data structure sketch - rev15112024

16MB cache, 64 byte cachelines, 16 way associative, assume 32 bit address

$2^{24} / 2^{6} = 2^{18}$ total cache lines, $2^{18} / 2^{4} = 2^{14}$ total sets with 16 ways per set

Byte Select: 6 bits
Set Index: 14 bits
PLRU: 15 bits
Tag: 12 bits
MESI: 2 bits



16 ways per set: 12 tag bits, 2 MESI bits.
Data not represented for simulation purposes.
15 PLRU bits per set.