Cache data structure sketch - rev10112024

16MB cache, 64 byte cachelines, 16 way associative, assume 32 bit address

$2^{24} / 2^6 = 2^{18}$ total cache lines, $2^{18} / 2^4 = 2^{14}$ total sets with 16 ways per set

Byte Select: 6 bits
Set Index: 14 bits
Tag: 12 bits
PLRU: 15 bits

*NOTE: MESI bits not accounted for.

Tag		Set		Byte	
31	20	19	6	5	0

16 ways per set (12 tag bits, 15 PLRU bits,
Dirty bit, Valid bit. Data not represented for
simulation purposes).

V	D	PLRU	Tag
V	D	PLRU	Tag
V	D	PLRU	Tag
V	D	PLRU	Tag
V	D	PLRU	Tag
V	D	PLRU	Tag
V	D	PLRU	Tag
V	D	PLRU	Tag
V	D	PLRU	Tag
V	D	PLRU	Tag
V	D	PLRU	Tag
V	D	PLRU	Tag
V	D	PLRU	Tag
V	D	PLRU	Tag
V	D	PLRU	Tag
V	D	PLRU	Tag

2^{14} Sets

00000000000000
00000000000001
00000000000010

11111111111111