FULLY-DIFFERENTIAL 8-BIT SAR ADC

DR. NIPUN KAUSHIK

OVERVIEW OF THE DESIGN

SAR SWITCHING SCHEMES

Scheme	Author/Year	Switching Energy	Comment
Conventional – Charge Redistribution	P. Grey et al. – 1975 [2]	1.0	Simple/High Power
Monotonic	Chen & Brodersen, ISSCC 2006 [3]	~0.5	Not centered around VCM
VCM Precharge	Y. Zhu et al., JSSCC 2010 [4]	0.25~0.3	Need extra precharge phase
Charge Recycling	Ginsberg, ISCAS 2005 [5-6]	0.37	Break MSB into Sub DAC, Charge recycling, high linearity
MCS (Merged Capacitor Switching)	CC Liu, JSSCC 2010 [7]	0.125-0.15	Power efficient/mismatch sensitive

SWITCHING SCHEME

- The switch capacitor switching scheme [1] is utilized due to
  - Breakdown of MSB into smaller bits
  - Charge the capacitors during the hold phase; change the decision bit caps per conversion until the LSB.
  - Breakdown MSB into smaller, lower DAC – Good for Power Side channel attack current spike in CDAC
  - The paper claims to reduce power consumption by 37% of the conventional charge redistribution scheme.

SPLIT CAPACITOR

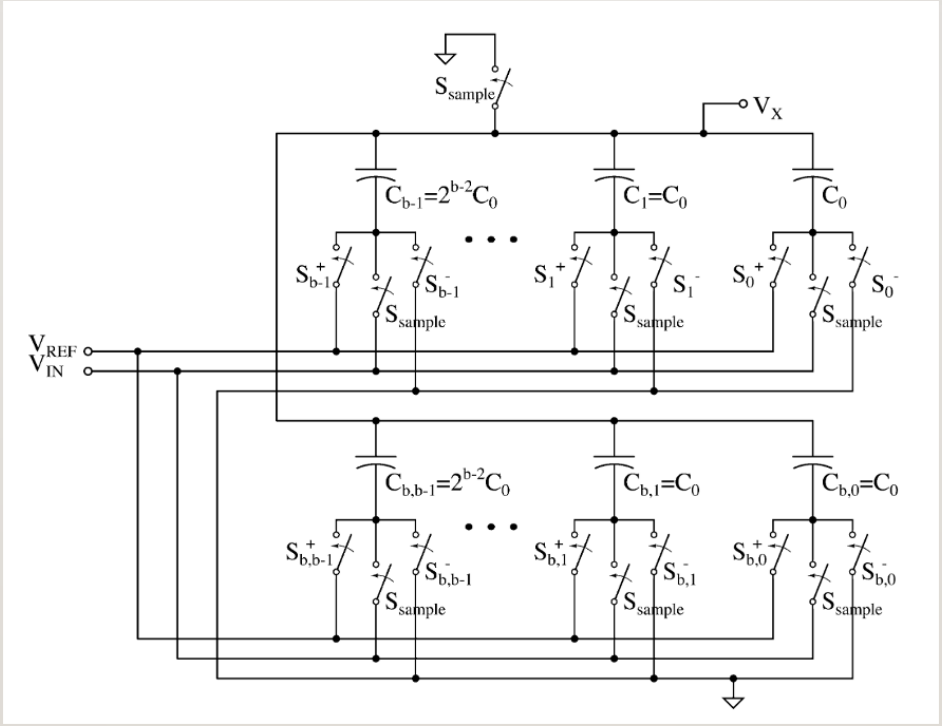


Fig1 : Split Capacitor switching scheme [5]

CHARGE RECYCLING

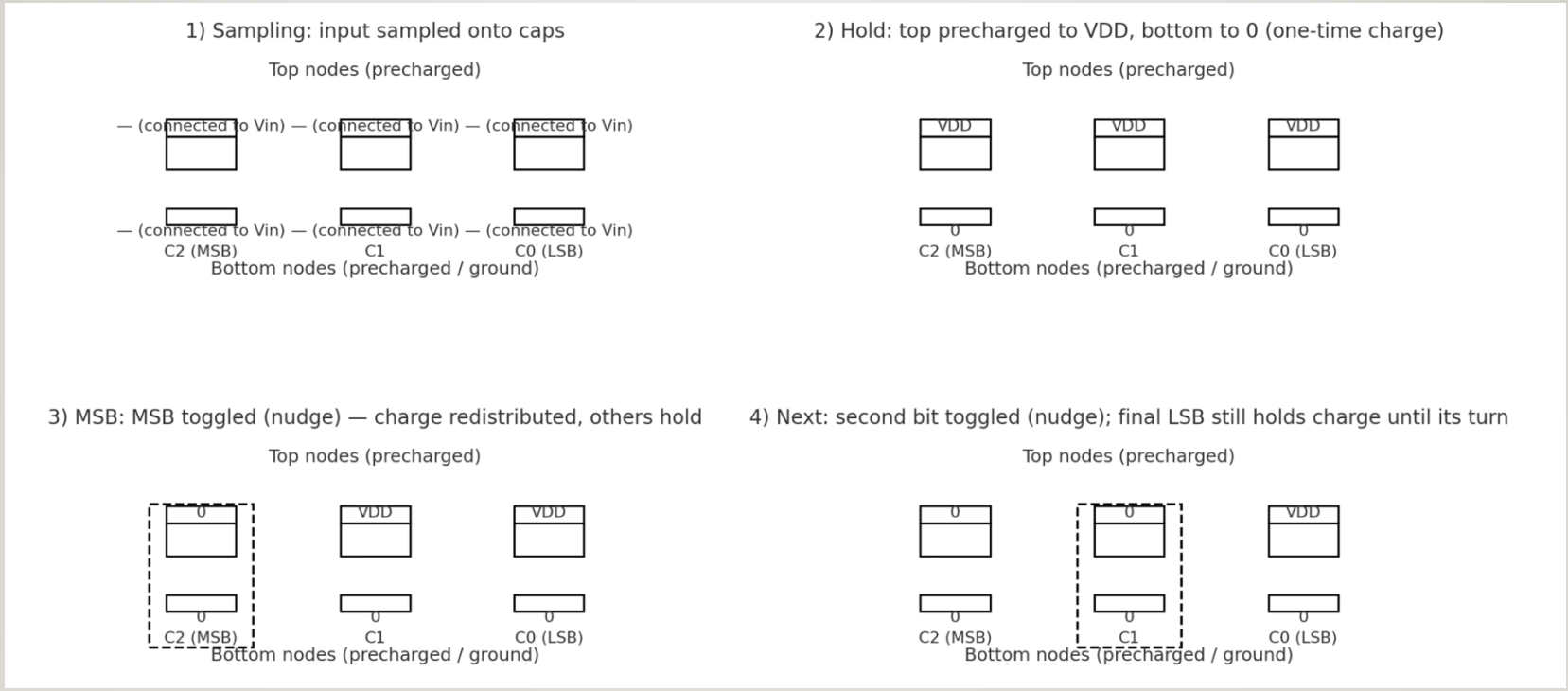


Fig 2: Charge recycling to save energy per conversion [6]

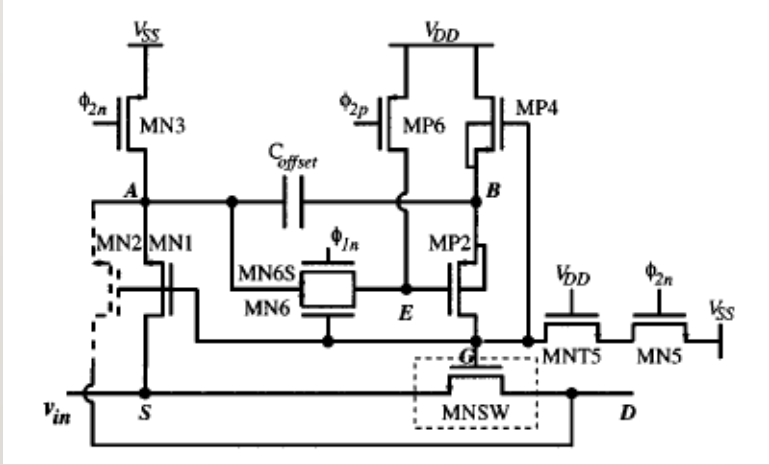
MAIN COMPONENTS OF THE DESIGN

- Bootstrap switch
- Comparator
- CDAC
- Digital Logic
- Reference Switches

BOOTSTRAP SWITCH

1. Dessouky & Kaiser (2001) – High Linearity [8]
2. The Bootstrapped Switch: A Circuit for All Seasons 2015 [9]

The first reference is utilized in this design to achieve high linearity.



COMPARATOR

- A double-tail comparator is used in the design. It provides a high-gain, pre-amplification with a latch. This design has been proven in various tape-outs.
- Few iterations to get the input offset less than 0.25-0.3LSB to maintain conversion integrity.
- The noise can be characterized by MC and transient sim, post-process in MATLAB/Excel to get the comparator sigma. For this design, it was 1mV.

DOUBLE TAIL COMPARATOR

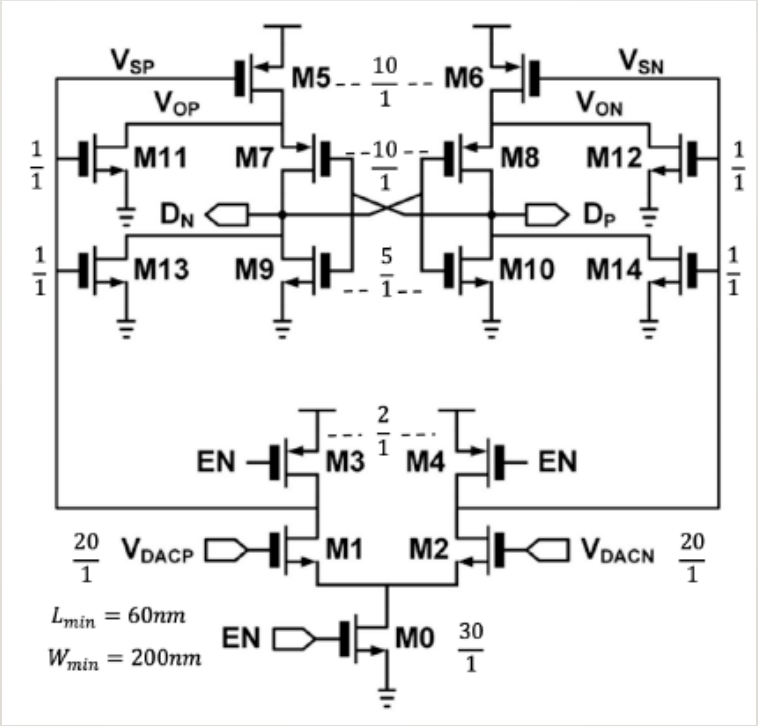


Fig 4: Double-tail comparator used for SAR conversion

CDAC ARRANGEMENT

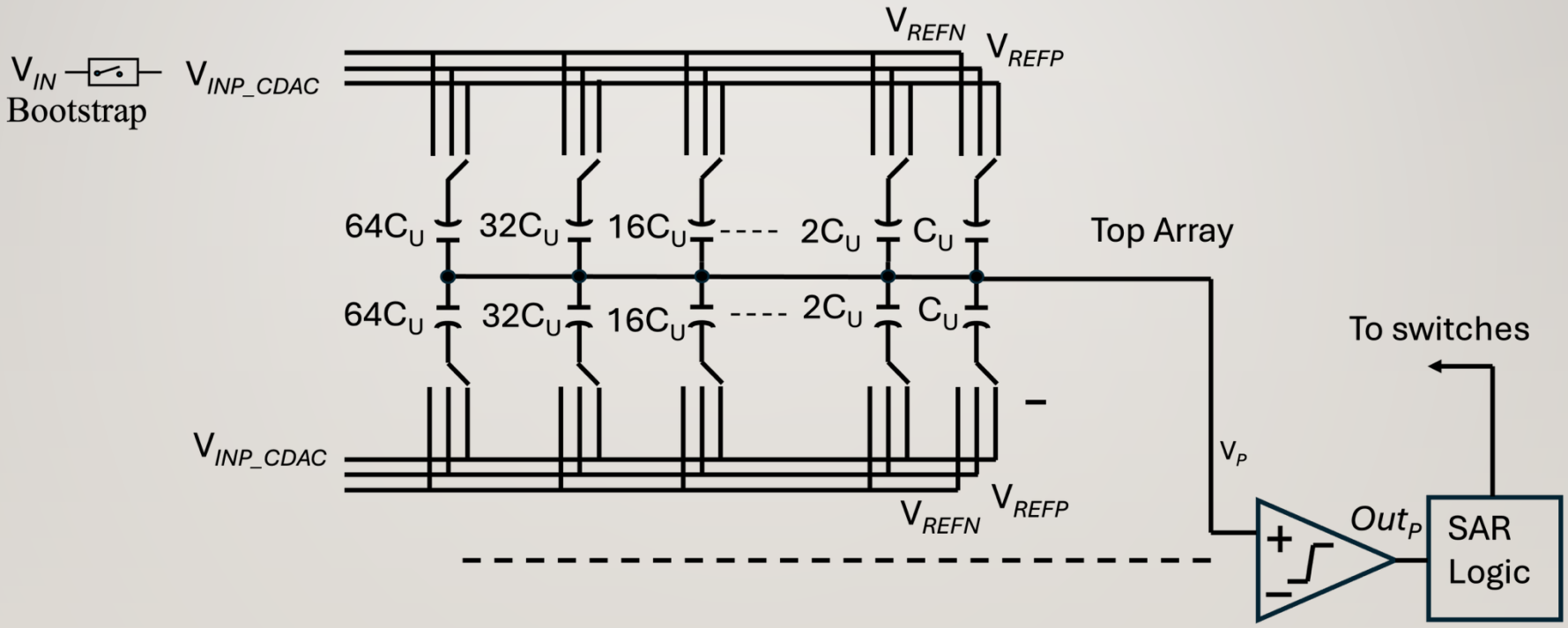


Fig 5: CDAC is arranged for 8-bit with a split capacitor arrangement.

DIGITAL LOGIC

- Synchronous Logic is used in the design for fixed timing. It comprises a D Flip-Flop Synchronizer, Switch control, DAC control, and a register to store the code.

DIGITAL LOGIC SCHEME

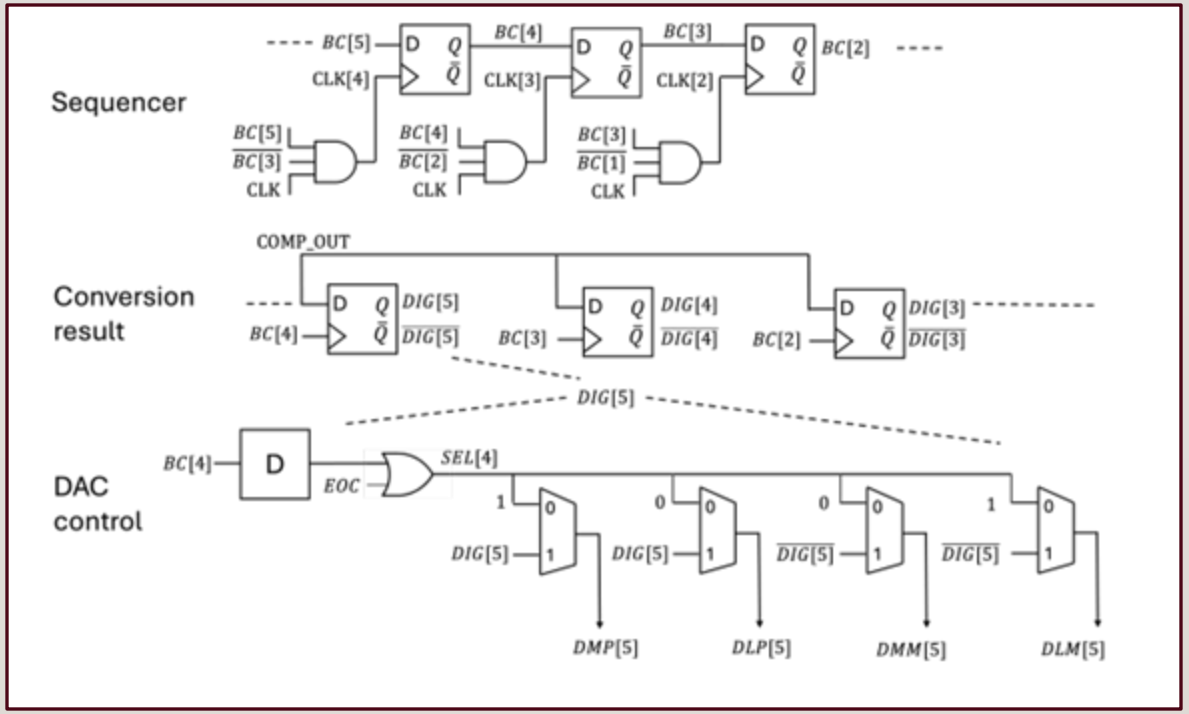
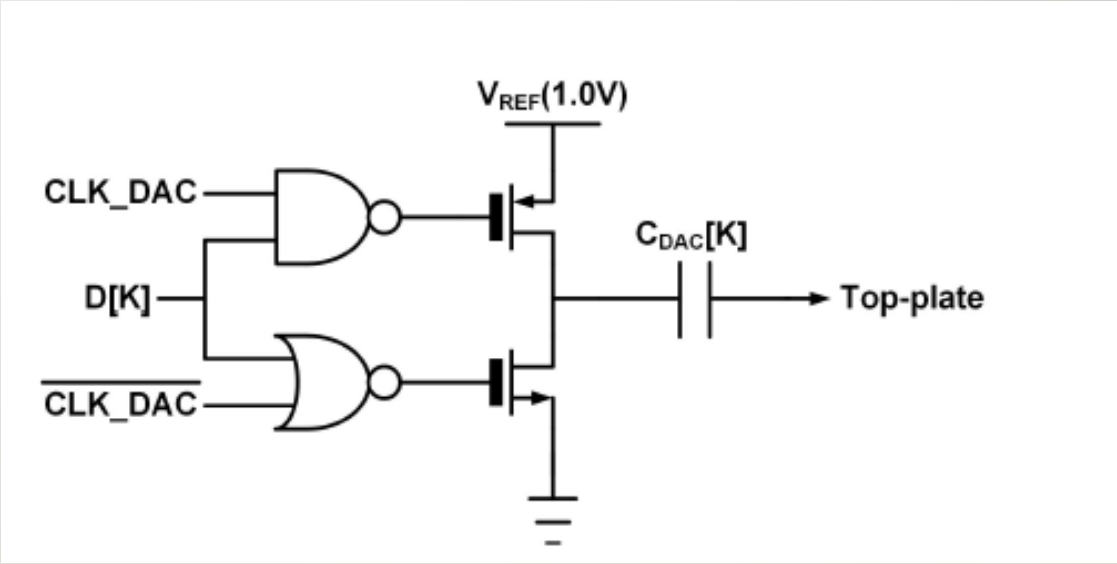


Fig 5: Split capacitor digital logic scheme for SAR conversion

REFERENCE SWITCHES

- The design used inverter-based switches to charge the capacitive arrays.
- SAR logic drives the switches in the DAC control phase.
- The CDAC is charged to 0.01 LSB within the sampling or clock period.



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