Pin List

SC Top Pin list

	Name	Package Pin #	Pin Type	ESD	V/I ratings	Domain	Comments	On chip connectivity
2	AVDD3V	TBD	Power Input	Techfile_Pad_Names	3.3V	I/O Domain	Analog HV Rail	
3	AVDD1	TBD	Power Input	Techfile_Pad_Names	1V	Core	Analog LV Rail	
5	VINSC	TBD	Analog input (G)	Techfile_Pad_Names	3.3V	I/O Domain	Switch 1 input (SW1)	D/S of PMOS HV (3.3)
6	CLKIN	TBD	Analog input (G)	Techfile_Pad_Names	3.3V	I/O Domain	Clock for system, Secondary ESD	GATE (Inverter and NAND)
7	VPROBE	TBD	Analog input (G)	Techfile_Pad_Names	3.3V	I/O Domain	Secondary ESD	GATE (Inverter)
8	VCMI	TBD	Analog input (G)	Techfile_Pad_Names	1V	Core	Input to OTA pair (VINP), Secondary ESD	GATE(NMOS and PMOS 1V)
9	VTHRESH	TBD	Analog input (G)	Techfile_Pad_Names	1V	Core	Input to Comparator (VINM). Seondary ESD	GATE (NMOS 1V)
10	VSET1	TBD	Analog input (G)	Techfile_Pad_Names	3.3V	I/O Domain	REFFILTER	Ressitor 110k
11	DETECTOUT	TBD	Analog input (G)	Techfile_Pad_Names	1V	Core	Comes from OUTDRIVER (1V rail)	
12	EXT_R1	TBD	Analog input (G)	Techfile_Pad_Names	3.3V	I/O	Set current as 1uA (1MEG RES)	Source of NMOS HV (3.3), regulated by OTA
14	AVSS	TBD	Power Input	Techfile_Pad_Names	Ground	I/O Domain adn Core	Ground	

Power and Ground	
Secondary ESD	
OUTPUT