FD FLASH-SAR 8-BIT ADC

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PARAMETERS

- This architecture utilizes a 2-bit flash to harness the speed of flash and a 6-bit SAR as a fine converter.
- Designs with non-integer bits were also explored, which can utilize digital correction. A 2.5-bit Flash with 5 comparators can reduce the comparator input offset [1-3].
- The number of comparators increases exponentially with the number of bits. This design uses 3 double-tail comparators with a preamplifier.
- The idea is to break down the reference current in the conversion process.
- Please refer to the vulnerability of the SAR ADC and the Power Side channel attack[4].

2-BIT FLASH

- Fully differential flash has multiple schemes that are widely used[5-7].
- This design uses an FD SAR based on [7]
  - Fully differential reference ladder
  - Sample the signal and differential reference in one phase.
  - Sample VCM voltage in the second phase, hold for signal settlement, and turn on the comparators.
- The signal thermometer code provided by three comparators is followed by
  - Bubble correction: Ensure monocity of the code, remove incorrect transitions.
  - Thermometer to 2-bit binary encoder – Used on Top two bits of SAR code register

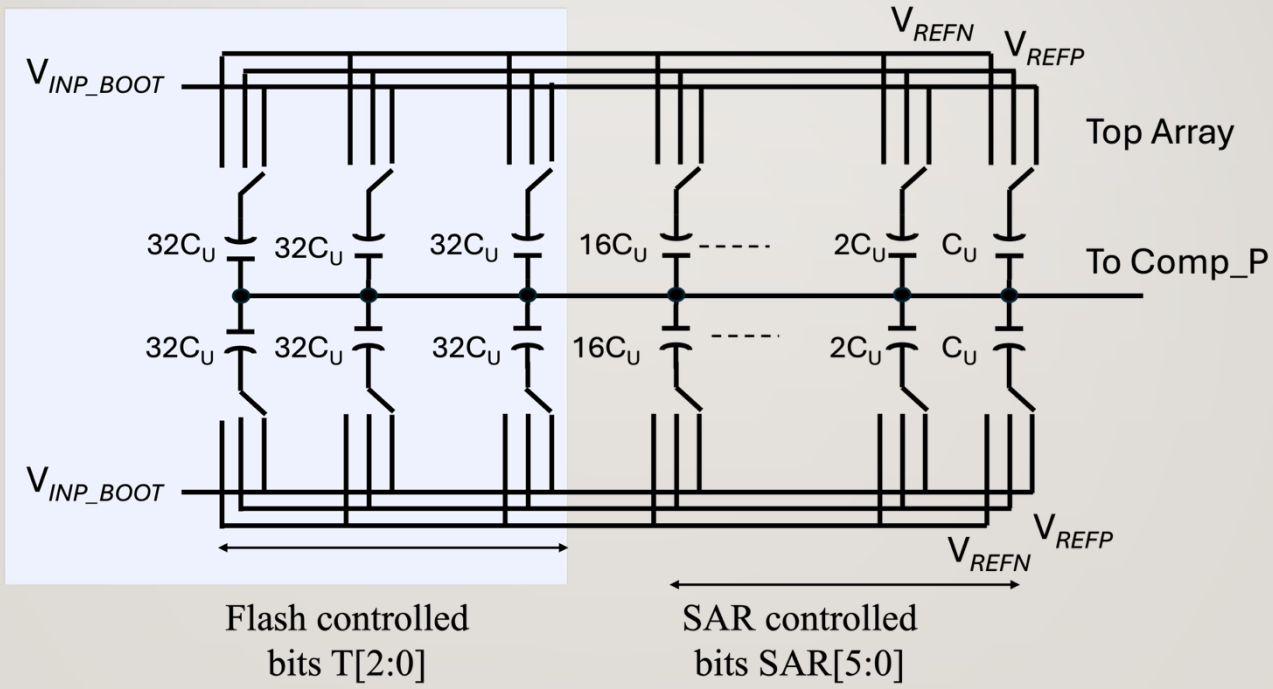
6- BIT SAR

- The 6-bit find SAR converter is based on a split-capacitor and charge recycling scheme similar to the 8-bit SAR converter [8,9].
- The code from Flash is saved on the SAR register after flash conversion, followed by the SAR codes.
- After the SAR conversion, the final 8-bit code is available at the end of the cycle

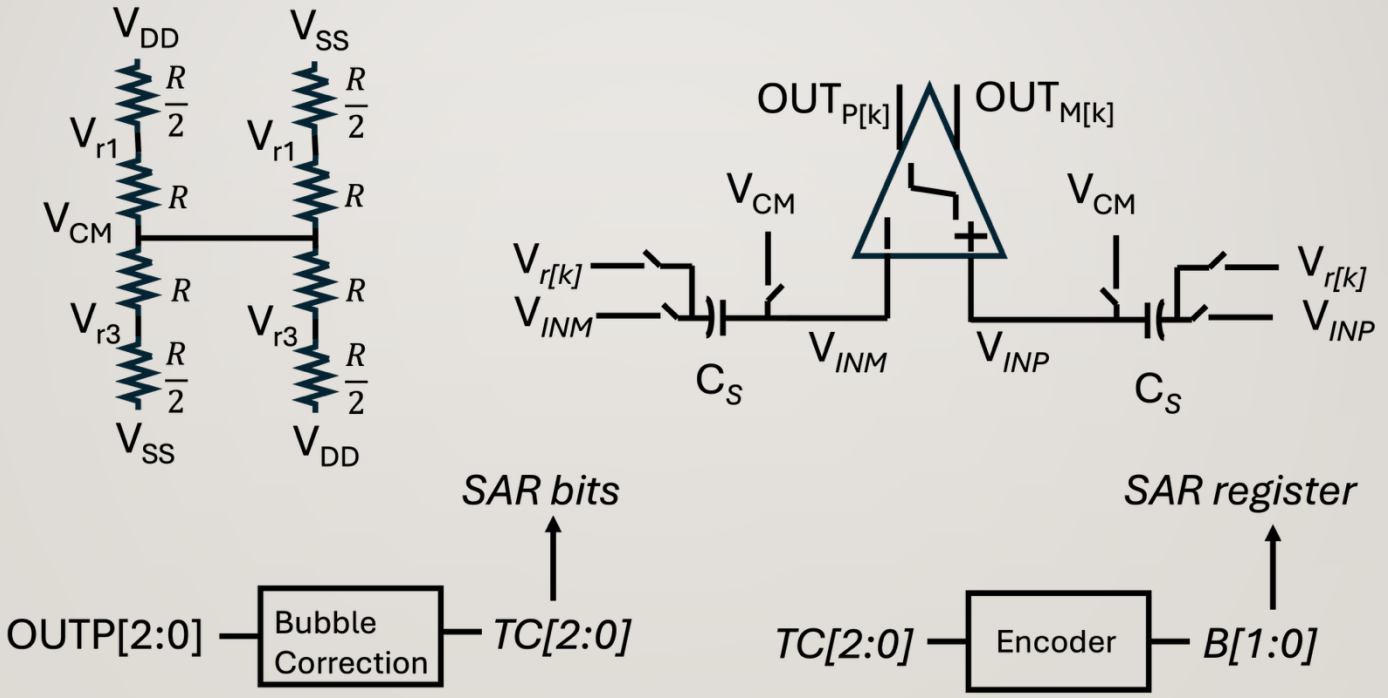
SECURE CDAC ARRANGEMENT

- The top two bits of the CDAC are divided equally to reduce the reference current in the CDAC.
- The top two bits equate to 32C+64C = 96C
  - This is broken down into 32C+32C+32C = 96C
- Flash thermometer output controls these three capacitors, which provide fine control and less charge dump at one time, leading to a spike.
- Spike reduction is controlled by a soft start mechanism, which turns on these bits with a delay.
- Delay lines are used to turn these bits with a fixed deterministic delay.

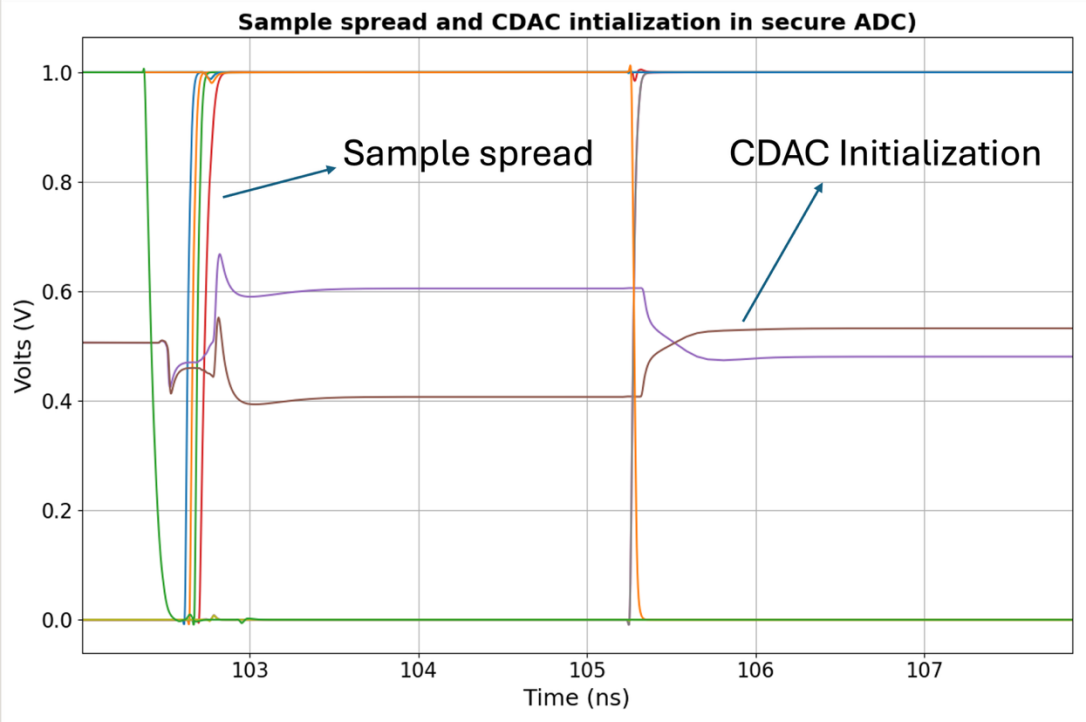
CDAC ARRANGEMENT



2-BIT FLASH CONVERTER



CDAC INITIALIZATION WITH FLASH BITS



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