

FD 8-BIT SAR

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DESIGN PARAMETERS

- Resolution = 8-bit
- $C_u = 20\text{fF}$
- $V_{\text{ref}} = 1\text{V}$
- Switching scheme = Charge recycling (Ginsberg et al., 2005 & 2006)
- CDAC arrangement = Split Capacitor DAC – MSB split into lower sub-DAC
- System Clock = 100 MHz

SCHEMATIC TOP

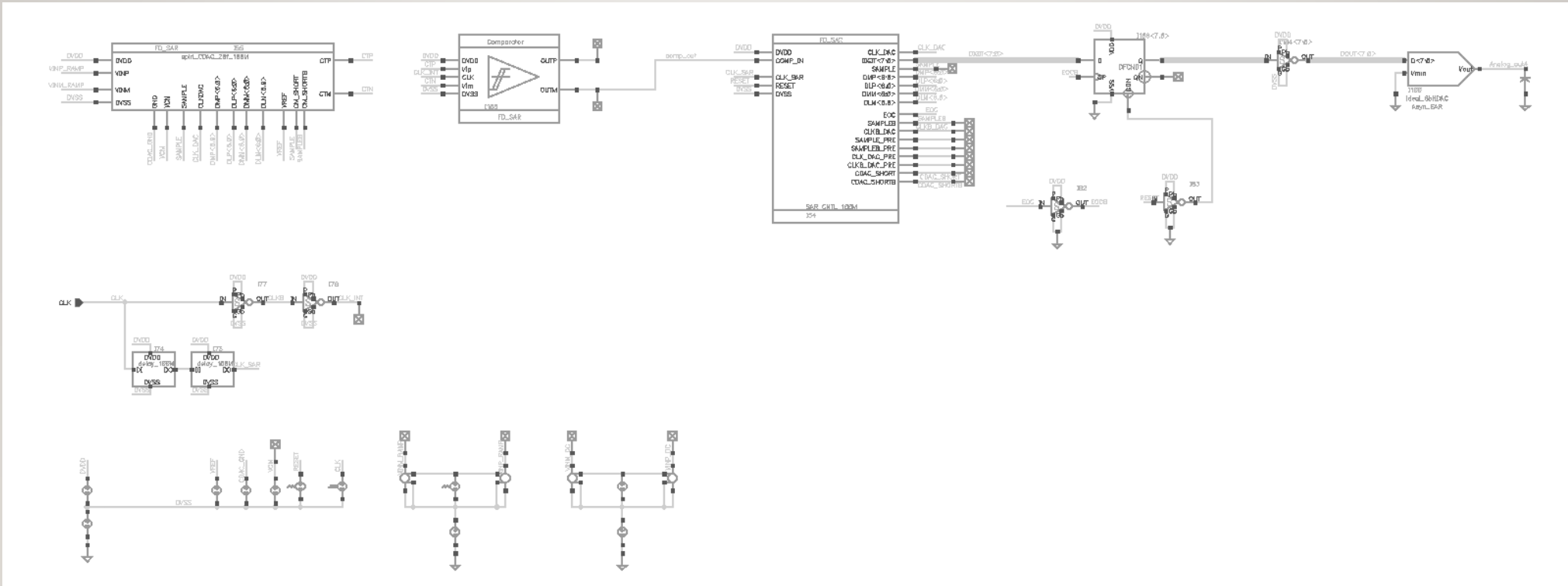


Fig 1: Top cadence schematic of the ADC

CDAC

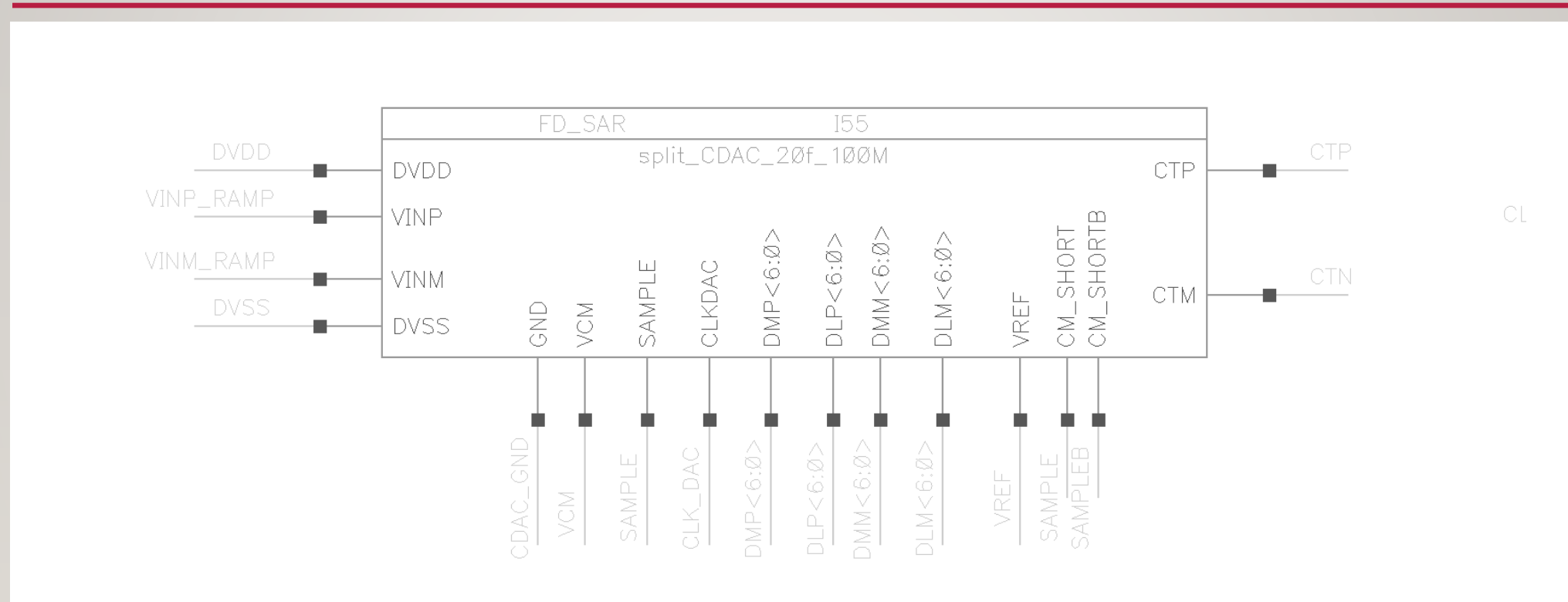


Fig 2: CDAC symbol and control signals

CDAC ARRANGEMENT

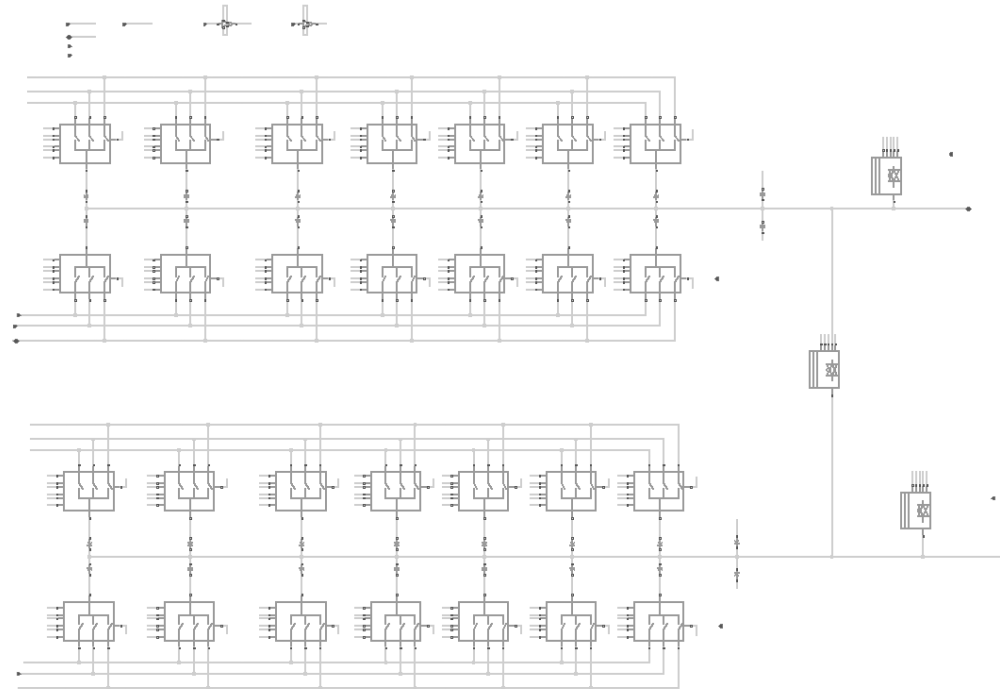


Fig 3: CDAC arrangement with reference switches

CDAC REFERENCE SWITCH

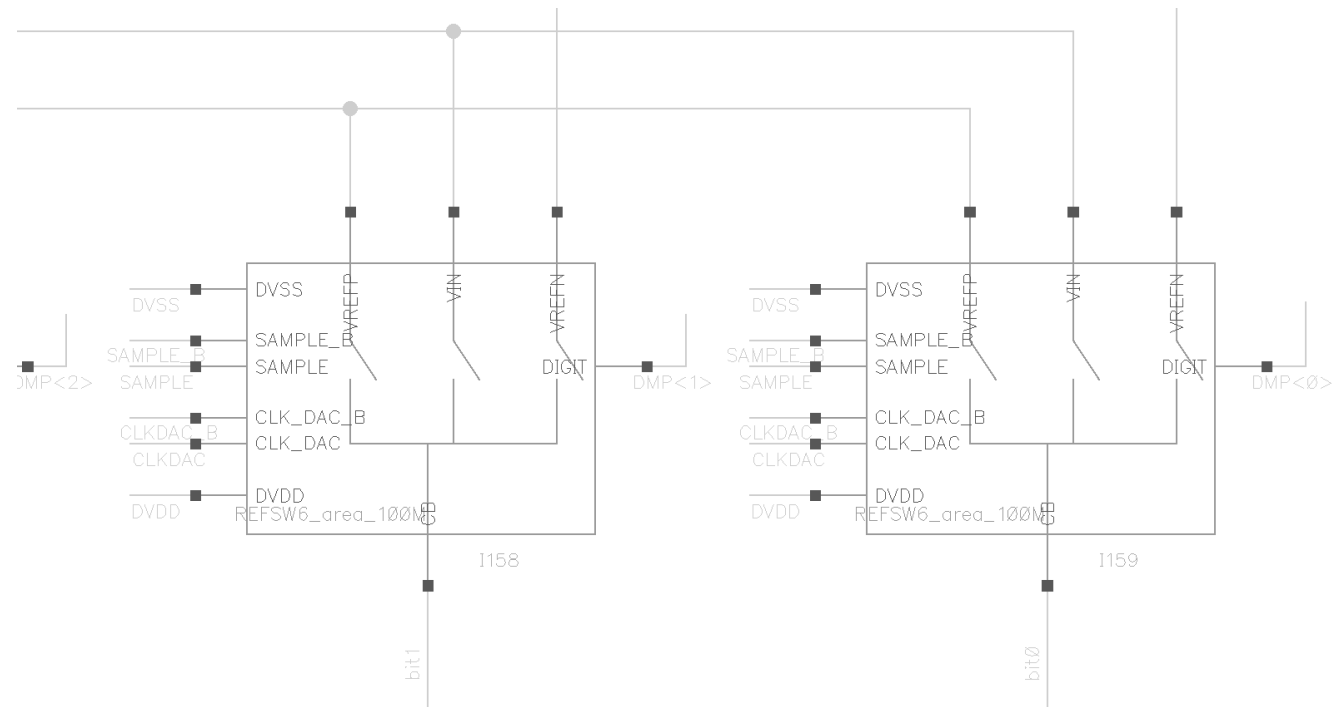


Fig 6: CDAC reference switch and control signals

CDAC SWITCH

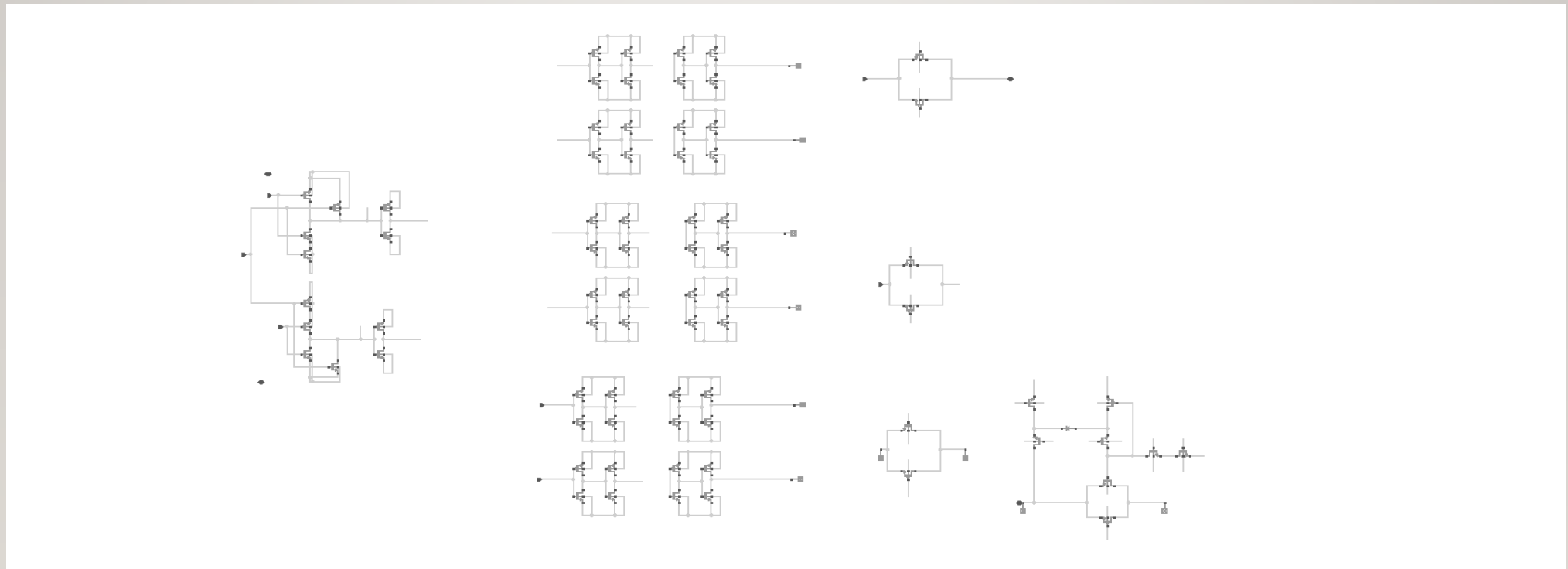


Fig 7: Reference switch and control signals

DOUBLE TAIL COMPARATOR

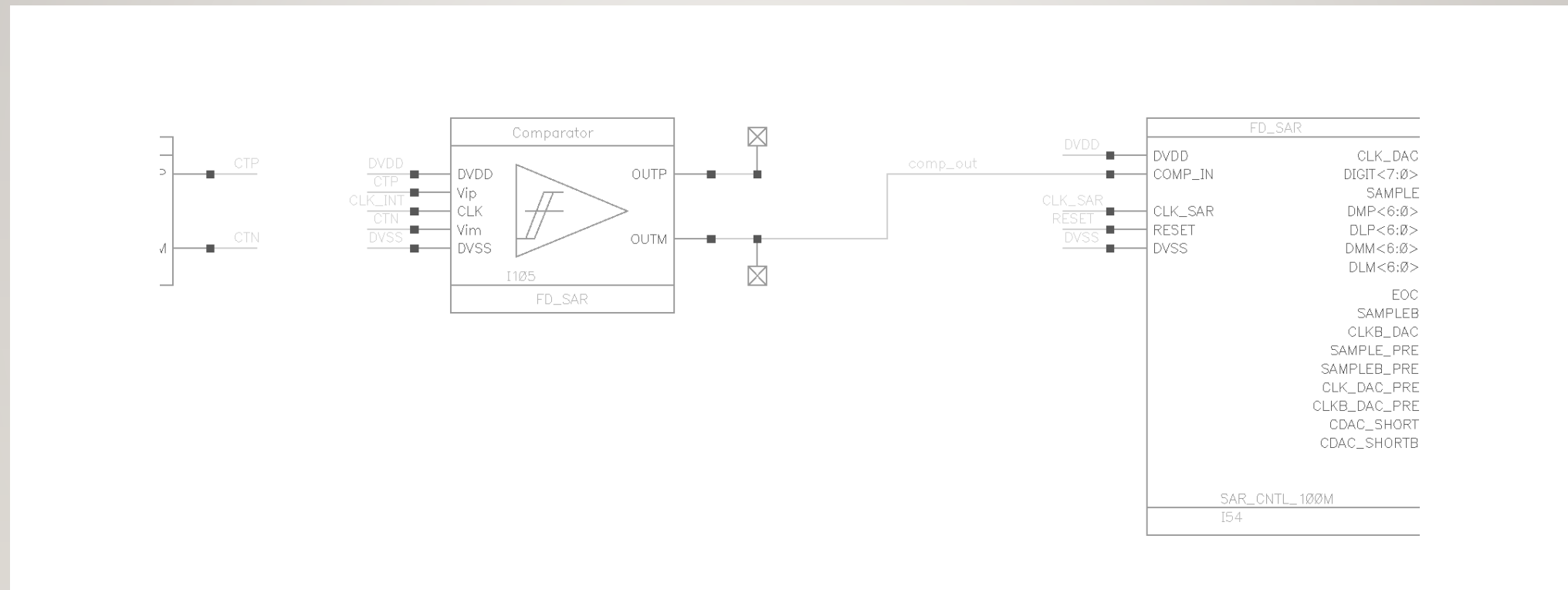


Fig 4: Comparator symbol and control signals

COMPARATOR SCHEMATIC

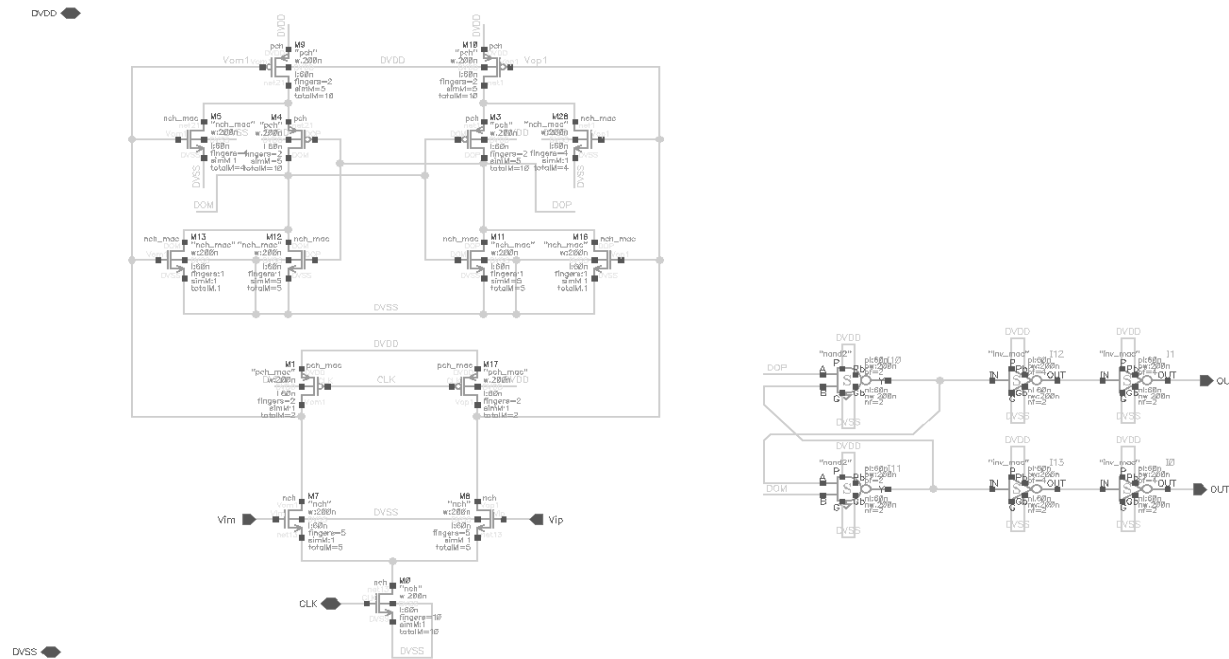


Fig 5: Double-tail comparator with SR latch

SAR LOGIC BLOCK

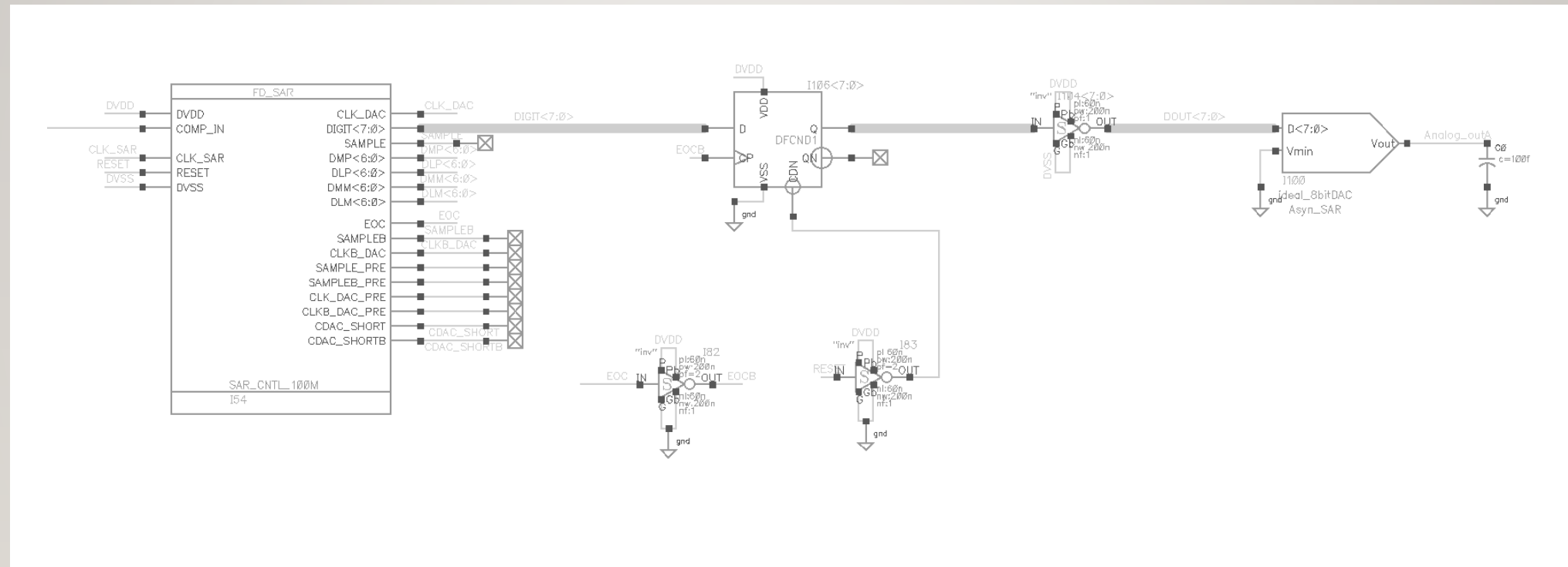


Fig 8: SAR logic and signals

SYNCHRONOUS FD LOGIC

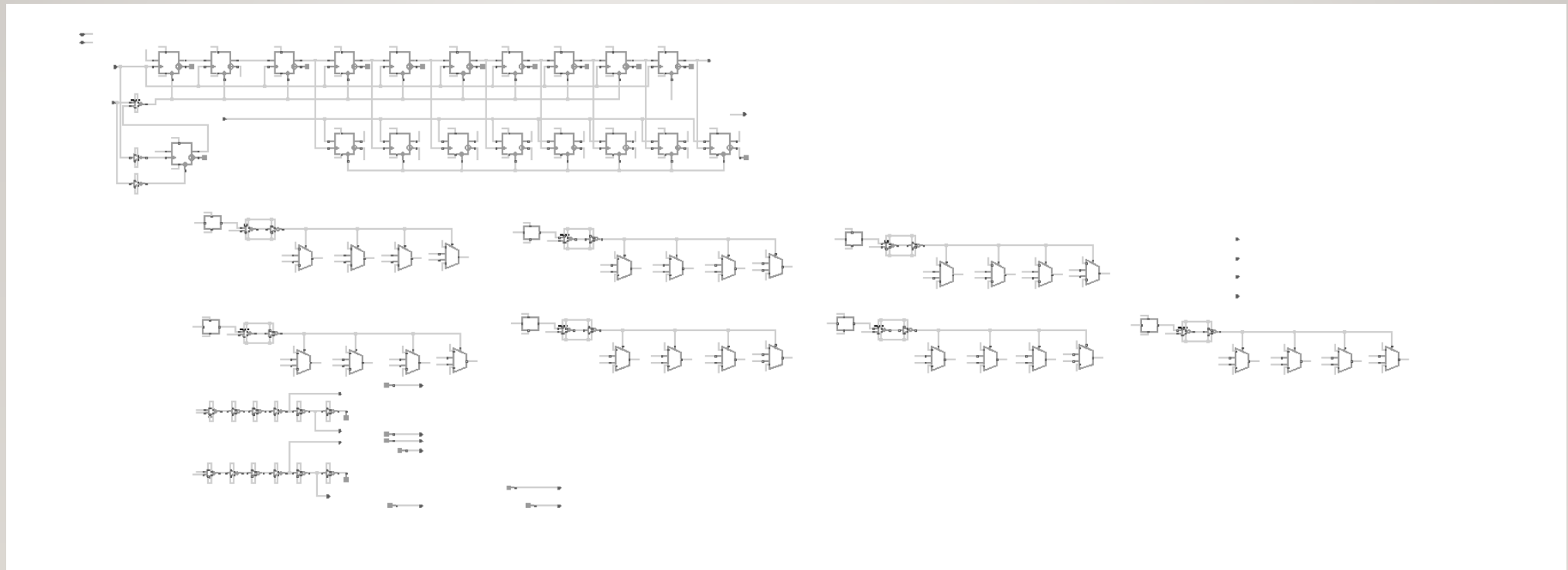


Fig 9: Sequencer, SAR registers, DAC control

SEQUENCER AND CODE REGISTERS

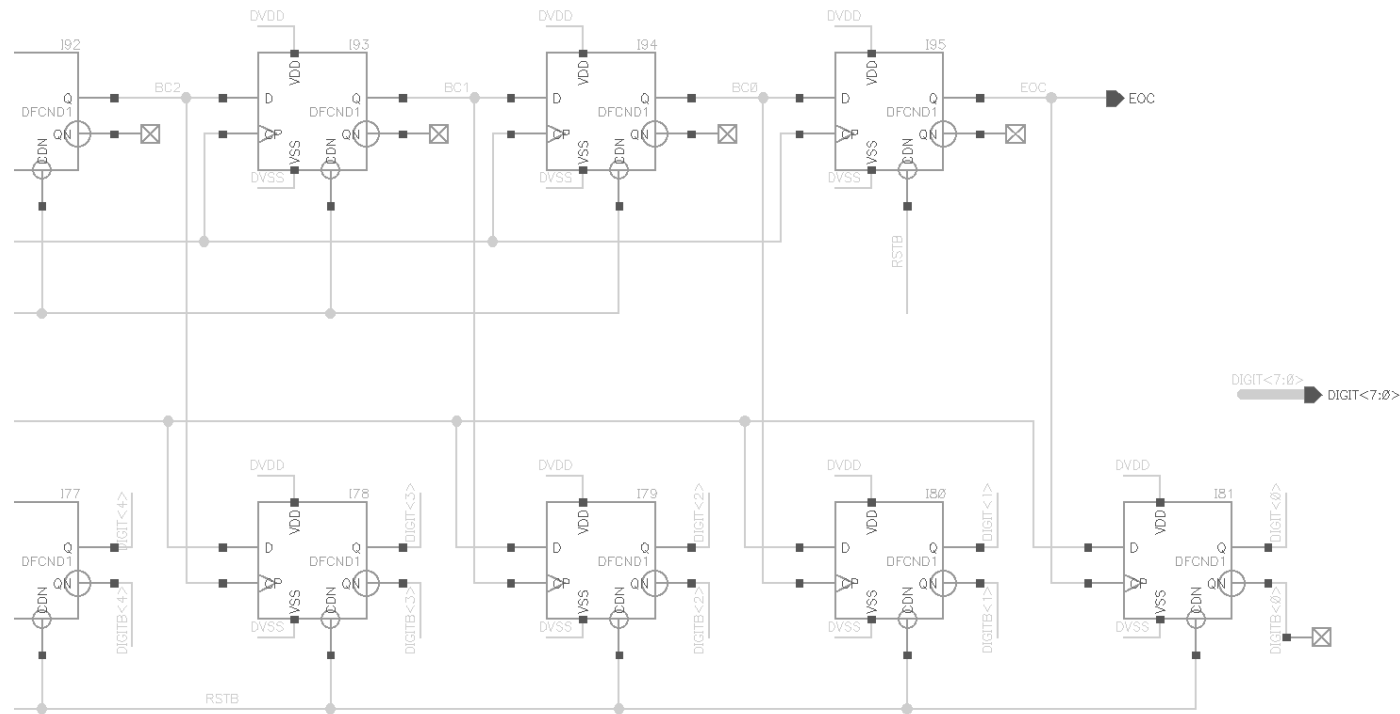


Fig 10: Sequencer and SAR registers

DAC CONTROL

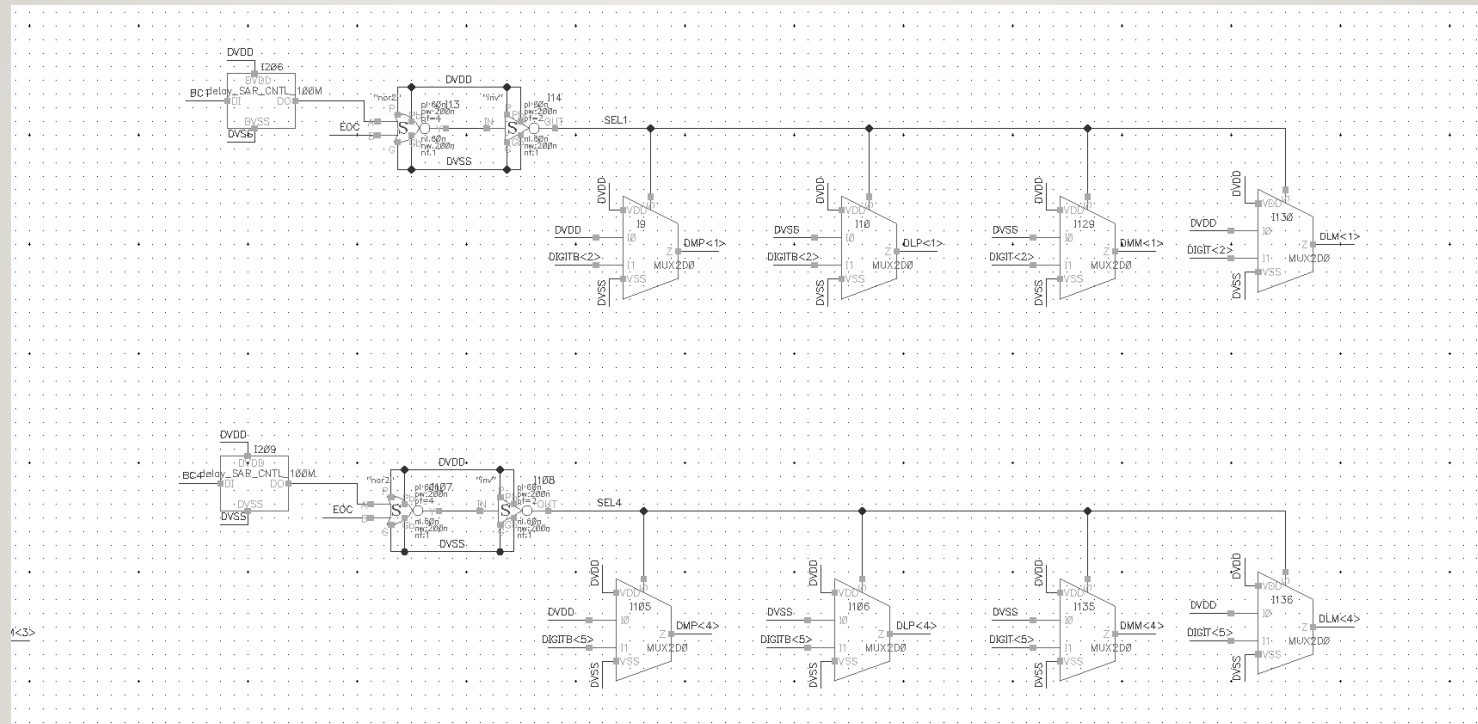


Fig 11: DAC control for upper and lower DAC

Upper DAC

Complementary Lower DAC

SIMULATION RESULTS

WAVEFORM

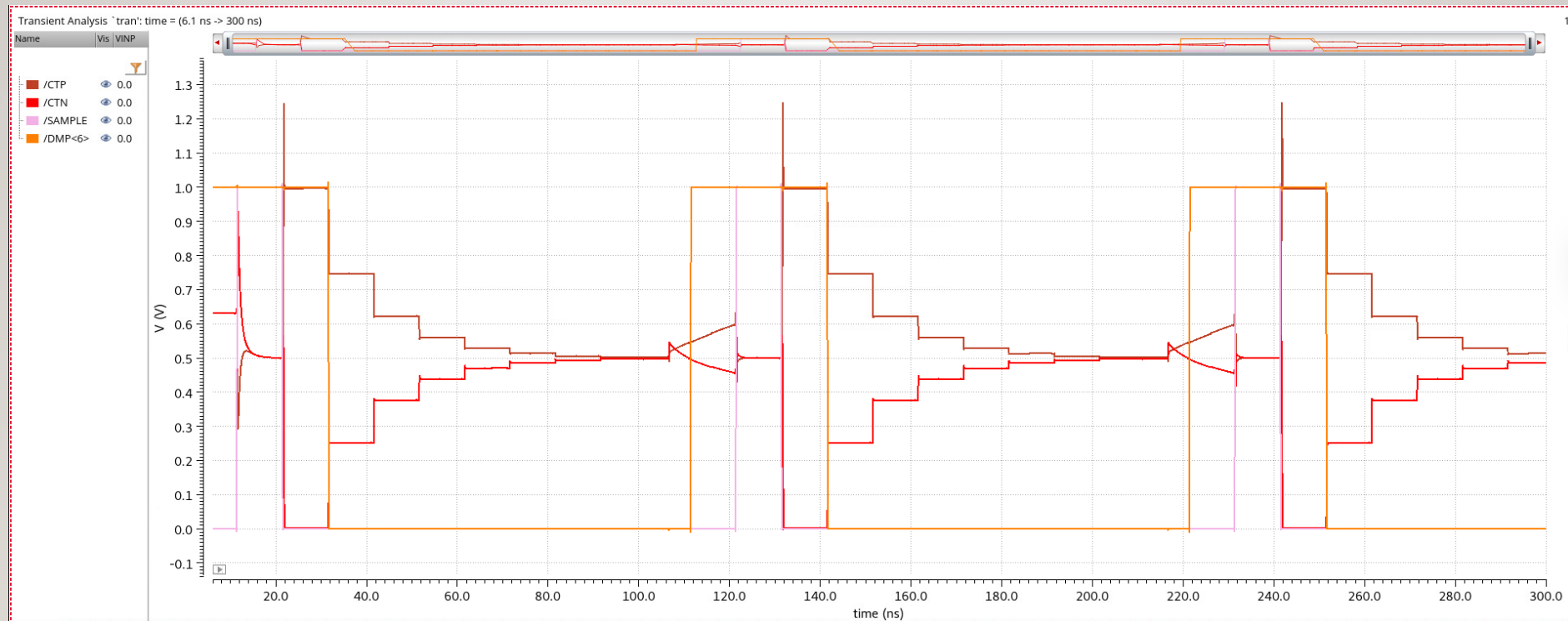


Fig 12: Transient simulation for a conversion cycle

RAMP

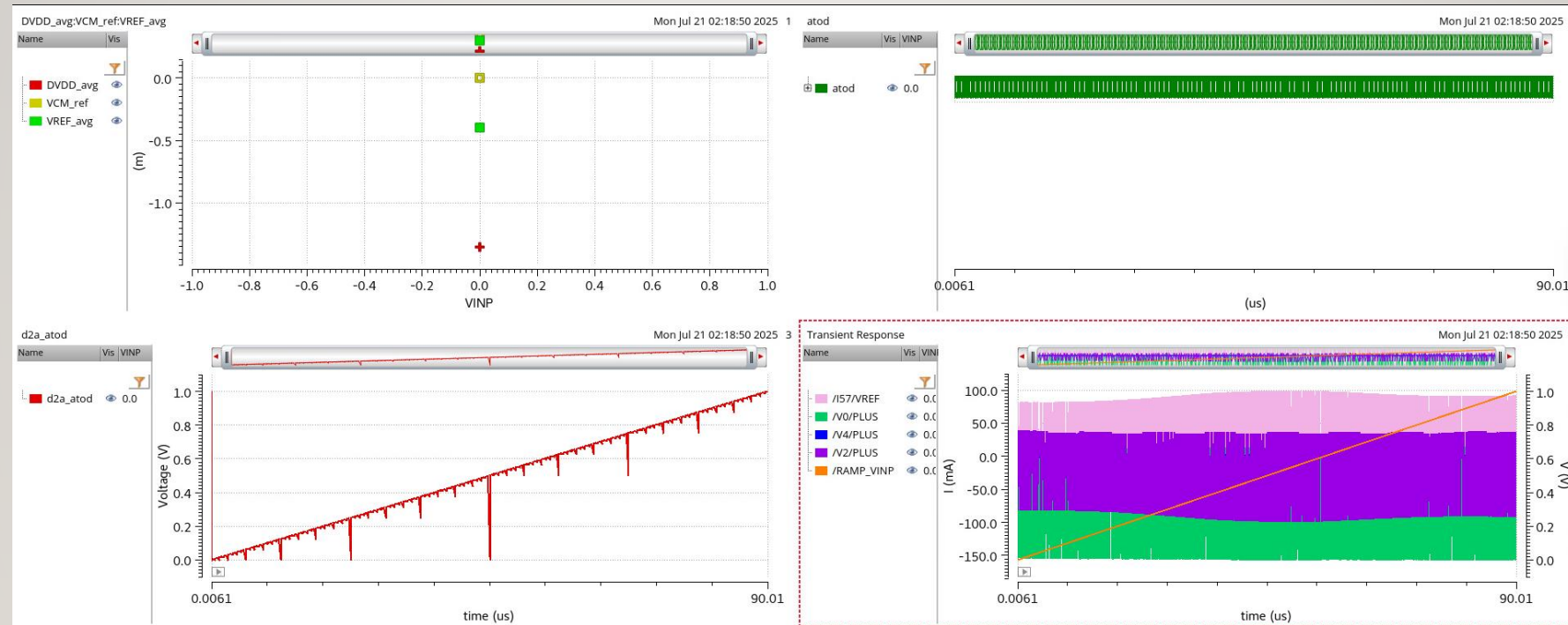


Fig 13: Full-scale ramp used for PSCA security characterization

FFT

- Unsecure time - 450.68u
- Target frequency around – 1Meg
- Points – 4096
- Sampling Rate = 9.09MSPS
- $\Delta f = \text{Sampling} \frac{\text{frequency}}{\text{Number of points}} = \frac{9.09\text{Meg}}{4096} = 2.21946 \text{ KHz}$
- Target frequency = k. Δf ; so k = 451 nearest round number
- Trecord = 4096*110ns = 450.6+tdelay

FFT

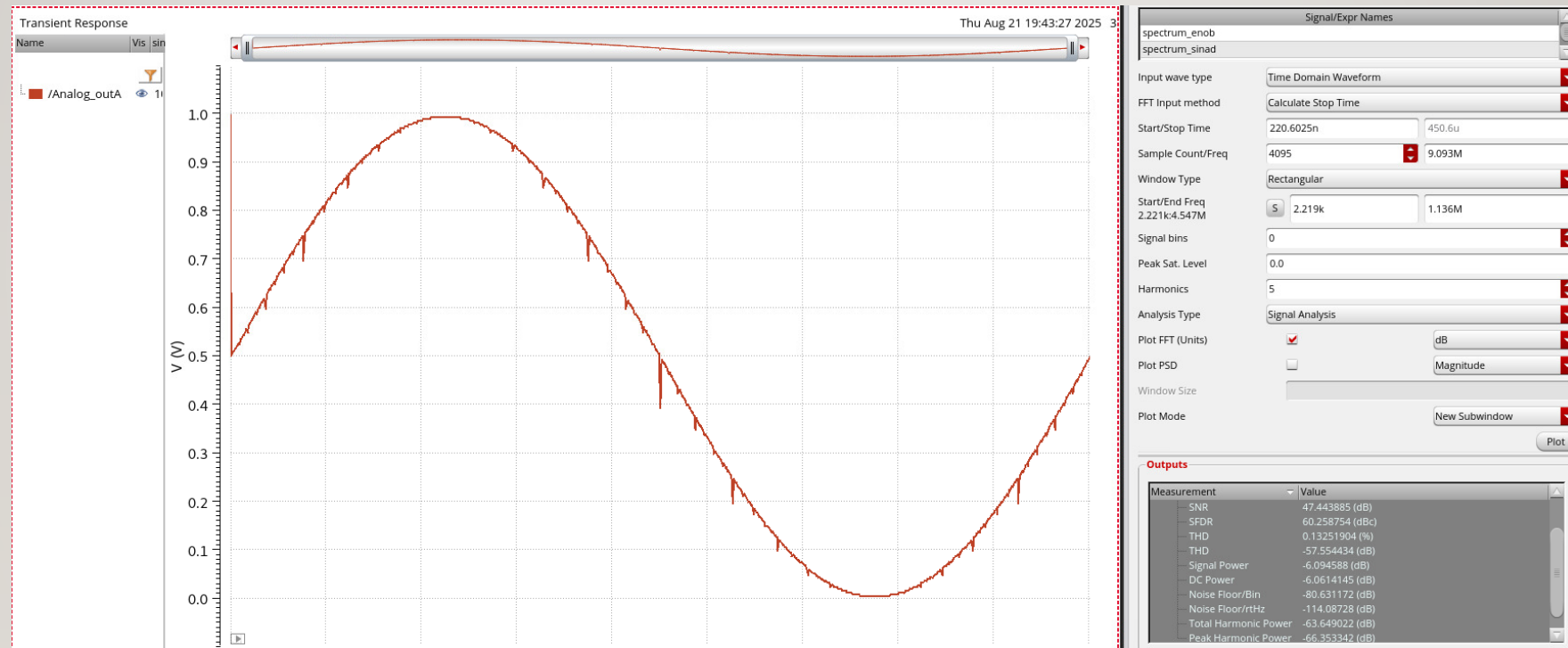


Fig. I4: Dynamic performance of the ADC

FFT RESULTS

- ENOB 7.526
- SINAD 47.07
- SNR 47.44
- SFDR 60.26
- THD 132.5E-3
- THDDB -57.55
- Sig Power - 6.095
- DC Power - 6.061
- SNB - 80.63
- SNRH - 114.1
- Total harmonic power - 63.65
- Peak Harmonic Power - 66.35
- FoMw = 7.49fF/c-step
- FoMs = 67.5fj/c-step
- FoMs(db) = 225.8dB

16	ENOB	7.526
17	SINAD	47.07
18	SNR	47.44
19	SFDR	60.26
20	THD	132.5m
21	THD_DB	-57.55
22	Signal_Power	-6.095
23	DC power	-6.061
24	SNB	-80.63
25	SNRH	-114.1
26	Total Harmonic Power	-63.65
27	Peak Harmonic Power	-66.35

DNL INL NORMALIZED

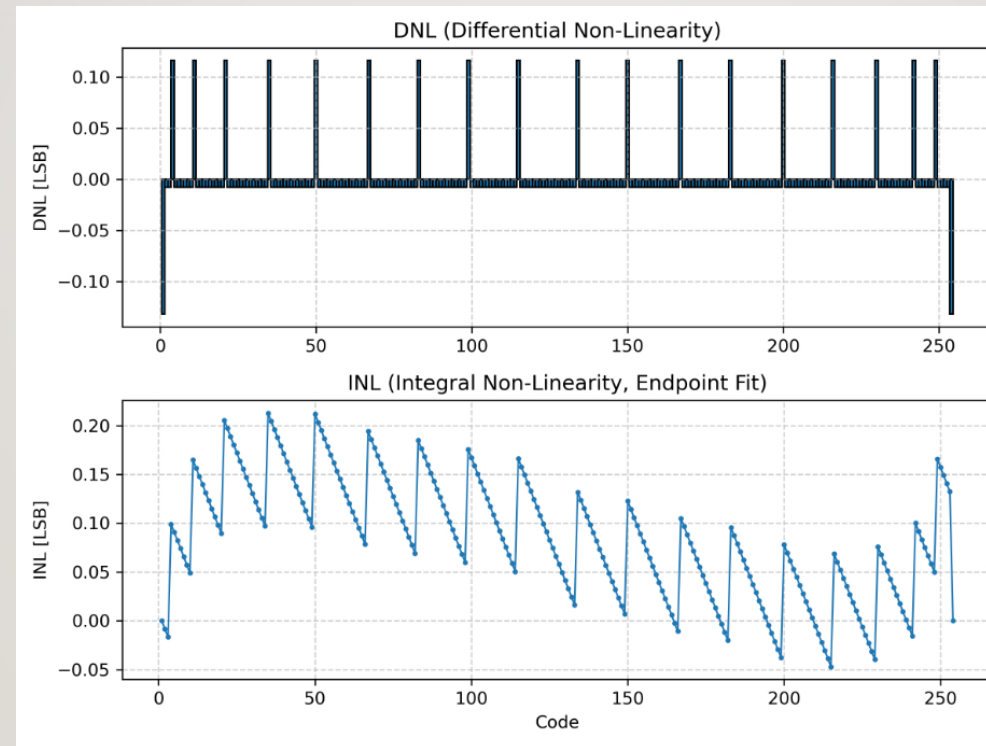


Fig 15: DNL (LSB) min: -0.1318, max: 0.1162; INL (LSB) min: -0.1665, max: 0.1440

POST PROCESSING

- DNL and INL were executed in Python
- FFT analysis was also verified in Python.
- Matplotlib is used for plotting, please refer to the files for code.

POWER CONSUMPTION – UNSECURE FINAL

Test ^	Output	Min	Max	Mean	Median	Std Dev	Spec	Pass/Fail
Tran	DVDD_avg	-78.95u	-77.1u	-77.72u	-77.67u	353.8n		
Tran	VCM_ref	3.977u	4.043u	4.007u	4.008u	11.93n		
Tran	VREF_avg	-64.39u	-52.74u	-60.35u	-61.73u	3.644u		
Tran	average(clip(IT("/V4/PLUS") 1.4e-07 2.4e-07))	-3.179n	11.59n	2.128n	1.406n	3.055n		
Tran	average(clip(IT("/V2/PLUS") 1.4e-07 2.4e-07))	-66.35u	-53.89u	-62.29u	-63.33u	3.652u		
Tran	average(clip(IT("/V0/PLUS") 1.4e-07 2.4e-07))	-78.04u	-75.88u	-76.67u	-76.63u	398n		
Tran	Value	1	254	127.5	127.5	73.32		

Fig 16: Power consumption for FoM

COMPARISON TABLE

TABLE II
SECURE ADC COMPARISON

Publication	TCAS-II'20 [1]		JSSC'21 [6]		CICC'22 [2]		VLSI'22 [3]		CICC'23 [4]		HOST'24 [5]		This Work	
Process (nm)	180		65		65		65		65		65 ^a		65 ^a	
Supply (V)	N/A ^b		1.2		1.2		1.2		1.2		1		1	
Resolution (bits)	10		12		8		12		12		8		8	
Topology	Single-Ended		Differential		Differential		Differential		Differential		Differential		Differential	
Protected	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes
Power (μ W)	63.5	65	83.2	158.5	43.4	50.2	539.8	539.8	722	698	145	150.7	138.96	373.45
Sample Rate (MS/s)	1.07	1	1.25	1.25	3.33	2	25	25	45	40	20	20	9.09	11.11
Area (mm^2)	0.07	0.075	0.34	0.5	0.064	0.073	0.072	0.072	0.075	0.075	0.015	0.017	0.356	0.384
ENOB (bit)	8.8	8.7	11.2 ^c	11.2 ^c	7.2	7.7	10.9	10.9	10.9 ^c	10.8 ^c	7.86	7.8	7.52	7.91
FoM _W (fJ/c.-s.)	130.8	151.5	27.9	54.3	88.6	120.7	11.3	11.3	8.5	9.8	31	33.8	7.49	124.30
INL	-1.2	-1.2	-0.87	-1.01	N/A ^b	-0.46	-0.76	-0.76	-0.67	-0.73	-0.53	-0.56	-0.16	-0.74
	+1.2	+1.2	+0.80	+0.86		+0.44	+0.67	+0.67	+0.72	+0.69	+0.53	+0.58	0.11	0.59
DNL	-0.6	-0.6	-0.53	-0.72	N/A ^b	-0.31	-0.49	-0.49	-0.62	-0.68	-0.5	-0.6	-0.13	-0.62
	+0.6	+0.6	+0.79	+0.77		+0.37	+0.35	+0.35	+0.37	+0.31	+0.45	+0.52	0.14	0.61
SFDR (dB)	64.5	64.3	86	89.6	53.7	54.6	86.6	86.6	80.5	80.2	N/A ^b	N/A ^b	60.26	60.05
Leakage RMSE (LSBs)	- ^d	- ^d	117.74/ 4096	384.04/ 4096	0.7/ 256	58/ 256	14.21/ 4096	1625.39/ 4096	52.76/ 4096	1985.25/ 4096	24.5/ 256	103/ 256	30.29/ 256	112.28/ 256
NRMSE	- ^d	- ^d	0.0287	0.0938	0.0027	0.2266	0.0035	0.3968	0.0129	0.4847	0.095	0.42	0.1183	0.4386
Random Bits (Mb/s)	NA	1	NA	0	NA	360 ^e	NA	275	NA	4080 ^e	NA	200	NA	0

^aSimulation only

^bValue not disclosed

^cCalculated from FoM_W, Power, and Sample Rate

^dReported an unprotected leakage ENOB of 4.6 bits and a protected leakage ENOB of 0.8, RMSE was not reported

^eA variable amount of random bits are required, the reported value is the average per conversion

Table I: Comparison with other works

FOR MORE INFORMATION

- Reach out to me at contact@nipunkaushik.com