FLASH-SAR HYBRID ADC

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DESIGN PARAMETERS

- Resolution = 8-bit (2-bit Flash, 6-bit SAR)
- Cu (Unit capacitor) = 20f
- Vref = 1V
- Switching scheme = Charge recycling (Ginsberg et al., 2005 & 2006)
- CDAC arrangement = Split Capacitor DAC – MSB split into lower sub-DAC
- System Clock = 100 MHz

SCHEMATIC TOP

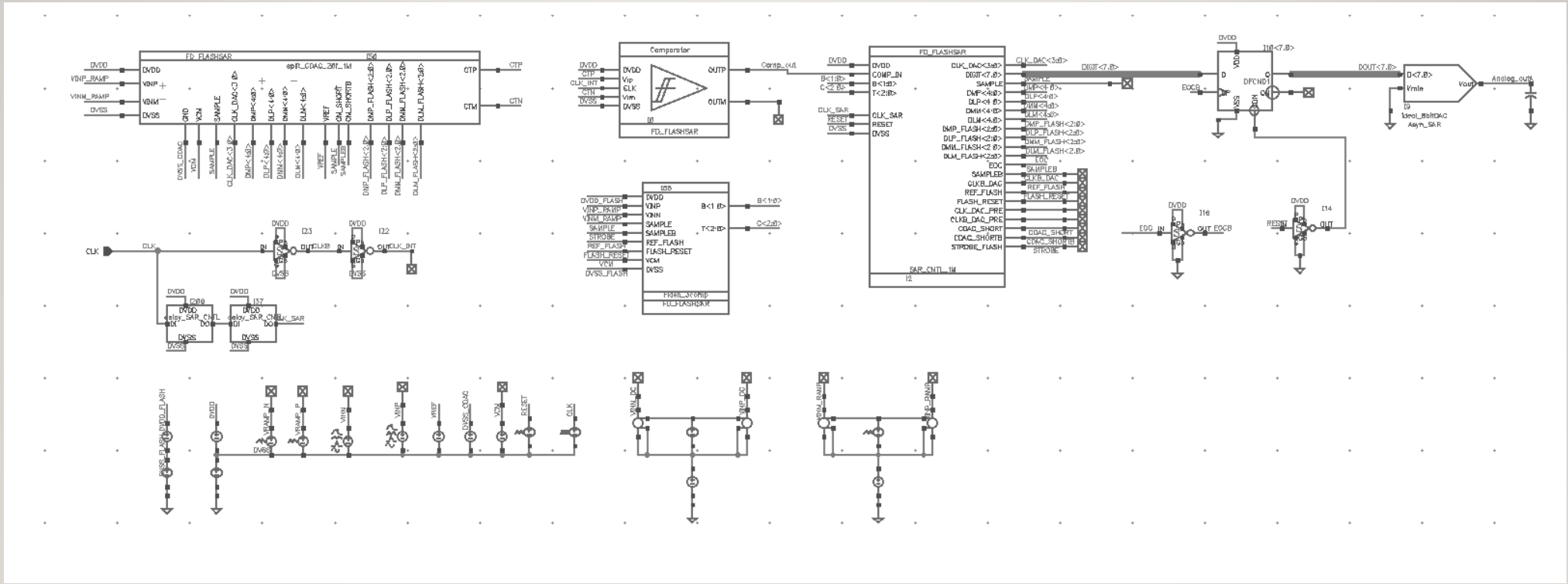

Fig 1: Top view of the hybrid ADC

2-BIT FLASH ADC

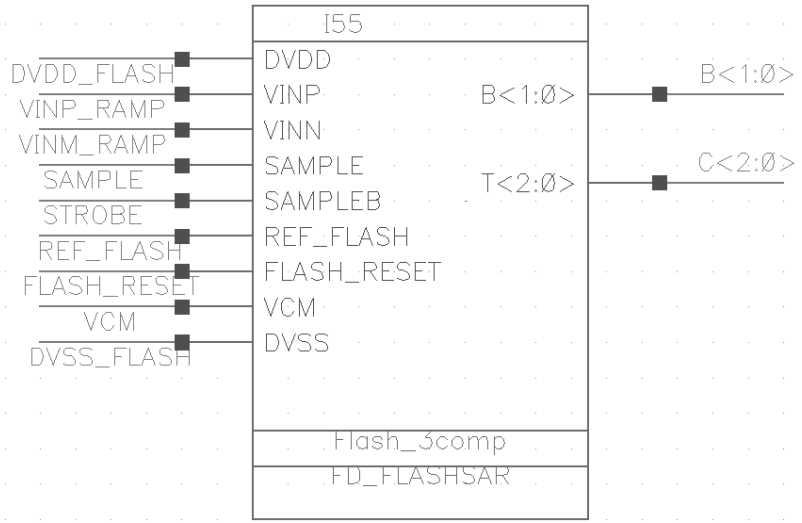

Fig 2: Flash ADC symbol and control signals

FLASH SCHEMATIC TOP

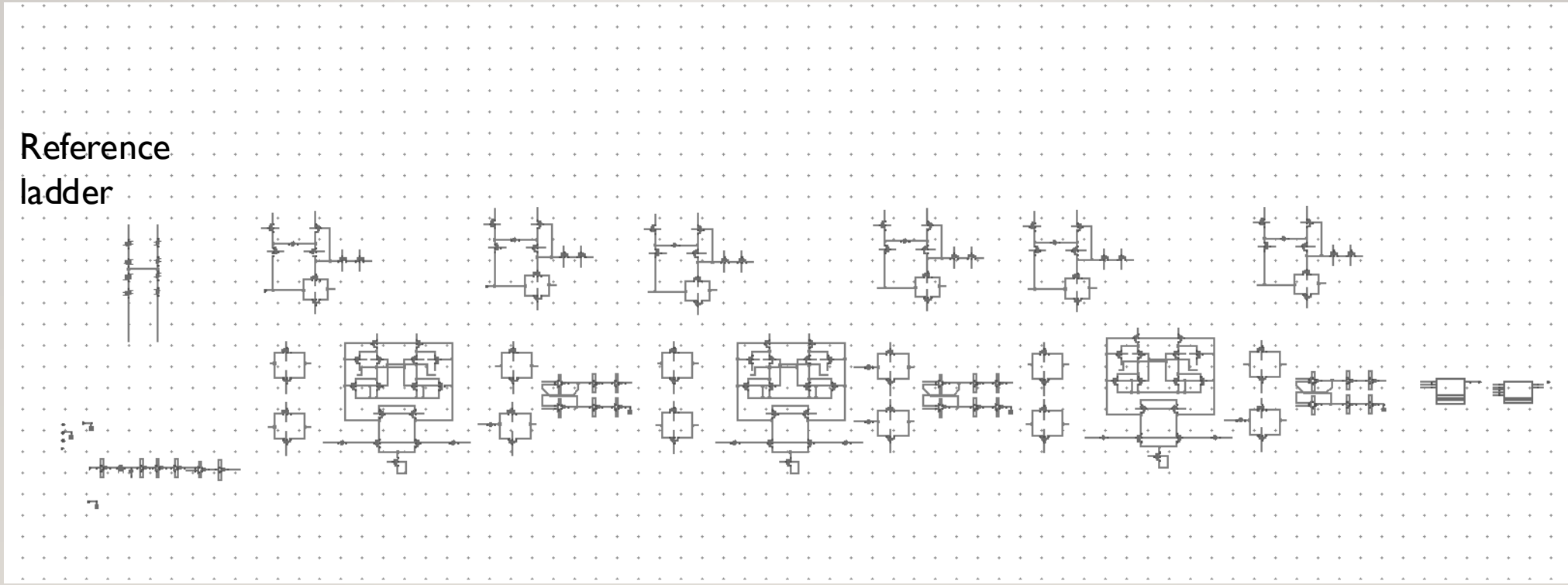

Fig 3: Flash schematic with bubble correction and encoder

BUBBLE CORRECTION AND 2-BIT ENCODER

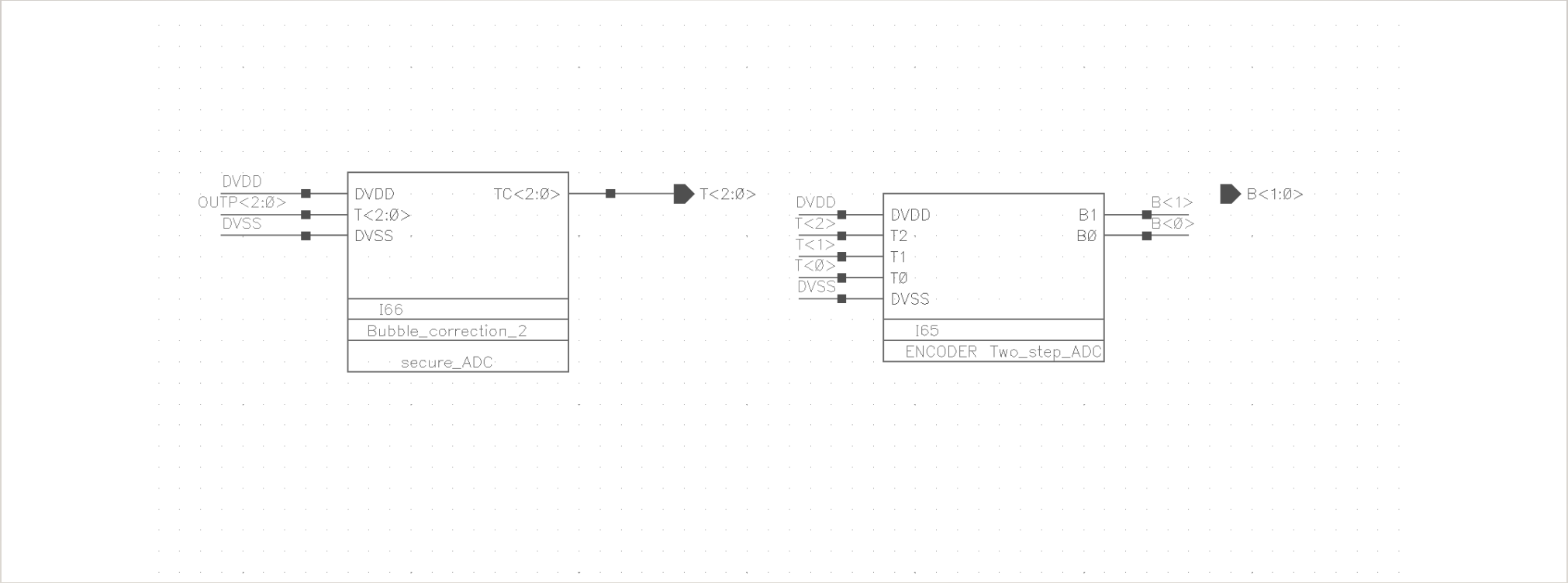

Fig 4: Symbol and controls for bubble correction and encoder

BUBBLE CORRECTION

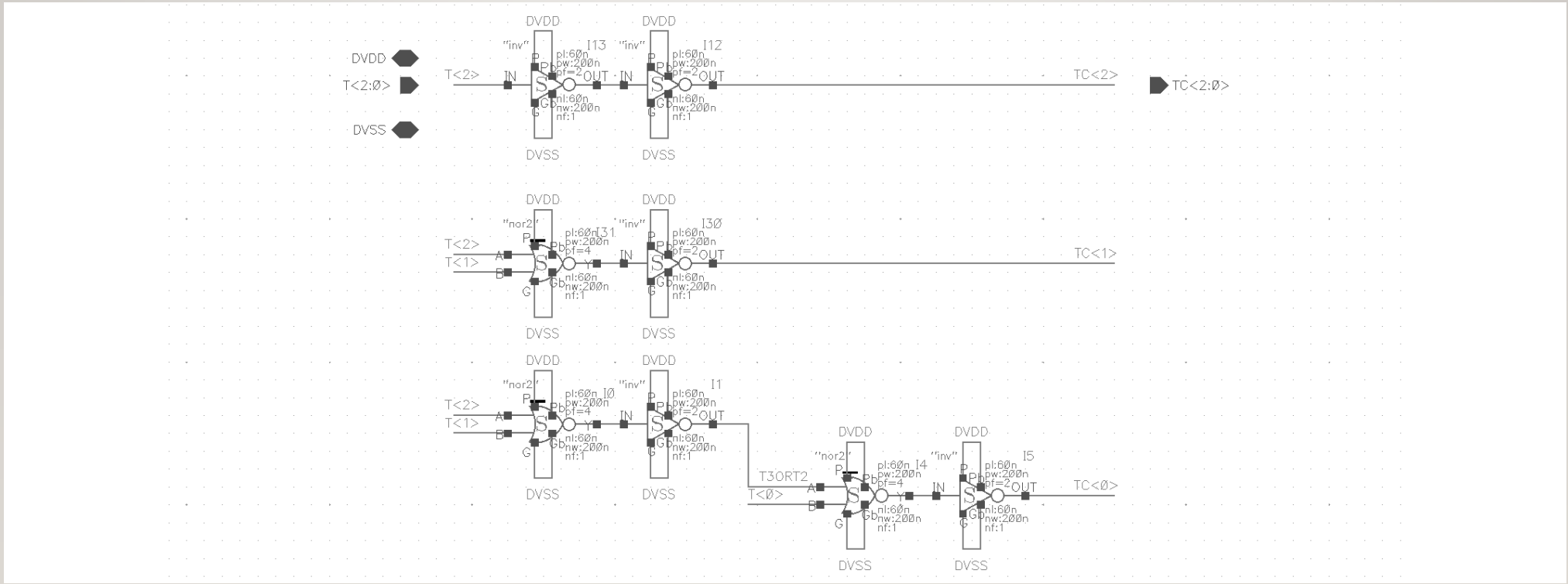

Fig 5: Schematic for bubble correction

THERMOMETER TO BINARY ENCODER

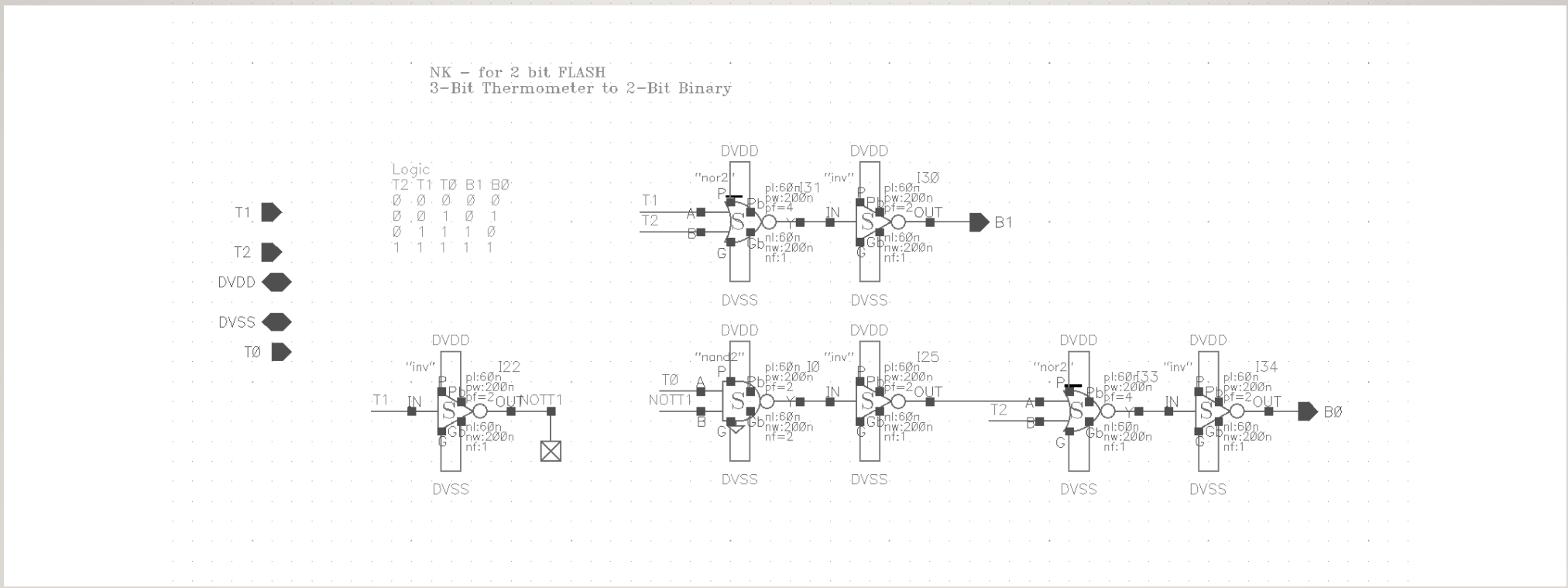

Fig 6: Schematic for Thermometer to Binary encoder

CDAC

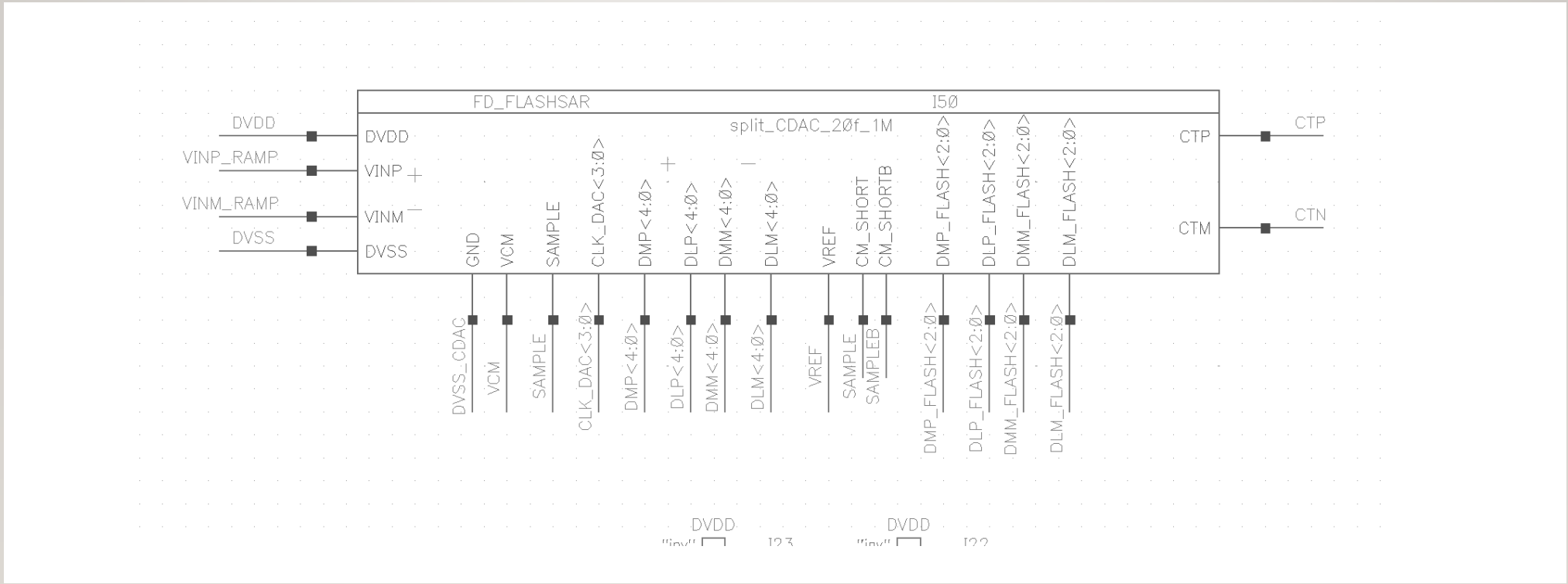

Fig 7: Symbol and control for CDAC

CDAC ARRANGEMENT

Controlled by
Thermometer bits

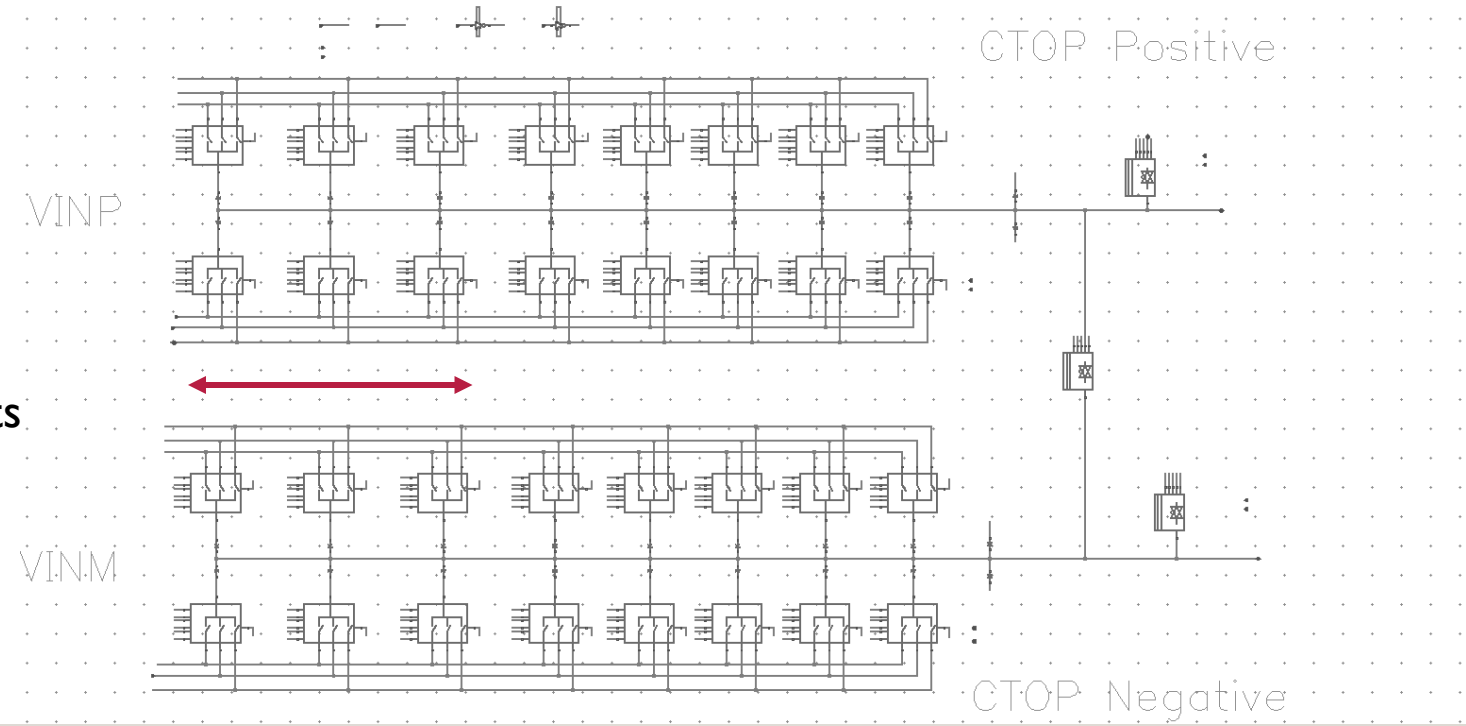

Fig 8: Schematic of Flash-SAR CDAC

SAMPLING SPREAD BY CLK_DAC

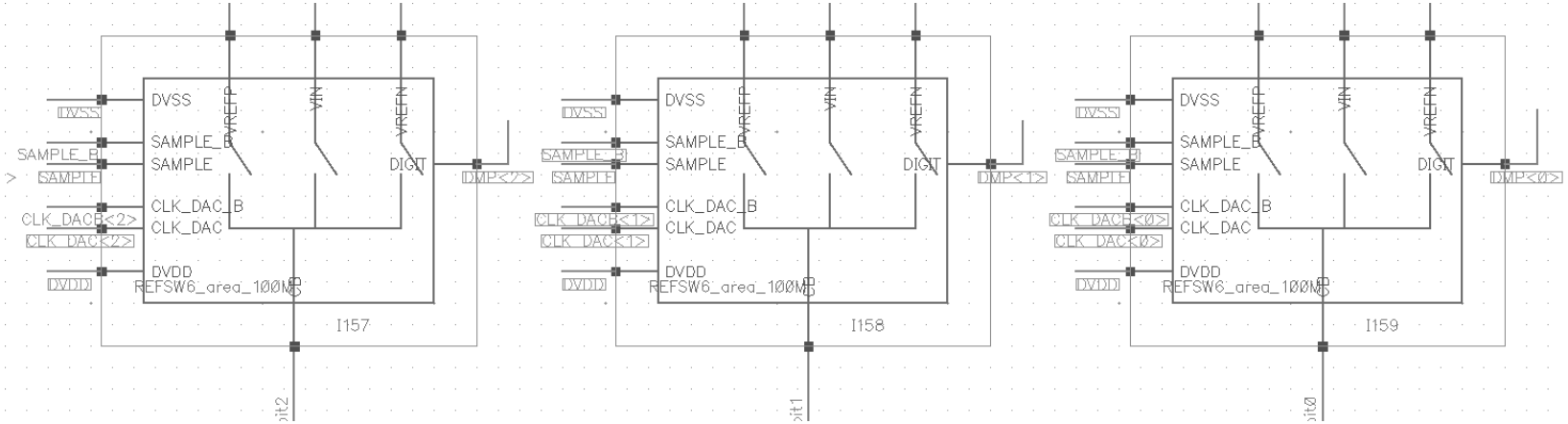

Fig 9: Soft start CDAC with delay to avoid current spike on VREF node

REFERENCE SWITCH SCHEMATIC

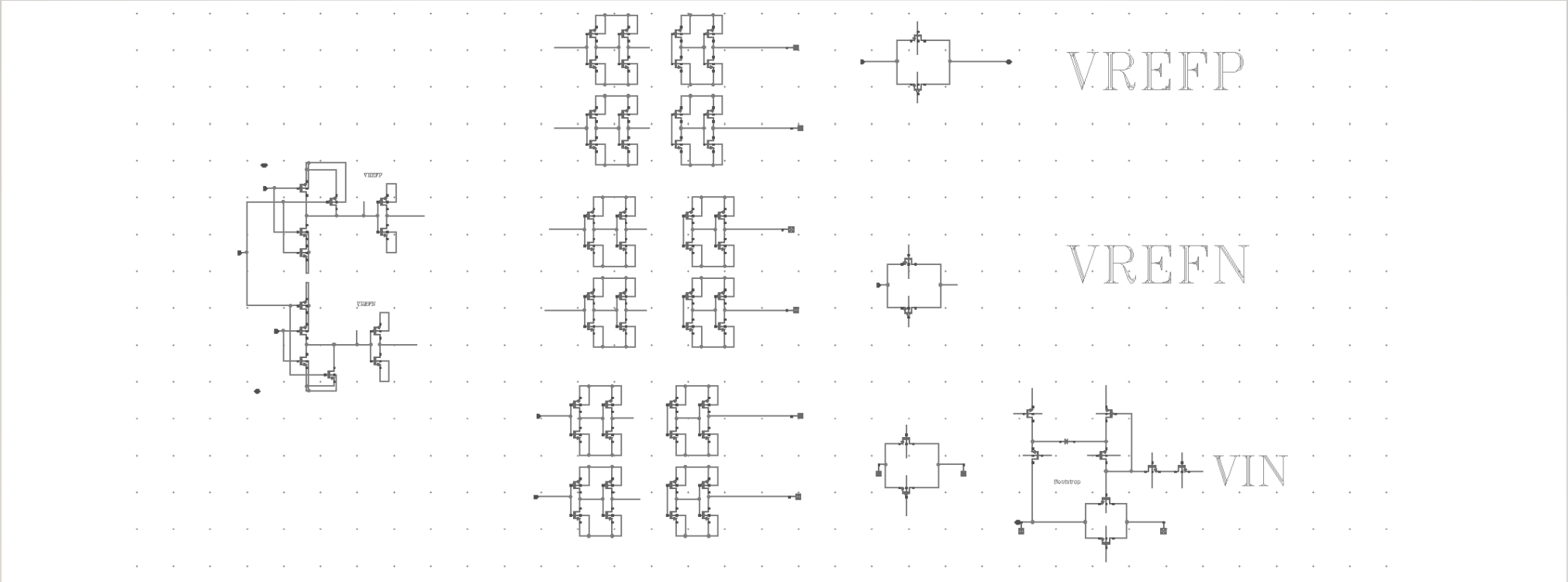

Fig 10: Reference switch schematic

SAR LOGIC

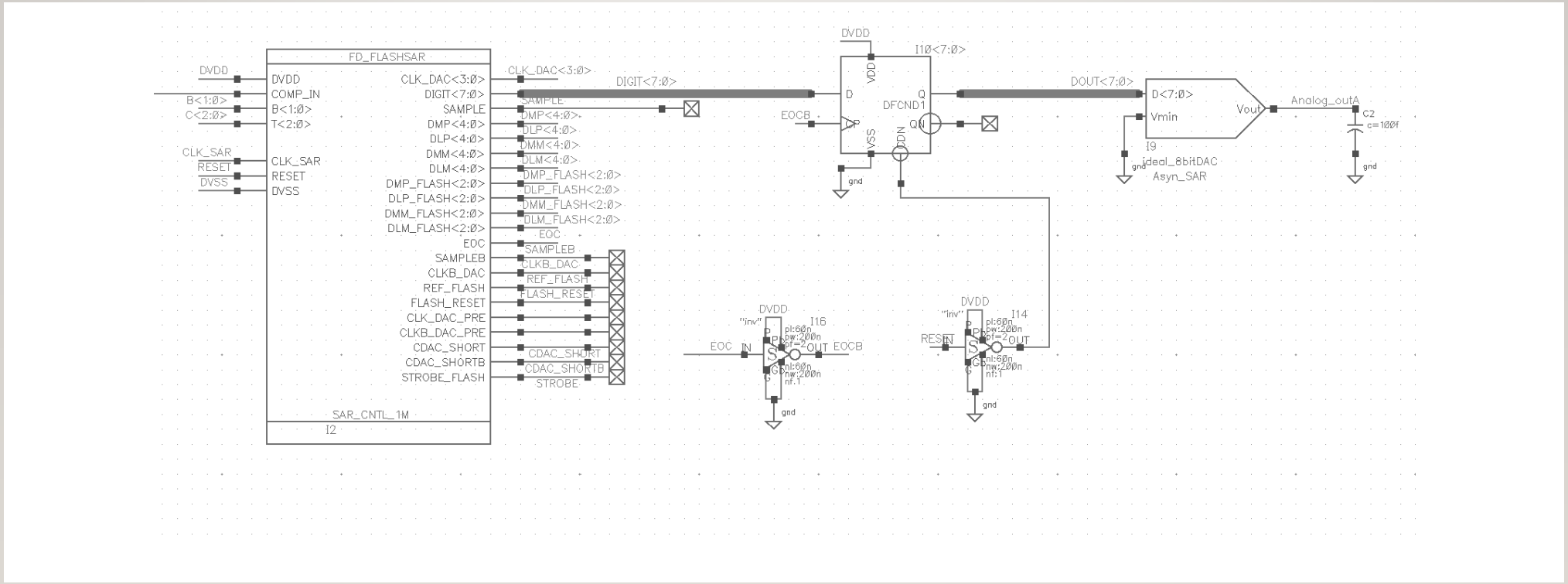

Fig 11: SAR Logic and control signals

SAR LOGIC AND CONTROL

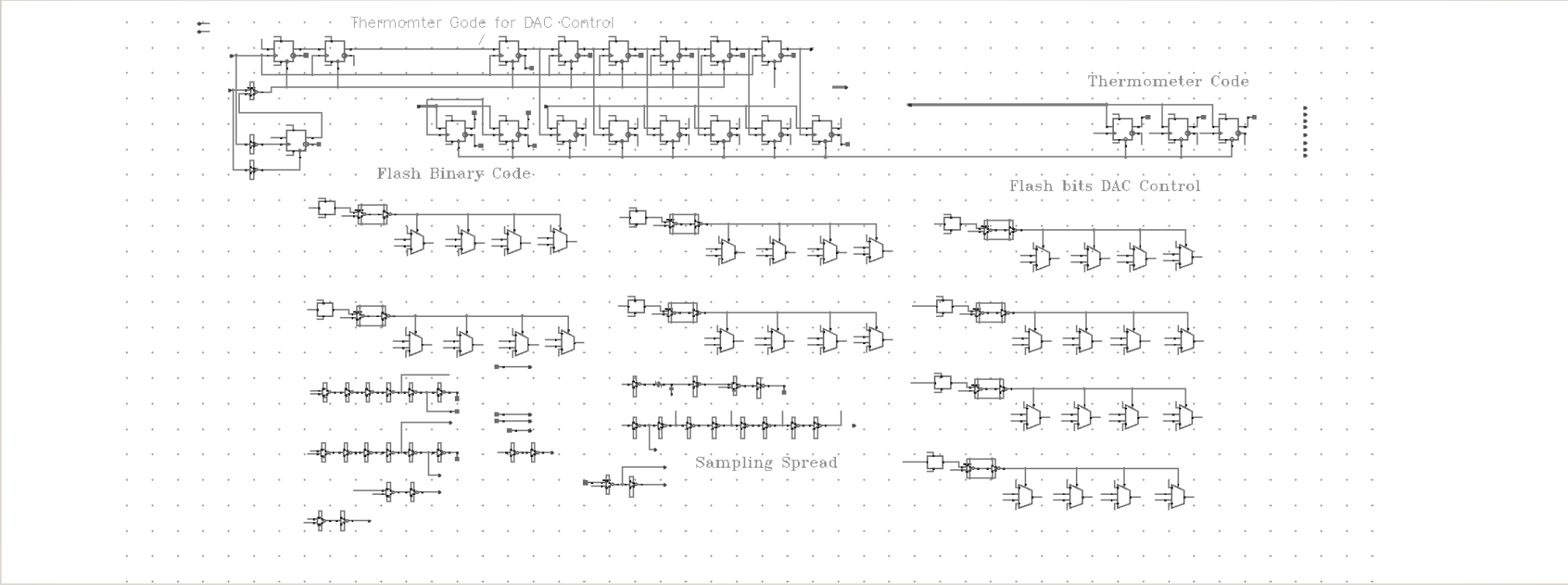

Fig 12: Sequencer, DAC control and code register

DAC CONTROL

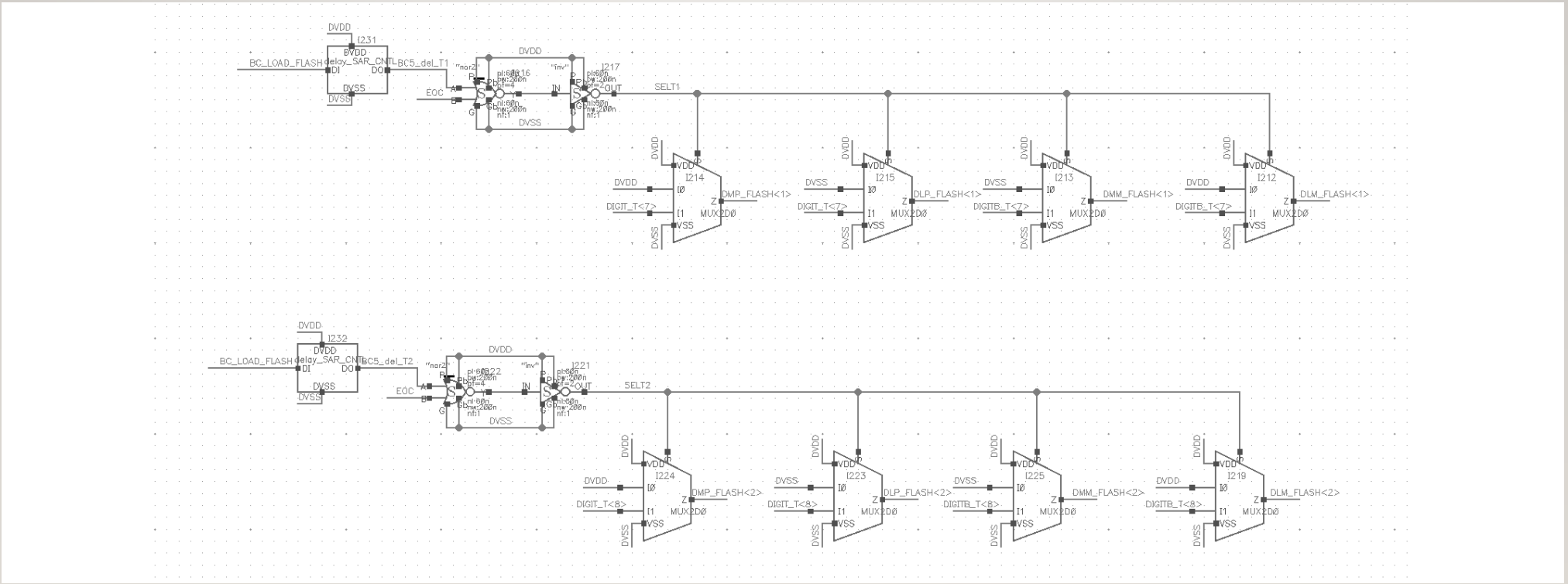

Fig 13: DAC control for thermometer bits

SIMULATION RESULTS

RAMP

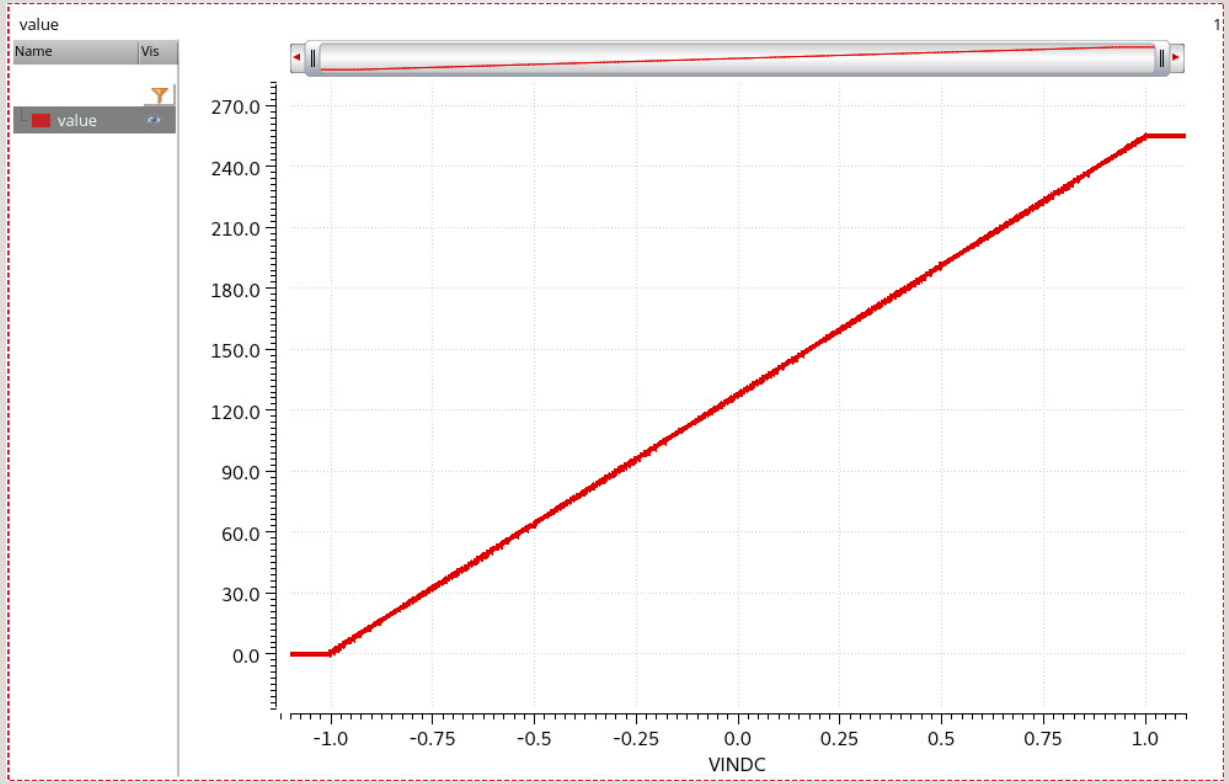

Fig 14: Digital code from 0 to 255 with input range of 2Vpp

SINGLE CYCLE

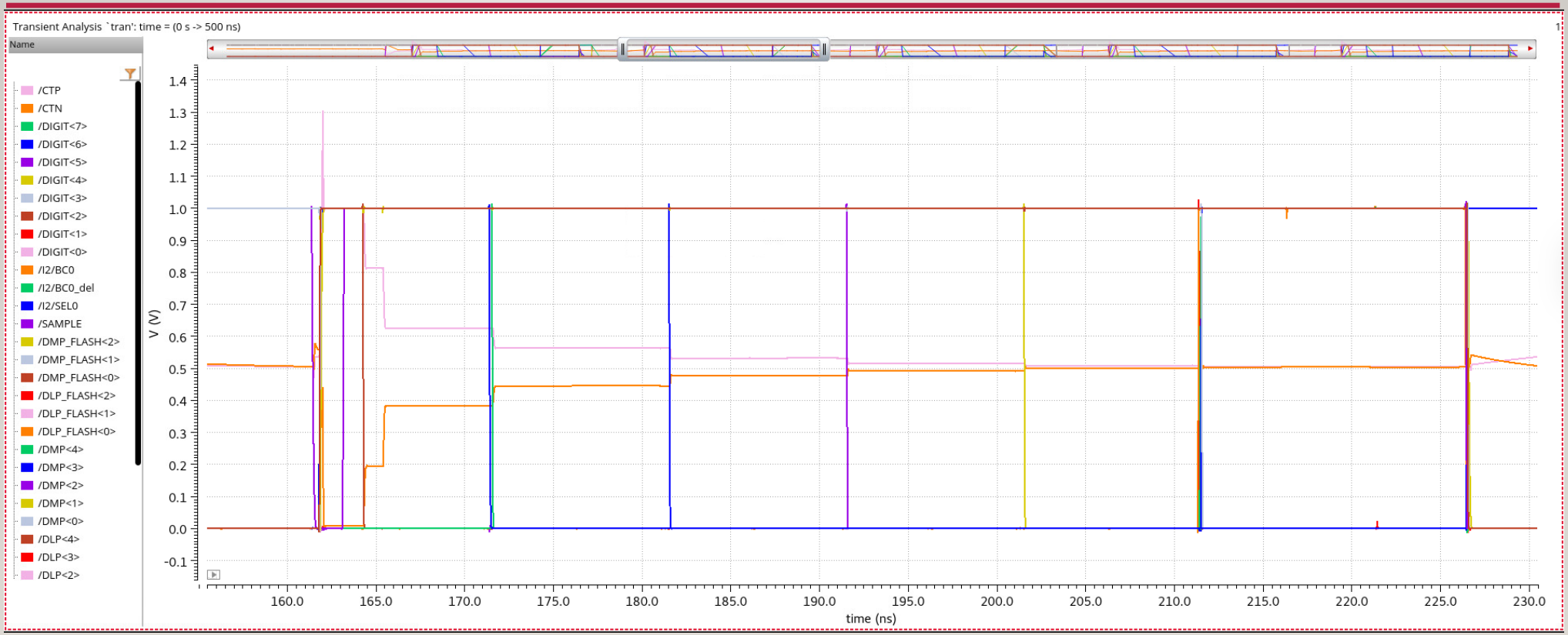

Fig 15: Single conversion cycle operation

SOFT START CDAC

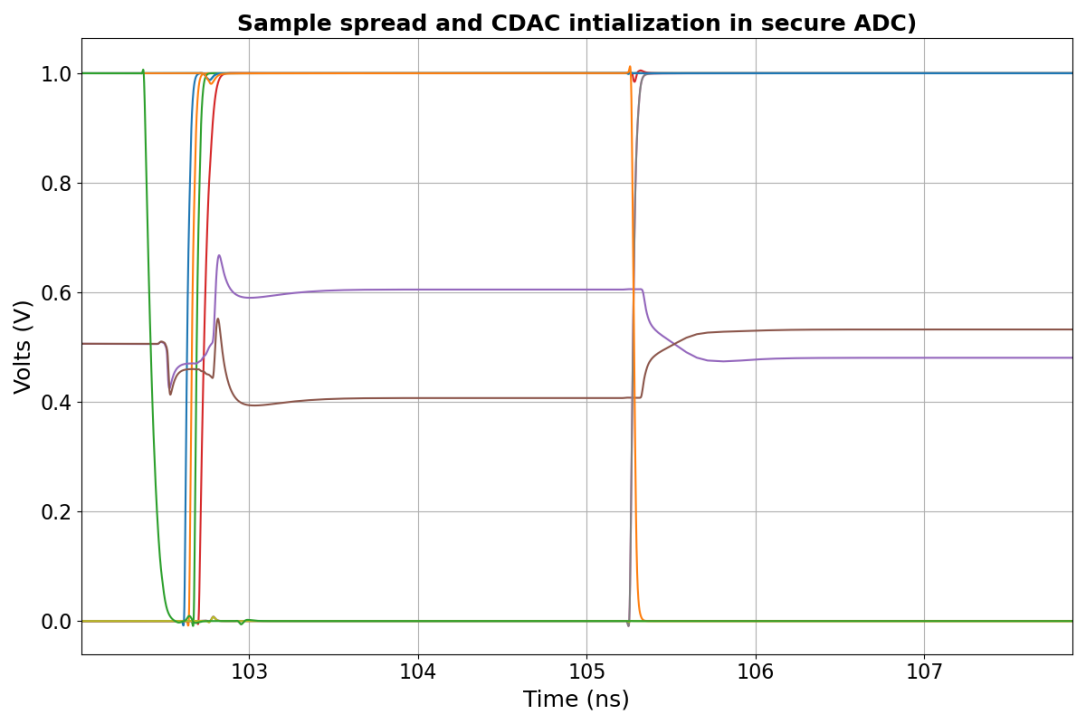

Fig 16: Soft start with CLK DAC

FFT PERFORMANCE

- --- ADC Performance ---
- Fundamental bin k: 1
- Peak frequency (Hz): 2712.673611
- Fundamental (RMS): 0.350971 V (-0.06 dBFS)
- Signal Power: 0.123181
- Noise Power: 1.339636e-06
- Harmonic Power: 9.894036e-08
- THD: 0.000896, -60.95 dB
- SNR: 49.64 dB
- SINAD: 49.33 dB
- ENOB: 7.901 bits
- SFDR: 60.98 dB
- Harmonic bins used: [2, 3, 4, 5]

DNL AND INL

DNL (LSB) min: -0.6281, max: 0.6115
Raw INL (LSB) min: -0.7186, max: 0.5913
Norm INL (LSB) min: -0.7457, max: 0.5057

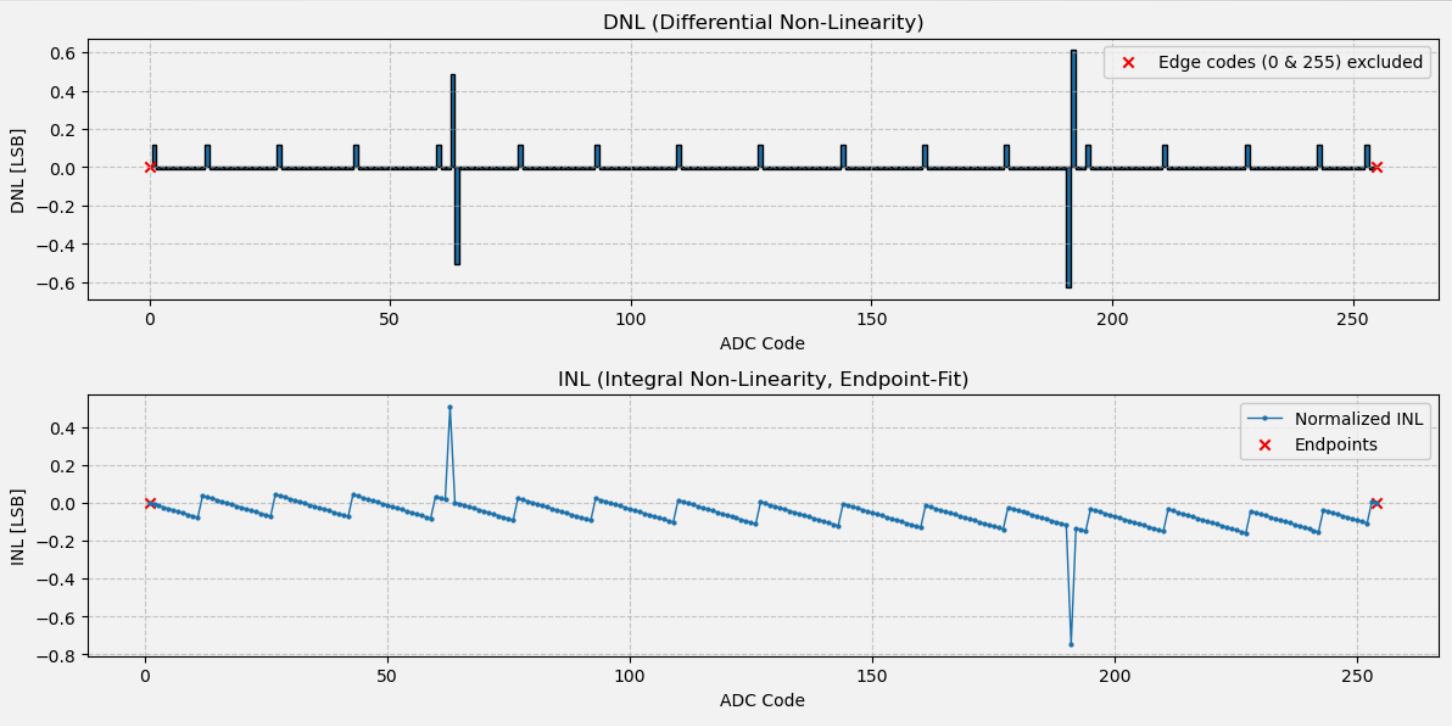

Fig 15: DNL and INL for Flash-SAR ADC

SAR ONLY DNL AND INL

DNL (LSB) min: -0.0083, max: 0.1157
Raw INL (LSB) min: -0.0744, max: 0.0661
Norm INL (LSB) min: -0.1072, max: 0.0399

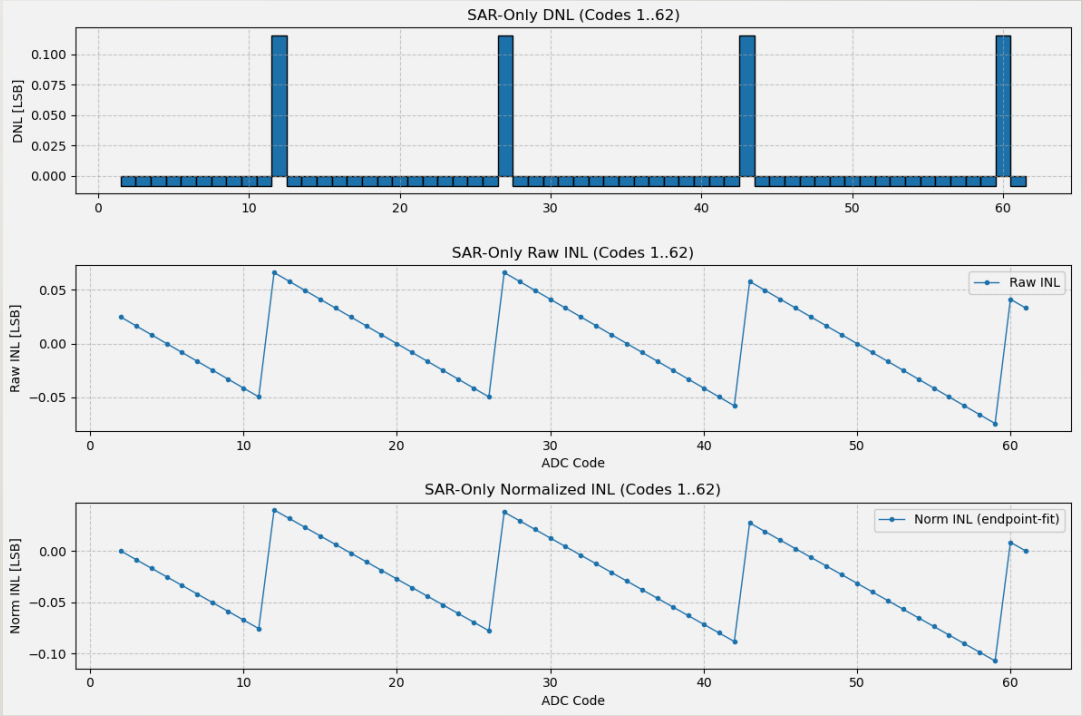

Fig 15: DNL and INL for SAR only portion

COMPARISON TABLE

TABLE II
SECURE ADC COMPARISON

Publication	TCAS-II'20 [1]		JSSC'21 [6]		CICC'22 [2]		VLSI'22 [3]		CICC'23 [4]		HOST'24 [5]		This Work	
Process (nm)	180		65		65		65		65		65[a]		65[a]	
Supply (V)	N/A[b]		1.2		1.2		1.2		1.2		1		1	
Resolution (bits)	10		12		8		12		12		8		8	
Topology	Single-Ended		Differential		Differential		Differential		Differential		Differential		Differential	
Protected	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes	No	Yes
Power (μW)	63.5	65	83.2	158.5	43.4	50.2	539.8	539.8	722	698	145	150.7	138.96	373.45
Sample Rate (MS/s)	1.07	1	1.25	1.25	3.33	2	25	25	45	40	20	20	9.09	11.11
Area (mm^2)	0.07	0.075	0.34	0.5	0.064	0.073	0.072	0.072	0.075	0.075	0.015	0.017	0.356	0.384
ENOB (bit)	8.8	8.7	11.2[c]	11.2[c]	7.2	7.7	10.9	10.9	10.9[c]	10.8[c]	7.86	7.8	7.52	7.91
FoM_W (fJ/c.-s.)	130.8	151.5	27.9	54.3	88.6	120.7	11.3	11.3	8.5	9.8	31	33.8	7.49	124.30
INL	-1.2 +1.2	-1.2 +1.2	-0.87 +0.80	-1.01 +0.86	N/A[b]	-0.46 +0.44	-0.76 +0.67	-0.76 +0.67	-0.67 +0.72	-0.73 +0.69	-0.53 +0.53	-0.56 +0.58	-0.16 0.11	-0.74 0.59
DNL	-0.6 +0.6	-0.6 +0.6	-0.53 +0.79	-0.72 +0.77	N/A[b]	-0.31 +0.37	-0.49 +0.35	-0.49 +0.35	-0.62 +0.37	-0.68 +0.31	-0.5 +0.45	-0.6 +0.52	-0.13 0.14	-0.62 0.61
SFDR (dB)	64.5	64.3	86	89.6	53.7	54.6	86.6	86.6	80.5	80.2	N/A[b]	N/A[b]	60.26	60.05
Leakage RMSE (LSBs)	-[d]	-[d]	117.74/ 4096	384.04/ 4096	0.7/ 256	58/ 256	14.21/ 4096	1625.39/ 4096	52.76/ 4096	1985.25/ 4096	24.5/ 256	103/ 256	30.29/ 256	112.28/ 256
NRMSE	-[d]	-[d]	0.0287	0.0938	0.0027	0.2266	0.0035	0.3968	0.0129	0.4847	0.095	0.42	0.1183	0.4386
Random Bits (Mb/s)	NA	1	NA	0	NA	360[e]	NA	275	NA	4080[e]	NA	200	NA	0

[a] Simulation only
[b] Value not disclosed
[c] Calculated from FoM_W, Power, and Sample Rate
[d] Reported an unprotected leakage ENOB of 4.6 bits and a protected leakage ENOB of 0.8, RMSE was not reported
[e] A variable amount of random bits are required, the reported value is the average per conversion

Table 1: Comparison with other works

THANK YOU