Foundations of Computer Systems Design Lab (CS2310)
Lab 3: Encoders, Decoders and Priority Encoders

20 August 2024

In this lab, we will learn how to implement *encoders* and *decoders* in Verilog, and then use them as building blocks to build higher level circuits for solving problems. In addition, we will also learn how to use *buses* (i.e. vector of wires) in Verilog.

1 Designing a decoder **(30m)**

Design a 2:4 decoder module that implements the following truth table:

Input		**Output**			
i[1]	**i[0]**	**o[3]**	**o[2]**	**o[1]**	**o[0]**
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

The module signature should be

```
module decoder(input [1:0] i, output [3:0] o);
```

2 Designing a priority encoder **(30m)**

Design a 4:2 priority encoder, where if more than one input line is set to 1, the module outputs the encoding of the lower valued line that is set. The expected truth table is shown below (where X indicates that the value can be either 0 or 1). The v bit represents the valid bit, which should be high when at least one of the input lines are high, i.e. when the output is valid.

Input				**Output**		
i[3]	**i[2]**	**i[1]**	**i[0]**	**o[1]**	**o[0]**	**v**
0	0	0	0	X	X	0
X	X	X	1	0	0	1
X	X	1	0	0	1	1
X	1	0	0	1	0	1
1	0	0	0	1	1	1

The module signature should be

```
module priority_encoder(input [3:0] i, output [1:0] o, output v);
```

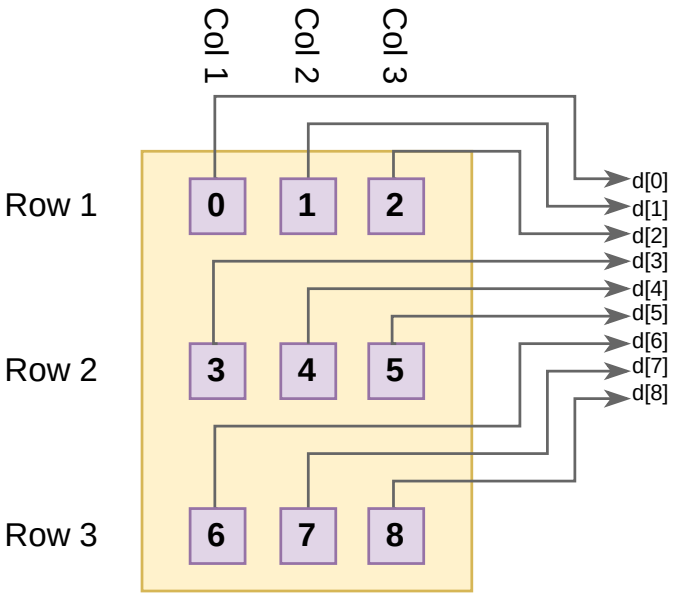
3 Designing a Row-Column encoder **(40m)**

Given a 3x3 grid of keys labelled from 0 to 8 as shown in the figure below. Assume that each of the wires in $d[8:0]$ is High (set to 1) when the corresponding key is pressed.

Use the priority encoder designed in the previous question for implementing a row-column decoder that takes the wires coming from the 9 keys as input and outputs the binary encoded row and column number of the key that is pressed.

- **You must use the priority encoder designed in the previous question for implementing this module.**
- You can assume that only one key will be pressed at any time.

- The row and column numbers start from 1 (not 0).
- The v bit indicates if the output is valid, i.e. at least one of the keys is pressed



The module signature should be

```
module row_col_encoder(input [8:0] d, output [1:0] row, output [1:0] col, output v);
```

Submission guidelines

- You must use only structural modelling for this lab.
- Use the same module name and port definitions as given in the question.
- Name your solution files as q1.v, q2.v, and so on corresponding to each question.
- Testbench files for all questions have been provided. Ensure that your Verilog code passes all testcases.