EE466
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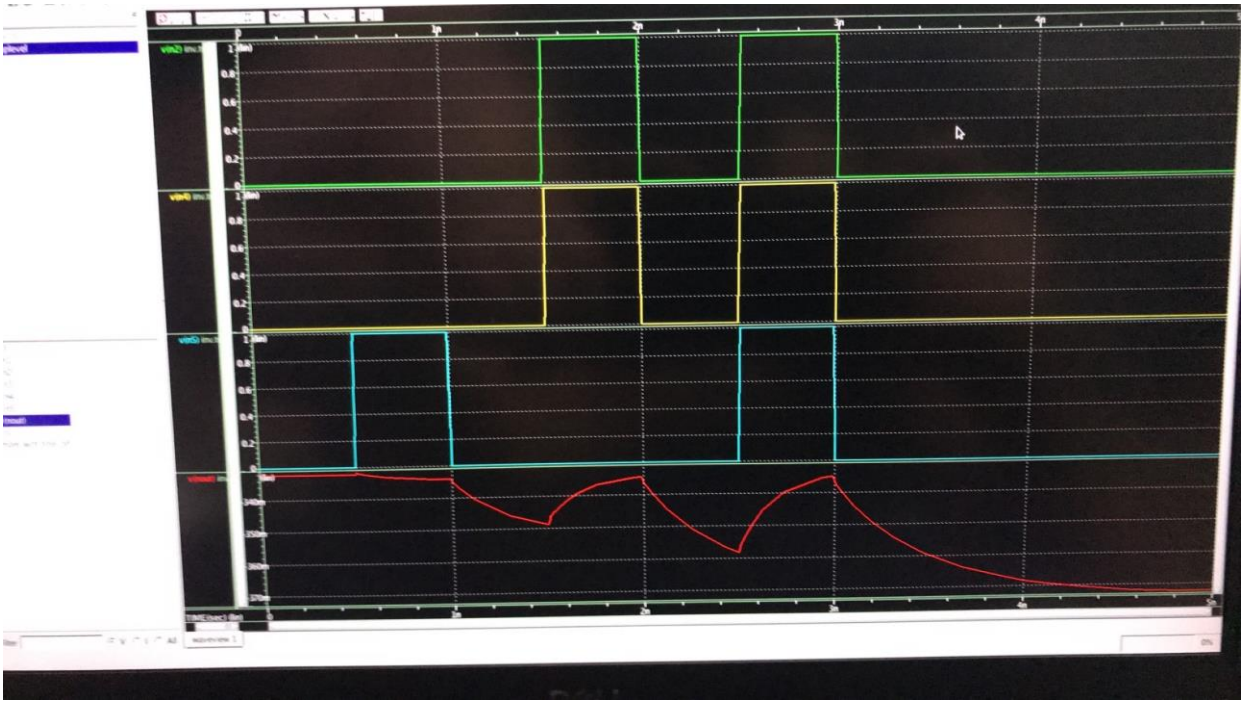
Lab1



* The first line is always a comment line.
* Case-insensitive

* Control
.option post INGOLD=2

* Include the following file to load transistor models.
.include './45nm_PTM_HP_v2.1.pm'

```
* Parameters
* Supply voltage
.param V = 1V

* Inverter. use NMOS_HP and PMOS_HP for NMOS and PMOS transistors.

*** Transistor names should begin with "m".
*** Use "nXXXXX" for node names.
*** Use 0 for the ground.
* Format: <transistor name> <drain> <gate> <source> <body> <type> L(Length) W(Width)
mn1 n3 n2 n1 NMOS_HP  L=45n W=50n
mn2 0 n4 n3 NMOS_HP L=45n W=50n
mn3 0 n5 n1 NMOS_HP L=45n W=50n
mp1 nout n1 V PMOS_HP L=45n W=75n
mn4 0 n1 nout NMOS_HP L=45n W=50n

*** Output load capacitance. Capacitors should begin with "c".
* Format: <capacitor name> <node 1> <node 2> <value>
cap nout 0 10f

* Power supply
* Format: <power supply name> <node 1> <node 2> <value>
*** Voltage source names should begin with "v".
VVdd V nout V

* Input signal (independent voltage source)
* Format: <signal name> <node 1> <node 2> <signal>
* For the signal, we use a piecewise linear (PWL) source. Format: ... PWL time1 value1 time2 value2 ...
VA n2 0 PWL
+ 0 0
+ 500p 0
+ 510p 0
+ 990p 0
+ 1n 0
+ 1.5n 0
+ 1.51n V
+ 1.99n V
+ 2n 0
+ 2.5n 0
+ 2.51n V
+ 2.99n V
+ 3n 0
+ 4n 0
```

```
VB n4 0 PWL
+ 0 0
+ 500p 0
+ 510p 0
+ 990p 0
+ 1n 0
+ 1.5n 0
+ 1.51n V
+ 1.99n V
+ 2n 0
+ 2.5n 0
+ 2.51n V
+ 2.99n V
+ 3n 0
+ 4n 0

VC n5 0 PWL
+ 0 0
+ 500p 0
+ 510p V
+ 990p V
+ 1n 0
+ 1.5n 0
+ 1.51n 0
+ 1.99n 0
+ 2n 0
+ 2.5n 0
+ 2.51n V
+ 2.99n V
+ 3n 0
+ 4n 0

* Transient analysis. Simulate up to 5ns.
.tran 1p 5n

.end
```