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EE466 - Project

IpDCO:

1. The energy vs. delay characteristics of these three semidynamic flops is shown in Figure 2a, while
2. Figure 2b plots the energy*delay product (E*D) as a function of delay.
3. Figure 2c summarizes the comparison in terms of D-Q .delay, minimum E*D product point, total device width, and total energy
4. For an equal energy per cycle of 40fJ, ip-DCO offers 8% - 10% better D-Q delay
5. Omprovement because transistor being driven by data in the 3-transistor stack of the input stage is located in the middle for HFF and SDFF, it is located close to the output node in ip-DCO
    - improves the speed when sampling a '1' because the intermediate slack nodes are discharged when the data signal arrives
6. .13uM sizing

For the ipDCO (implicit-pulsed, data-close-to-output) the energy compared to the HLFF and semi-dynamic DFF has a better delay than the two. The delay for the falling is about 80ps from the waveform, and for the rising it is about 100ps. The average power consumption is around 16.73uW from 1ns to 2.25ns.

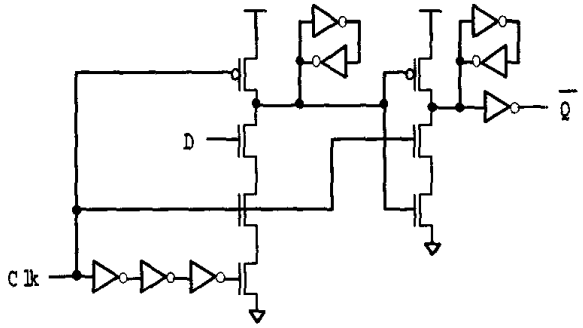
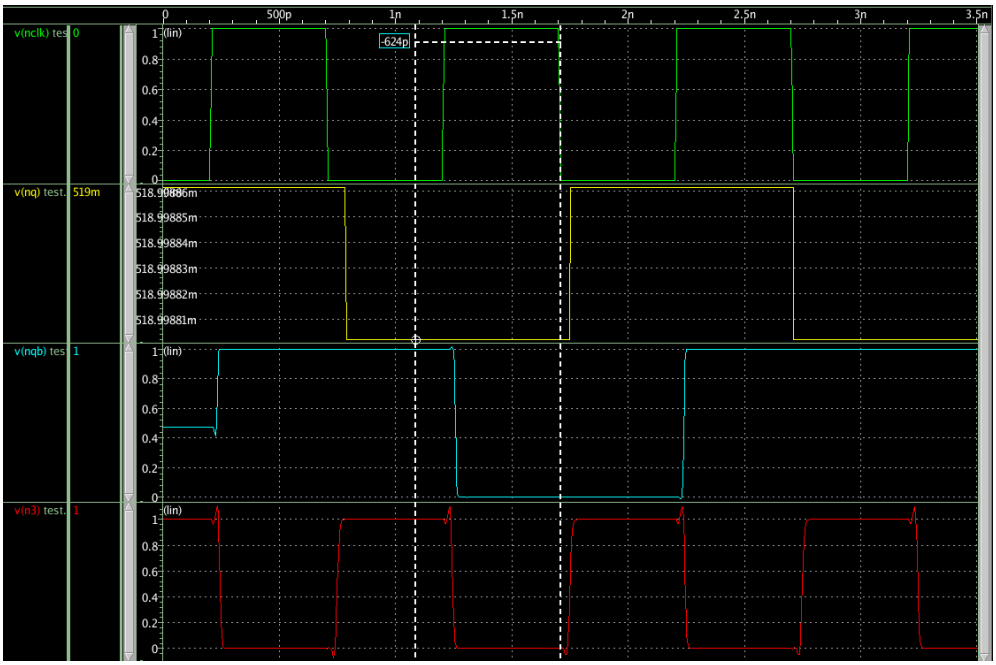


Figure 1. Implicit pulsed semidynamic flip-flop (ip-DCO).



HLFF:

For the HLFF circuit the half volage is at time 565ps and begins to decrease at 300ps. This produces a time difference in 265ps from the rise of the voltage to the halfway point. Base off Figure.1 setup the time delay recorded is 240ps which is relatively close to the time delay I received.

Before the rising clock edge, N1 and N4 are active low. While N3 N6, and P1 are active high. This allows X to pre-charge to vdd and allows Q to hold the previous data. At the rising clock edge N1 and N4 are active high while the other 3 stay on for a short period which allows the data at D to be stored into the latch. When CKDB goes to low, X is decoupled from D and begins to discharge to vdd. When the clock falls P1 is fully charged or holds X at vdd until the clock rises again. As the clock rises, P1 discharges.

Shown in the graph as clock is low nqb is active high and begins to discharge once nq behind to charge. Once the clock edge rises nqb begins to charge with a delay of 50ps. The delay for the inverters I1-I3 is 60ps with an average power consumption of 277uW

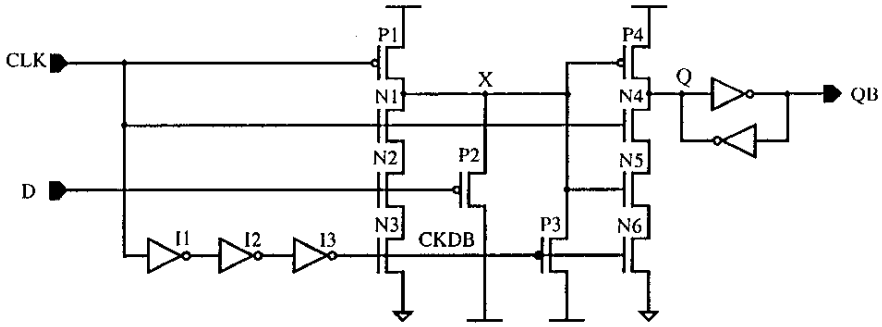


Figure 1: Basic HLFF circuit.

Semi-dynamic DFF

For the semi-dynamic DFF, the internal node of X is dynamic. This makes it not actively driven by any device. Q is high impedance when the clock is active low. The circuit contains both the dynamic and static circuits combined. The input D produces an output QB where the delay from nQB discharging to nQ charging is about a 50ps delay. On the falling edge of the clock the f/f enters the pre-charge phase. Node X becomes pre-recharged to active high cutting off Q from the input stage. The intervers 5 and 6 holds the previous logic level of Q and QB. The transistor N1 stay on when clock is low which forces S to be high as well. But if D is low the f/f latches to zero and node X will be high which is held by inverters 3 and 4. If D were high then it would latch to one instead of zero and node X would become discharged.

The inverters 3 and 4 will hold the value of X even if D were driven low. The NAND gate coupled to node X and clock the shutoff of pulldown is conditioned to the state of input. This allows to not shutoff when D is held high.