Design and Fabrication of a Microwave Resonator Using Aluminum on a Silicon Substrate for 50 Ω Impedance Matching

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1 Introduction

Microwave resonators are essential devices employed in RF communications, quantum circuits, and superconducting electronics, designed to selectively resonate at specific frequencies with minimal signal losses. With aluminum metallization on a silicon substrate, several resonator configurations can be realized, notably coplanar waveguide (CPW), microstrip, and lumped-element resonators.

The coplanar waveguide resonator consists of a central conductive strip separated by narrow gaps from parallel ground planes, enabling precise control of characteristic impedance and compatibility with planar processing techniques. Microstrip resonators, featuring a conductive strip above a grounded silicon substrate, offer simple geometries but require precise control over dielectric properties and substrate thickness for accurate impedance matching. Lumped-element resonators, composed of discrete inductors and capacitors fabricated in planar form, allow compact device size and straightforward frequency tuning but face fabrication complexity and limitations in achieving very high Q-factors.

The CPW resonator is selected as the optimal solution due to its robust ease of fabrication, precise impedance control, and strong compatibility with standard lithographic processing methods. CPW resonators also integrate smoothly into quantum circuits and superconducting devices, aligning perfectly with the group's capabilities, infrastructure, and expertise.

This report is structured as follows: Firstly, the theoretical foundations behind transmission lines, impedance matching principles, and resonator behavior are explained. Secondly, the detailed fabrication methodology using photolithography and aluminum deposition is described. Lastly, the results from numerical simulations performed with COMSOL Multiphysics are presented, validating the resonator design through accurate impedance matching, resonant frequency verification, and minimized signal reflections.

2 Theoretical Background

Microwave resonators are devices that store electromagnetic energy at specific frequencies. They are fundamental components in many high-frequency systems such as filters, oscillators, and quantum circuits. Designing a resonator requires a deep understanding of how electromagnetic waves behave in transmission lines, how resonance arises from standing wave patterns, and how different geometries support specific electromagnetic modes. In this section, we begin with the basic concepts of wave propagation and gradually build up to the principles of resonator design.

2.1 Basic Concepts of Transmission Lines

At its core, a transmission line serves as a pathway for high-frequency electromagnetic energy. Unlike low-frequency circuits, where voltage and current are assumed uniform along wires, at microwave frequencies the wavelength of the signal becomes comparable to the physical dimensions of the circuit. As a result, we must consider distributed models where electrical quantities vary with position.

A transmission line can be modeled as an infinite sequence of infinitesimal elements, each consisting of:

- R: resistance per unit length (Ω/m), accounting for ohmic losses in the conductor,

- L: inductance per unit length (H/m), due to magnetic field energy,
- G: conductance per unit length (S/m), representing dielectric losses,
- C: capacitance per unit length (F/m), arising from the electric field between conductors.

Applying Kirchhoff's laws leads to the telegrapher's equations:

$$\frac{\partial V}{\partial z} = -RI - L\frac{\partial I}{\partial t}, \quad \frac{\partial I}{\partial z} = -GV - C\frac{\partial V}{\partial t}$$

Assuming sinusoidal time variation ($e^{j\omega t}$), we obtain wave equations:

$$\frac{d^2V}{dz^2} = \gamma^2 V, \quad \frac{d^2I}{dz^2} = \gamma^2 I$$

with the complex propagation constant:

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$$

The characteristic impedance Z_0, defining the voltage-to-current ratio for traveling waves, is:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

In the special case of a lossless line ($R = G = 0$):

$$Z_0 = \sqrt{\frac{L}{C}}, \quad \gamma = j\omega\sqrt{LC}$$

Reflections occur when the load impedance Z_L doesn't match Z_0. The reflection coefficient Γ expresses this mismatch:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}$$

When $\Gamma = 0$, power is maximally transferred — a condition known as impedance matching.

2.2 Coplanar Waveguide (CPW) Resonators

Coplanar waveguide (CPW) resonators are planar transmission lines composed of a central conductor flanked by two ground planes on the same substrate surface, separated by narrow slots. This geometry supports a quasi-transverse electromagnetic (quasi-TEM) mode, where the dominant electric and magnetic fields are transverse to the direction of propagation. The mode resembles that of coaxial lines or parallel-plate waveguides, but with some longitudinal field components due to the asymmetric dielectric environment (air above, dielectric below).

The CPW layout enables easy photolithographic fabrication and eliminates the need for via-holes, making it ideal for monolithic microwave circuits and superconducting qubit readout structures. According to Göppl et al. [2], CPW resonators show superior performance in planar superconducting circuit QED experiments due to their open-access geometry, efficient mode confinement, and straightforward integration into coplanar feedlines.

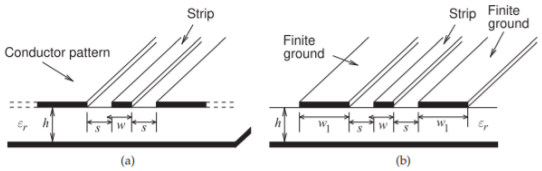

Figure 1: Coplanar waveguide (CPW): (a) conventional; and (b) finite ground CPW (FGCPW). Image from [5]

A central parameter in CPW design is the effective dielectric constant ε_{eff}, which governs the wave velocity and resonance frequency. A simple approximation is:

$$\varepsilon_{\text{eff}} \approx \frac{\varepsilon_r + 1}{2}$$

where ε_r is the relative permittivity of the substrate. This assumes equal energy distribution in the air and dielectric. For more accurate values, particularly when the gaps are small or the substrate is thick, conformal mapping or FEM simulations are used to extract ε_{eff}.

The resonance frequency of a CPW $\lambda/4$ resonator, open at one end and shorted or capacitively coupled at the other, is given by:

$$f_0 = \frac{c}{4L\sqrt{\varepsilon_{\text{eff}}}}$$

where L is the physical length of the resonator. Higher-order odd harmonics appear at $3f_0, 5f_0, \ldots$, while even harmonics are suppressed due to the boundary condition asymmetry.

The characteristic impedance Z_0 of a CPW line can be derived via conformal mapping and expressed in terms of elliptic integrals [5]:

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_{\text{eff}}}} \cdot \frac{K(k')}{K(k)}$$

with:

$$k = \frac{W}{W + 2S}, \quad k' = \sqrt{1 - k^2}$$

where: - W: width of the center conductor, - S: gap between conductor and ground, - $K(k)$: complete elliptic integral of the first kind.

This expression links CPW geometry to impedance, allowing for direct design targeting of 50 Ω operation by adjusting W and S. Reducing S increases capacitance and lowers Z_0, while widening W also decreases Z_0. This tunability makes CPW resonators highly attractive for integrated devices requiring compact layouts and matched interfaces. Moreover, the resonator's electromagnetic field is largely confined near the surface, which simplifies simulation and enables high field concentration — a useful feature in nonlinear or quantum applications.

In summary, the CPW resonator combines ease of fabrication, precise impedance control, and robust theoretical modeling — making it an ideal choice for microwave resonators built on silicon with aluminum metallization.

2.3 Coupling Mechanisms and Quality Factors

To utilize a resonator in a microwave circuit, it must be coupled to external transmission lines, enabling excitation and readout. This coupling can be achieved through electric (capacitive) or magnetic (inductive) fields, depending on the resonator geometry. In CPW-based planar designs, capacitive coupling is the most prevalent and practical method. The strength of this coupling has a direct influence on the resonator's performance and is characterized by its effect on the system's quality factors.

2.3.1 Internal, External, and Loaded Quality Factors

The total losses in a resonator are expressed through three distinct quality factors:

- Q_i: The **internal quality factor**, which quantifies losses due to dielectric dissipation, conductor resistance, and radiation.
- Q_e: The **external quality factor**, representing energy leakage into the external environment via the coupling element.
- Q_L: The **loaded quality factor**, which is the total measured quality factor, incorporating both internal and external losses.

These are related by:

$$\frac{1}{Q_L} = \frac{1}{Q_i} + \frac{1}{Q_e}$$

2.3.2 Dependence on Geometry

Each of the quality factors above depends — either directly or indirectly — on the resonator's geometry:

Internal Quality Factor Q_i: This factor is primarily influenced by:

- **Resonator length** L: Longer resonators store more energy, which tends to increase Q_i assuming losses are constant per unit length.
- **Conductor width** W **and gap** S: Narrower conductors and smaller gaps concentrate electric fields, leading to higher dielectric losses in the substrate and reduced Q_i. A carefully chosen W/S ratio minimizes current crowding and dielectric breakdown.
- **Substrate thickness and permittivity** ε_r: These affect the mode confinement and the effective dielectric constant ε_{eff}, which in turn alters field distributions and losses.

External Quality Factor Q_e: This depends on the coupling geometry:

- **Coupling gap** g_c between the feedline and the resonator: A smaller gap increases the coupling capacitance C_c, decreasing Q_e.
- **Overlap length or coupling length** l_c: A longer overlap leads to stronger coupling, again reducing Q_e.
- **Coupling configuration (end vs side coupling)**: End-coupled resonators couple more efficiently at electric field antinodes, enabling precise tuning of Q_e.

Designers tune these parameters lithographically to target a desired external coupling rate and ensure proper impedance matching to measurement systems or quantum processors.

2.3.3 Reflection Line Shape and Bandwidth

The frequency response of a coupled CPW resonator is typically analyzed through its reflection coefficient $S_{11}(f)$, which exhibits a resonance dip at the fundamental frequency f_0. Near resonance, this response approximates a Lorentzian line shape:

$$|S_{11}(f)| = \left| 1 - \frac{Q_L/Q_e}{1 + 2jQ_L\frac{f-f_0}{f_0}} \right|$$

This expression reveals two critical features of the resonance:

- **Depth of the dip:** Controlled by the ratio Q_L/Q_e. At critical coupling ($Q_e = Q_i$), the dip reaches zero, indicating complete energy transfer from the feedline to the resonator. If $Q_e \gg Q_i$, the system is undercoupled and the dip is shallow; if $Q_e \ll Q_i$, the system is overcoupled and the dip remains deep but broadened.
- **Width of the dip:** Defined by the loaded quality factor Q_L, which determines the resonance bandwidth:
$$Q_L = \frac{f_0}{\Delta f}$$
where Δf is the full width at half maximum (FWHM) of the resonance. A high Q_L corresponds to a narrow resonance and better frequency selectivity.

Since Q_L is jointly determined by the internal and external quality factors, and since Q_e is governed by geometrical coupling parameters such as the coupling gap g_c and length l_c, the shape of the $S_{11}(f)$ curve can be directly tailored through design choices. For instance: - Reducing g_c (bringing the feedline closer) increases coupling capacitance, lowers Q_e, and broadens the dip. - Increasing l_c (overlap length) enhances the coupling strength, again reducing Q_e, and shifts the resonator toward the overcoupled regime.

Thus, the reflection response becomes a sensitive probe of both the physical quality of the resonator and the lithographically defined geometry of its coupling region.

3 Experimental Techniques

3.1 Lithography Principles and Process

Lithography is the cornerstone patterning technique in microfabrication, used to transfer geometrically defined designs onto substrates for subsequent material processing. In the context of microwave resonator fabrication, lithography is responsible for defining the planar geometry of the CPW structure with high fidelity and dimensional accuracy, directly impacting the resonator's frequency response and impedance matching.

There are two major lithographic techniques relevant for this purpose: optical (photolithography) and electron-beam lithography (EBL). While photolithography is the standard for batch processing with micron-scale features, EBL offers higher resolution and is often used in research environments where rapid prototyping or sub-micron structures are needed.

3.1.1 Photolithography Process Overview

Photolithography is a parallel process where a photoresist (PR) layer is exposed to UV light through a photomask, and subsequently developed to reveal the underlying substrate in patterned regions. The basic steps involved are as follows [1, 3]:

1. **Surface preparation and dehydration bake:** Silicon wafers are first cleaned (e.g., with acetone, isopropanol, DI water) and baked at 120°C to eliminate moisture, which hinders photoresist adhesion.

2. **Adhesion promotion:** Hexamethyldisilazane (HMDS) is often applied via vapor priming or spin coating to chemically modify the wafer surface, improving resist wettability and adhesion.

3. **Spin coating:** A uniform layer of liquid photoresist is dispensed and spun at high speed (typically 3000–5000 rpm), yielding resist films in the 0.5–2 µm range. Film thickness affects resolution, exposure time, and subsequent lift-off success.

4. **Soft bake (prebake):** The coated wafer is baked (typically 90−100°C for 60–90 seconds) to remove residual solvents. This stabilizes the resist and improves resolution during exposure.

5. **UV exposure through a mask:** The wafer is aligned with a chromium-on-glass photomask and exposed to near-UV light (e.g., 365 nm for i-line). For positive resists, exposed regions become more soluble in developer due to photo-induced chain scission.

6. **Post-exposure bake (optional):** Some resist systems require a short bake after exposure to complete the photochemical reaction and enhance development contrast.

7. **Development:** The exposed resist is immersed in or sprayed with a developer solution (e.g., aqueous TMAH). Exposed areas (in positive resist) are dissolved, revealing openings in the resist where material will later be deposited or etched.

8. **Hard bake (optional):** After patterning, wafers may be baked again (e.g., at 120−150°C) to improve chemical resistance during subsequent processing (e.g., metal deposition or etching).

Key process parameters such as resist thickness, exposure dose, and development time must be optimized for resolution, edge roughness, and profile control. Undercut or sloped resist profiles are often desirable for successful lift-off.

3.1.2 Resolution Limits and Optical Considerations

The resolution of photolithography is fundamentally limited by diffraction, governed by the Rayleigh criterion:

$$R = \frac{k_1 \lambda}{NA}$$

where: - R is the minimum resolvable feature size, - λ is the exposure wavelength, - NA is the numerical aperture of the optical system, - k_1 is a process-dependent constant (typically 0.4–0.8).

With conventional UV exposure tools and standard positive resists (e.g., S1813), minimum features of 1–2 µm are achievable. For our CPW resonator, where gaps and line widths are 10–20 µm, photolithography is fully sufficient and provides excellent throughput and uniformity.

3.1.3 Electron-Beam Lithography (EBL)

Electron-beam lithography is a direct-write technique where a focused beam of high-energy electrons (10–100 keV) is scanned across an electron-sensitive resist (e.g., PMMA). EBL is maskless and capable of nanometer-scale resolution, ideal for fine-feature research applications.

Advantages of EBL include:

- Pattern flexibility without masks (CAD-based design).
- Resolution down to 10–20 nm.
- Suitable for small-volume or prototype fabrication.

Drawbacks include:

- Long write times due to serial exposure.
- Proximity effects from electron scattering in the resist/substrate.
- Complex process control for dose and focus.

While not necessary for the current resonator geometry, EBL may be used for high-frequency quantum devices where feature sizes shrink below the optical resolution limit.

3.1.4 Lithography for Resonator Definition

For our aluminum-on-silicon CPW resonator, photolithography is used to define the signal line and adjacent ground planes. The pattern is transferred into a positive resist (e.g., AZ or S1813), leaving openings where aluminum will be deposited. A well-optimized lithographic process ensures clean, steep resist profiles, enabling sharp metal edges and minimal loss in the final device.

The design must ensure that:

- CPW dimensions match the desired impedance (typically 50 Ω).
- The open end of the $\lambda/4$ resonator is properly aligned for capacitive coupling.
- Undercut or bilayer resists (e.g., LOR + PR) are used for reliable lift-off.

3.2 Thin-Film Deposition: Aluminum Metallization

After patterning the photoresist, the next fabrication step is the deposition of a thin aluminum (Al) film to form the resonator's conductive structures. Aluminum is widely used in microwave and quantum circuits due to its favorable electrical properties, ease of deposition, and compatibility with superconducting applications at cryogenic temperatures. In our context, the aluminum layer forms the signal line and ground planes of the CPW resonator.

3.2.1 Material Considerations

Aluminum offers several advantages as a metallization layer:

- High electrical conductivity ($\rho \approx 2.65 \times 10^{-8}\ \Omega \cdot \mathrm{m}$), ensuring low resistive losses.
- Strong adhesion to silicon substrates (especially after oxide removal).
- Relatively low melting point (660 °C), making it suitable for thermal evaporation.
- Forms a native oxide (Al_2O_3) that is self-passivating and useful in some superconducting circuits.

For CPW resonators operating at microwave frequencies, the aluminum film must be sufficiently thick (e.g., 100–200 nm) to ensure the current is confined within the film thickness, especially beyond the skin depth at GHz frequencies.

3.2.2 Deposition Techniques

Two main deposition techniques are used in thin-film processing of Al: thermal evaporation and electron-beam (e-beam) evaporation.

Thermal Evaporation Thermal evaporation involves heating aluminum in a vacuum chamber until it evaporates and condenses on the wafer surface. The process steps are:

- Aluminum pellets are placed in a tungsten boat or crucible.
- Under high vacuum ($\sim 10^{-6}$ Torr), the metal is resistively heated to 1100–1400 °C.
- Aluminum atoms evaporate and travel in line-of-sight to the substrate, forming a conformal film.

Advantages:

- Simpler and more cost-effective than e-beam evaporation.
- Low-energy process that avoids substrate damage.

Limitations:

- Less suitable for high melting point materials.
- Shadowing effects and poor step coverage over complex topographies.

Electron-Beam (E-Beam) Evaporation In e-beam evaporation, a high-energy electron beam is focused onto an aluminum source, which melts and evaporates without heating the surrounding crucible. This method offers:

- Higher purity films with precise control over deposition rate and thickness.
- Capability to deposit refractory metals (e.g., Nb, W).
- Low contamination due to localized heating.

Typical deposition parameters:

- Base pressure: $\leq 5 \times 10^{-7}$ Torr
- Rate: 0.5–2 Å/s
- Final thickness: 100–200 nm

In both cases, film uniformity and adhesion depend on wafer cleanliness, resist profile, and chamber vacuum quality. Aluminum should be deposited immediately after resist development to minimize surface contamination or oxide regrowth.

3.2.3 Post-Deposition Considerations

Once the metal is deposited, several checks are important:

- **Thickness monitoring:** Achieved via quartz crystal microbalance (QCM) during deposition.
- **Adhesion test:** Visual inspection or tape test to check metal-substrate bonding.
- **Line edge quality:** Observed under an optical microscope to verify pattern fidelity.

No thermal annealing is typically required for aluminum CPW resonators, as deposition at room temperature yields acceptable film morphology and grain structure for microwave performance.

3.2.4 Importance in Resonator Design

The electrical properties of the deposited aluminum — specifically its surface roughness and resistivity — directly influence the internal quality factor Q_i. Surface oxidation is usually unavoidable but forms a stable passivation layer that does not severely impact performance unless operating at cryogenic temperatures, where superconducting losses become critical.

The film thickness must be greater than the skin depth δ at the design frequency f, given by:

$$\delta = \sqrt{\frac{2\rho}{\mu_0 \omega}} \quad \text{with} \quad \omega = 2\pi f$$

For aluminum at 5GHz, this yields $\delta \sim 1\,\mu$m, but since most current flows near the surface, even thinner films (100–200nm) are acceptable if losses are tolerable.

3.3 Lift-Off Process

The lift-off process is a subtractive microfabrication technique used to define metal structures on a substrate without the need for etching. It is particularly useful when the material to be patterned — such as aluminum — is difficult to etch selectively or when ultra-fine features are required. In this project, lift-off is used to form the aluminum patterns for the CPW resonator after lithographic definition.

3.3.1 Principle of Lift-Off

Unlike etching, where excess metal is removed after full-surface deposition, lift-off relies on a sacrificial resist pattern to define where metal should *not* be deposited. The basic idea is:

1. Pattern the resist so that it covers only the regions where metal is not wanted.
2. Deposit metal uniformly over the entire wafer.
3. Remove the resist underneath the unwanted metal by dissolving it in a solvent, "lifting off" the overlying film.

For lift-off to succeed, the resist profile must have a **re-entrant** or undercut shape. This ensures that the metal deposited on top of the resist is discontinuous with the metal on the substrate, allowing the solvent to access and dissolve the resist easily.

3.3.2 Resist Stack and Undercut Profile

To achieve the necessary undercut profile, a bilayer resist process is commonly used:

- **Bottom layer:** A low molecular weight resist (e.g., LOR or PMGI), which dissolves faster and creates the undercut.
- **Top layer:** A standard positive-tone photoresist (e.g., S1813), patterned by UV lithography.

Upon development, the bottom layer is isotropically etched more than the top, producing the desired re-entrant geometry. This profile prevents the metal from forming continuous sidewalls that would otherwise make lift-off impossible.

3.3.3 Process Flow

The complete lift-off procedure includes the following steps:

1. **Surface Preparation:** Clean the silicon wafer with acetone, IPA, and O_2 plasma to ensure resist adhesion.
2. **Resist Coating:** Spin coat the bilayer resist stack. Bake each layer according to specifications (e.g., 180°C for 1–2 minutes).

3. **Exposure:** Use contact lithography (or e-beam for sub-micron features) to expose the resist through a mask.
4. **Development:** Immerse in developer solution (e.g., MF-319) to dissolve the exposed regions and form an undercut.
5. **Metal Deposition:** Deposit aluminum via thermal or e-beam evaporation. Maintain a vertical deposition angle to avoid shadowing.
6. **Lift-Off:** Submerge the wafer in acetone or NMP (N-methyl-2-pyrrolidone) to dissolve the resist. Use mild sonication if needed.

3.3.4 Design Considerations

Several factors influence the quality and success of lift-off:

- **Metal Thickness:** Should be less than or comparable to the resist thickness to prevent edge fencing.
- **Resist Profile:** A well-defined undercut ensures clean separation.
- **Deposition Directionality:** Lift-off works best with directional deposition methods like evaporation; sputtering is less favorable due to its isotropy.
- **Feature Size:** Lift-off is ideal for features down to the sub-micron regime, especially when combined with e-beam lithography.

3.3.5 Outcome and Relevance

After successful lift-off, the wafer exhibits clean, sharply defined aluminum structures with the desired CPW geometry. The line edges are determined by the lithographic pattern, and the film properties depend on the deposition parameters. This process enables precise control over signal and ground line widths, which directly affect the characteristic impedance Z_0, effective dielectric constant ε_{eff}, and resonance frequency of the fabricated resonator.

4 Discussion and Design Implications

The COMSOL simulation confirms the proper functioning of the CPW resonator and validates the modeling strategy using numeric TEM ports. The extracted results are in close agreement with theoretical expectations for a quarter-wave structure at 10 GHz.

- The first resonant mode is found at $f_0 = 10.00\,\text{GHz}$, matching the designed quarter-wavelength condition:
$$f_0 = \frac{c}{4L\sqrt{\varepsilon_{\text{eff}}}}, \quad L = 3.0\,\text{mm}, \quad \varepsilon_{\text{eff}} \approx 6.2$$
- The computed characteristic impedance of the coplanar waveguide from the numeric port is:
$$Z_0 = 51.3\,\Omega$$
which is very close to the standard 50Ω, ensuring compatibility with RF instrumentation and minimal reflection.
- The electric field distribution shows strong confinement within the CPW slot, with a standing wave pattern consistent with the $\lambda/4$ mode and negligible radiation loss, supporting efficient energy storage and high-Q operation.
- Mode field plots confirm excitation of a clean quasi-TEM mode, and the impedance value is computed from the voltage and power integrals along the user-defined integration line.
- While minor geometry adjustments could achieve an exact 50Ω match, the current configuration already provides excellent impedance matching for practical purposes.

In summary, the simulation validates both the electromagnetic performance and the physical layout of the device, demonstrating that the structure is ready for fabrication and testing.