```
1   `timescale 1ns / 1ns // `timescale time_unit/time_precision
2
3   // top level module
4   module mux2to1(LEDR, SW);
5
6       input [9:0] SW;
7       output [9:0] LEDR;
8       wire not2_and2, and3_or1, and6_or2;
9
10      v7404 notGate (
11        .pin1(SW[9]),
12        .pin2(not2_and2)
13      );
14
15      v7408 andGate (
16        .pin1(SW[0]),
17        .pin2(not2_and2),
18        .pin3(and3_or1),
19        .pin4(SW[9]),
20        .pin5(SW[1]),
21        .pin6(and6_or2)
22      );
23
24      v7432 orGate (
25        .pin1(and3_or1),
26        .pin2(and6_or2),
27        .pin3(LEDR[0])
28      );
29
30  endmodule
31
32  // not gate
33  module v7404 (input pin1, pin3, pin5, pin9, pin11, pin13,
34                output pin2, pin4, pin6, pin8, pin10, pin12);
35
36     assign pin2 = ~pin1;
37     assign pin4 = ~pin3;
38     assign pin6 = ~pin5;
39     assign pin12 = ~pin13;
40     assign pin10 = ~pin11;
41     assign pin8 = ~pin9;
42
43  endmodule
44
45  // and gate
46  module v7408 (input pin1, pin2, pin4, pin5, pin12, pin13, pin10, pin9,
47                output pin3, pin6, pin11, pin8);
48
49     assign pin3 = pin1 & pin2;
50     assign pin6 = pin4 & pin5;
51     assign pin8 = pin10 & pin9;
52     assign pin11 = pin12 & pin13;
53
54  endmodule
55
56  // or gate
57  module v7432 (input pin1, pin2, pin4, pin5, pin13, pin12, pin10, pin9,
58                output pin3, pin6, pin11, pin8);
59
60     assign pin3 = pin1 | pin2;
61     assign pin6 = pin4 | pin5;
62     assign pin11 = pin13 | pin12;
63     assign pin8 = pin9 | pin10;
64
65  endmodule
66
```