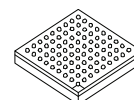




MCIMX6QxCxxxxC
MCIMX6DxCxxxxC

i.MX 6Dual/6Quad Applications Processors for Industrial Products



Package Information
Case FCPBGA 21 x 21 mm, 0.8 mm pitch

Ordering Information

See [Table 1 on page 3](#)

1 Introduction

The i.MX 6Dual and i.MX 6Quad processors feature Freescale's advanced implementation of the quad ARM Cortex™-A9 core, which operates at speeds up to 1 GHz. They include 2D and 3D graphics processors, 3D 1080p video processing, and integrated power management. Each processor provides a 64-bit DDR3/LVDDR3/LPDDR2-1066 memory interface and a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

The i.MX 6Dual/6Quad processors are specifically useful for applications such as the following:

The i.MX 6Dual/6Quad processors have some very exciting features, for example:

- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2,

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NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND, including eMMC up to rev 4.4.

- **Smart speed technology**—The processors have power management throughout the device that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- **Dynamic voltage and frequency scaling**—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- **Multimedia powerhouse**—The multimedia performance of each processor is enhanced by a multilevel cache system, Neon MPE (Media Processor Engine) co-processor, a multi-standard hardware video codec, 2 autonomous and independent image processing units (IPU), and a programmable smart DMA (SDMA) controller.
- **Powerful graphics acceleration**—Each processor provides three independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with four shaders (up to 200 MT/s and OpenCL support), 2D graphics accelerator, and dedicated OpenVG™ 1.1 accelerator.
- **Interface flexibility**—Each processor supports connections to a variety of interfaces: LCD controller for up to four displays (including parallel display, HDMI1.4, MIPI display, and LVDS display), dual CMOS sensor interface (parallel or through MIPI), high-speed USB on-the-go with PHY, high-speed USB host with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100/1000 Mbps Gigabit Ethernet controller, and a variety of other popular interfaces (such as UART, I²C, and I²S serial audio, SATA-II, and PCIe-II).
- **Advanced security**—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the i.MX 6Dual/6Quad security reference manual. Contact your local Freescale representative for more information.
- **Integrated power management**—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

1.1 Ordering Information

Table 1 shows examples of orderable part numbers covered by this datasheet. Table 1 does not include all possible orderable part numbers. The latest part numbers are available on freescale.com/imx6series. If your desired part number is not listed in Table 1, or you have questions about available parts, see freescale.com/imx6series or contact your Freescale representative.

Table 1. Example Industrial Grade Orderable Part Numbers

Part Number	Quad/Dual CPU	Options	Speed Grade	Temperature Grade	Package
MCIMX6Q7CVT08AC	i.MX 6Quad	With VPU, GPU	800 MHz	Industrial	21 mm x 21 mm, 0.8 mm pitch, FCBGA (lidded)
MCIMX6D7CVT08AC	i.MX 6Dual	With VPU, GPU	800 MHz	Industrial	21 mm x 21 mm, 0.8 mm pitch, FCBGA (lidded)

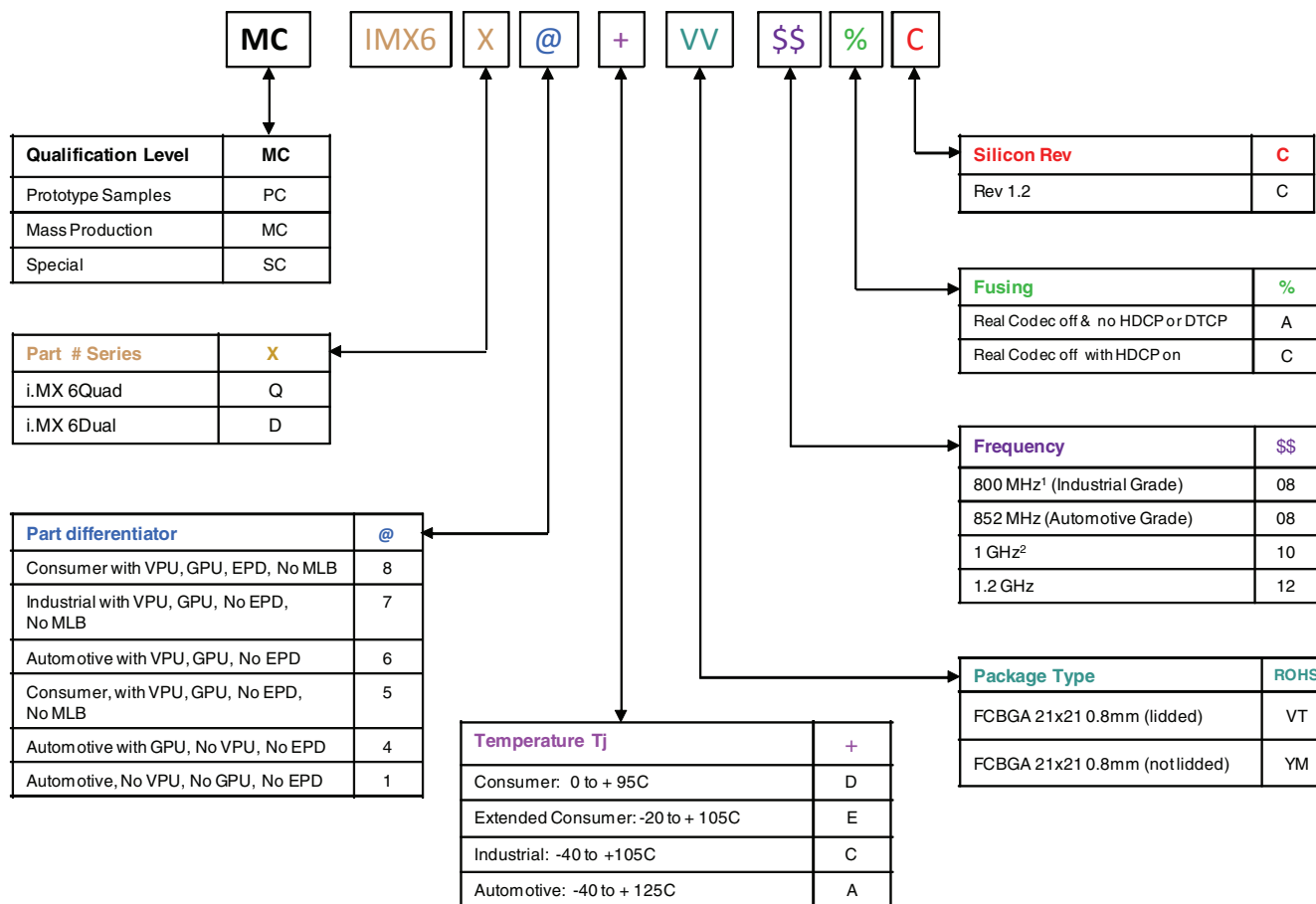
Figure 1 describes the part number nomenclature so that users can identify the characteristics of the specific part number they have (for example, cores, frequency, temperature grade, fuse options, silicon revision). Figure 1 applies to the i.MX 6Quad and i.MX 6Dual.

The primary characteristic that describes which datasheet a specific part applies to is the temperature grade (junction) field:

- The i.MX 6Dual/6Quad Automotive and Infotainment Applications Processors datasheet (IMX6DQAECE) covers parts listed with “A (Automotive temp)”
- The i.MX 6Dual/6Quad Applications Processors for Consumer Products datasheet (IMX6DQCECE) covers parts listed with “D (Consumer temp)” or “E (Extended Consumer temp)”
- The i.MX 6Dual/6Quad Applications Processors for Industrial Products datasheet (IMX6DQIECE) covers parts listed with “C (Industrial temp)”

Ensure that you have the right datasheet for your specific part by checking the temperature grade (junction) field and matching it to the right datasheet. If you have questions, see freescale.com/imx6series or contact your Freescale representative.

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1. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 792 MHz.
2. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

Figure 1. Part Number Nomenclature—i.MX 6Quad and i.MX 6Dual

1.2 Features

The i.MX 6Dual/6Quad processors are based on ARM Cortex-A9 MPCore™ Platform, which has the following features:

- ARM Cortex-A9 MPCore 4xCPU Processor (with TrustZone)
- The core configuration is symmetric, where each core includes:
 - 32 KByte L1 Instruction Cache
 - 32 KByte L1 Data Cache
 - Private Timer and Watchdog
 - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 1 MB unified I/D L2 cache, shared by two/four cores
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Frequency of the core (including Neon and L1 cache) as per [Table 7, "Operating Ranges," on page 22](#)
- NEON MPE coprocessor
 - SIMD Media Processing Architecture
 - NEON register file with 32x64-bit general-purpose registers
 - NEON Integer execute pipeline (ALU, Shift, MAC)
 - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
 - NEON load/store and permute pipeline

The memory system consists of the following components:

- Level 1 Cache—32 KB Instruction, 32 KB Data cache per core
- Level 2 Cache—Unified instruction and data (1 MByte)
- On-Chip Memory:
 - Boot ROM, including HAB (96 KB)
 - Internal multimedia / shared, fast access RAM (OCRAM, 256 KB)
 - Secure/non-secure RAM (16 KB)
- External memory interfaces:
 - 16-bit, 32-bit, and 64-bit DDR3-1066, LVDDR3-1066, and 1/2 LPDDR2-1066 channels, supporting DDR interleaving mode, for 2x32 LPDDR2-1066
 - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bit.
 - 16/32-bit NOR Flash. All EIMv2 pins are muxed on other interfaces.
 - 16/32-bit PSRAM, Cellular RAM

Each i.MX 6Dual/6Quad processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Hard Disk Drives—SATA II, 3.0 Gbps
- Displays—Total five interfaces available. Total raw pixel rate of all interfaces is up to 450 Mpixels/sec, 24 bpp. Up to four interfaces may be active in parallel.
 - One Parallel 24-bit display port, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz or dual HD1080 and WXGA at 60 Hz)
 - LVDS serial ports—One port up to 165 Mpixels/sec or two ports up to 85 MP/sec (for example, WUXGA at 60 Hz) each
 - HDMI 1.4 port
 - MIPI/DSI, two lanes at 1 Gbps
- Camera sensors:
 - Parallel Camera port (up to 20 bit and up to 240 MHz peak)
 - MIPI CSI-2 serial camera port, supporting up to 1000 Mbps/lane in 1/2/3-lane mode and up to 800 Mbps/lane in 4-lane mode. The CSI-2 Receiver core can manage one clock lane and up to four data lanes. Each i.MX 6Dual/6Quad processor has four lanes.
- Expansion cards:
 - Four MMC/SD/SDIO card ports all supporting:
 - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
 - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- USB:
 - One High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB PHY
 - Three USB 2.0 (480 Mbps) hosts:
 - One HS host with integrated High Speed PHY
 - Two HS hosts with integrated HS-IC USB (High Speed Inter-Chip USB) PHY
- Expansion PCI Express port (PCIe) v2.0 one lane
 - PCI Express (Gen 2.0) dual mode complex, supporting Root complex operations and Endpoint operations. Uses x1 PHY configuration.
- Miscellaneous IPs and interfaces:
 - Three I2S/SSI/AC97, up to 1.4 Mbps each
 - Enhanced Serial Audio Interface (ESAI), up to 1.4 Mbps per channel
 - Five UARTs, up to 4.0 Mbps each:
 - Providing RS232 interface
 - Supporting 9-bit RS485 multidrop mode
 - One of the five UARTs (UART1) supports 8-wire while others four supports 4-wire. This is due to the SoC IOMUX limitation, since all UART IPs are identical.
 - Five eCSPI (Enhanced CSPI)

- Three I2C, supporting 400 kbps
- Gigabit Ethernet Controller (IEEE1588 compliant), 10/100/1000¹ Mbps
- Four Pulse Width Modulators (PWM)
- System JTAG Controller (SJC)
- GPIO with interrupt capabilities
- 8x8 Key Pad Port (KPP)
- Sony Philips Digital Interconnect Format (SPDIF), Rx and Tx
- Two Controller Area Network (FlexCAN), 1 Mbps each
- Two Watchdog timers (WDOG)
- Audio MUX (AUDMUX)

The i.MX 6Dual/6Quad processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use Software State Retention and Power Gating for ARM and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6Dual/6Quad processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6Dual/6Quad processors incorporate the following hardware accelerators:

- VPU—Video Processing Unit
- IPUv3H—Image Processing Unit version 3H (2 IPU's)
- GPU3Dv4—3D Graphics Processing Unit (OpenGL ES 2.0) version 4
- GPU2Dv2—2D Graphics Processing Unit (BitBlit)
- GPUVG—OpenVG 1.1 Graphics Processing Unit
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing 16 KB secure RAM and True and Pseudo Random Number Generator (NIST certified)
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock

1. The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Dual/6Quad errata document (IMX6DQCE).

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- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6Dual/6Quad processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6Dual/6Quad processor system.

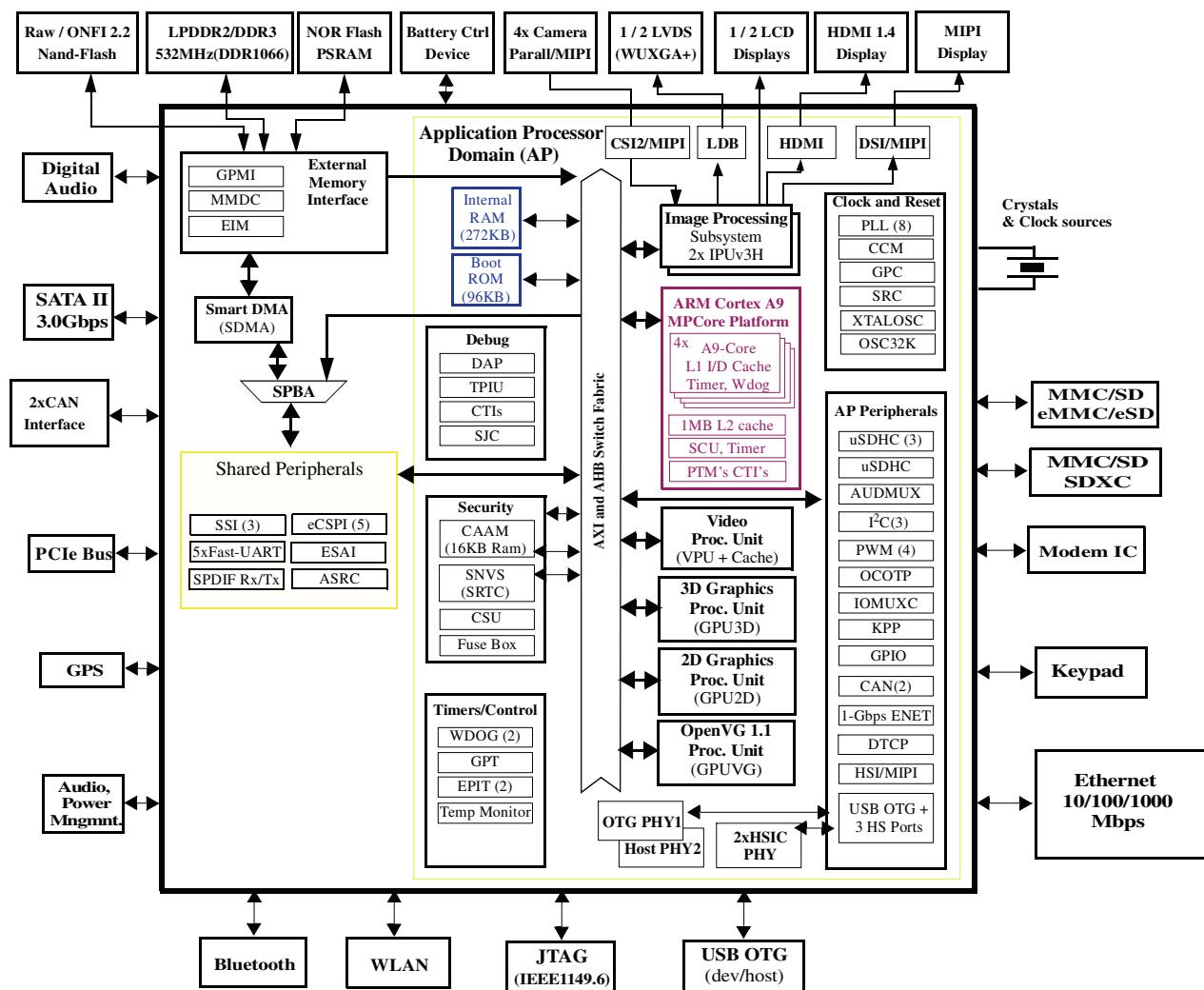


Figure 2. i.MX 6Dual/6Quad Industrial Grade System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

3 Modules List

The i.MX 6Dual/6Quad processors contain a variety of digital and analog modules. [Table 2](#) describes these modules in alphabetical order.

Table 2. i.MX 6Dual/6Quad Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
512x8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6Dual/6Quad processors consist of 512x8-bit fuse box accessible through OCOTP_CTRL interface.
APBH-DMA	NAND Flash and BCH ECC DMA Controller	System Control Peripherals	DMA controller used for GPMI2 operation
ARM	ARM Platform	ARM	The ARM Cortex-A9 platform consists of 4x (four) Cortex-A9 cores version r2p10 and associated sub-blocks, including Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, Watchdog, and CoreSight debug modules.
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
BCH40	Binary-BCH ECC Processor	System Control Peripherals	The BCH40 module provides up to 40-bit ECC encryption/decryption for NAND Flash controller (GPMI)
CAAM	Cryptographic Accelerator and Assurance Module	Security	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, and a Pseudo Random Number Generator (PRNG). The pseudo random number generator is certified by Cryptographic Algorithm Validation Program (CAVP) of National Institute of Standards and Technology (NIST). Its DRBG validation number is 94 and its SHS validation number is 1455. CAAM also implements a Secure Memory mechanism. In i.MX 6Dual/6Quad processors, the security memory provided is 16 KB.
CCM GPC SRC	Clock Control Module, Global Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CSI	MIPI CSI-2 Interface	Multimedia Peripherals	The CSI IP provides MIPI CSI-2 standard camera interface port. The CSI-2 interface supports up to 1 Gbps for up to 3 data lanes and up to 800 Mbps for 4 data lanes.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6Dual/6Quad platform. The Security Control Registers (SCR) of the CSU are set during boot time by the HAB and are locked to prevent further writing.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: <ul style="list-style-type: none"> • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCIC-0 DCIC-1	Display Content Integrity Checker	Automotive IP	The DCIC provides integrity check on portion(s) of the display. Each i.MX 6Dual/6Quad processor has two such modules, one for each IPU.
DSI	MIPI DSI interface	Multimedia Peripherals	The MIPI DSI IP provides DSI standard display port interface. The DSI interface support 80 Mbps to 1 Gbps speed per data lane.
eCSP11-5	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
ENET	Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The i.MX 6Dual/6Quad processors also consist of hardware assist for IEEE 1588 standard. For details, see the ENET chapter of the i.MX 6Dual/6Quad reference manual. Note: The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Dual/6Quad errata document (IMX6DQCE).
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available. The ESAI has 12 pins for data and clocking connection to external devices.
FlexCAN-1 FlexCAN-2	Flexible Controller Area Network	Connectivity Peripherals	The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external devices. Each GPIO module supports 32 bits of I/O.
GPMI	General Media Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices. 40-bit ECC encryption/decryption for NAND Flash controller (GPMI2). The GPMI supports separate DMA channels per NAND device.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2Dv2	Graphics Processing Unit-2D, ver. 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
GPU3Dv4	Graphics Processing Unit, ver. 4	Multimedia Peripherals	The GPU3Dv4 provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays up to HD1080 resolution. The GPU3D provides OpenGL ES 2.0, including extensions, OpenGL ES 1.1, and OpenVG 1.1
GPUVGv2	Vector Graphics Processing Unit, ver. 2	Multimedia Peripherals	OpenVG graphics accelerator provides OpenVG 1.1 support as well as other accelerations, including Real-time hardware curve tessellation of lines, quadratic and cubic Bezier curves, 16x Line Anti-aliasing, and various Vector Drawing functions.
HDMI Tx	HDMI Tx interface	Multimedia Peripherals	The HDMI module provides HDMI standard interface port to an HDMI 1.4 compliant display.
HSI	MIPI HSI interface	Connectivity Peripherals	The MIPI HSI provides a standard MIPI interface to the applications processor.
I ² C-1 I ² C-2 I ² C-3	I ² C Interface	Connectivity Peripherals	I ² C provide serial interface for external devices. Data rates of up to 400 kbps are supported.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
IPUv3H-1 IPUv3H-2	Image Processing Unit, ver. 3H	Multimedia Peripherals	<p>IPUv3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation.</p> <p>The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces:</p> <ul style="list-style-type: none"> • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver <p>The processing includes:</p> <ul style="list-style-type: none"> • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	<p>KPP Supports 8 x 8 external key pad matrix. KPP features are:</p> <ul style="list-style-type: none"> • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: <ul style="list-style-type: none"> • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: <ul style="list-style-type: none"> • Support 16/32/64-bit DDR3-1066 (LV) or LPDDR2-1066 • Supports both dual x32 for LPDDR2 and x64 DDR3 / LPDDR2 configurations (including 2x32 interleaved mode) • Support up to 4 GByte DDR memory space
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSES). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory Controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6Dual/6Quad processors, the OCRM is used for controlling the 256 KB multimedia RAM through a 64-bit AXI bus.
OSC 32 kHz	OSC 32 kHz	Clocking	Generates 32.768 kHz clock from an external crystal.
PCIe	PCI Express 2.0	Connectivity Peripherals	The PCIe IP provides PCI Express Gen 2.0 functionality.
PMU	Power-Management Functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
RAM 16 KB	Secure/non-secure RAM	Secured Internal Memory	Secure/non-secure Internal RAM, interfaced through the CAAM.
RAM 256 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRM memory controller.
ROM 96KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection.
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SATA	Serial ATA	Connectivity Peripherals	The SATA controller and PHY is a complete mixed-signal IP solution designed to implement SATA II, 3.0 Gbps HDD connectivity.
SDMA	Smart Direct Memory Access	System Control Peripherals	<p>The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features:</p> <ul style="list-style-type: none"> • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast context-switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	<p>The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6Dual/6Quad processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards.</p> <p>The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6Dual/6Quad SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.</p>
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality.
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	<p>The SSI is a full-duplex synchronous interface, which is used on the processor to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options.</p> <p>The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.</p>

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
TEMPMON	Temperature Monitor	System Control Peripherals	The temperature monitor/sensor IP module for detecting high temperature conditions. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die. Temperature distribution may not be uniformly distributed; therefore, the read out value may not be the reflection of the temperature value for the entire die.
TZASC	Trust-Zone Address Space Controller	Security	The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations: <ul style="list-style-type: none"> • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 4 MHz. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard and the i.MX31 UART modules. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH3A	USB 2.0 High Speed OTG and 3x HS Hosts	Connectivity Peripherals	USBOH3 contains: <ul style="list-style-type: none"> • One high-speed OTG module with integrated HS USB PHY • One high-speed Host module with integrated HS USB PHY • Two identical high-speed Host modules connected to HSIC USB ports.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-2 uSDHC-4	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	<p>i.MX 6Dual/6Quad specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are:</p> <ul style="list-style-type: none"> Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.2/4.3/4.4 including high-capacity (size > 2 GB) cards HC MMC. Hardware reset as specified for eMMC cards is supported at ports #3 and #4 only. Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB. Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10 Fully compliant with SD Card Specification, Part A2, SD Host Controller Standard Specification, v2.00 <p>All four ports support:</p> <ul style="list-style-type: none"> 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) <p>However, the SoC-level integration and I/O muxing logic restrict the functionality to the following:</p> <ul style="list-style-type: none"> Instances #1 and #2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card Detection” and “Write Protection” pads and do not support hardware reset. Instances #3 and #4 are primarily intended to serve interfaces to embedded MMC memory or interfaces to on-board SDIO devices. These ports do not have “Card detection” and “Write Protection” pads and do support hardware reset. All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports #1 and #2 in four bit configuration (SD interface). Port #3 is placed in his own independent power domain and port #4 shares power domain with some other interfaces.
VDOA	VDOA	Multimedia Peripherals	The Video Data Order Adapter (VDOA) is used to re-order video data from the “tiled” order used by the VPU to the conventional raster-scan order needed by the IPU.
VPU	Video Processing Unit	Multimedia Peripherals	<p>A high-performing video processing unit (VPU), which covers many SD-level and HD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing, such as rotation and mirroring.</p> <p>See the i.MX 6Dual/6Quad reference manual for complete list of VPU's decoding/encoding capabilities.</p>
WDOG-1	Watchdog	Timer Peripherals	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.

Table 2. i.MX 6Dual/6Quad Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such a situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
EIM	NOR-Flash/PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: <ul style="list-style-type: none"> • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
XTALOSC	Crystal Oscillator interface		The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

3.1 Special Signal Considerations

The package contact assignments can be found in [Section 6, “Package Information and Contact Assignments.”](#) Signal descriptions are defined in the i.MX 6Dual/6Quad reference manual. Special signal consideration information is contained in Chapter 1 of Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

3.2 Recommended Connections for Unused Analog Interfaces

The recommended connections for unused analog interfaces can be found in Section 1.8, “Unused analog interfaces,” of the Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors (IMX6DQ6SDLHDG).

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6Dual/6Quad processors.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the SoC. See [Table 3](#) for a quick reference to the individual tables and sections.

Table 3. i.MX 6Dual/6Quad Chip-Level Conditions

For these characteristics, ...	Topic appears ...
Absolute Maximum Ratings	on page 20
FCPBGA Package Thermal Resistance	on page 20
Operating Ranges	on page 22
External Clock Sources	on page 24
Maximal Supply Currents	on page 25
Low Power Mode Supply Currents	on page 27
USB PHY Current Consumption	on page 28
SATA Typical Power Consumption	on page 30
PCIe 2.0 Maximum Power Consumption	on page 31
HDMI Maximum Power Consumption	on page 31

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under [Table 4](#) may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the Operating Ranges or Parameters tables is not implied.

Table 4. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core supply voltages	VDDARM_IN VDDSOC_IN	-0.3	1.5	V
Internal supply voltages	VDDARM_CAP VDDARM23_CAP VDDSOC_CAP VDDPU_CAP	-0.3	1.3	V
GPIO supply voltage	Supplies denoted as I/O supply	-0.5	3.6	V
DDR I/O supply voltage	Supplies denoted as I/O supply	-0.4	1.975	V
LVDS I/O supply voltage	Supplies denoted as I/O supply	-0.3	2.8	V
VDDHIGH_IN supply voltage	VDDHIGH_IN	-0.3	3.6	V
USB VBUS	VBUS	—	5.25	V
Input voltage on USB_OTG_DP, USB_OTG_DN, USB_H1_DP, USB_H1_DN pins	USB_DP/USB_DN	-0.3	3.63	V
Input/output voltage range	V_{in}/V_{out}	-0.5	OVDD ¹ +0.3	V
ESD damage immunity: • Human Body Model (HBM) • Charge Device Model (CDM)	V_{esd}	— —	2000 500	V
Storage temperature range	$T_{STORAGE}$	-40	150	°C

¹ OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

4.1.2.1 FCPBGA Package Thermal Resistance

Table 5 provides the FCPBGA package thermal resistance data.

Table 5. FCPBGA Package Thermal Resistance Data

Thermal Parameter	Test Conditions	Symbol	Value		Unit
			No Lid	Lid	
Junction to Ambient ¹	Single-layer board (1s); natural convection ²	$R_{\theta JA}$	31	24	°C/W
	Four-layer board (2s2p); natural convection ²	$R_{\theta JA}$	22	15	°C/W
Junction to Ambient ¹	Single-layer board (1s); air flow 200 ft/min ³	$R_{\theta JMA}$	24	17	°C/W
	Four-layer board (2s2p); air flow 200 ft/min ³	$R_{\theta JMA}$	18	12	°C/W
Junction to Board ^{1,4}	—	$R_{\theta JB}$	12	5	°C/W
Junction to Case (top) ^{1,5}	—	$R_{\theta JTop}$	<0.1	1	°C/W

- ¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- ² Per JEDEC JESD51-3 with the single layer board horizontal. Thermal test board meets JEDEC specification for the specified package.
- ³ Per JEDEC JESD51-6 with the board horizontal.
- ⁴ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- ⁵ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1). The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4.1.3 Operating Ranges

Table 7 provides the operating ranges of the i.MX 6Dual/6Quad processors.

Table 7. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max ¹	Unit	Comment
Run mode: LDO enabled	VDDARM_IN VDDARM23_IN ²	1.35 ³		1.5	V	LDO Output Set Point (VDDARM_CAP ⁴) of 1.225 V minimum for operation up to 852 MHz or 996 MHz (depending on the device speed grade).
		1.25 ³		1.5	V	LDO Output Set Point (VDDARM_CAP ⁴) of 1.125 V minimum for operation up to 792 MHz.
		1.05 ³		1.5	V	LDO Output Set Point (VDDARM_CAP ⁴) of 0.925 V minimum for operation up to 396 MHz.
	VDDSOC_IN ⁵	1.350 ^{3,6}		1.5	V	264 MHz < VPU ≤ 352 MHz; VDDSOC and VDDPU LDO outputs (VDDSOC_CAP and VDDPU_CAP) require 1.225 V minimum.
		1.275 ^{3,6}		1.5	V	VPU ≤ 264 MHz; VDDSOC and VDDPU LDO outputs (VDDSOC_CAP and VDDPU_CAP) require 1.15 V minimum.
Run mode: LDO bypassed	VDDARM_IN VDDARM23_IN ²	1.225		1.3	V	LDO bypassed for operation up to 852 MHz or 996 MHz (depending on the device speed grade).
		1.125		1.3	V	LDO bypassed for operation up to 792 MHz.
		0.925		1.3	V	LDO bypassed for operation up to 396 MHz.
	VDDSOC_IN ⁵	1.225 ⁶		1.3	V	264 MHz < VPU ≤ 352 MHz
		1.15 ⁶		1.3	V	VPU ≤ 264 MHz
Standby/DSM Mode	VDDARM_IN VDDARM23_IN ²	0.9		1.3	V	See Table 11, "Stop Mode Current and Power Consumption," on page 27.
	VDDSOC_IN	0.9		1.3	V	
VDDHIGH internal Regulator	VDDHIGH_IN ⁷	2.8		3.3	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN ⁷	2.8		3.3	V	Should be supplied from the same supply as VDDHIGH_IN, if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG_VBUS	4.4		5.25	V	
	USB_H1_VBUS	4.4		5.25	V	
DDR I/O supply	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2, DDR3-U
		1.425	1.5	1.575	V	DDR3
		1.283	1.35	1.45	V	DDR3_L

Table 7. Operating Ranges (continued)

Supply for RGMII I/O power group ⁸	NVCC_RGMII	1.15		2.625	V	<ul style="list-style-type: none"> 1.15 V – 1.30 V in HSIC 1.2 V mode 1.43 V – 1.58 V in RGMII 1.5 V mode 1.70 V – 1.90 V in RGMII 1.8 V mode 2.25 V – 2.625 V in RGMII 2.5 V mode
GPIO supplies ⁸	NVCC_CSI, NVCC_EIM0, NVCC_EIM1, NVCC_EIM2, NVCC_ENET, NVCC_GPIO, NVCC_LCD, NVCC_NANDF, NVCC_SD1, NVCC_SD2, NVCC_SD3, NVCC_JTAG	1.65	1.8, 2.8, 3.3	3.6	V	Isolation between the NVCC_EIMx and NVCC_SDx different supplies allow them to operate at different voltages within the specified range. Example: NVCC_EIM1 can operate at 1.8 V while NVCC_EIM2 operates at 3.3 V.
	NVCC_LVDS2P5 ⁹ NVCC_MIPI	2.25	2.5	2.75	V	
HDMI supply voltages	HDMI_VP	0.99	1.1	1.3	V	
	HDMI_VPH	2.25	2.5	2.75	V	
PCIe supply voltages	PCIE_VP	1.023	1.1	1.3	V	
	PCIE_VPH	2.325	2.5	2.75	V	
	PCIE_VPTX	1.023	1.1	1.3	V	
SATA Supply voltages	SATA_VP	0.99	1.1	1.3	V	
	SATA_VPH	2.25	2.5	2.75	V	
Junction temperature	T _J	-40	90	105	°C	See Industrial qualification report for details (including product lifetime information).

¹ Applying the maximum voltage results in maximum power consumption and heat generation. Freescale recommends a voltage set point = (Vmin + the supply tolerance). This results in an optimized power/speed ratio.

² For Quad core system, connect to VDDARM_IN. For Dual core system, may be shorted to GND together with VDDARM23_CAP to reduce leakage.

³ VDDARM_IN and VDDSOC_IN must be at least 125 mV higher than the LDO Output Set Point for correct voltage regulation.

⁴ VDDARM_CAP must not exceed VDD_CACHE_CAP by more than 50 mV. VDD_CACHE_CAP must not exceed VDDARM_CAP by more than 200 mV.

⁵ VDDSOC_CAP and VDDPU_CAP must be equal.

⁶ VDDSOC and VDDPU output voltages must be set according to this rule: VDDARM-VDDSOC/PU<50mV.

⁷ While setting VDD_SNVS_IN voltage with respect to Charging Currents and RTC, see Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

⁸ All digital I/O supplies (NVCC_xxxx) must be powered under normal conditions whether the associated I/O pins are in use or not, and associated I/O pins need to have a pull-up or pull-down resistor applied to limit any floating gate current.

⁹ This supply also powers the pre-drivers of the DDR I/O pins; therefore, it must always be provided, even when LVDS is not used.

Table 8 shows on-chip LDO regulators that can supply on-chip loads.

Table 8. On-Chip LDOs¹ and their On-Chip Loads

Voltage Source	Load	Comment
VDDHIGH_CAP	NVCC_LVDS2P5	Board-level connection to VDDHIGH_CAP
	NVCC_MIPI	
	HDMI_VPH	
	PCIE_VPH	
	SATA_VPH	
VDDSOC_CAP ²	VDD_CACHE_CAP ³	Board-level connection to VDDSOC_CAP
	HDMI_VP	
	PCIE_VP	
	PCIE_VPTX	
	SATA_VP	

¹ On-chip LDOs are designed to supply the i.MX 6Dual/6Quad loads and must not be used to supply external loads.

² VDDARM_CAP/VDDARM23_CAP must not exceed VDDSOC_CAP by more than 50 mV.

³ VDD_CACHE_CAP must not exceed VDDARM_CAP by more than 200 mV. VDDARM_CAP must not exceed VDD_CACHE_CAP by more than 50 mV.

4.1.4 External Clock Sources

Each i.MX 6Dual/6Quad processor has two external input system clocks: a low frequency (RTC_XTAL) and a high frequency (XTAL).

The RTC_XTAL is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watchdog counters. The clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can substitute the RTC_XTAL, in case accuracy is not important.

The system clock input XTAL is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier.

Table 9 shows the interface frequency requirements.

Table 9. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTAL Oscillator ^{1,2}	f_{ckil}	—	32.768 ³ /32.0	—	kHz
XTAL Oscillator ^{4,2}	f_{xtal}		24		MHz

¹ External oscillator or a crystal with internal oscillator amplifier.

² The required frequency stability of this clock source is application dependent. For recommendations, see Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

³ Recommended nominal frequency 32.768 kHz.

⁴ External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in [Table 9](#) are required for use with Freescale BSPs to ensure precise time keeping and USB operation. For RTC_XTAL operation, two clock sources are available:

- On-chip 40 kHz ring oscillator: This clock source has the following characteristics:
 - Approximately 25 μ A more I_{dd} than crystal oscillator
 - Approximately $\pm 50\%$ tolerance
 - No external component required
 - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit
 - At power up, an internal ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
 - Higher accuracy than ring oscillator.
 - If no external crystal is present, then the ring oscillator is utilized.

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximal Supply Currents

The Power Virus numbers shown in [Table 10](#) represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The MMPF0100xxxx, Freescale's power management IC targeted for the i.MX 6x family, supports the Power Virus mode operating at 1% duty cycle. Higher duty cycles are allowed, but a robust thermal design is required for the increased system power dissipation.

See the i.MX 6Dual/6Quad Power Consumption Measurement Application Note (AN4509) for more details on typical power consumption under various use case definitions.

Table 10. Maximal Supply Currents

Power Line	Conditions	Max Current	Unit
VDDARM_IN+VDDARM23_IN	996 MHz ARM clock based on Power Virus operation	3920	mA
VDDSOC_IN	996 MHz ARM clock	1890	mA
VDDHIGH_IN	—	125 ¹	mA
VDD_SNVS_IN	—	275 ²	μ A
USB_OTG_VBUS/USB_H1_VBUS (LDO 3P0)	—	25 ³	mA
Primary Interface (IO) Supplies			

Table 10. Maximal Supply Currents (continued)

Power Line	Conditions	Max Current	Unit
NVCC_DRAM	—	— ⁴	
NVCC_ENET	N=10	Use maximal IO equation ⁵	
NVCC_LCD	N=29	Use maximal IO equation ⁵	
NVCC_GPIO	N=24	Use maximal IO equation ⁵	
NVCC_CSI	N=20	Use maximal IO equation ⁵	
NVCC_EIM0	N=19	Use maximal IO equation ⁵	
NVCC_EIM1	N=14	Use maximal IO equation ⁵	
NVCC_EIM2	N=20	Use maximal IO equation ⁵	
NVCC_JTAG	N=6	Use maximal IO equation ⁵	
NVCC_RGMII	N=12	Use maximal IO equation ⁵	
NVCC_SD1	N=6	Use maximal IO equation ⁵	
NVCC_SD2	N=6	Use maximal IO equation ⁵	
NVCC_SD3	N=11	Use maximal IO equation ⁵	
NVCC_NANDF	N=26	Use maximal IO equation ⁵	
NVCC_MIPi	—	25.5	mA
MISC			
DRAM_VREF	—	1	mA

¹ The actual maximum current drawn from VDDHIGH_IN will be as shown plus any additional current drawn from the VDDHIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_LVDS2P5, NVCC_MIPi, or HDMI, PCIe, and SATA VPH supplies).

² The maximum VDD_SNVs_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVs_IN can draw up to 1 mA, if available. VDD_SNVs_CAP charge time will increase if less than 1 mA is available.

³ This is the maximum current per active USB physical interface.

⁴ The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination. See the i.MX 6Dual/6Quad Power Consumption Measurement Application Note (AN4509) for examples of DRAM power consumption during specific use case scenarios.

⁵ General equation for estimated, maximal power consumption of an IO power supply:

$$I_{\max} = N \times C \times V \times (0.5 \times F)$$

Where:

N—Number of IO pins supplied by the power line

C—Equivalent external capacitive load

V—IO voltage

(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)

In this equation, I_{max} is in Amps, C in Farads, V in Volts, and F in Hertz.

4.1.6 Low Power Mode Supply Currents

Table 11 shows the current core consumption (not including I/O) of i.MX 6Dual/6Quad processors in selected low power modes.

Table 11. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical ¹	Unit
WAIT	<ul style="list-style-type: none"> ARM, SoC, and PU LDOs are set to 1.225 V HIGH LDO set to 2.5 V Clocks are gated DDR is in self refresh PLLs are active in bypass (24 MHz) Supply voltages remain ON 	VDDARM_IN (1.4 V)	6	mA
		VDDSoC_IN (1.4 V)	23	mA
		VDDHIGH_IN (3.0 V)	3.7	mA
		Total	52	mW
STOP_ON	<ul style="list-style-type: none"> ARM LDO set to 0.9 V SoC and PU LDOs set to 1.225 V HIGH LDO set to 2.5 V PLLs disabled DDR is in self refresh 	VDDARM_IN (1.4 V)	7.5	mA
		VDDSoC_IN (1.4 V)	22	mA
		VDDHIGH_IN (3.0 V)	3.7	mA
		Total	52	mW
STOP_OFF	<ul style="list-style-type: none"> ARM LDO set to 0.9 V SoC LDO set to 1.225 V PU LDO is power gated HIGH LDO set to 2.5 V PLLs disabled DDR is in self refresh 	VDDARM_IN (1.4 V)	7.5	mA
		VDDSoC_IN (1.4 V)	13.5	mA
		VDDHIGH_IN (3.0 V)	3.7	mA
		Total	41	mW
STANDBY	<ul style="list-style-type: none"> ARM and PU LDOs are power gated SoC LDO is in bypass HIGH LDO is set to 2.5 V PLLs are disabled Low voltage Well Bias ON XTAL is enabled 	VDDARM_IN (0.9 V)	0.1	mA
		VDDSoC_IN (0.9 V)	13	mA
		VDDHIGH_IN (3.0 V)	3.7	mA
		Total	22	mW
Deep Sleep Mode (DSM)	<ul style="list-style-type: none"> ARM and PU LDOs are power gated SoC LDO is in bypass HIGH LDO is set to 2.5 V PLLs are disabled Low voltage Well Bias ON XTAL and bandgap are disabled 	VDDARM_IN (0.9 V)	0.1	mA
		VDDSoC_IN (0.9 V)	2	mA
		VDDHIGH_IN (3.0 V)	0.5	mA
		Total	3.4	mW

¹ The typical values shown here are for information only and are not guaranteed. These values are average values measured on a worst-case wafer at 25°C.

4.1.7 USB PHY Current Consumption

4.1.7.1 Power Down Mode

In power down mode, everything is powered down, including the VBUS valid detectors, typ condition. [Table 12](#) shows the USB interface current consumption in power down mode.

Table 12. USB PHY Current Consumption in Power Down Mode

	VDDUSB_CAP (3.0 V)	VDDHIGH_CAP (2.5 V)	NVCC_PLL_OUT (1.1 V)
Current	5.1 μ A	1.7 μ A	<0.5 μ A

NOTE

The currents on the VDDHIGH_CAP and VDDUSB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.1.8 SATA Typical Power Consumption

Table 23 provides SATA PHY currents for certain Tx operating modes.

NOTE

Tx power consumption values are provided for a single transceiver. If
 T = single transceiver power and C = Clock module power, the total power
 required for N lanes = $N \times T + C$.

Table 13. SATA PHY Current Drain

Mode	Test Conditions	Supply	Typical Current	Unit
PO: Full-power state ¹	Single Transceiver	SATA_VP	11	mA
		SATA_VPH	13	
	Clock Module	SATA_VP	6.9	
		SATA_VPH	6.2	
PO: Mobile ²	Single Transceiver	SATA_VP	11	mA
		SATA_VPH	11	
	Clock Module	SATA_VP	6.9	
		SATA_VPH	6.2	
P0s: Transmitter idle	Single Transceiver	SATA_VP	9.4	mA
		SATA_VPH	2.9	
	Clock Module	SATA_VP	6.9	
		SATA_VPH	6.2	
P1: Transmitter idle, Rx powered down, LOS disabled	Single Transceiver	SATA_VP	0.67	mA
		SATA_VPH	0.23	
	Clock Module	SATA_VP	6.9	
		SATA_VPH	6.2	
P2: Powered-down state, only LOS and POR enabled	Single Transceiver	SATA_VP	0.53	mA
		SATA_VPH	0.11	
	Clock Module	SATA_VP	0.036	
		SATA_VPH	0.12	
PDDQ mode ³	Single Transceiver	SATA_VP	0.13	mA
		SATA_VPH	0.012	
	Clock Module	SATA_VP	0.008	
		SATA_VPH	0.004	

¹ Programmed for 1.0 V peak-to-peak Tx level.

² Programmed for 0.9 V peak-to-peak Tx level with no boost or attenuation.

³ LOW power non-functional.

4.1.9 PCIe 2.0 Maximum Power Consumption

Table 25 provides PCIe PHY currents for certain operating modes.

Table 14. PCIe PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
PO: Normal Operation	5G Operations	PCIe_VP (1.1 V)	40	mA
		PCIe_VPTX (1.1 V)	20	
		PCIe_VPH (2.5 V)	21	
	2.5G Operations	PCIe_VP (1.1 V)	27	
		PCIe_VPTX (1.1 V)	20	
		PCIe_VPH (2.5 V)	20	
POs: Low Recovery Time Latency, Power Saving State	5G Operations	PCIe_VP (1.1 V)	30	mA
		PCIe_VPTX (1.1 V)	2.4	
		PCIe_VPH (2.5 V)	18	
	2.5G Operations	PCIe_VP (1.1 V)	20	
		PCIe_VPTX (1.1 V)	2.4	
		PCIe_VPH (2.5 V)	18	
P1: Longer Recovery Time Latency, Lower Power State		PCIe_VP (1.1 V)	12	mA
		PCIe_VPTX (1.1 V)	2.4	
		PCIe_VPH (2.5 V)	12	
Power Down		PCIe_VP (1.1 V)	1.3	mA
		PCIe_VPTX (1.1 V)	0.18	
		PCIe_VPH (2.5 V)	0.36	

4.1.10 HDMI Maximum Power Consumption

Table 15 provides HDMI PHY currents for both Active 3D Tx with LFSR15 data pattern and Power-down modes.

Table 15. HDMI PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
Active	Bit rate 251.75 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.1	mA
	Bit rate 279.27 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.2	mA
	Bit rate 742.5 Mbps	HDMI_VPH	17	mA
		HDMI_VP	7.5	mA
	Bit rate 1.485 Gbps	HDMI_VPH	17	mA
		HDMI_VP	12	mA
	Bit rate 2.275 Gbps	HDMI_VPH	16	mA
		HDMI_VP	17	mA
	Bit rate 2.97 Gbps	HDMI_VPH	19	mA
		HDMI_VP	22	mA
Power-down		HDMI_VPH	49	μA
		HDMI_VP	1100	μA

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor

4.2.1 Power-Up Sequence

For power-up sequence, the restrictions are as follows:

- VDD_SNVS_IN supply must be turned ON before any other power supply. It may be connected (shorted) with VDDHIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- If VDDARM_IN and VDDSOC_IN are connected to different external supply sources, then VDDARM_IN supply must be turned ON together with VDDSOC_IN supply or not delayed more than 1 ms.

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the i.MX 6Dual/6Quad reference manual for further details and to ensure that all necessary requirements are being met.

NOTE

Ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG_VBUS and USB_H1_VBUS are not part of the power supply sequence and can be powered at any time.

4.2.2 Power-Down Sequence

No special restrictions for i.MX 6Dual/6Quad SoC.

4.2.3 Power Supplies Usage

- All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_XXX) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Group” column of [Table 93, "21 x 21 mm Functional Contact Assignments,"](#) on page 146.

- When the SATA interface is not used, the SATA_VP and SATA_VPH supplies should be grounded. The input and output supplies for rest of the ports (SATA_REFCLKM, SATA_REFCLKP, SATA_REXT, SATA_RXM, SATA_RXP, and SATA_TXM) can be left floating. It is recommended not to turn OFF the SATA_VPH supply while the SATA_VP supply is ON, as it may lead to excessive power consumption. If boundary scan test is used, SATA_VP and SATA_VPH must remain powered.
- When the PCIE interface is not used, the PCIE_VP, PCIE_VPH, and PCIE_VPTX supplies should be grounded. The input and output supplies for rest of the ports (PCIE_REXT, PCIE_RXM, PCIE_RXP, PCIE_TXM, and PCIE_TXP) can be left floating. It is recommended not to turn the PCIE_VPH supply OFF while the PCIE_VP supply is ON, as it may lead to excessive power consumption. If boundary scan test is used, PCIE_VP, PCIE_VPH, and PCIE_VPTX must remain powered.

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the i.MX 6Dual/6Quad reference manual for details on the power tree scheme recommended operation.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on die trimming. This translates into more voltage for the die producing higher operating frequencies. These regulators have three basic modes.

- Bypass. The regulation FET is switched fully on passing the external voltage, DCDC_LOW, to the load unaltered. The analog part of the regulator is powered down in this state, removing any loss other than the IR drop through the power grid and FET.
- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

For additional information, see the i.MX 6Dual/6Quad reference manual.

4.3.2 Analog Regulators

4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDDHIGH_IN (see [Table 7](#) for min and max input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. Since we are not testing the accuracy or the % regulation, and only testing with the LDO set to either 1.0V or 1.2V, this is the only range that is guaranteed. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 μ F (2.2 μ F should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For additional information, see the i.MX 6Dual/6Quad reference manual.

4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDDHIGH_IN (see [Table 7](#) for min and max input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. Since we are not testing the accuracy or the % regulation, and only testing with the LDO set to either 2.25V or 2.75V, this is the only range that is guaranteed. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 μ F (2.2 μ F should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω .

For additional information, see the i.MX 6Dual/6Quad reference manual.

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB_OTG_VBUS and USB_H1_VBUS voltages (4.4 V–5.25 V) to produce a nominal 3.0 V output voltage. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 μ F (2.2 μ F should be considered the recommended minimum value), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either VBUS supply, when both are present. If only one of the

VBUS voltage is present, then the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets. If no VBUS voltage is present, then the VBUSVALID threshold setting will prevent the regulator from being enabled.

For additional information, see the i.MX 6Dual/6Quad reference manual.

4.4 PLL Electrical Characteristics

4.4.1 Audio/Video PLL Electrical Parameters

Table 16. Audio/Video PLL Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.2 528 MHz PLL

Table 17. 528 MHz PLL Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.3 Ethernet PLL

Table 18. Ethernet PLL Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.4 480 MHz PLL

Table 19. 480 MHz PLL Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles

4.4.5 ARM PLL

Table 20. ARM PLL Electrical Parameters

Parameter	Value
Clock output range	650 MHz~1.3 GHz
Reference clock	24 MHz
Lock time	<2250 reference cycles

4.5 On-Chip Oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements an oscillator. The oscillator is powered from NVCC_PLL_OUT.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDDHIGH_IN such as the oscillator consumes power from VDDHIGH_IN when that supply is available and transitions to the back up battery when VDDHIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 kHz clock will automatically switch to a crude internal ring oscillator. The frequency range of this block is approximately 10–45 kHz. It highly depends on the process, voltage, and temperature.

The OSC32k runs from VDD_SNVS_CAP, which comes from the VDDHIGH_IN/VDD_SNVS_IN power mux. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDDHIGH_IN range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs

depends on the charge current limit that depends on the chosen coin cell. For example, for Panasonic ML621:

- Average Discharge Voltage is 2.5 V
- Maximum Charge Current is 0.6 mA

For a charge voltage of 3.2 V, $R_s = (3.2 - 2.5) / 0.6 \text{ m} = 1.17 \text{ k}$

NOTE

Always refer to the chosen coin cell manufacturer's data sheet for the latest information.

Table 21. OSC32K Main Characteristics

Parameter	Min	Typ	Max	Comments
Fosc		32.768 kHz		This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.
Current consumption		4 μA		The typical value shown is only for the oscillator, driven by an external crystal. If the internal ring oscillator is used instead of an external crystal, then approximately 25 μA should be added to this value.
Bias resistor		14 M Ω		This is the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amplifier. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Target Crystal Properties				
Cload		10 pF		Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR		50 k Ω	100 k Ω	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O

NOTE

The term 'OVDD' in this section refers to the associated supply rail of an input or output.

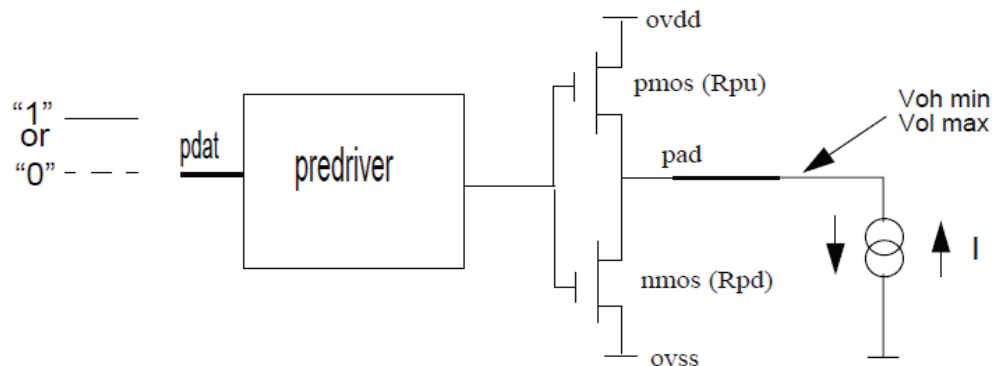


Figure 3. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 General Purpose I/O (GPIO) DC Parameters

Table 22 shows DC parameters for GPIO pads. The parameters in Table 22 are guaranteed per the operating ranges in Table 7, unless otherwise noted.

Table 22. GPIO I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage ¹	Voh	Ioh = -0.1 mA (DSE ² = 001, 010) Ioh = -1 mA (DSE = 011, 100, 101, 110, 111)	OVDD - 0.15	—	V
Low-level output voltage ¹	Vol	Iol = 0.1 mA (DSE ² = 001, 010) Iol = 1 mA (DSE = 011, 100, 101, 110, 111)	—	0.15	V
High-Level DC input voltage ^{1, 3}	Vih	—	0.7 × OVDD	OVDD	V
Low-Level DC input voltage ^{1, 3}	Vil	—	0	0.3 × OVDD	V
Input Hysteresis	Vhys	OVDD = 1.8 V OVDD = 3.3 V	0.25	—	V
Schmitt trigger VT+ ^{3, 4}	VT+	—	0.5 × OVDD	—	V
Schmitt trigger VT- ^{3, 4}	VT-	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = OVDD or 0	-1	1	μA
Input current (22 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	212 1	μA
Input current (47 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	100 1	μA
Input current (100 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	48 1	μA
Input current (100 kΩ pull-down)	Iin	Vin = 0 V Vin = OVDD	—	1 48	μA
Keeper circuit resistance	Rkeep	Vin = 0.3 × OVDD Vin = 0.7 × OVDD	105	175	kΩ

Table 22. GPIO I/O DC Parameters (continued)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Sink current in Open Drain mode	Iskod	—	—	7	mA
Sink/source current in Push-Pull mode	Isspp	—	—	7	mA

¹ Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

² DSE is the Drive Strength Field setting in the associated IOMUX control register.

³ To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

⁴ Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.2 DDR I/O DC Parameters

The DDR I/O pads support LPDDR2 and DDR3/DDR3L operational modes.

4.6.2.1 LPDDR2 Mode I/O DC Parameters

The LPDDR2 interface mode fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The parameters in [Table 23](#) are guaranteed per the operating ranges in [Table 7](#), unless otherwise noted.

Table 23. LPDDR2 I/O DC Electrical Parameters¹

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	Voh	Ioh = -0.1 mA	0.9*OVDD	—	V
Low-level output voltage	Vol	Iol = 0.1 mA	—	0.1*OVDD	V
Input reference voltage	Vref		0.49*OVDD	0.51*OVDD	
DC input High Voltage	Vih(dc)	—	Vref+0.13V	OVDD	V
DC input Low Voltage	Vil(dc)	—	OVSS	Vref-0.13V	V
Differential Input Logic High	Vih(diff)		0.26	See Note ²	
Differential Input Logic Low	Vil(diff)		See Note ²	-0.26	
Input current (no pull-up/down)	Iin	Vin = 0 or OVDD	-2.5	2.5	μA
Pull-up/pull-down impedance mismatch	MMpupd		-15	+15	%
240 Ω unit calibration resolution	Rres			10	Ω
Keeper circuit resistance	Rkeep	—	110	175	kΩ

¹ Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

² The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot (see [Table 28](#)).

4.6.2.2 DDR3/DDR3L Mode I/O DC Parameters

The DDR3/DDR3L interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008. The parameters in Table 24 are guaranteed per the operating ranges in Table 7, unless otherwise noted.

Table 24. DDR3/DDR3L I/O DC Electrical Parameters

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	Voh	Ioh = -0.1 mA Voh (DSE = 001)	0.8*OVDD ¹	—	V
		Ioh = -1 mA Voh (for all except DSE = 001)			
Low-level output voltage	Vol	Iol = 0.1 mA Vol (DSE = 001)	—	0.2*OVDD	V
		Iol = 1 mA Vol (for all except DSE = 001)			
Input reference voltage	Vref ²		0.49*OVDD	0.51*OVDD	
DC input Logic High	Vih(dc)	—	Vref+0.1	OVDD	V
DC input Logic Low	Vil(dc)	—	OVSS	Vref-0.1	V
Differential input Logic High	Vih(diff)	—	0.2	See Note ³	V
Differential input Logic Low	Vil(diff)	—	See Note ³	-0.2	V
Termination Voltage	Vtt	Vtt tracking OVDD/2	0.49*OVDD	0.51*OVDD	V
Input current (no pull-up/down)	Iin	Vin = 0 or OVDD	-2.9	2.9	μA
Pull-up/pull-down impedance mismatch	MMpupd	—	-10	10	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper circuit resistance	Rkeep	—	105	175	kΩ

¹ OVDD – I/O power supply (1.425 V–1.575 V for DDR3 and 1.283 V–1.45 V for DDR3L)

² Vref – DDR3/DDR3L external reference voltage

³ The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot (see Table 29).

4.6.3 LVDS I/O DC Parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

Table 25 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 25. LVDS I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Differential Voltage	V _{OD}	Rload=100 Ω between padP and padN	250	450	mV

Table 25. LVDS I/O DC Parameters (continued)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output High Voltage	V_{OH}	$I_{OH} = 0 \text{ mA}$	1.25	1.6	V
Output Low Voltage	V_{OL}	$I_{OL} = 0 \text{ mA}$	0.9	1.25	
Offset Voltage	V_{OS}	—	1.125	1.375	

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in [Figure 4](#) and [Figure 5](#).

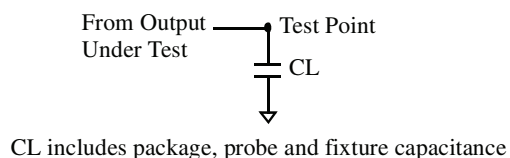


Figure 4. Load Circuit for Output

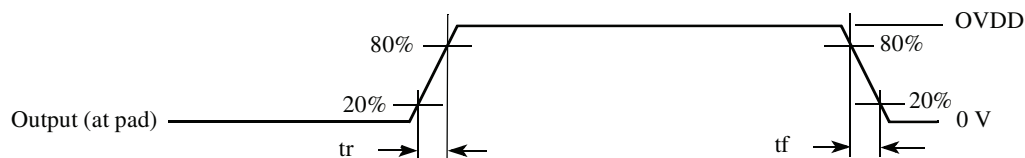


Figure 5. Output Transition Time Waveform

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the [Table 26](#) and [Table 27](#), respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 26. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times ¹	trm	—	—	—	25	ns

¹ Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 27. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive, ipp_dse=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times ¹	trm	—	—	—	25	ns

¹ Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.7.2 DDR I/O AC Parameters

The LPDDR2 interface mode fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3/DDR3L interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 28 shows the AC parameters for DDR I/O operating in LPDDR2 mode.

Table 28. DDR I/O LPDDR2 Mode AC Parameters¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.22	V
AC differential input high voltage ²	Vidh(ac)	—	0.44	—	—	V
AC differential input low voltage	Vidl(ac)	—	—	—	0.44	V
Input AC differential cross point voltage ³	Vix(ac)	Relative to Vref	-0.12	—	0.12	V
Over/undershoot peak	Vpeak	—	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	533 MHz	—	—	0.3	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 40 Ω \pm 30%	1.5	—	3.5	V/ns
		50 Ω to Vref. 5pF load. Drive impedance = 60 Ω \pm 30%	1	—	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t _{SKD}	clk = 533 MHz	—	—	0.1	ns

¹ Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

² Vid(ac) specifies the input differential voltage $V_{tr} - V_{cp}$ required for switching, where V_{tr} is the “true” input signal and V_{cp} is the “complementary” input signal. The Minimum value is equal to $V_{ih}(ac) - V_{il}(ac)$.

³ The typical value of Vix(ac) is expected to be about 0.5 * OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 29 shows the AC parameters for DDR I/O operating in DDR3/DDR3L mode.

Table 29. DDR I/O DDR3/DDR3L Mode AC Parameters¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.175	V
AC differential input voltage ²	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage ³	Vix(ac)	Relative to Vref	Vref – 0.15	—	Vref + 0.15	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	533 MHz	—	—	0.5	V-ns

Table 29. DDR I/O DDR3/DDR3L Mode AC Parameters¹ (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	Driver impedance = 34 Ω	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t _{SKD}	clk = 533 MHz	—	—	0.1	ns

¹ Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

² Vid(ac) specifies the input differential voltage |Vtr-Vcpl| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

³ The typical value of Vix(ac) is expected to be about 0.5 * OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.7.3 LVDS I/O AC Parameters

The differential output transition time waveform is shown in Figure 6.

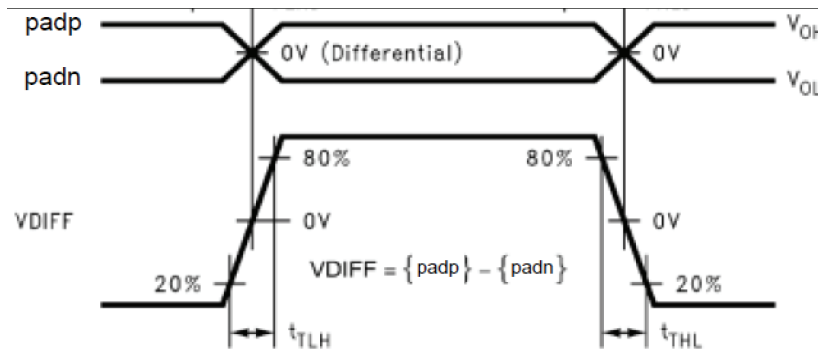


Figure 6. Differential LVDS Driver Transition Time Waveform

Table 30 shows the AC parameters for LVDS I/O.

Table 30. I/O AC Parameters of LVDS Pad

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew ¹	t _{SKD}	Rload = 100 Ω , Cload = 2 pF	—	—	0.25	ns
Transition Low to High Time ²	t _{TLH}		—	—	0.5	
Transition High to Low Time ²	t _{THL}		—	—	0.5	
Operating Frequency	f	—	—	600	800	MHz
Offset voltage imbalance	Vos	—	—	—	150	mV

¹ t_{SKD} = |t_{PHLD} - t_{PLHD}|, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

² Measurement levels are 20-80% from output voltage.

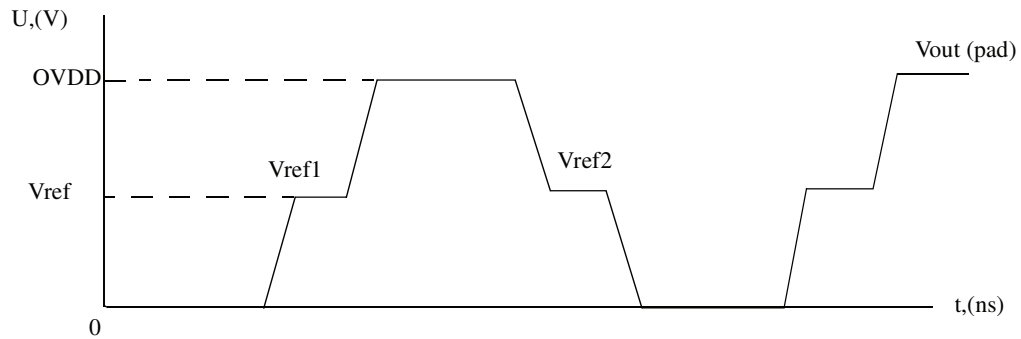
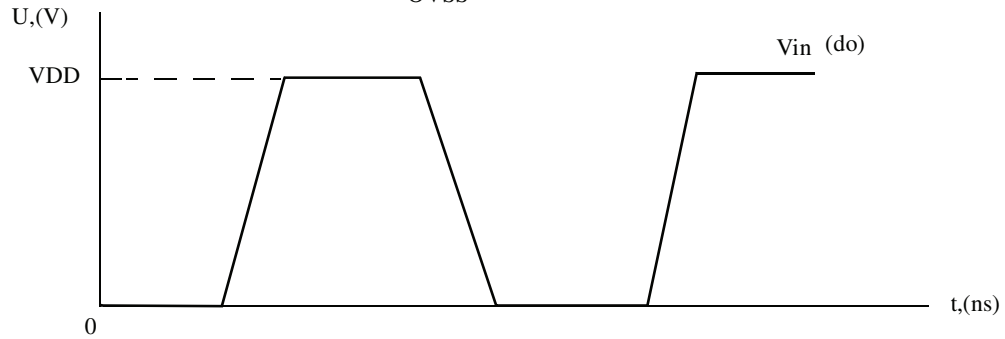
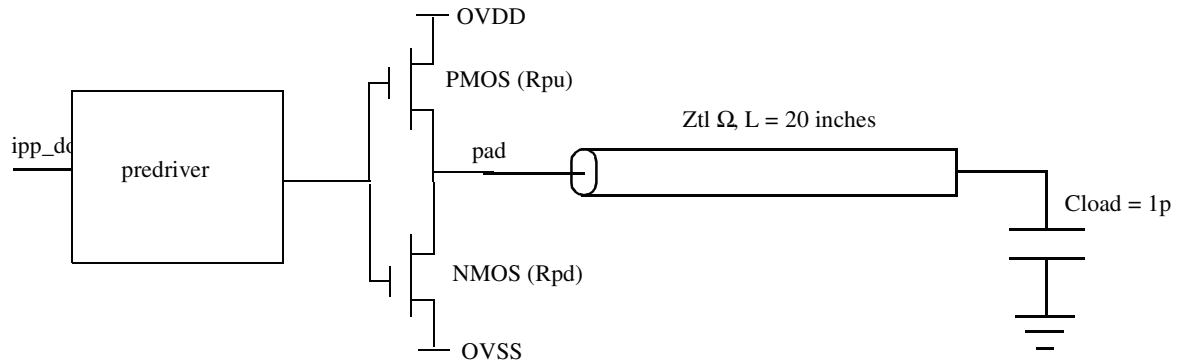
4.8 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters of the i.MX 6Dual/6Quad processors for the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2, and DDR3 modes
- LVDS I/O

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Z_{tl} attached to I/O pad and incident wave launched into transmission line. R_{pu}/R_{pd} and Z_{tl} form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see [Figure 7](#)).



$$R_{pu} = \frac{V_{ovdd} - V_{ref1}}{V_{ref1}} \times Z_{tl}$$

$$R_{pd} = \frac{V_{ref2}}{V_{ovdd} - V_{ref2}} \times Z_{tl}$$

Figure 7. Impedance Matching Load for Measurement

4.8.1 GPIO Output Buffer Impedance

Table 31 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 31. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
Output Driver Impedance	Rdrv	001	260	Ω
		010	130	
		011	90	
		100	60	
		101	50	
		110	40	
		111	33	

Table 32 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 32. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
Output Driver Impedance	Rdrv	001	150	Ω
		010	75	
		011	50	
		100	37	
		101	30	
		110	25	
		111	20	

4.8.2 DDR I/O Output Buffer Impedance

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 33 shows DDR I/O output buffer impedance of i.MX 6Dual/6Quad processors.

Table 33. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	Drive Strength (DSE) =			Ω
		000	Hi-Z	Hi-Z	
		001	240	240	
		010	120	120	
		011	80	80	
		100	60	60	
		101	48	48	
		110	40	40	
		111	34	34	

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.
2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is $\pm 5\%$ (max/min impedance) across PVTs.

4.8.3 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6Dual/6Quad processor.

4.9.1 Reset Timings Parameters

Figure 8 shows the reset timing and Table 34 lists the timing parameters.

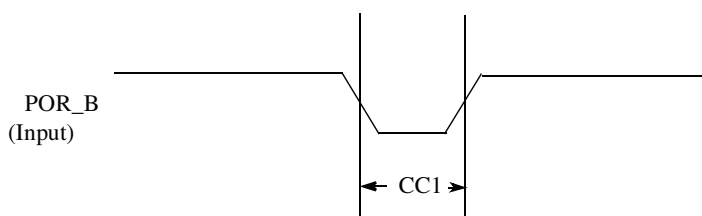


Figure 8. Reset Timing Diagram

Table 34. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid (input slope ≤ 5 ns)	1	—	RTC_XTALI cycle

4.9.2 WDOG Reset Timing Parameters

Figure 9 shows the WDOG reset timing and Table 35 lists the timing parameters.

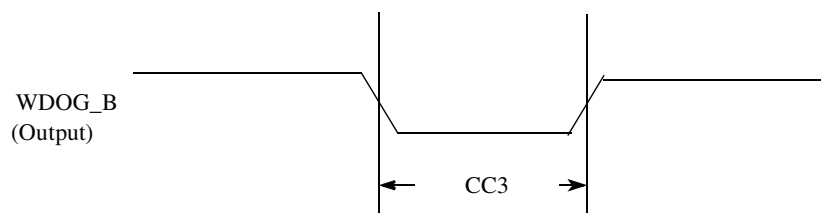


Figure 9. WDOG_B Timing Diagram

Table 35. WDOG_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG_B Assertion	1	—	RTC_XTALI cycle

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 μ s.

NOTE

WDOG_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM.

4.9.3.1 EIM Signal Cross Reference

Table 36 is a guide intended to help the user identify the signals in the EIM chapter of the i.MX 6Dual/6Quad reference manual that are identical to those mentioned in this data sheet.

Table 36. EIM Signal Cross Reference

Reference Manual EIM Chapter Nomenclature	Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUXC Controller Chapter Nomenclature
BCLK	EIM_BCLK
CSx_B	EIM_CSx
WE_B	EIM_RW
OE_B	EIM_OE
BEy_B	EIM_EBx
ADV_B	EIM_LBA
ADDR	EIM_A[25:16], EIM_DA[15:0]
ADDR/M_DATA	EIM_DAx (Addr/Data muxed mode)
DATA	EIM_NFC_D (Data bus shared with NAND Flash) EIM_Dx (dedicated data bus)
WAIT_B	EIM_WAIT

4.9.3.2 EIM Interface Pads Allocation

EIM supports 32-bit, 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. Table 37 provides EIM interface pads allocation in different modes.

Table 37. EIM Internal Module Multiplexing¹

Setup	Non Multiplexed Address/Data Mode							Multiplexed Address/Data mode	
	8 Bit				16 Bit		32 Bit	16 Bit	32 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 110	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 0, DSZ = 011	MUM = 1, DSZ = 001	MUM = 1, DSZ = 011
A[15:0]	EIM_DA_A [15:0]	EIM_DA_A [15:0]	EIM_DA_A [15:0]	EIM_DA_A [15:0]	EIM_DA_A [15:0]	EIM_DA_A [15:0]	EIM_DA_A [15:0]	EIM_DA_A [15:0]	EIM_DA_A [15:0]
A[25:16]	EIM_A [25:16]	EIM_A [25:16]	EIM_A [25:16]	EIM_A [25:16]	EIM_A [25:16]	EIM_A [25:16]	EIM_A [25:16]	EIM_A [25:16]	EIM_D [9:0]
D[7:0], EIM_EB0	EIM_D [7:0]	—	—	—	EIM_D [7:0]	—	EIM_D [7:0]	EIM_DA_A [7:0]	EIM_DA_A [7:0]
D[15:8], EIM_EB1	—	EIM_D [15:8]	—	—	EIM_D [15:8]	—	EIM_D [15:8]	EIM_DA_A [15:8]	EIM_DA_A [15:8]
D[23:16], EIM_EB2	—	—	EIM_D [24:16]	—	—	EIM_D [23:16]	EIM_D [23:16]	—	EIM_D [7:0]
D[31:24], EIM_EB3	—	—	—	EIM_D [31:24]	—	EIM_D [31:24]	EIM_D [31:24]	—	EIM_D [15:8]

¹ For more information on configuration ports mentioned in this table, see the i.MX 6Dual/6Quad reference manual.

4.9.3.3 General EIM Timing-Synchronous Mode

Figure 10, Figure 11, and Table 38 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

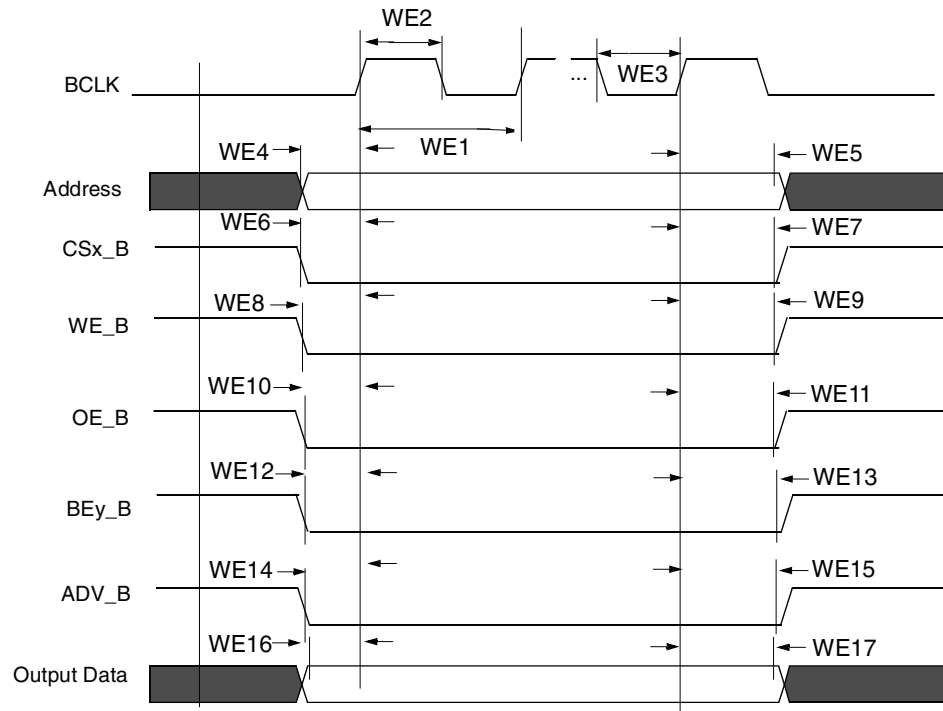


Figure 10. EIM Output Timing Diagram

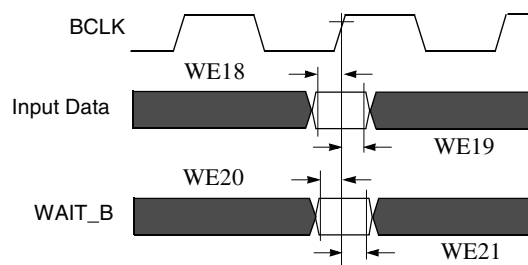


Figure 11. EIM Input Timing Diagram

4.9.3.4 Examples of EIM Synchronous Accesses

Table 38. EIM Bus Timing Parameters

ID	Parameter	Min ¹	Max ¹	Unit
WE1	BCLK cycle time ²	$t^*(k+1)$	—	ns
WE2	BCLK high level width	$0.4 * t^*(k+1)$	—	ns

Table 38. EIM Bus Timing Parameters (continued)

WE3	BCLK low level width	$0.4 \cdot t \cdot (k+1)$	—	ns
WE4	Clock rise to address valid	—	$-0.5 \cdot t \cdot (k+1)/2 + 2.25$	ns
WE5	Clock rise to address invalid	$0.5 \cdot t \cdot (k+1)/2 - 1.25$	—	ns
WE6	Clock rise to CSx_B valid	—	$-0.5 \cdot t \cdot (k+1)/2 + 2.25$	ns
WE7	Clock rise to CSx_B invalid	$0.5 \cdot t \cdot (k+1)/2 - 1.25$	—	ns
WE8	Clock rise to WE_B valid	—	$-0.5 \cdot t \cdot (k+1)/2 + 2.25$	ns
WE9	Clock rise to WE_B invalid	$0.5 \cdot t \cdot (k+1)/2 - 1.25$	—	ns
WE10	Clock rise to OE_B valid	—	$-0.5 \cdot t \cdot (k+1)/2 + 2.25$	ns
WE11	Clock rise to OE_B invalid	$0.5 \cdot t \cdot (k+1)/2 - 1.25$	—	ns
WE12	Clock rise to BEy_B valid	—	$-0.5 \cdot t \cdot (k+1)/2 + 2.25$	ns
WE13	Clock rise to BEy_B invalid	$0.5 \cdot t \cdot (k+1)/2 - 1.25$	—	ns
WE14	Clock rise to ADV_B valid	—	$-0.5 \cdot t \cdot (k+1)/2 + 2.25$	ns
WE15	Clock rise to ADV_B invalid	$0.5 \cdot t \cdot (k+1)/2 - 1.25$	—	ns
WE16	Clock rise to output data valid	—	$-(k+1) \cdot t/2 + 2.75$	ns
WE17	Clock rise to output data invalid	$(k+1) \cdot t/2 - 1.25$	—	ns
WE18	Input data setup time to clock rise	2.3	—	ns
WE19	Input data hold time from clock rise	2	—	ns
WE20	WAIT_B setup time to clock rise	2	—	ns
WE21	WAIT_B hold time from clock rise	2	—	ns

¹ k represents BCD value² EIM maximum operating frequency is 104 MHz (t = 9.165 ns)

Figure 12 to Figure 15 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

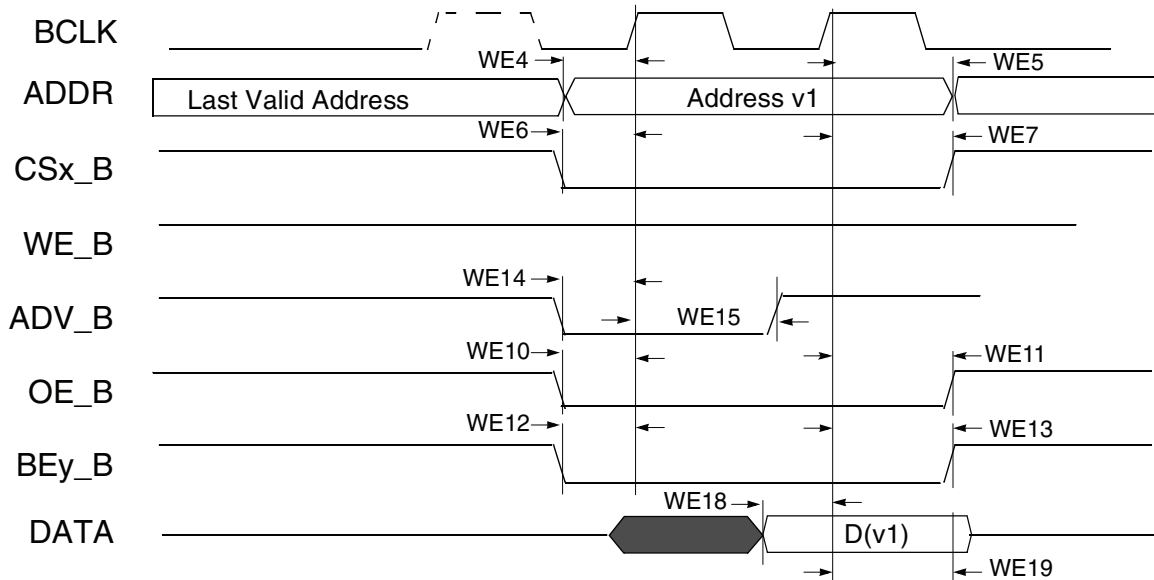


Figure 12. Synchronous Memory Read Access, WSC=1

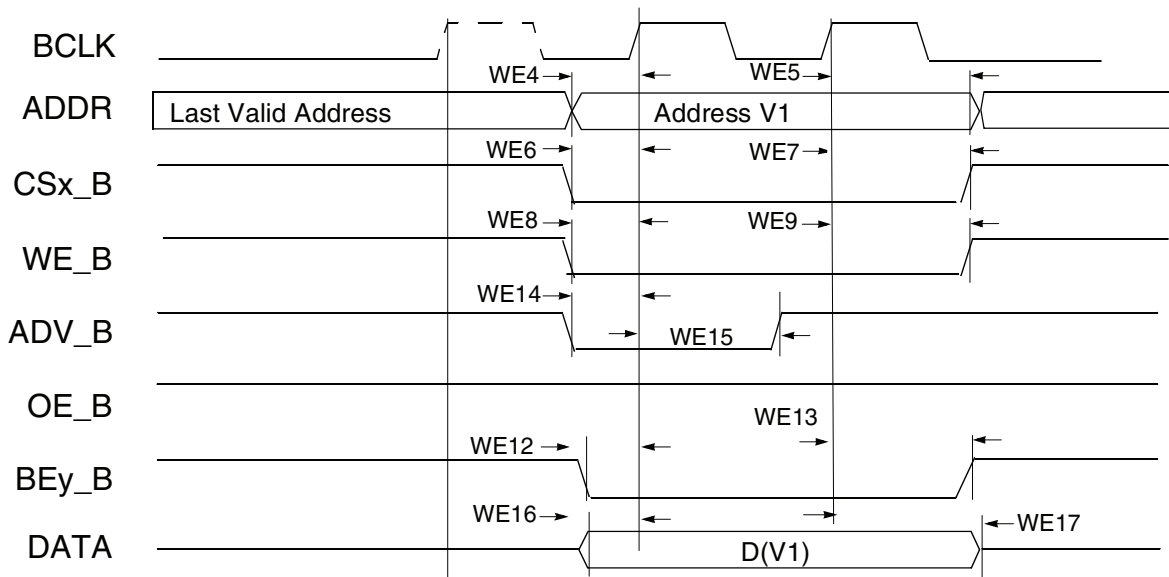


Figure 13. Synchronous Memory, Write Access, WSC=1, WBEA=0 and WADVN=0

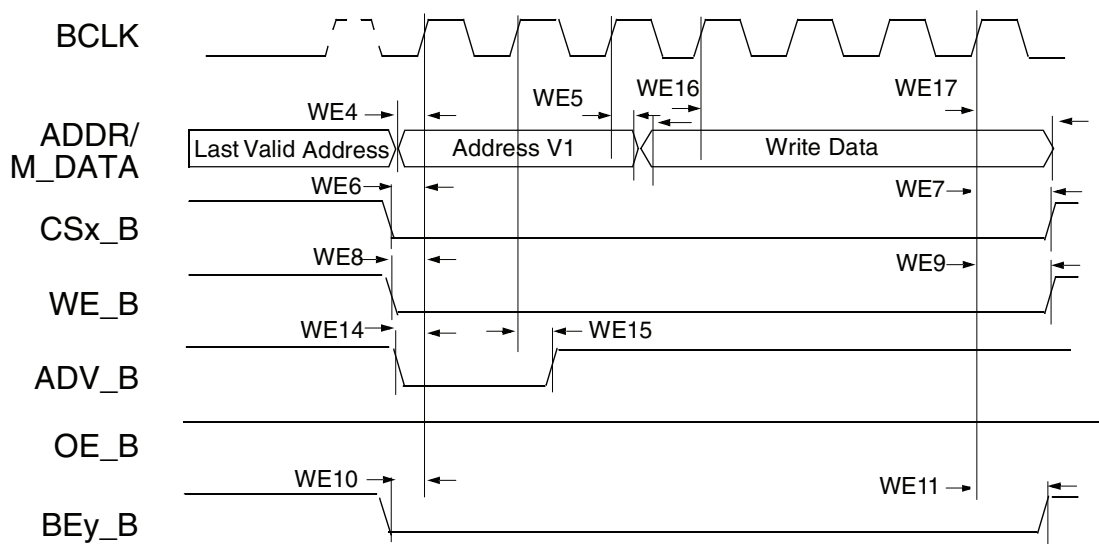


Figure 14. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6,ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

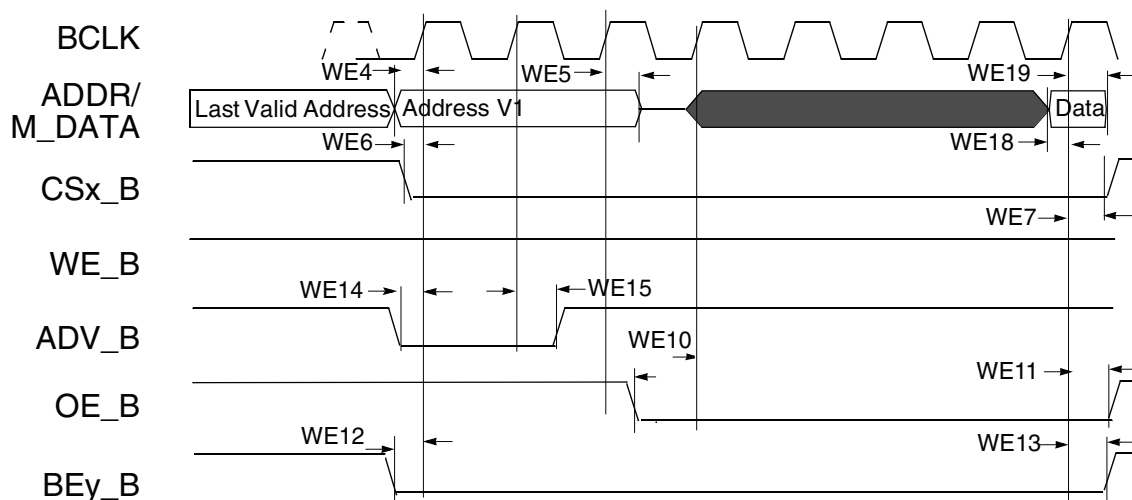


Figure 15. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.5 General EIM Timing-Asynchronous Mode

Figure 16 through Figure 20 and Table 39 provide timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 16 through Figure 19 as RWSC, OEN & CSN is configured differently. See the i.MX 6Dual/6Quad reference manual for the EIM programming model.

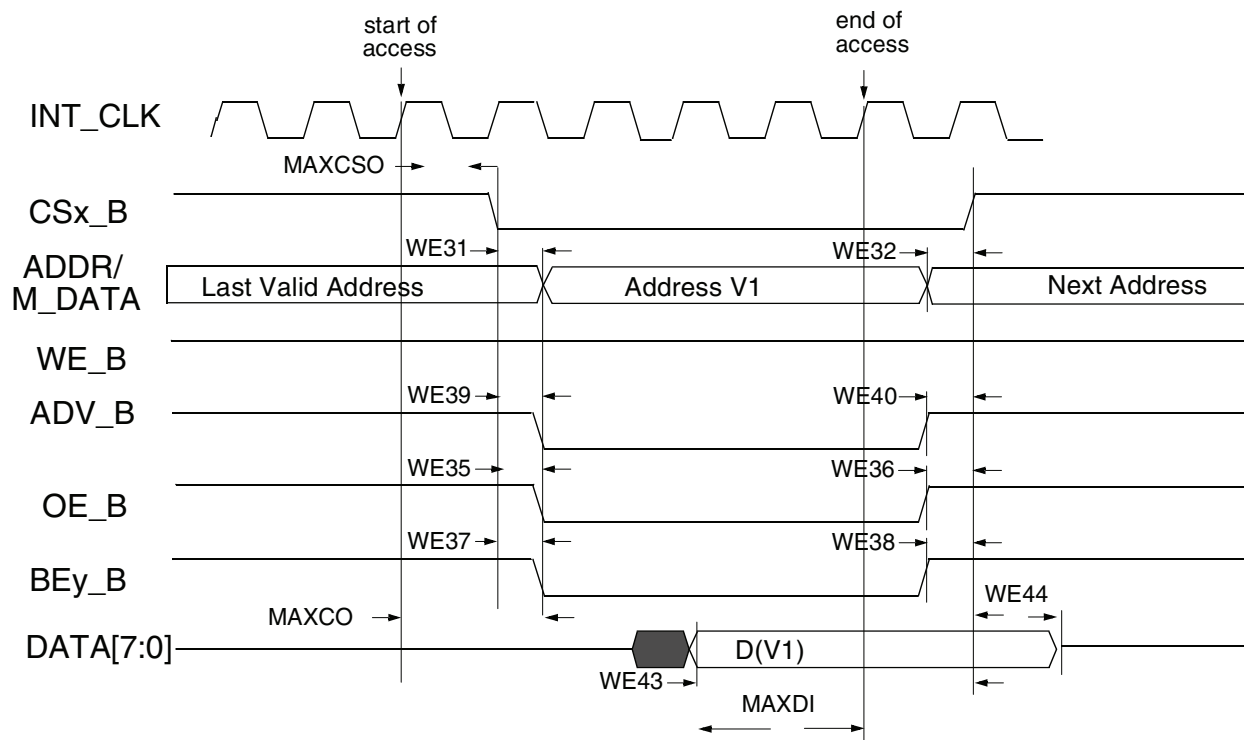


Figure 16. Asynchronous Memory Read Access (RWSC = 5)

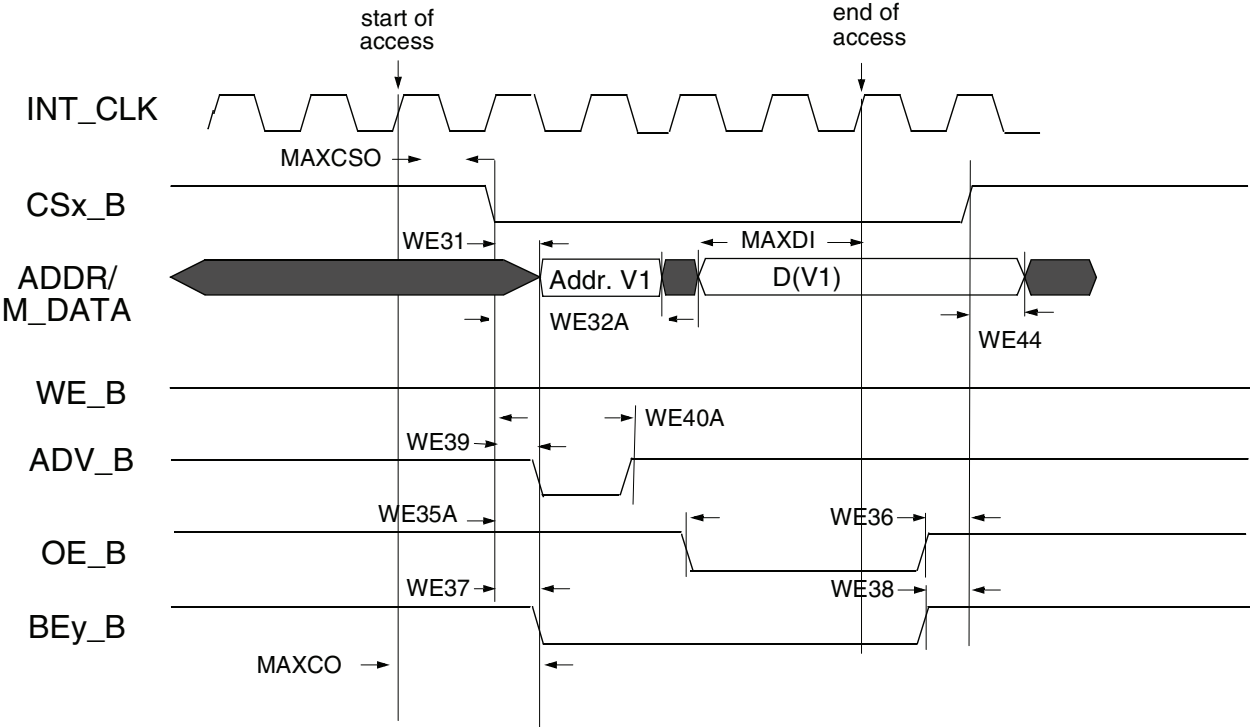


Figure 17. Asynchronous A/D Muxed Read Access (RWSC = 5)

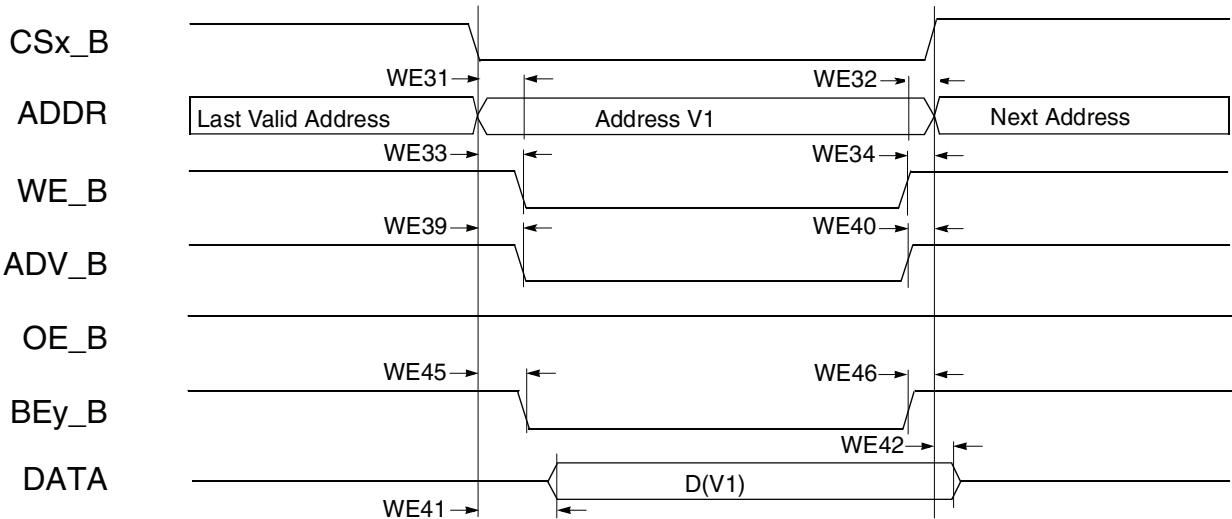


Figure 18. Asynchronous Memory Write Access

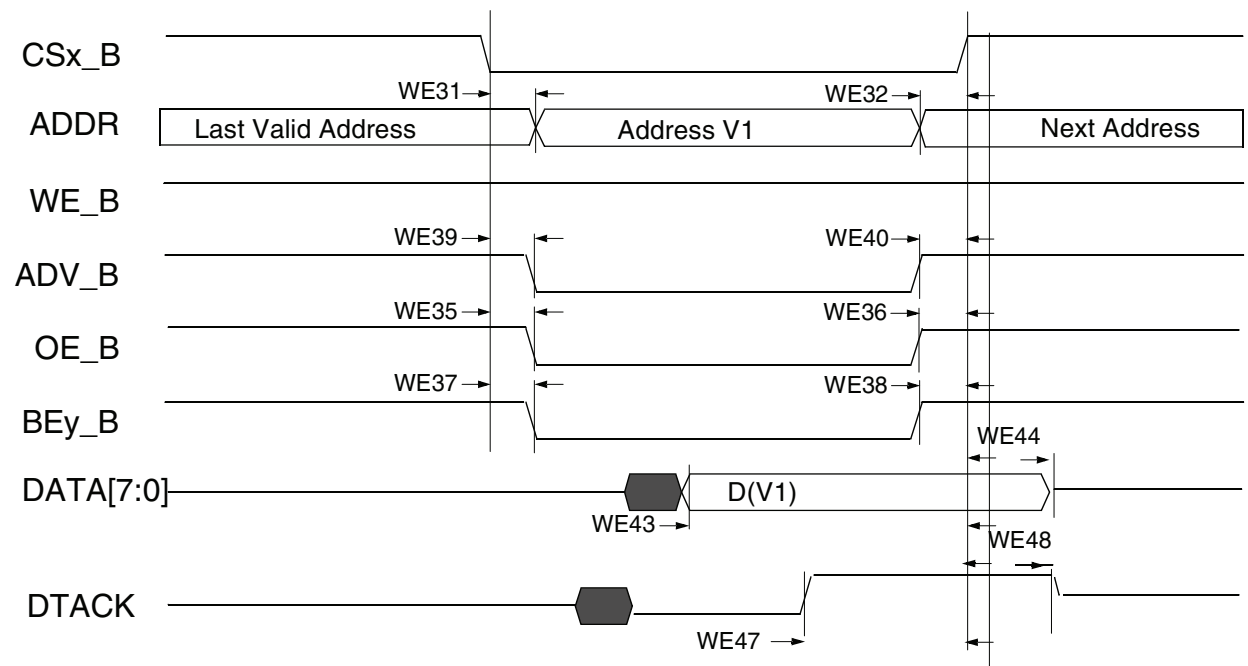
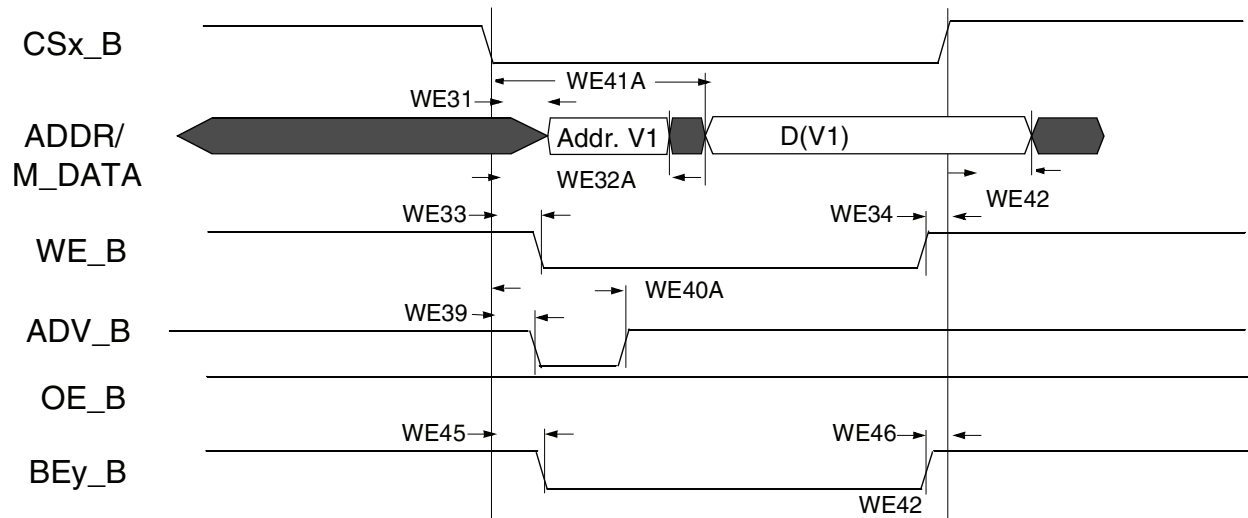


Figure 20. DTACK Read Access (DAP=0)

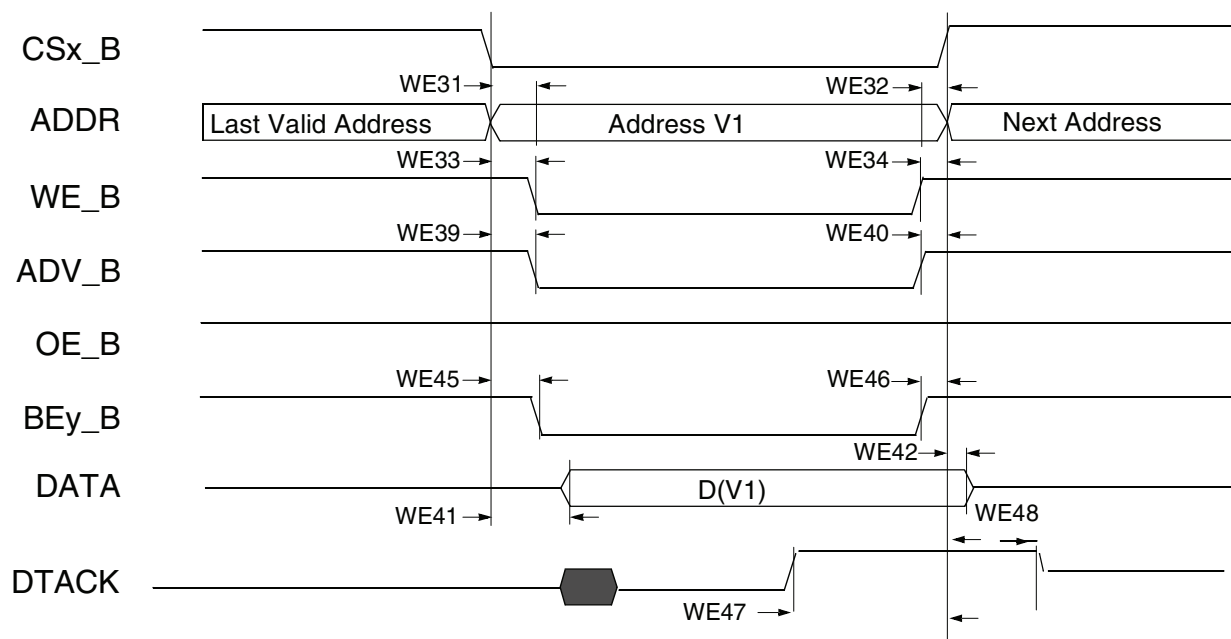


Figure 21. DTACK Write Access (DAP=0)

Table 39. EIM Asynchronous Timing Parameters Table Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters ¹	Min	Max (If 132 MHz is supported by SoC)	Unit
WE31	CSx_B valid to Address Valid	WE4 - WE6 - CSA ²	—	3 - CSA	ns
WE32	Address Invalid to CSx_B invalid	WE7 - WE5 - CSN ³	—	3 - CSN	ns
WE32A (muxed A/D)	CSx_B valid to Address Invalid	$t^4 + WE4 - WE7 + (ADV_N^5 + ADVA^6 + 1 - CSA)$	-3 + (ADV_N + ADVA + 1 - CSA)	—	ns
WE33	CSx_B Valid to WE_B Valid	WE8 - WE6 + (WEA - WCSA)	—	3 + (WEA - WCSA)	ns
WE34	WE_B Invalid to CSx_B Invalid	WE7 - WE9 + (WEN - WCSN)	—	3 - (WEN - WCSN)	ns
WE35	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA - RCSA)	—	3 + (OEA - RCSA)	ns
WE35A (muxed A/D)	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - RCSA)	-3 + (OEA + RADVN + RADVA + ADH + 1 - RCSA)	3 + (OEA + RADVN + RADVA + ADH + 1 - RCSA)	ns
WE36	OE_B Invalid to CSx_B Invalid	WE7 - WE11 + (OEN - RCSN)	—	3 - (OEN - RCSN)	ns
WE37	CSx_B Valid to BEy_B Valid (Read access)	WE12 - WE6 + (RBEA - RCSA)	—	3 + (RBEA - RCSA)	ns
WE38	BEy_B Invalid to CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - RCSN)	—	3 - (RBEN - RCSN)	ns
WE39	CSx_B Valid to ADV_B Valid	WE14 - WE6 + (ADVA - CSA)	—	3 + (ADVA - CSA)	ns

Table 39. EIM Asynchronous Timing Parameters Table Relative Chip Select (continued)

Ref No.	Parameter	Determination by Synchronous measured parameters ¹	Min	Max (If 132 MHz is supported by SoC)	Unit
WE40	ADV_B Invalid to CSx_B Invalid (ADVL is asserted)	WE7 - WE15 - CSN	—	3 - CSN	ns
WE40A (muxed A/D)	CSx_B Valid to ADV_B Invalid	WE14 - WE6 + (ADV _N + ADVA + 1 - CSA)	-3 + (ADV _N + ADVA + 1 - CSA)	3 + (ADV _N + ADVA + 1 - CSA)	ns
WE41	CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA	—	3 - WCSA	ns
WE41A (muxed A/D)	CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADV _N + WADVA + ADH + 1 - WCSA)	—	3 + (WADV _N + WADVA + ADH + 1 - WCSA)	ns
WE42	Output Data Invalid to CSx_B Invalid	WE17 - WE7 - CSN	—	3 - CSN	ns
MAXCO	Output max. delay from internal driving ADDR/control FFs to chip outputs.	10	—	—	ns
MAXCSO	Output max. delay from CSx internal driving FFs to CSx out.	10	—	—	
MAXDI	DATA MAXIMUM delay from chip input data to its internal FF	5	—	—	
WE43	Input Data Valid to CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	CSx_B Valid to BEy_B Valid (Write access)	WE12 - WE6 + (WBEA - WCSA)	—	3 + (WBEA - WCSA)	ns
WE46	BEy_B Invalid to CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - WCSN)	—	-3 + (WBEN - WCSN)	ns
MAXDTI	DTACK MAXIMUM delay from chip dtack input to its internal FF + 2 cycles for synchronization	10	—	—	—
WE47	Dtack Active to CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	CSx_B Invalid to Dtack invalid	0	0	—	ns

¹ For more information on configuration parameters mentioned in this table, see the i.MX 6Solo/6DualLite reference manual.

² In this table, CSA means WCSA when write operation or RCSA when read operation.

³ In this table, CSN means WCSN when write operation or RCSN when read operation.

⁴ t is axi_clk cycle time.

⁵ In this table, ADV_N means WADV_N when write operation or RADV_N when read operation.

⁶ In this table, ADVA means WADVA when write operation or RADVA when read operation.

4.9.4 DDR SDRAM Specific Parameters (DDR3/DDR3L and LPDDR2)

4.9.4.1 DDR3/DDR3L Parameters

Figure 22 shows the DDR3/DDR3L basic timing diagram. The timing parameters for this diagram appear in Table 40.

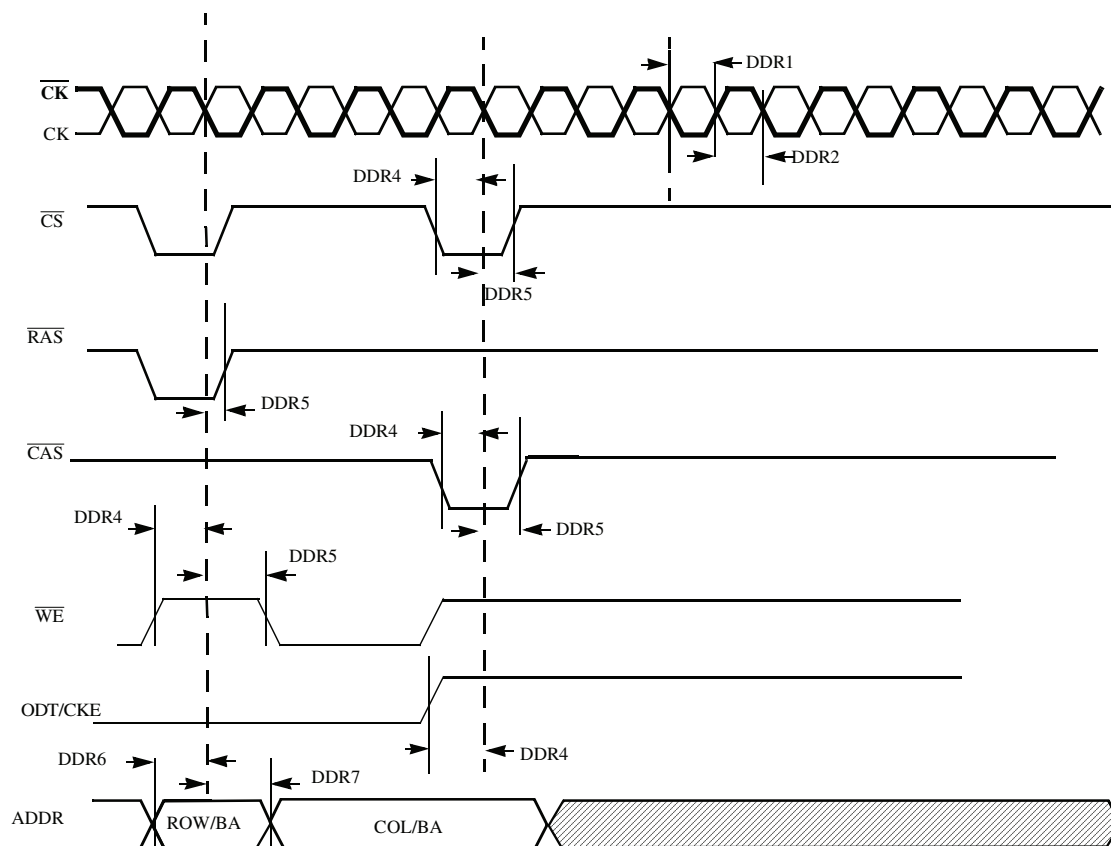


Figure 22. DDR3/DDR3L Command and Address Timing Diagram

Table 40. DDR3/DDR3L Timing Parameter Table

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR1	CK clock high-level width	tCH	0.47	0.53	tck
DDR2	CK clock low-level width	tCL	0.47	0.53	tck
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	tIS	500	—	ps
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	tIH	400	—	ps

Table 40. DDR3/DDR3L Timing Parameter Table (continued)

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR6	Address output setup time	tIS	500	—	ps
DDR7	Address output hold time	tIH	400	—	ps

¹ All measurements are in reference to Vref level.

² Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 23 shows the DDR3/DDR3L write timing diagram. The timing parameters for this diagram appear in Table 41.

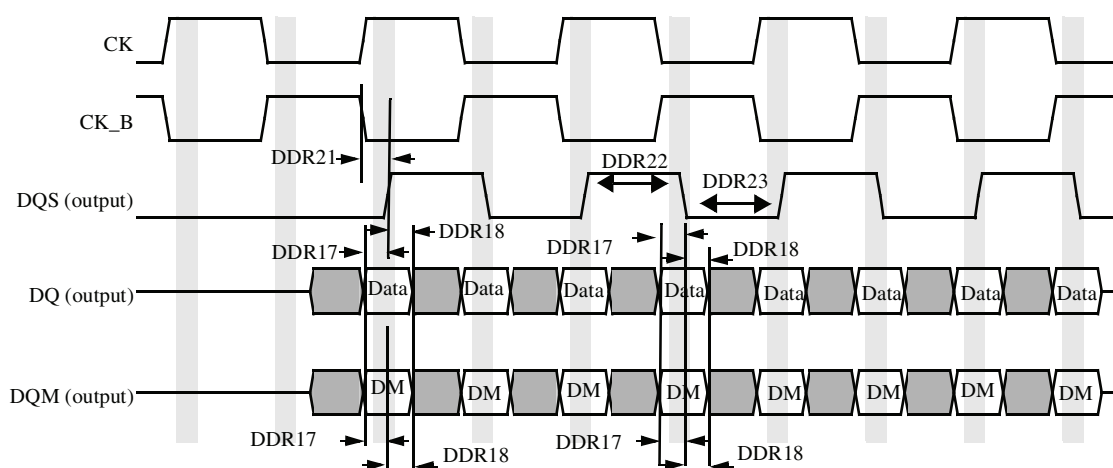


Figure 23. DDR3/DDR3L Write Cycle

Table 41. DDR3/DDR3L Write Cycle

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (differential strobe)	tDS	240	—	ps
DDR18	DQ and DQM hold time to DQS (differential strobe)	tDH	240	—	ps
DDR21	DQS latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
DDR22	DQS high level width	tDQSH	0.45	0.55	tCK
DDR23	DQS low level width	tDQSL	0.45	0.55	tCK

¹ To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

² All measurements are in reference to Vref level.

³ Measurements were taken using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 24 shows the DDR3/DDR3L read timing diagram. The timing parameters for this diagram appear in Table 42.

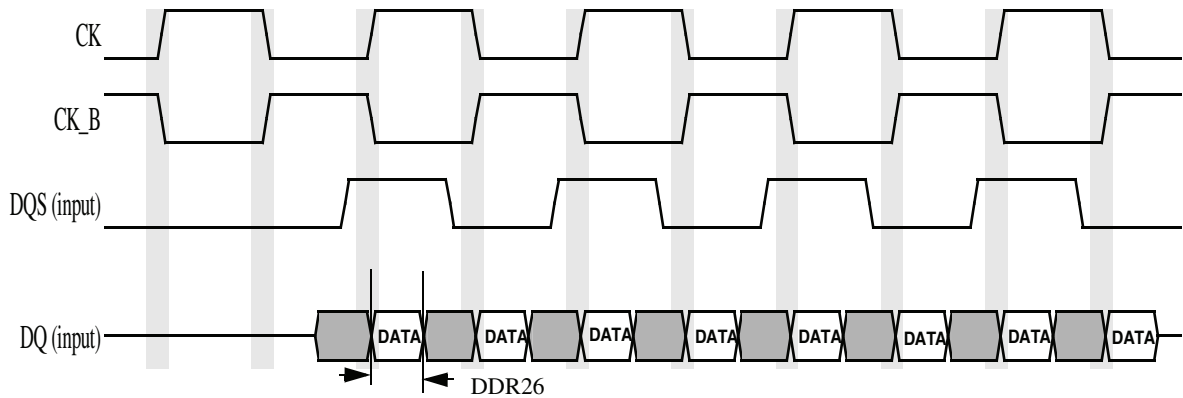


Figure 24. DDR3/DDR3L Read Cycle

Table 42. DDR3/DDR3L Read Cycle

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
DDR26	Minimum required DQ valid window width	—	450	—	ps

¹ To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

² All measurements are in reference to Vref level.

³ Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

4.9.4.2 LPDDR2 Parameters

Figure 25 shows the LPDDR2 basic timing diagram. The timing parameters for this diagram appear in Table 43.

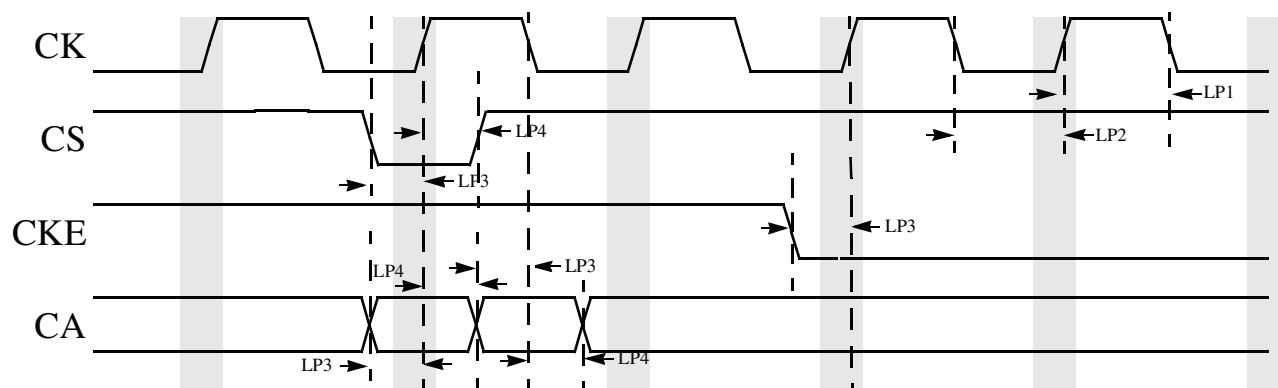


Figure 25. LPDDR2 Command and Address Timing Diagram

Table 43. LPDDR2 Timing Parameter

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
LP1	SDRAM clock high-level width	t _{CH}	0.45	0.55	t _{CK}
LP2	SDRAM clock low-level width	t _{CL}	0.45	0.55	t _{CK}
LP3	CS, CKE setup time	t _{IS}	270	—	ps
LP4	CS, CKE hold time	t _{IH}	270	—	ps
LP3	CA setup time	t _{IS}	230	—	ps
LP4	CA hold time	t _{IH}	230	—	ps

¹ All measurements are in reference to V_{ref} level.

² Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 26 shows the LPDDR2 write timing diagram. The timing parameters for this diagram appear in Table 44.

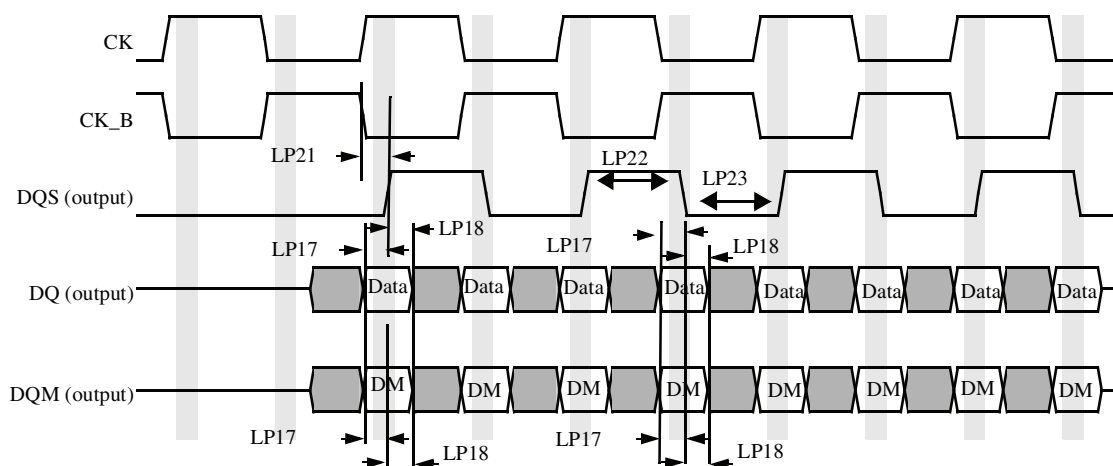


Figure 26. LPDDR2 Write Cycle

Table 44. LPDDR2 Write Cycle

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
LP17	DQ and DQM setup time to DQS (differential strobe)	t _{DS}	235	—	ps
LP18	DQ and DQM hold time to DQS (differential strobe)	t _{DH}	235	—	ps
LP21	DQS latching rising transitions to associated clock edges	t _{DQSS}	-0.25	+0.25	tCK
LP22	DQS high level width	t _{DQSH}	0.4	-	tCK
LP23	DQS low level width	t _{DQSL}	0.4	-	tCK

¹ To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

² All measurements are in reference to V_{ref} level.

³ Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 27 shows the LPDDR2 read timing diagram. The timing parameters for this diagram appear in Table 45.

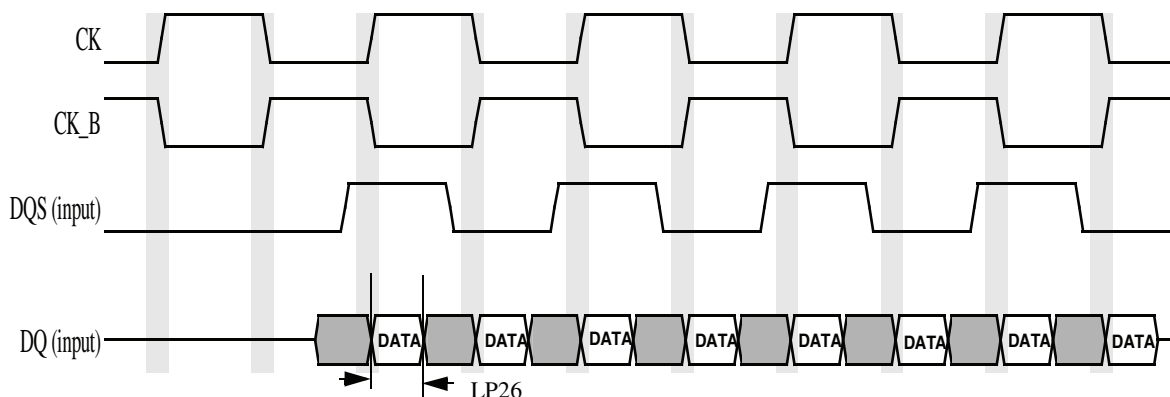


Figure 27. LPDDR2 Read Cycle

Table 45. LPDDR2 Read Cycle

ID	Parameter	Symbol	CK = 532 MHz		Unit
			Min	Max	
LP26	Minimum required DQ valid window width for LPDDR2	—	250	—	ps

¹ To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

² All measurements are in reference to Vref level.

³ Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

4.10 General-Purpose Media Interface (GPMI) Timing

The i.MX 6Dual/6Quad GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select. It supports Asynchronous timing mode, Source Synchronous timing mode, and Samsung Toggle timing mode separately described in the following subsections.

4.10.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The Maximum I/O speed of GPMI in Asynchronous mode is about 50 MB/s. Figure 28 through Figure 31 depict the relative timing between GPMI signals at the module level for different operations under Asynchronous mode. Table 46 describes the timing parameters (NF1–NF17) that are shown in the figures.

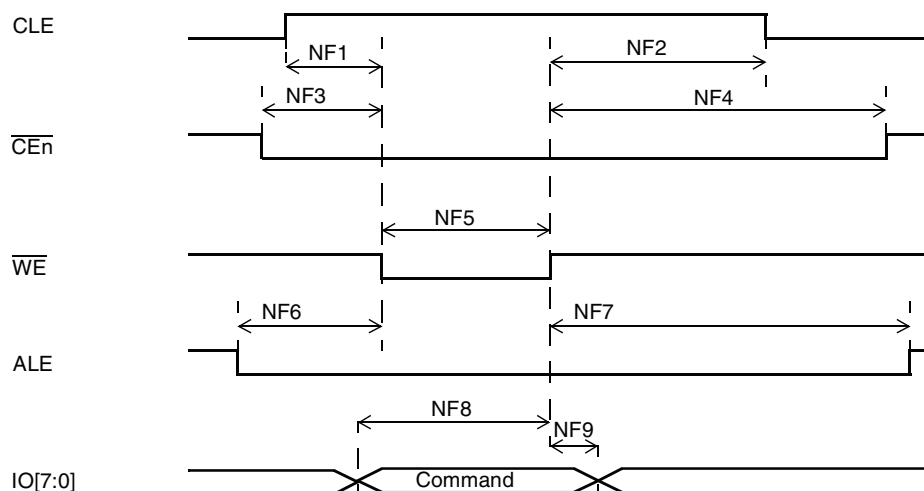


Figure 28. Command Latch Cycle Timing Diagram

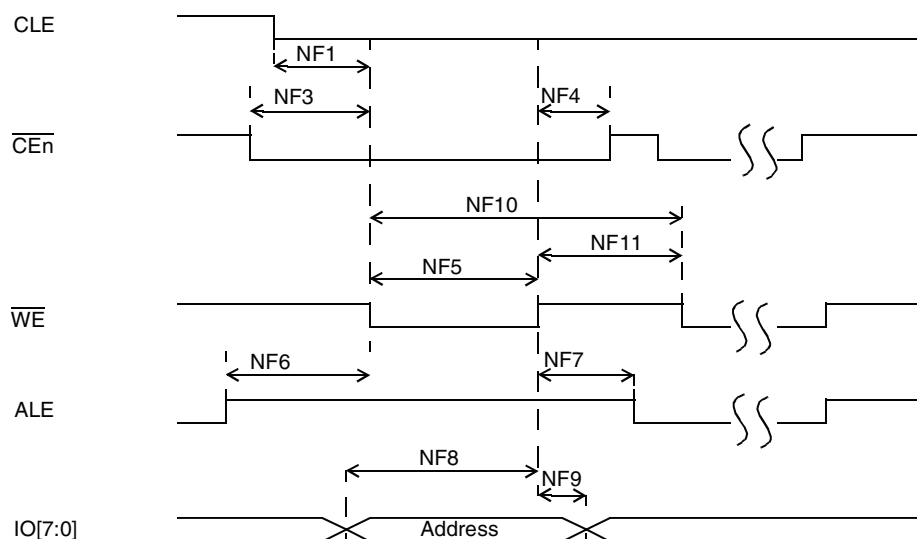


Figure 29. Address Latch Cycle Timing Diagram

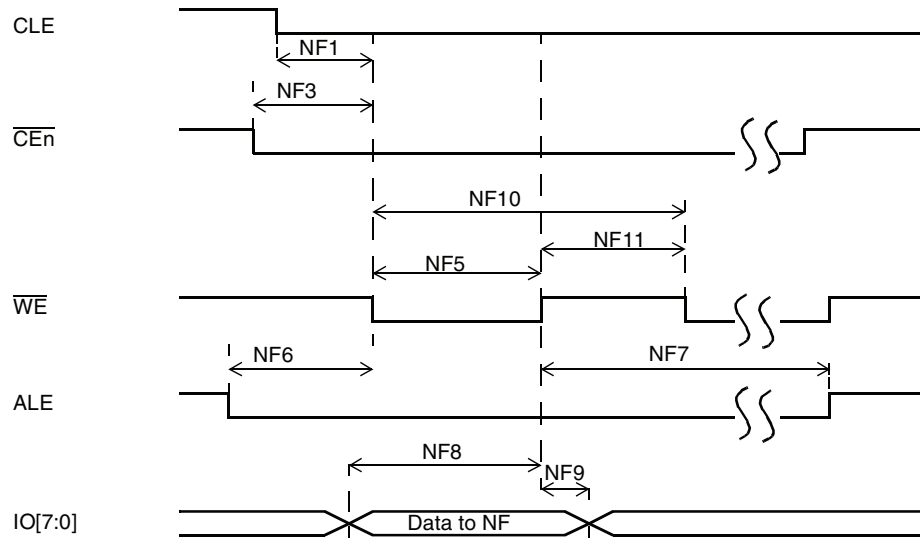


Figure 30. Write Data Latch Cycle Timing Diagram

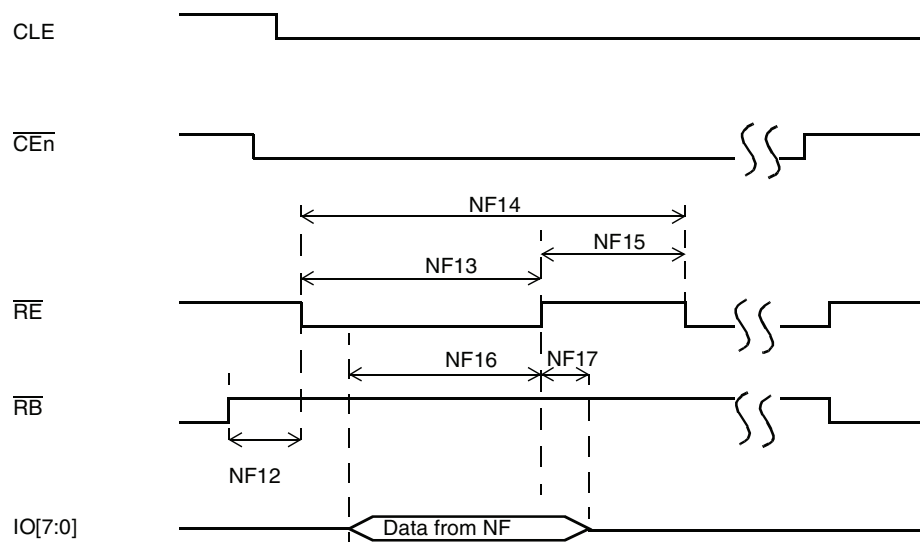


Figure 31. Read Data Latch Cycle Timing Diagram (Non-EDO Mode)

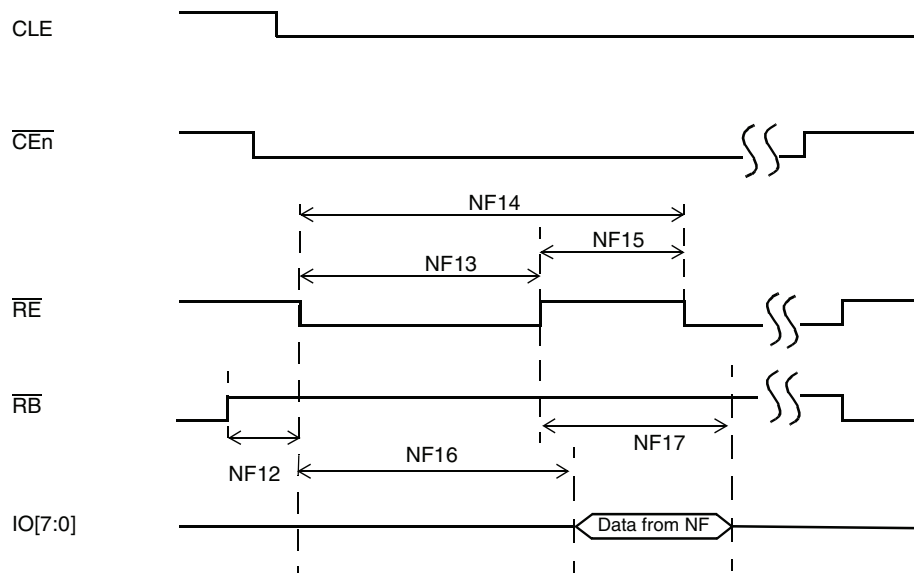


Figure 32. Read Data Latch Cycle Timing Diagram (EDO Mode)

Table 46. Asynchronous Mode Timing Parameters¹

ID	Parameter	Symbol	Timing $T^2 = \text{GPMI Clock Cycle}$		Example Timing for GPMI Clock $\approx 100 \text{ MHz}$ $T = 10 \text{ ns}$		Unit
			Min.	Max.	Min.	Max.	
NF1	CLE setup time	tCLS	$(AS^3+1)*T$	—	10	—	ns
NF2	CLE hold time	tCLH	$(DH+1)*T$	—	20	—	ns
NF3	$\overline{\text{CEn}}$ setup time	tCS	$(AS+1)*T$	—	10	—	ns
NF4	$\overline{\text{CE}}$ hold time	tCH	$(DH+1)*T$	—	20	—	ns
NF5	$\overline{\text{WE}}$ pulse width	tWP	$DS*T$		10		ns
NF6	ALE setup time	tALS	$(AS+1)*T$	—	10	—	ns
NF7	ALE hold time	tALH	$(DH+1)*T$	—	20	—	ns
NF8	Data setup time	tDS	$DS*T$	—	10	—	ns
NF9	Data hold time	tDH	$DH*T$	—	10	—	ns
NF10	Write cycle time	tWC	$(DS+DH)*T$		20		ns
NF11	$\overline{\text{WE}}$ hold time	tWH	$DH*T$		10		ns
NF12	Ready to $\overline{\text{RE}}$ low	tRR	$(AS+1)*T$	—	10	—	ns
NF13	$\overline{\text{RE}}$ pulse width	tRP	$DS*T$	—	10	—	ns
NF14	READ cycle time	tRC	$(DS+DH)*T$	—	20	—	ns
NF15	$\overline{\text{RE}}$ high hold time	tREH	$DH*T$		10	—	ns
NF16	Data setup on read	tDSR	N/A		10	—	ns
NF17	Data hold on read	tDHR	N/A		10	—	ns

- ¹ GPMI's Async Mode output timing could be controlled by module's internal register, say GPMI_TIMING0_ADDRESS_SETUP, GPMI_TIMING0_DATA_SETUP, GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers' settings. In the above table, we use AS/DS/DH to represent each of these settings.
- ² T represents the GPMI clock period.
- ³ AS minimum value could be 0, while DS/DH minimum value is 1.

In EDO mode (Figure 32), NF16/NF17 are different from the definition in non-EDO mode (Figure 31). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical value for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample IO[7:0] at rising edge of delayed \overline{RE} provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the i.MX 6Dual/6Quad reference manual). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.10.2 Source Synchronous Mode AC Timing (ONFI 2.x Compatible)

Below diagrams show the write and read timing of Source Synchronous mode.

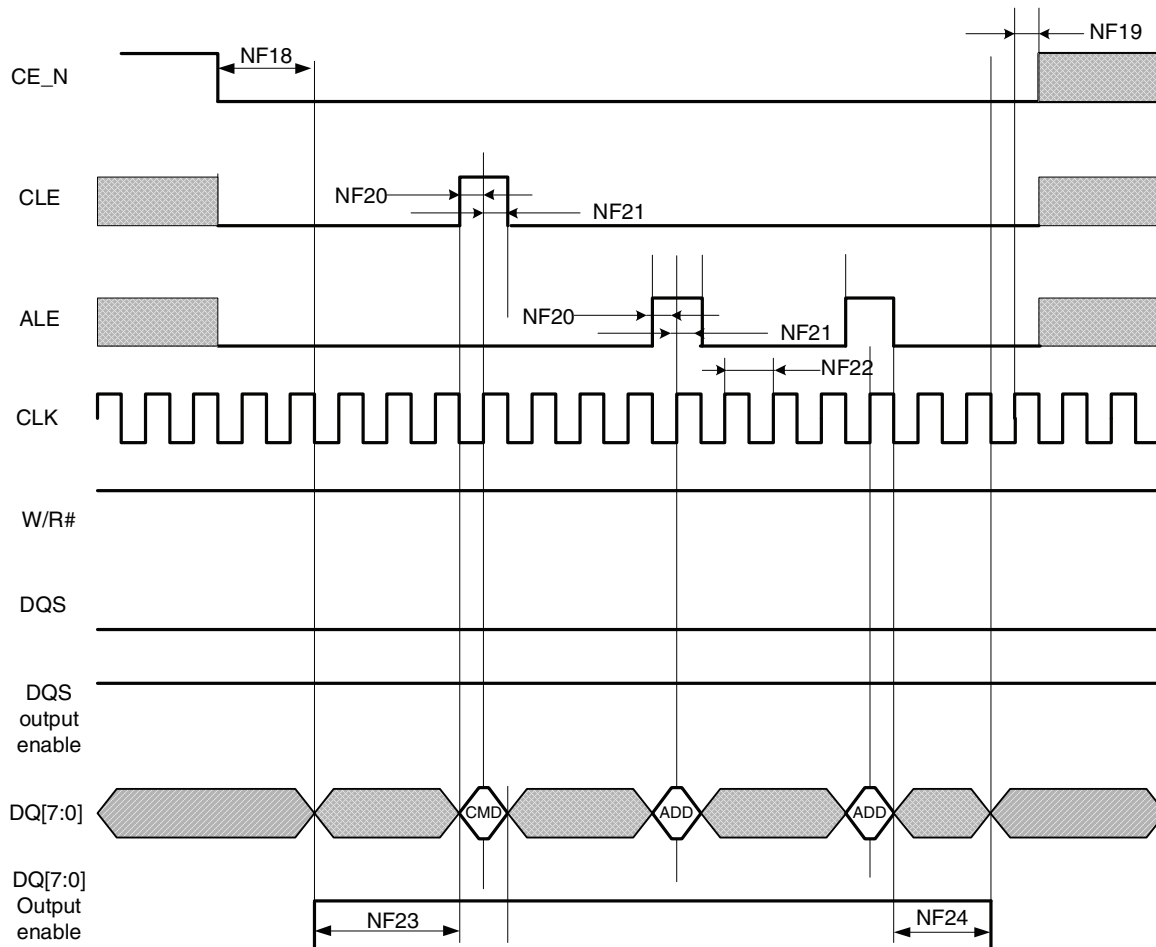


Figure 33. Source Synchronous Mode Command and Address Timing Diagram

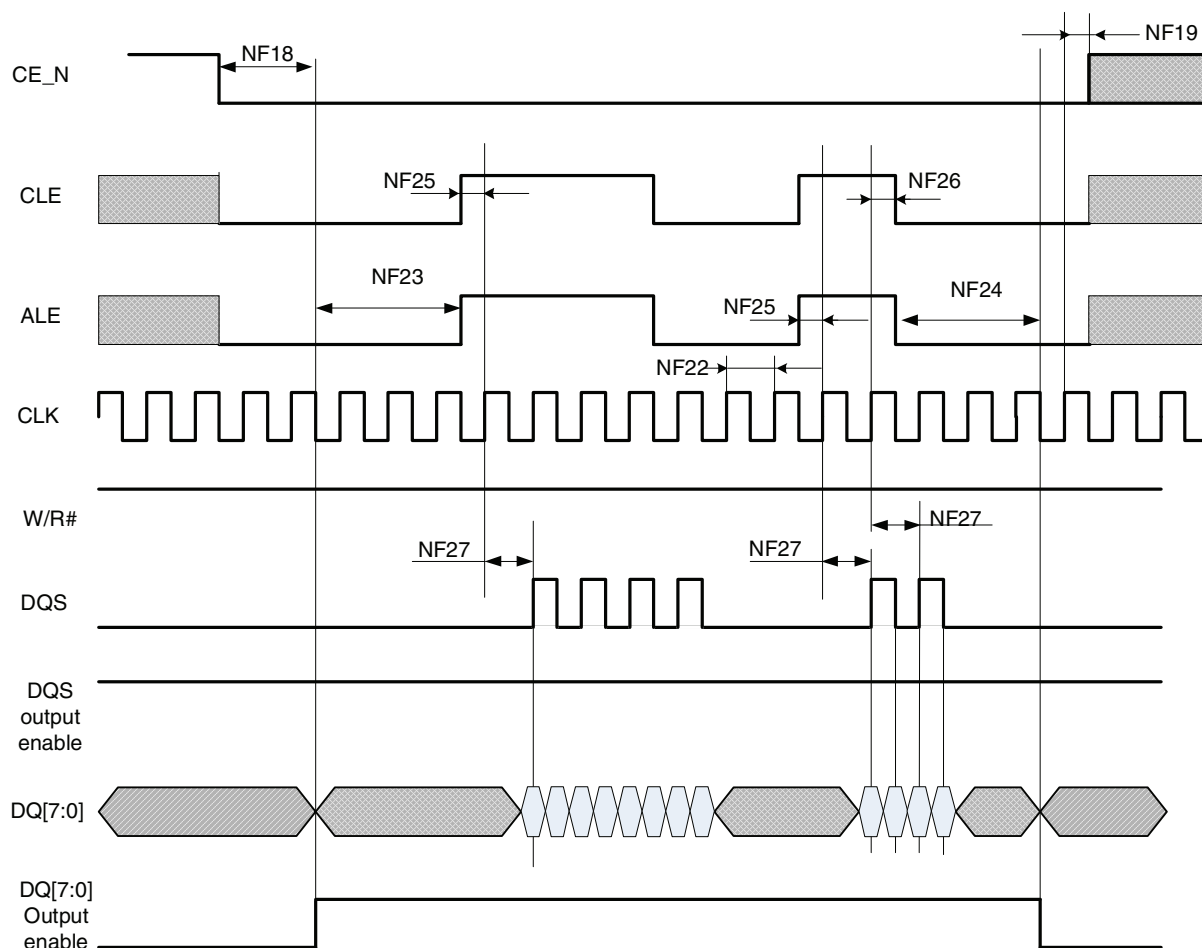


Figure 34. Source Synchronous Mode Data Write Timing Diagram

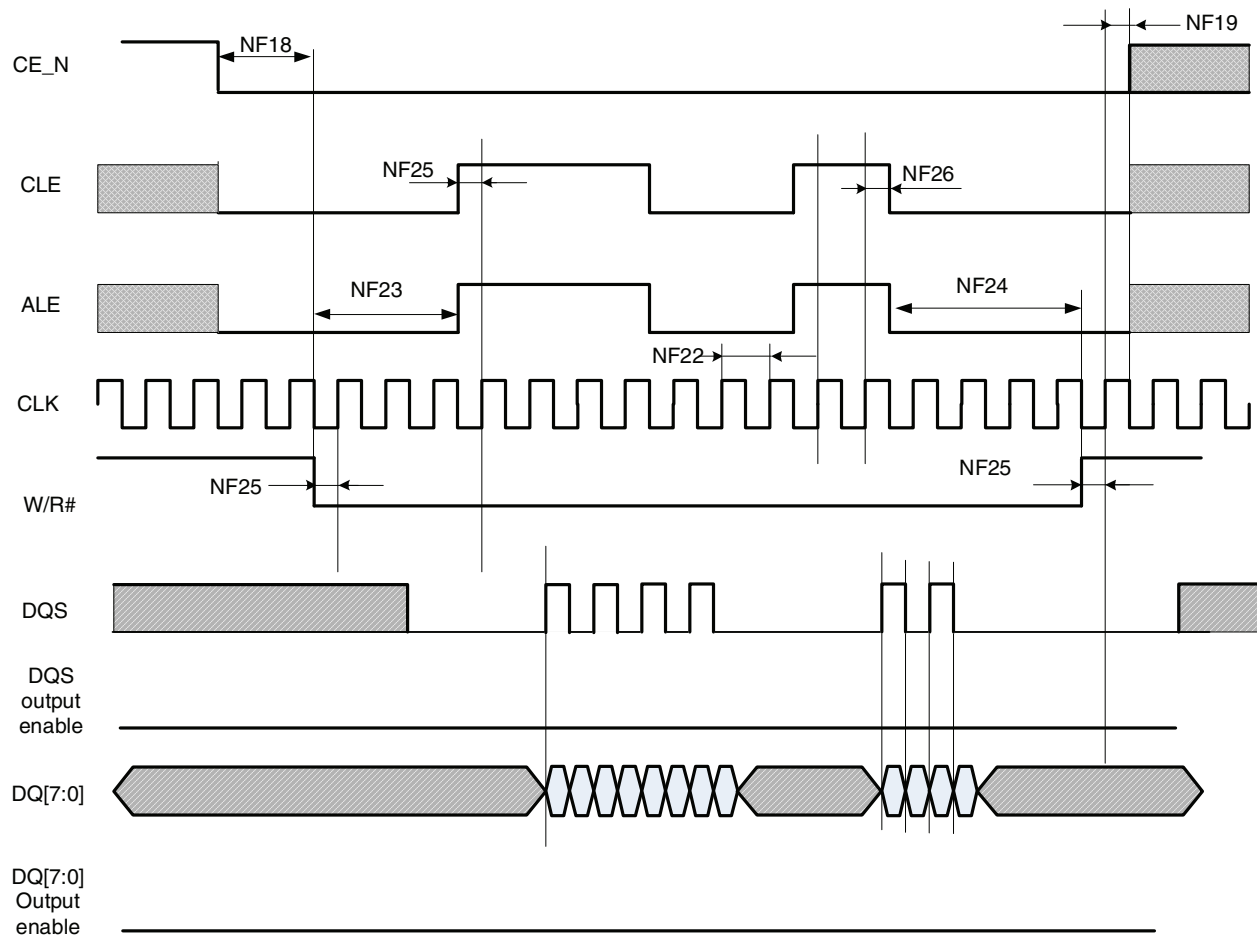


Figure 35. Source Synchronous Mode Data Read Timing Diagram

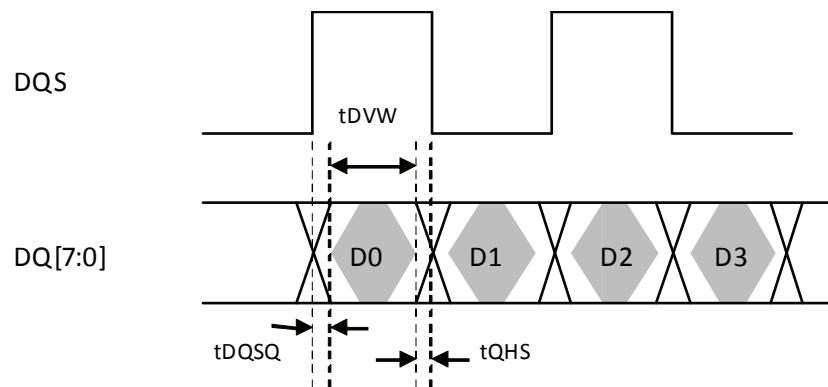


Figure 36. DQS/DQ Read Valid Window

Table 47. Source Synchronous Mode Timing Parameters¹

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	tCE	CE_DELAY*tCK	—	ns
NF19	CE# hold time	tCH	0.5 *tCK	—	ns
NF20	Command/address DQ setup time	tCAS	0.5*tCK	—	ns
NF21	Command/address DQ hold time	tCAH	0.5*tCK	—	ns
NF22	clock period	tCK	5	--	ns
NF23	preamble delay	tPRE	PRE_DELAY*tCK	—	ns
NF24	postamble delay	tPOST	POST_DELAY*tCK	—	ns
NF25	CLE and ALE setup time	tCALS	0.5*tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5*tCK	—	ns
NF27	Data input to first DQS latching transition	tDQSS	tCK	—	ns

¹ GPMI's Source sync mode output timing could be controlled by module's internal register, say GPMI_TIMING2_CE_DELAY, GPMI_TIMING2_PREAMBLE_DELAY, GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers' settings. In the above table, we use CE_DELAY/PRE_DELAY/POST_DELAY to represent each of these settings.

Figure 36 shows the timing diagram of DQS/DQ read valid window. For Source Synchronous mode, the typical value of tDQSQ is 0.85 ns (max) and 1 ns (max) for tQHS at 200MB/s. GPMI will sample DQ[7:0] at both rising and falling edge of an delayed DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6Dual/6Quad reference manual). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.10.3 Samsung Toggle Mode AC Timing

4.10.3.1 Command and Address Timing

Samsung Toggle mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See [Section 4.10.1, “Asynchronous Mode AC Timing \(ONFI 1.0 Compatible\)”](#) for details.

4.10.3.2 Read and Write Timing

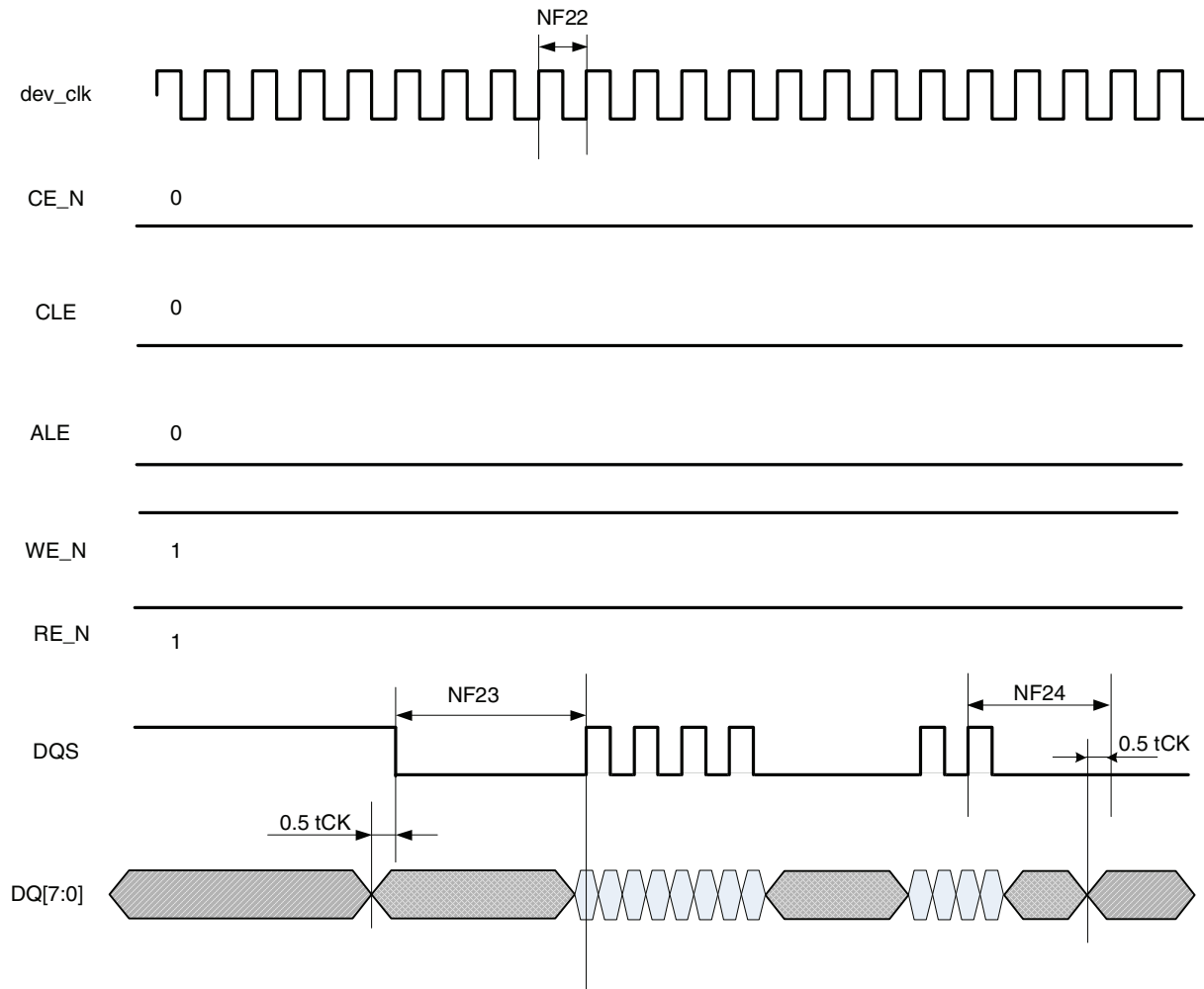


Figure 37. Samsung Toggle Mode Data Write Timing

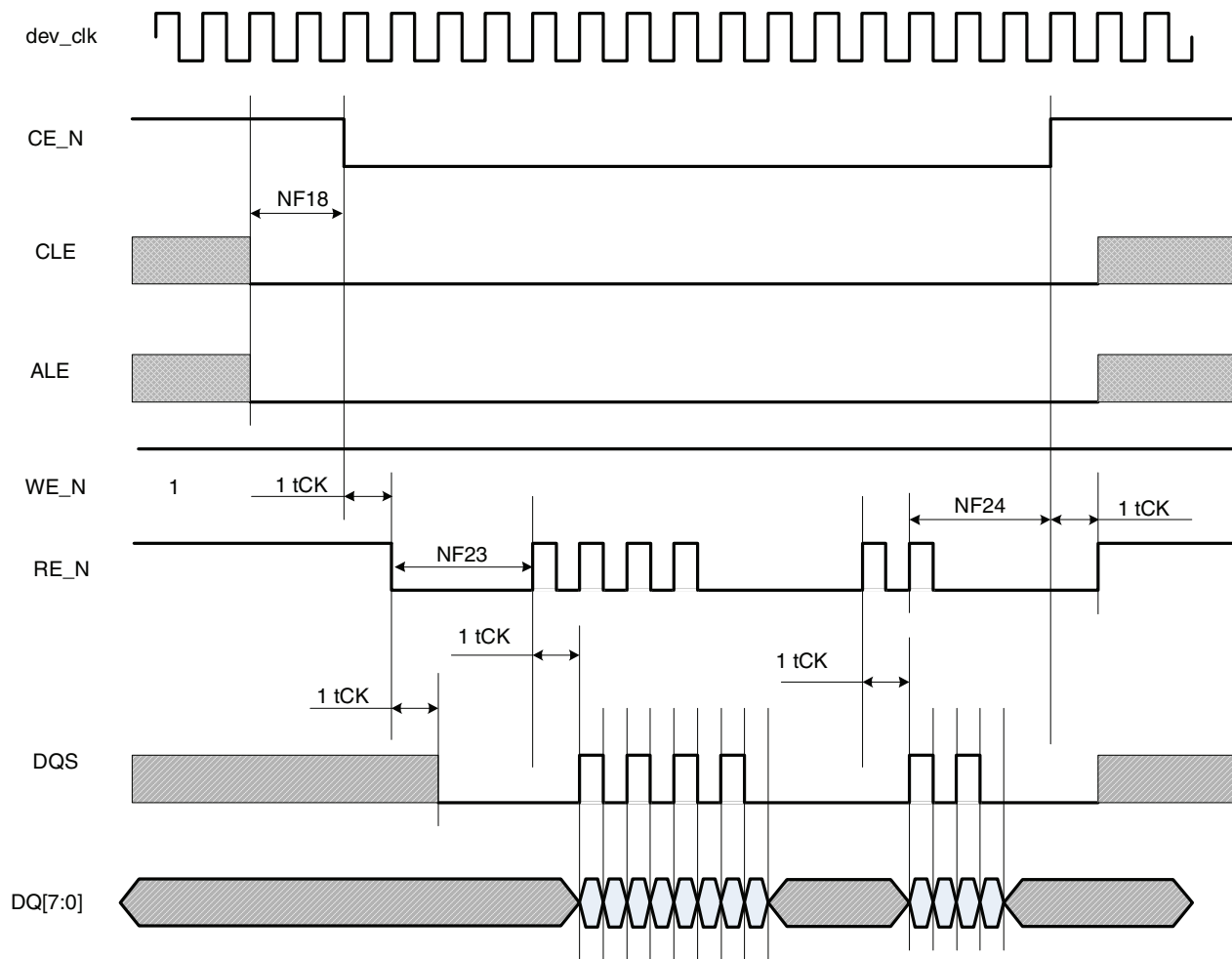


Figure 38. Samsung Toggle Mode Data Read Timing

Table 48. Samsung Toggle Mode Timing Parameters

ID	Parameter	Symbol	Timing T = GPML Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	tCE	CE_DELAY*tCK	—	ns
NF19	CE# hold time	tCH	0.5 *tCK	—	ns
NF20	Command/address DQ setup time	tCAS	0.5*tCK	—	ns
NF21	Command/address DQ hold time	tCAH	0.5*tCK	—	ns
NF22	clock period	tCK	7.5	—	ns
NF23	preamble delay	tPRE	(PRE_DELAY+1)*tCK	—	ns
NF24	postamble delay	tPOST	POST_DELAY*tCK	—	ns
NF25	CLE and ALE setup time	tCALS	0.5*tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5*tCK	—	ns

Figure 36 shows the timing diagram of DQS/DQ read valid window. For DDR Toggle mode, the typical value of t_{DQSQ} is 1.4 ns (max) and 1.4 ns (max) for t_{QHS} at 133 MB/s. GPMI will sample $DQ[7:0]$ at both rising and falling edge of an delayed DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by GPMI register

`GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET` (see the GPMI chapter of the i.MX 6Dual/6Quad reference manual). Generally, the typical delay value is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

4.11.1 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.11.2 ECSPi Timing Parameters

This section describes the timing parameters of the ECSPi block. The ECSPi has separate timing parameters for master and slave modes.

4.11.2.1 ECSPi Master Mode Timing

Figure 39 depicts the timing of ECSPi in master mode and Table 49 lists the ECSPi master mode timing characteristics.

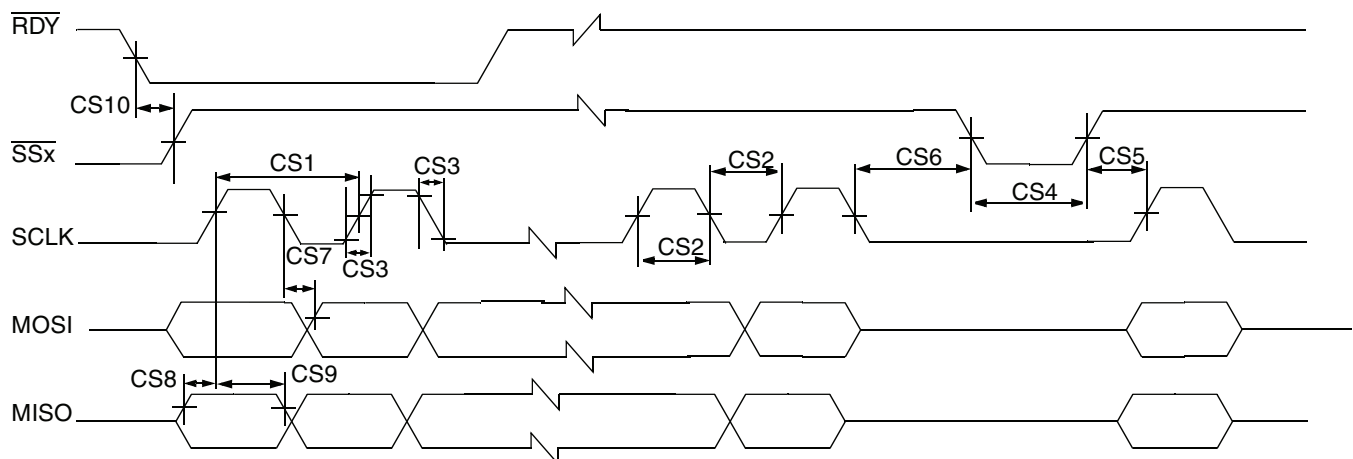


Figure 39. ECSPi Master Mode Timing Diagram

Table 49. ECSPi Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time—Read • Slow group ¹ • Fast group ² SCLK Cycle Time—Write	t_{clk}	55 40 15	—	ns
CS2	SCLK High or Low Time—Read • Slow group ¹ • Fast group ² SCLK High or Low Time—Write	t_{sw}	26 20 7	—	ns
CS3	SCLK Rise or Fall ³	$t_{RISE/FALL}$	—	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	Half SCLK period - 4	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	Half SCLK period	—	ns
CS7	MOSI Propagation Delay ($C_{LOAD} = 20$ pF)	t_{PDmosi}	-1	1	ns
CS8	MISO Setup Time • Slow group ¹ • Fast group ²	t_{Smiso}	21.5 16	—	ns
CS9	MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to SSx Time ⁴	t_{SDRY}	5	—	ns

¹ ECSPi slow include:

ECSPi1/DISP0_DAT22, ECSPi1/KEY_COL1, ECSPi1/CSI0_DAT6, ECSPi2/EIM_OE, ECSPi2/DISP0_DAT17, ECSPi2/CSI0_DAT10, ECSPi3/DISP0_DAT2

² ECSPi fast include:

ECSPi1/EIM_D17, ECSPi4/EIM_D22, ECSPi5/SD2_DAT0, ECSPi5/SD1_DAT0

³ See specific I/O AC parameters [Section 4.7, “I/O AC Parameters.”](#)

⁴ SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.11.2.2 ECSPi Slave Mode Timing

Figure 40 depicts the timing of ECSPi in slave mode and Table 50 lists the ECSPi slave mode timing characteristics.

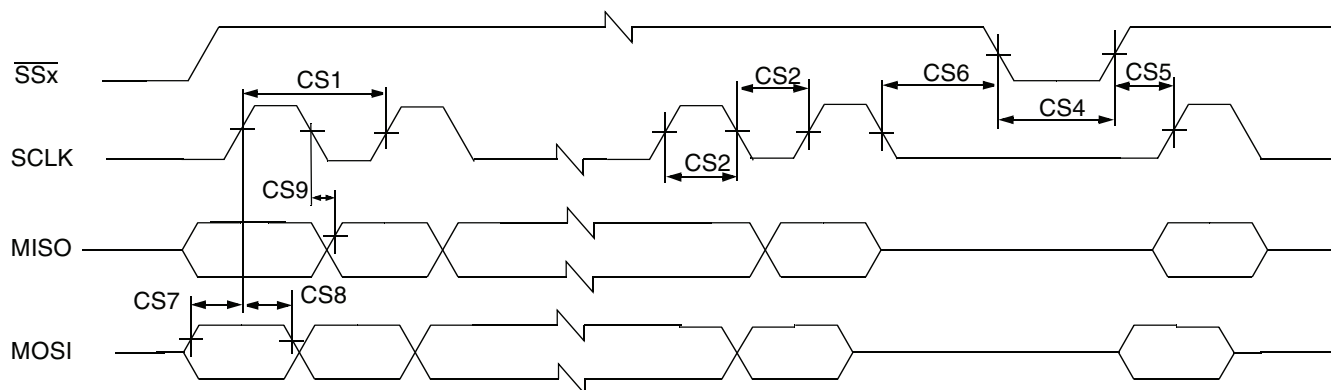


Figure 40. ECSPi Slave Mode Timing Diagram

Table 50. ECSPi Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time—Read • Slow group ¹ • Fast group ² SCLK Cycle Time—Write	t_{clk}	55 40 15	—	ns
CS2	SCLK High or Low Time—Read • Slow group ¹ • Fast group ² SCLK High or Low Time—Write	t_{sw}	26 20 7	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	MISO Propagation Delay ($C_{LOAD} = 20$ pF) • Slow group ¹ • Fast group ²	t_{PDmiso}	4	25 17	ns

¹ ECSPi slow include:

ECSPi1/DISP0_DAT22, ECSPi1/KEY_COL1, ECSPi1/CSI0_DAT6, ECSPi2/EIM_OE, ECSPi2/DISP0_DAT17, ECSPi2/CSI0_DAT10, ECSPi3/DISP0_DAT2

² ECSPi fast include:

ECSPi1/EIM_D17, ECSPi4/EIM_D22, ECSPi5/SD2_DAT0, ECSPi5/SD1_DAT0

4.11.3 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 51 shows the interface timing values. The number field in the table refers to timing signals found in Figure 41 and Figure 42.

Table 51. Enhanced Serial Audio Interface (ESAI) Timing

ID	Parameter ^{1,2}	Symbol	Expression ²	Min	Max	Condition ³	Unit
62	Clock cycle ⁴	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
64	Clock low period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
65	SCKR rising edge to FSR out (bl) high	— —	— —	— —	19.0 7.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	— —	— —	— —	19.0 7.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high ⁵	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low ⁵	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	— —	— —	— —	19.0 6.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge ⁵	— —	— —	2.0 19.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	— —	— —	2.0 19.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	SCKT rising edge to FST out (bl) high	— —	— —	— —	19.0 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
80	SCKT rising edge to FST out (wr) high ⁵	— —	— —	— —	20.0 10.0	x ck i ck	ns

Table 51. Enhanced Serial Audio Interface (ESAI) Timing (continued)

ID	Parameter ^{1,2}	Symbol	Expression ²	Min	Max	Condition ³	Unit
81	SCKT rising edge to FST out (wr) low ⁵	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	SCKT rising edge to data out valid	— —	— —	— —	19.0 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance ^{6,7}	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge ⁵	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
95	HCKR/HCKT clock cycle	—	$2 \times T_C$	15	—	—	ns
96	HCKT input rising edge to SCKT output	—	—	—	18.0	—	ns
97	HCKR input rising edge to SCKR output	—	—	—	18.0	—	ns

- ¹ i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that SCKT and SCKR are the same clock)

- ² bl = bit length
wl = word length
wr = word length relative

- ³ SCKT(SCKT pin) = transmit clock
SCKR(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

- ⁴ For the internal clock, the external clock cycle is defined by lcy and the ESAI control register.

- ⁵ The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

- ⁶ Periodically sampled and not 100% tested.

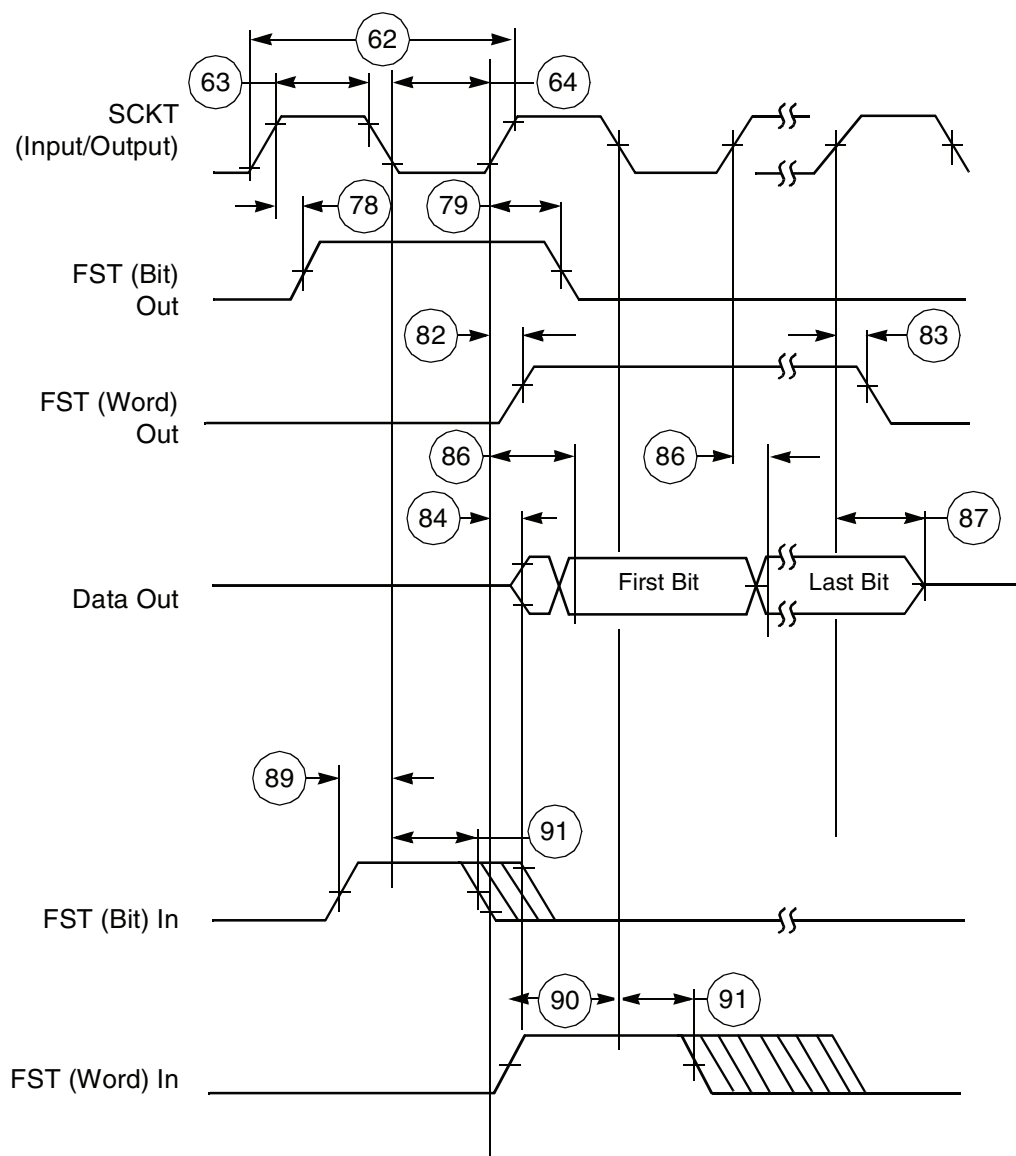


Figure 41. ESAT Transmitter Timing

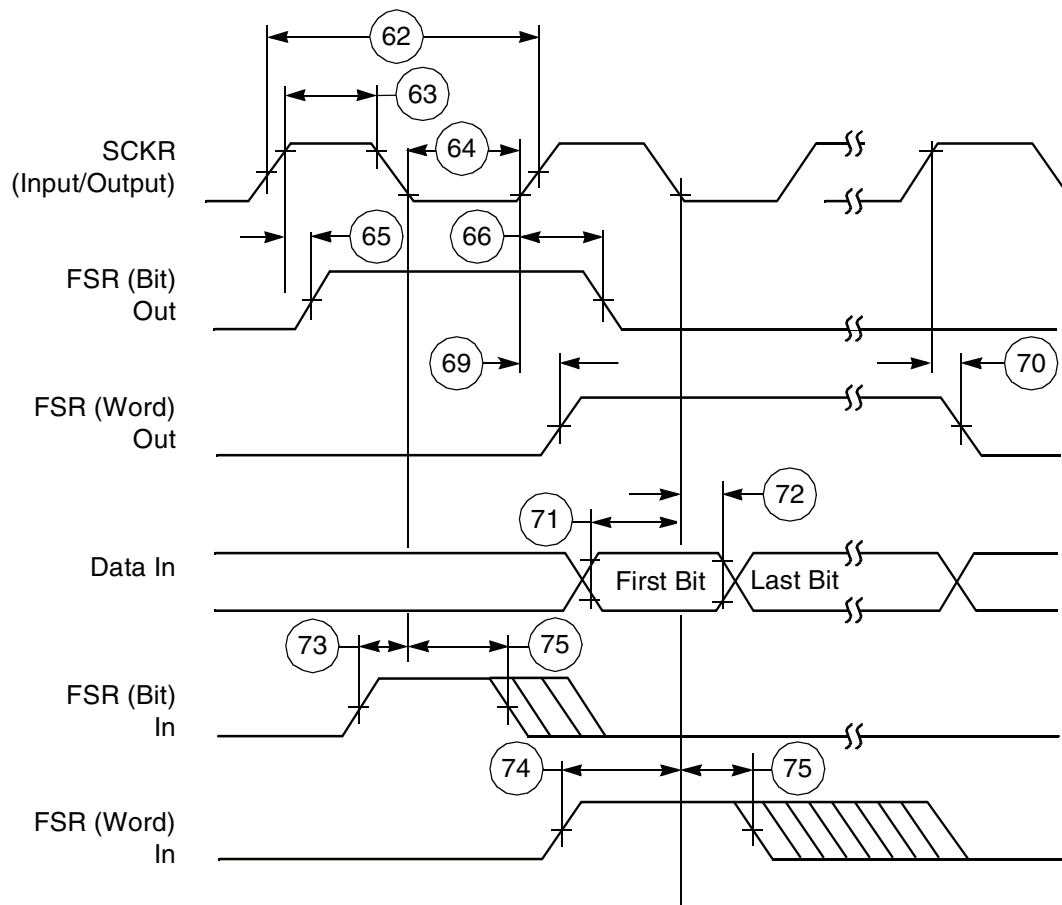


Figure 42. ESAI Receiver Timing

4.11.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4 (Dual Data Rate) timing.

4.11.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 43 depicts the timing of SD/eMMC4.3, and Table 52 lists the SD/eMMC4.3 timing characteristics.

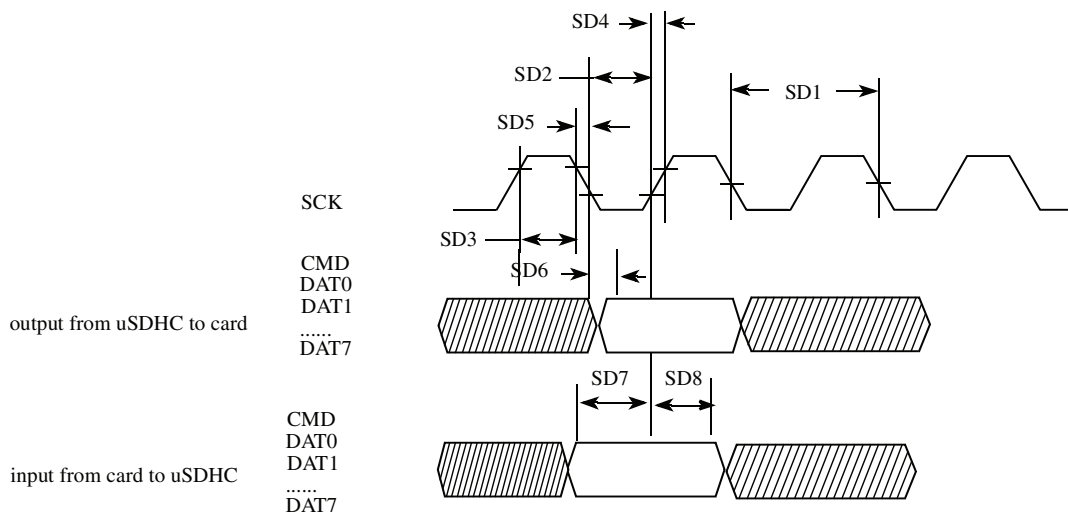


Figure 43. SD/eMMC4.3 Timing

Table 52. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}^1	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}^2	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}^3	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	eSDHC Output Delay	t_{OD}	−6.6	3.6	ns

Table 52. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
eSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time ⁴	t_{IH}	5.6	—	ns

¹ In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

² In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

³ In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

⁴To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.11.4.2 eMMC4.4 (Dual Data Rate) eSDHCv3 AC Timing

Figure 44 depicts the timing of eMMC4.4. Table 53 lists the eMMC4.4 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

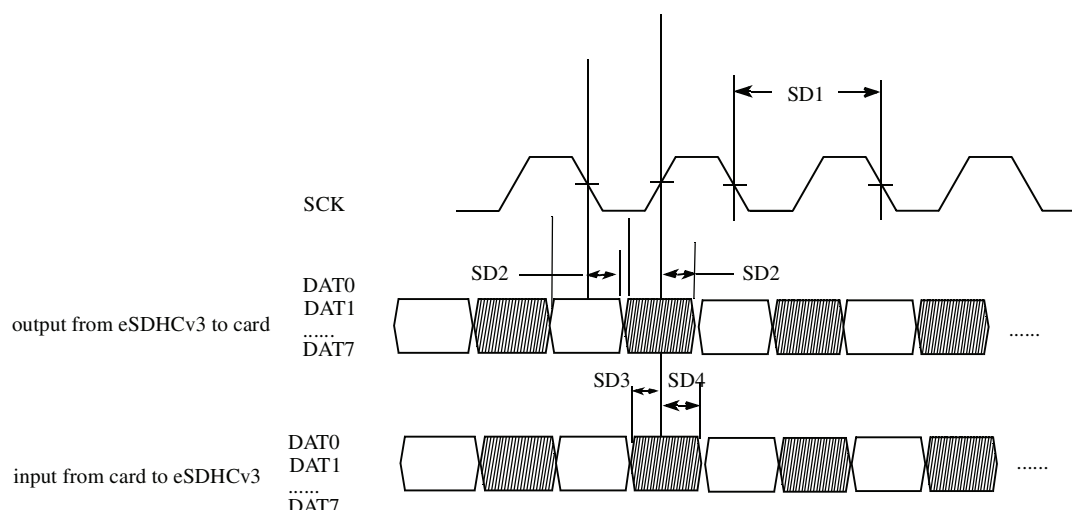


Figure 44. eMMC4.4 Timing

Table 53. eMMC4.4 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (EMMC4.4 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs CMD, DAT (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.5	7.1	ns

Table 53. eMMC4.4 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input / Card Outputs CMD, DAT (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	2.6	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

4.11.4.3 SDR50/SDR104 AC Timing

Figure 45 depicts the timing of SDR50/SDR104, and Table 52 lists the SDR50/SDR104 timing characteristics.

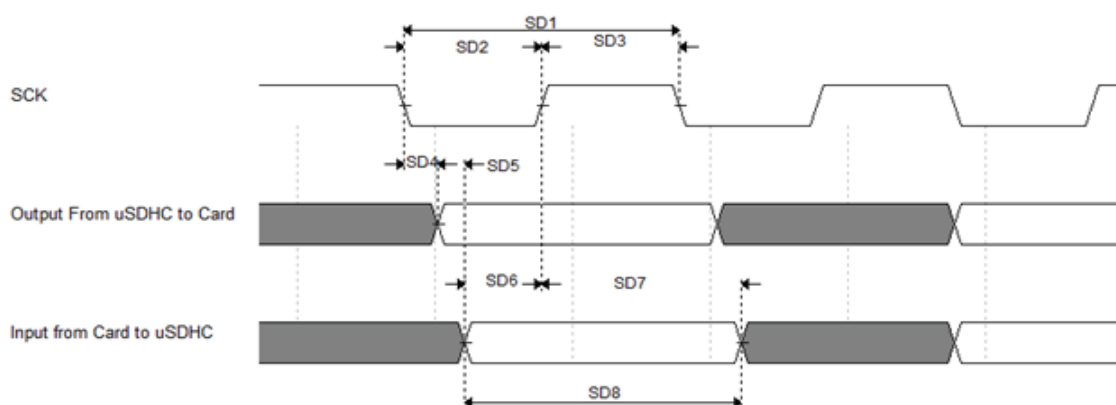


Figure 45. SDR50/SDR104 Timing

Table 54. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	$0.3 \cdot t_{CLK}$	$0.7 \cdot t_{CLK}$	ns
SD2	Clock High Time	t_{CH}	$0.3 \cdot t_{CLK}$	$0.7 \cdot t_{CLK}$	ns
uSDHC Output/Card Inputs CMD, DAT in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	-3	1	ns
uSDHC Output/Card Inputs CMD, DAT in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	-1.6	1	ns
uSDHC Input/Card Outputs CMD, DAT in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

Table 54. SDR50/SDR104 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs CMD, DAT in SDR104 (Reference to CLK) ¹					
SD8	Card Output Data Window	t_{ODW}	$0.5 \cdot t_{CLK}$	—	ns

¹Data window in SDR100 mode is variable.

4.11.4.4 Bus Operation Condition for 3.3 V and 1.8 V Signaling

Signaling level of SD/eMMC4.3 and eMMC4.4 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1, NVCC_SD2, and NVCC_SD3 supplies are identical to those shown in [Table 22, "GPIO I/O DC Parameters,"](#) on page 38.

4.11.5 Ethernet Controller (ENET) AC Electrical Specifications

4.11.5.1 ENET MII Mode Timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.11.5.1.1 MII Receive Signal Timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

[Figure 46](#) shows MII receive signal timings. [Table 55](#) describes the timing parameters (M1–M4) shown in the figure.

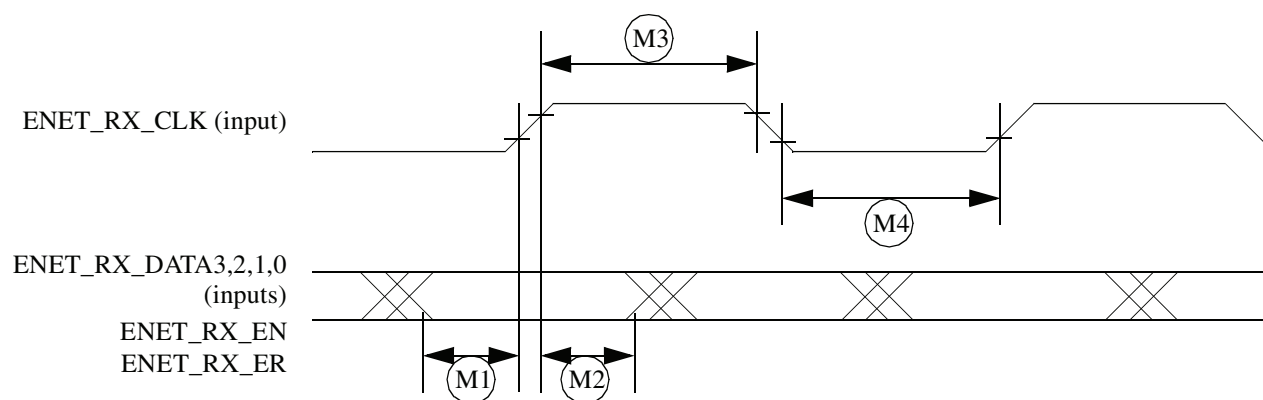


Figure 46. MII Receive Signal Timing Diagram

Table 55. MII Receive Signal Timing

ID	Characteristic ¹	Min.	Max.	Unit
M1	ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup	5	—	ns
M2	ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold	5	—	ns
M3	ENET_RX_CLK pulse width high	35%	65%	ENET_RX_CLK period
M4	ENET_RX_CLK pulse width low	35%	65%	ENET_RX_CLK period

¹ ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

4.11.5.1.2 MII Transmit Signal Timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

Figure 47 shows MII transmit signal timings. Table 56 describes the timing parameters (M5–M8) shown in the figure.

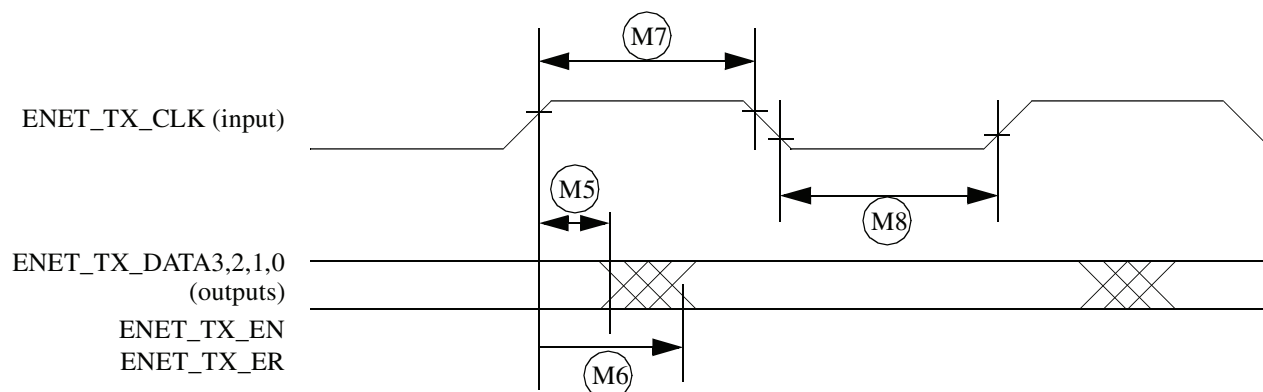


Figure 47. MII Transmit Signal Timing Diagram

Table 56. MII Transmit Signal Timing

ID	Characteristic ¹	Min.	Max.	Unit
M5	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid	5	—	ns
M6	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid	—	20	ns
M7	ENET_TX_CLK pulse width high	35%	65%	ENET_TX_CLK period
M8	ENET_TX_CLK pulse width low	35%	65%	ENET_TX_CLK period

¹ ENET_TX_EN, ENET_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

4.11.5.1.3 MII Asynchronous Inputs Signal Timing (ENET_CRS and ENET_COL)

Figure 48 shows MII asynchronous input timings. Table 57 describes the timing parameter (M9) shown in the figure.

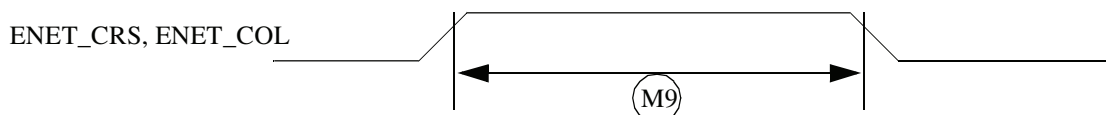


Figure 48. MII Async Inputs Timing Diagram

Table 57. MII Asynchronous Inputs Signal Timing

ID	Characteristic	Min.	Max.	Unit
M9 ¹	ENET_CRS to ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

¹ ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.11.5.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 49 shows MII asynchronous input timings. Table 58 describes the timing parameters (M10–M15) shown in the figure.

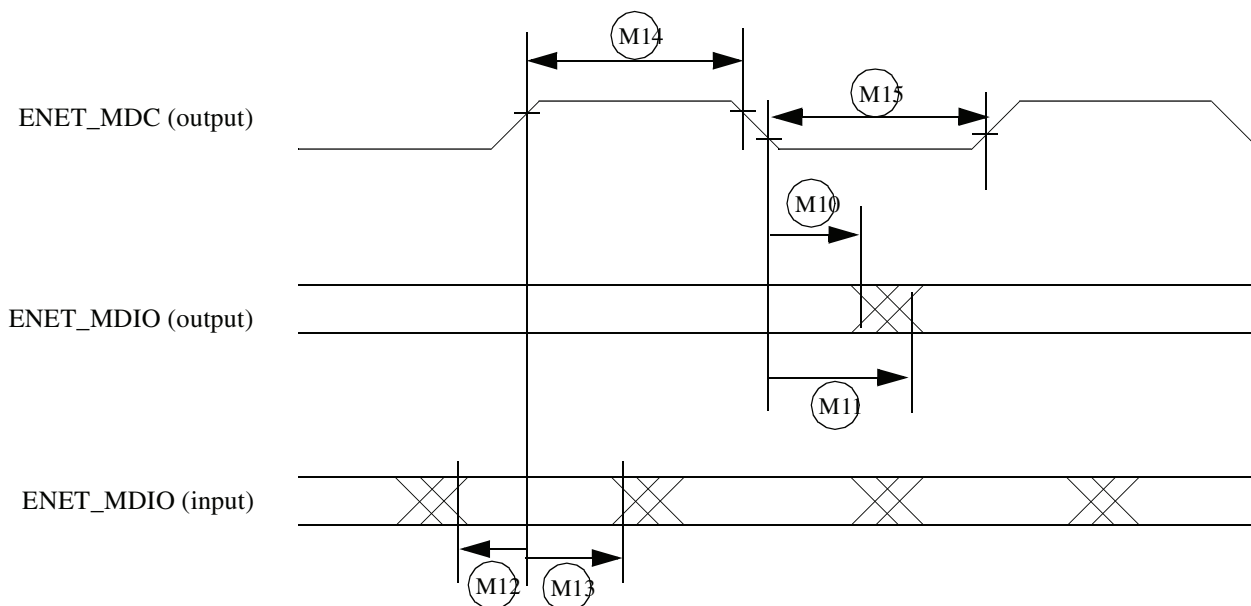


Figure 49. MII Serial Management Channel Timing Diagram

Table 58. MII Serial Management Channel Timing

ID	Characteristic	Min.	Max.	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

4.11.5.2 RMII Mode Timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz \pm 50 ppm continuous reference clock. ENET_RX_EN is used as the CRS_DV in RMII. Other signals under RMII mode include ENET_TX_EN, ENET0_TXD[1:0], ENET0_RXD[1:0] and ENET_RX_ER.

Figure 50 shows RMII mode timings. Table 59 describes the timing parameters (M16–M21) shown in the figure.

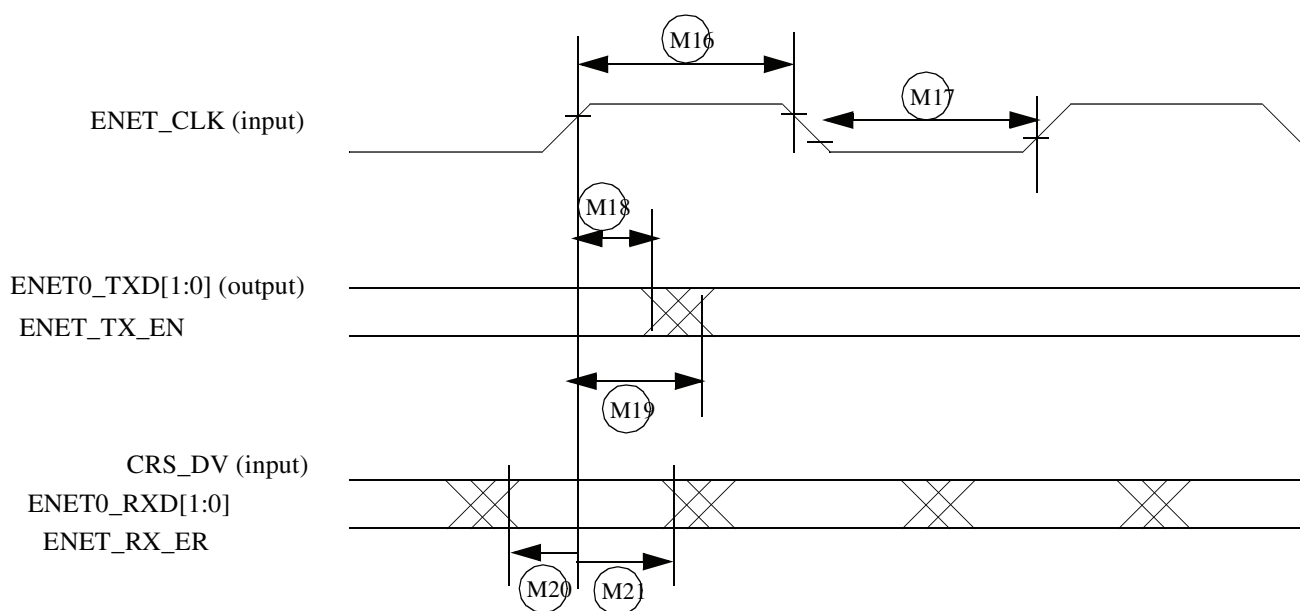
**Figure 50. RMII Mode Signal Timing Diagram**

Table 59. RMI Signal Timing

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_EN invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_EN valid	—	15	ns
M20	ENET0_RXD[1:0], CRS_DV(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	4	—	ns
M21	ENET_CLK to ENET0_RXD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

4.11.5.3 RGMII Signal Switching Specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 60. RGMII Signal Switching Specifications¹

Symbol	Description	Min.	Max.	Unit
T_{cyc}^2	Clock cycle duration	7.2	8.8	ns
T_{skewT}^3	Data to clock output skew at transmitter	-100	900	ps
T_{skewR}^3	Data to clock input skew at receiver	1	2.6	ps
Duty_G ⁴	Duty cycle for Gigabit	45	55	%
Duty_T ⁴	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

¹ The timings assume the following configuration:

DDR_SEL = (11)b

DSE (drive-strength) = (111)b

² For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns \pm 40 ns and 40 ns \pm 4 ns respectively.

³ For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional delay of greater than 1.2 ns and less than 1.7 ns will be added to the associated clock signal. For 10/100, the max value is unspecified.

⁴ Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three T_{cyc} of the lowest speed transitioned between.

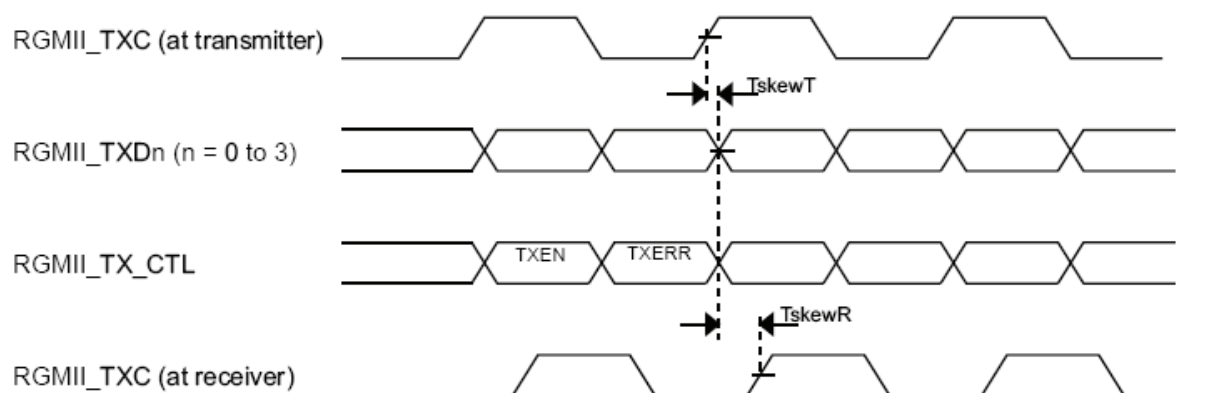


Figure 51. RGMII Transmit Signal Timing Diagram Original

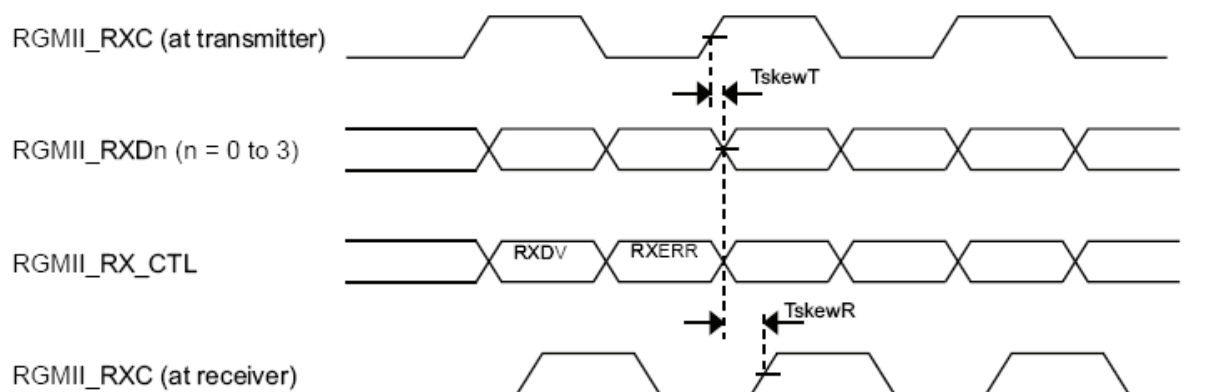


Figure 52. RGMII Receive Signal Timing Diagram Original

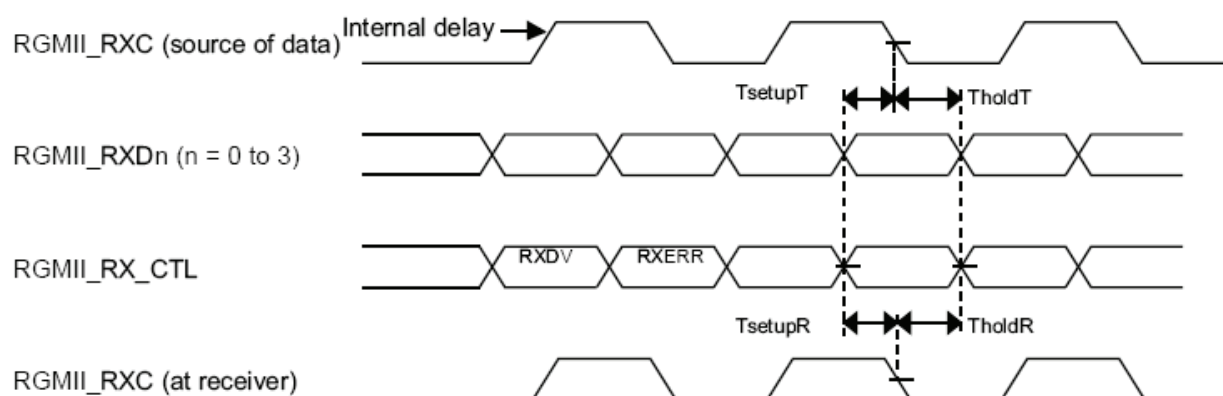


Figure 53. RGMII Receive Signal Timing Diagram with Internal Delay

4.11.6 Flexible Controller Area Network (FlexCAN) AC Electrical Specifications

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. The processor has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the i.MX 6Dual/6Quad reference manual to see which pins expose Tx and Rx pins; these ports are named TXCAN and RXCAN, respectively.

4.11.7 HDMI Module Timing Parameters

4.11.7.1 Latencies and Timing Information

Power-up time (time between TX_PWRON assertion and TX_READY assertion) for the HDMI 3D Tx PHY while operating with the slowest input reference clock supported (13.5 MHz) is 3.35 ms.

Power-up time for the HDMI 3D Tx PHY while operating with the fastest input reference clock supported (340 MHz) is 133 μ s.

4.11.7.2 Electrical Characteristics

The table below provides electrical characteristics for the HDMI 3D Tx PHY. The following three figures illustrate various definitions and measurement conditions specified in the table below.

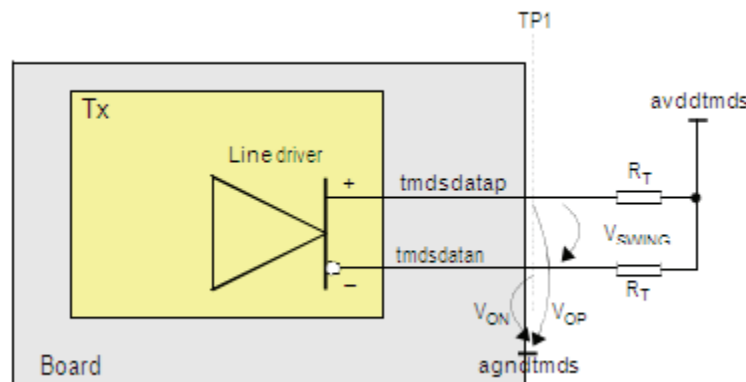


Figure 54. Driver Measuring Conditions

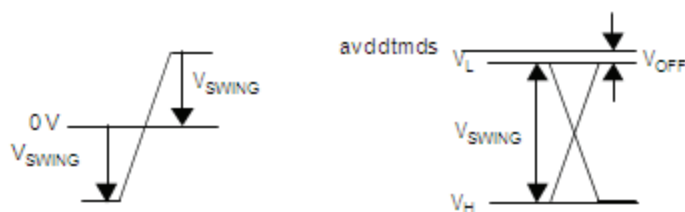


Figure 55. Driver Definitions

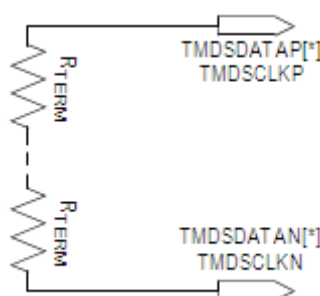


Figure 56. Source Termination

Table 61. Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Operating conditions for HDMI						
avddtmDs	Termination supply voltage	-	3.15	3.3	3.45	V
R_T	Termination resistance	-	45	50	55	Ω
TMDS drivers DC specifications						
V_{OFF}	Single-ended standby voltage	$R_T = 50 \Omega$	$avddtmDs \pm 10 \text{ mV}$			mV
V_{SWING}	Single-ended output swing voltage	For measurement conditions and definitions, see the first two figures above. Compliance point TP1 as defined in the HDMI specification, version 1.3a, section 4.2.4.	400	-	600	mV
V_H	Single-ended output high voltage For definition, see the second figure above.	If attached sink supports TMSCLK < or = 165 MHz	$avddtmDs \pm 10 \text{ mV}$			mV
		If attached sink supports TMSCLK > 165 MHz	$avddtmDs - 200 \text{ mV}$	-	$avddtmDs + 10 \text{ mV}$	mV
V_L	Single-ended output low voltage For definition, see the second figure above.	If attached sink supports TMSCLK < or = 165 MHz	$avddtmDs - 600 \text{ mV}$	-	$avddtmDs - 400 \text{ mV}$	mV
		If attached sink supports TMSCLK > 165 MHz	$avddtmDs - 700 \text{ mV}$	-	$avddtmDs - 400 \text{ mV}$	mV

Table 61. Electrical Characteristics (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
R_{TERM}	Differential source termination load (inside HDMI 3D Tx PHY) Although the HDMI 3D Tx PHY includes differential source termination, the user-defined value is set for each single line (for illustration, see the third figure above). Note: R_{TERM} can also be configured to be open and not present on TMDS channels.	-	50	-	200	Ω
Hot plug detect specifications						
HPD^{VH}	Hot plug detect high range	-	2.0	-	5.3	V
VHPD_{VL}	Hot plug detect low range	-	0	-	0.8	V
HPD_{Z}	Hot plug detect input impedance	-	10	-	-	k Ω
HPD_{t}	Hot plug detect time delay	-	-	-	100	μs

4.11.8 Switching Characteristics

Table 62 describes switching characteristics for the HDMI 3D Tx PHY. Figure 57 to Figure 62 illustrate various parameters specified in table.

NOTE

All dynamic parameters related to the TMDS line drivers' performance imply the use of assembly guidelines.

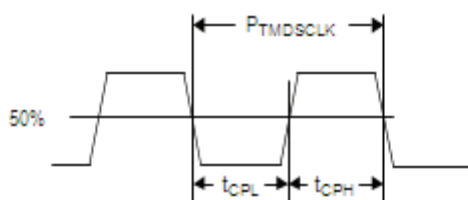


Figure 57. TMDS Clock Signal Definitions

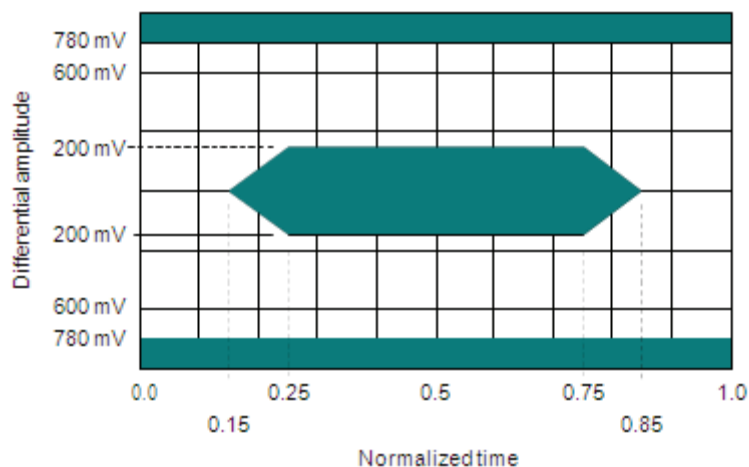


Figure 58. Eye Diagram Mask Definition for HDMI Driver Signal Specification at TP1

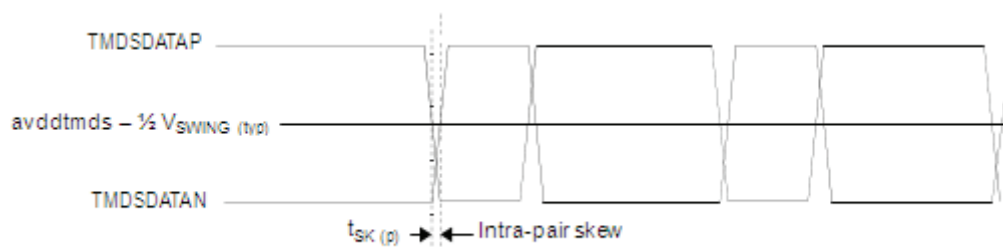


Figure 59. Intra-Pair Skew Definition

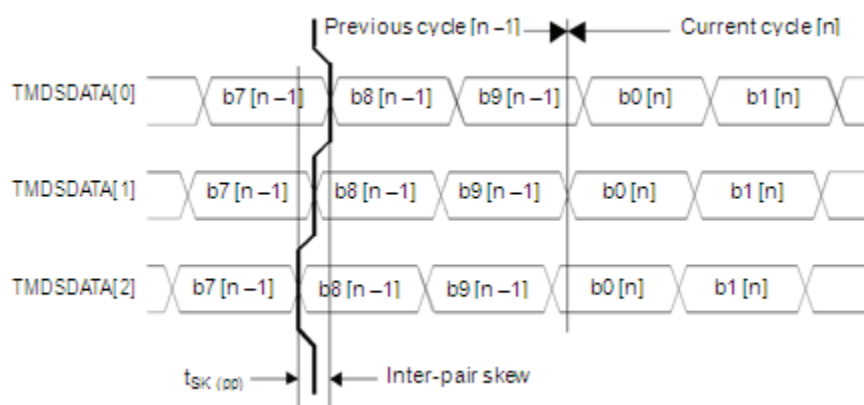


Figure 60. Inter-Pair Skew Definition

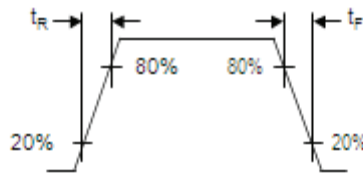


Figure 61. TMDS Output Signals Rise and Fall Time Definition

Color Depth = 8 bits

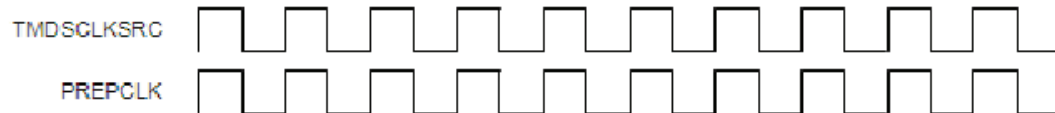


Figure 62. PREPCLK Frequencies

Table 62. Switching Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
TMDS Drivers Specifications						
—	Maximum serial data rate	—	—	—	3.4	Gbps
F_{TMDCLK}	TMDCLK frequency	On TMDCLKP/N outputs	25	—	340	MHz
P_{TMDCLK}	TMDCLK period	$RL = 50 \Omega$ See Figure 57.	2.94	—	40	ns
t_{CDC}	TMDCLK duty cycle	$t_{\text{CDC}} = t_{\text{CPH}} / P_{\text{TMDCLK}}$ $RL = 50 \Omega$ See Figure 57.	40	50	60	%
t_{CPH}	TMDCLK high time	$RL = 50 \Omega$ See Figure 57.	4	5	6	UI
t_{CPL}	TMDCLK low time	$RL = 50 \Omega$ See Figure 57.	4	5	6	UI
—	TMDCLK jitter ¹	$RL = 50 \Omega$	—	—	0.25	UI
$t_{\text{SK(p)}}$	Intra-pair (pulse) skew	$RL = 50 \Omega$ See Figure 59.	—	—	0.15	UI
$t_{\text{SK(pp)}}$	Inter-pair skew	$RL = 50 \Omega$ See Figure 60.	—	—	1	UI
t_{R}	Differential output signal rise time	20–80% $RL = 50 \Omega$ See Figure 61.	75	—	0.4 UI	ps
t_{F}	Differential output signal fall time	20–80% $RL = 50 \Omega$ See Figure 61.	75	—	0.4 UI	ps
—	Differential signal overshoot	Referred to $2 \times V_{\text{SWING}}$	—	—	15	%

Table 62. Switching Characteristics (continued)

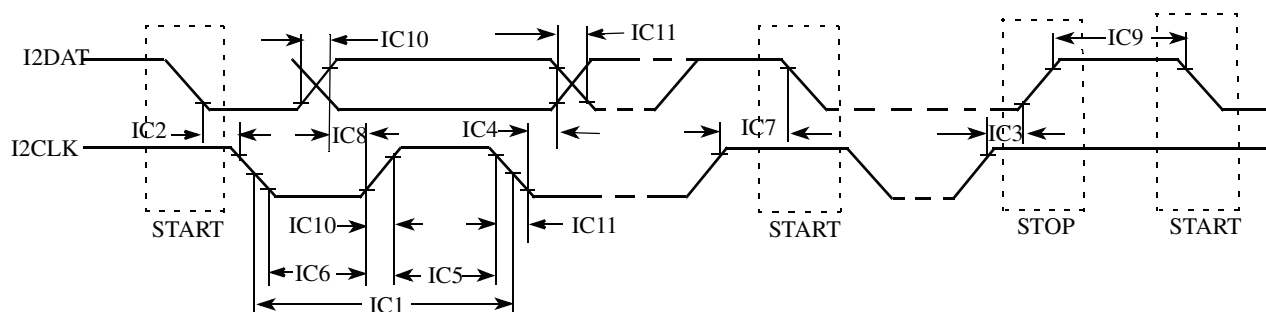
—	Differential signal undershoot	Referred to $2 \times V_{\text{SWING}}$	—	—	25	%
Data and Control Interface Specifications						
$t_{\text{Power-up}}^2$	HDMI 3D Tx PHY power-up time	From power-down to TX_READY assertion	—	—	3.35	ms

¹ Relative to ideal recovery clock, as specified in the HDMI specification, version 1.4a, section 4.2.3.

² For information about latencies and associated timings, see [Section 4.11.7.1, “Latencies and Timing Information.”](#)

4.11.9 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. [Figure 63](#) depicts the timing of I²C module, and [Table 63](#) lists the I²C module timing characteristics.

Figure 63. I²C Bus TimingTable 63. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2CLK cycle time	10	—	2.5	—	μs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	μs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	μs
IC4	Data hold time	0 ¹	3.45 ²	0 ¹	0.9 ²	μs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	μs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	μs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	μs
IC8	Data set-up time	250	—	100 ³	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	μs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	$20 + 0.1C_b^4$	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	$20 + 0.1C_b^4$	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

- ¹ A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.
- ² The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal.
- ³ A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line $\text{max_rise_time (IC9)} + \text{data_setup_time (IC7)} = 1000 + 250 = 1250$ ns (according to the Standard-mode I2C-bus specification) before the I2CLK line is released.
- ⁴ C_b = total capacitance of one bus line in pF.

4.11.10 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

4.11.10.1 IPU Sensor Interface Signal Mapping

The IPU supports a number of sensor input formats. Table 64 defines the mapping of the Sensor Interface Pins used for various supported interface formats.

Table 64. Camera Input Signal Cross Reference, Format, and Bits Per Cycle

Signal Name ¹	RGB565 8 bits 2 cycles	RGB565 ² 8 bits 3 cycles	RGB666 ³ 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr ⁴ 8 bits 2 cycles	RGB565 ⁵ 16 bits 2 cycles	YCbCr ⁶ 16 bits 1 cycle	YCbCr ⁷ 16 bits 1 cycle	YCbCr ⁸ 20 bits 1 cycle
CSIx_DAT0	—	—	—	—	—	—	—	0	C[0]
CSIx_DAT1	—	—	—	—	—	—	—	0	C[1]
CSIx_DAT2	—	—	—	—	—	—	—	C[0]	C[2]
CSIx_DAT3	—	—	—	—	—	—	—	C[1]	C[3]
CSIx_DAT4	—	—	—	—	—	B[0]	C[0]	C[2]	C[4]
CSIx_DAT5	—	—	—	—	—	B[1]	C[1]	C[3]	C[5]
CSIx_DAT6	—	—	—	—	—	B[2]	C[2]	C[4]	C[6]
CSIx_DAT7	—	—	—	—	—	B[3]	C[3]	C[5]	C[7]
CSIx_DAT8	—	—	—	—	—	B[4]	C[4]	C[6]	C[8]
CSIx_DAT9	—	—	—	—	—	G[0]	C[5]	C[7]	C[9]
CSIx_DAT10	—	—	—	—	—	G[1]	C[6]	0	Y[0]
CSIx_DAT11	—	—	—	—	—	G[2]	C[7]	0	Y[1]
CSIx_DAT12	B[0], G[3]	R[2],G[4],B[2]	R/G/B[4]	R/G/B[0]	Y/C[0]	G[3]	Y[0]	Y[0]	Y[2]
CSIx_DAT13	B[1], G[4]	R[3],G[5],B[3]	R/G/B[5]	R/G/B[1]	Y/C[1]	G[4]	Y[1]	Y[1]	Y[3]
CSIx_DAT14	B[2], G[5]	R[4],G[0],B[4]	R/G/B[0]	R/G/B[2]	Y/C[2]	G[5]	Y[2]	Y[2]	Y[4]
CSIx_DAT15	B[3], R[0]	R[0],G[1],B[0]	R/G/B[1]	R/G/B[3]	Y/C[3]	R[0]	Y[3]	Y[3]	Y[5]
CSIx_DAT16	B[4], R[1]	R[1],G[2],B[1]	R/G/B[2]	R/G/B[4]	Y/C[4]	R[1]	Y[4]	Y[4]	Y[6]
CSIx_DAT17	G[0], R[2]	R[2],G[3],B[2]	R/G/B[3]	R/G/B[5]	Y/C[5]	R[2]	Y[5]	Y[5]	Y[7]
CSIx_DAT18	G[1], R[3]	R[3],G[4],B[3]	R/G/B[4]	R/G/B[6]	Y/C[6]	R[3]	Y[6]	Y[6]	Y[8]
CSIx_DAT19	G[2], R[4]	R[4],G[5],B[4]	R/G/B[5]	R/G/B[7]	Y/C[7]	R[4]	Y[7]	Y[7]	Y[9]

¹ CSIx stands for CSI1 or CSI2.

² The MSB bits are duplicated on LSB bits implementing color extension.

³ The two MSB bits are duplicated on LSB bits implementing color extension.

⁴ YCbCr, 8 bits—Supported within the BT.656 protocol (sync embedded within the data stream).

⁵ RGB, 16 bits—Supported in two ways: (1) As a “generic data” input—with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.

⁶ YCbCr, 16 bits—Supported as a “generic-data” input—with no on-the-fly processing.

⁷ YCbCr, 16 bits—Supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).

⁸ YCbCr, 20 bits—Supported only within the BT.1120 protocol (syncs embedded within the data stream).

4.11.10.2 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.11.10.2.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the CSIx_VSYNC and CSIx_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is CSIx_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering CSIx_VSYNC and CSIx_HSYNC signals for internal use. On BT.656 one component per cycle is received over the CSIx_DATA bus. On BT.1120 two components per cycle are received over the CSIx_DATA bus.

4.11.10.2.2 Gated Clock Mode

The CSIx_VSYNC, CSIx_HSYNC, and CSIx_PIX_CLK signals are used in this mode. See [Figure 64](#).

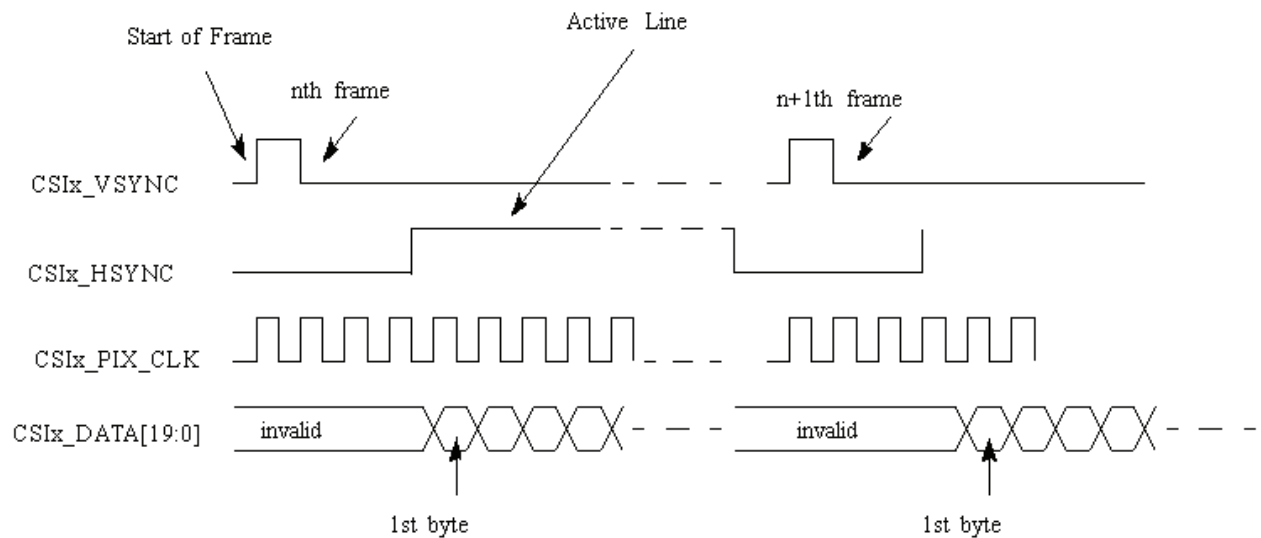


Figure 64. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on CSIx_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then CSIx_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as CSIx_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. CSIx_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For the next line, the CSIx_HSYNC timing repeats. For the next frame, the CSIx_VSYNC timing repeats.

4.11.10.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in [Section 4.11.10.2.2, “Gated Clock Mode,”](#)) except for the CSIx_HSYNC signal, which is not used (see [Figure 65](#)). All incoming pixel clocks are valid and cause data to be latched into the input FIFO. The CSIx_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

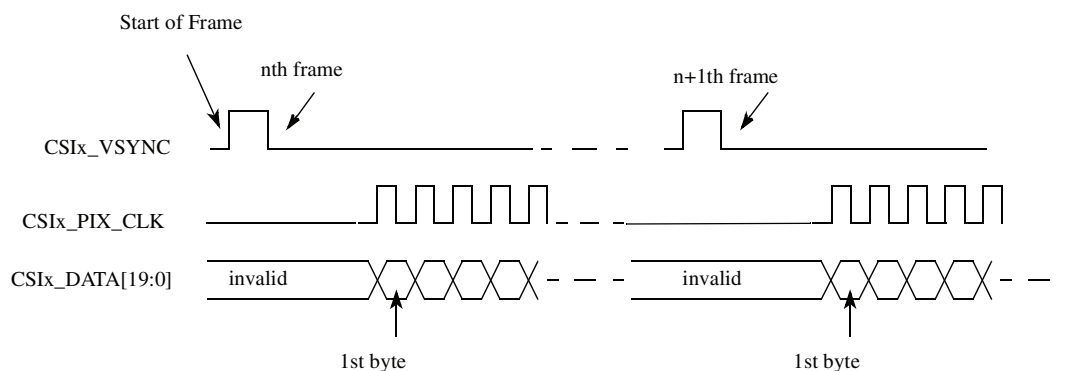


Figure 65. Non-Gated Clock Mode Timing Diagram

The timing described in [Figure 65](#) is that of a typical sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered CSIx_VSYNC; active-high/low CSIx_HSYNC; and rising/falling-edge triggered CSIx_PIX_CLK.

4.11.10.3 Electrical Characteristics

Figure 66 depicts the sensor interface timing. CSIx_MCLK signal described here is not generated by the IPU. Table 65 lists the sensor interface timing characteristics.

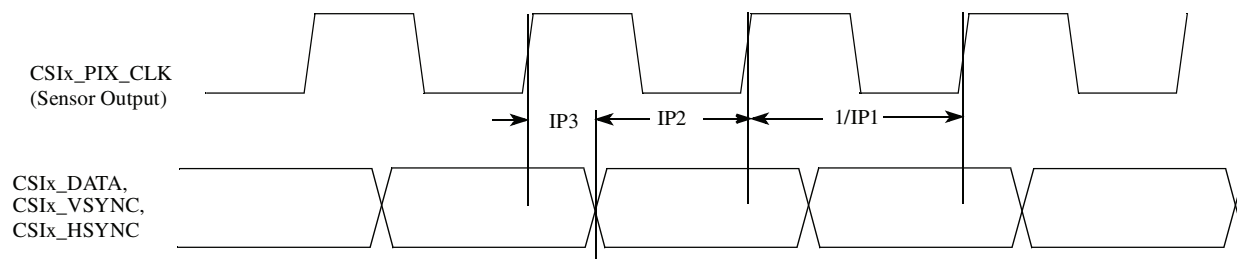


Figure 66. Sensor Interface Timing Diagram

Table 65. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	180	MHz
IP2	Data and control setup time	Tsu	2	—	ns
IP3	Data and control holdup time	Thd	1	—	ns

4.11.10.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 66 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 66. Video Signal Cross-Reference

i.MX 6Dual/6Quad	LCD							Comment ¹
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb ²	16-bit YCrCb	20-bit YCrCb	
DISPx_DAT0	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	<p>The restrictions are as follows:</p> <ul style="list-style-type: none">• There are maximal three continuous groups of bits that could be independently mapped to the external bus. Groups should not be overlapped.• The bit order is expressed in each of the bit groups, for example, B[0] = least significant blue pixel bit.
DISPx_DAT1	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	
DISPx_DAT2	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	
DISPx_DAT3	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	
DISPx_DAT4	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	
DISPx_DAT5	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	
DISPx_DAT6	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	
DISPx_DAT7	DAT[7]	G[2]	G[1]	B[7]	Y/C[7]	C[7]	C[7]	
DISPx_DAT8	DAT[8]	G[3]	G[2]	G[0]	—	Y[0]	C[8]	
DISPx_DAT9	DAT[9]	G[4]	G[3]	G[1]	—	Y[1]	C[9]	
DISPx_DAT10	DAT[10]	G[5]	G[4]	G[2]	—	Y[2]	Y[0]	
DISPx_DAT11	DAT[11]	R[0]	G[5]	G[3]	—	Y[3]	Y[1]	
DISPx_DAT12	DAT[12]	R[1]	R[0]	G[4]	—	Y[4]	Y[2]	
DISPx_DAT13	DAT[13]	R[2]	R[1]	G[5]	—	Y[5]	Y[3]	
DISPx_DAT14	DAT[14]	R[3]	R[2]	G[6]	—	Y[6]	Y[4]	
DISPx_DAT15	DAT[15]	R[4]	R[3]	G[7]	—	Y[7]	Y[5]	
DISPx_DAT16	DAT[16]	—	R[4]	R[0]	—	—	Y[6]	
DISPx_DAT17	DAT[17]	—	R[5]	R[1]	—	—	Y[7]	
DISPx_DAT18	DAT[18]	—	—	R[2]	—	—	Y[8]	
DISPx_DAT19	DAT[19]	—	—	R[3]	—	—	Y[9]	
DISPx_DAT20	DAT[20]	—	—	R[4]	—	—	—	
DISPx_DAT21	DAT[21]	—	—	R[5]	—	—	—	

Table 66. Video Signal Cross-Reference (continued)

i.MX 6Dual/6Quad	LCD							Comment ¹
Port Name (x = 0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb ²	16-bit YCrCb	20-bit YCrCb	
DISPx_DAT22	DAT[22]	—	—	R[6]	—	—	—	—
DISPx_DAT23	DAT[23]	—	—	R[7]	—	—	—	—
Dlx_DISP_CLK	PixCLK							—
Dlx_PIN1	—							May be required for anti-tearing
Dlx_PIN2	HSYNC							—
Dlx_PIN3	VSYNC							VSYNC out
Dlx_PIN4	—							Additional frame/row synchronous signals with programmable timing
Dlx_PIN5	—							
Dlx_PIN6	—							
Dlx_PIN7	—							
Dlx_PIN8	—							
Dlx_D0_CS	—							—
Dlx_D1_CS	—							Alternate mode of PWM output for contrast or brightness control
Dlx_PIN11	—							—
Dlx_PIN12	—							—
Dlx_PIN13	—							Register select signal
Dlx_PIN14	—							Optional RS2
Dlx_PIN15	DRDY/DV							Data validation/blank, data enable
Dlx_PIN16	—							Additional data synchronous signals with programmable features/timing
Dlx_PIN17	Q							

¹ Signal mapping (both data and control/synchronization) is flexible. The table provides examples.

² This mode works in compliance with recommendation ITU-R BT.656. The timing reference signals (frame start, frame end, line start, and line end) are embedded in the 8-bit data bus. Only video data is supported, transmission of non-video related data during blanking intervals is not supported.

NOTE

Table 66 provides information for both the Disp0 and Disp1 ports. However, Disp1 port has reduced pinout depending on IOMUXC configuration and therefore may not support all the above configurations. See the IOMUXC table for details.

4.11.10.5 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls.

4.11.10.5.1 Synchronous Controls

The synchronous control changes its value as a function of a system or of an external clock. This control has a permanent period and a permanent waveform.

There are special physical outputs to provide synchronous controls:

- The `ipp_disp_clk` is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The `ipp_pin_1–ipp_pin_7` are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYCN) calculation. The internal event (local start point) is synchronized with internal `DI_CLK`. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half `DI_CLK` resolution. A full description of the counter system can be found in the IPU chapter of the i.MX 6Dual/6Quad reference manual.

4.11.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The `ipp_d0_cs` and `ipp_d1_cs` pins are dedicated to provide chip select signals to two displays.
- The `ipp_pin_11–ipp_pin_17` are general purpose asynchronous pins, that can be used to provide WR, RD, RS or any other data-oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data on the bus, a new internal start (local start point) is generated. The signal generators calculate predefined UP and DOWN values to change pins states with half `DI_CLK` resolution.

4.11.10.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.11.10.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated “local start point”. The synchronous display controls can be placed on time axis with DI’s offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

4.11.10.6.2 LCD Interface Functional Description

Figure 67 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure, signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock is used for calculation of other controls.
- IPP_DISP_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, IPP_DISP_CLK runs continuously.
- HSYNC causes the panel to start a new line. (Usually IPP_PIN_2 is used as HSYNC.)
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse. (Usually IPP_PIN_3 is used as VSYNC.)
- DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off. (DRDY can be used either synchronous or asynchronous generic purpose pin as well.)

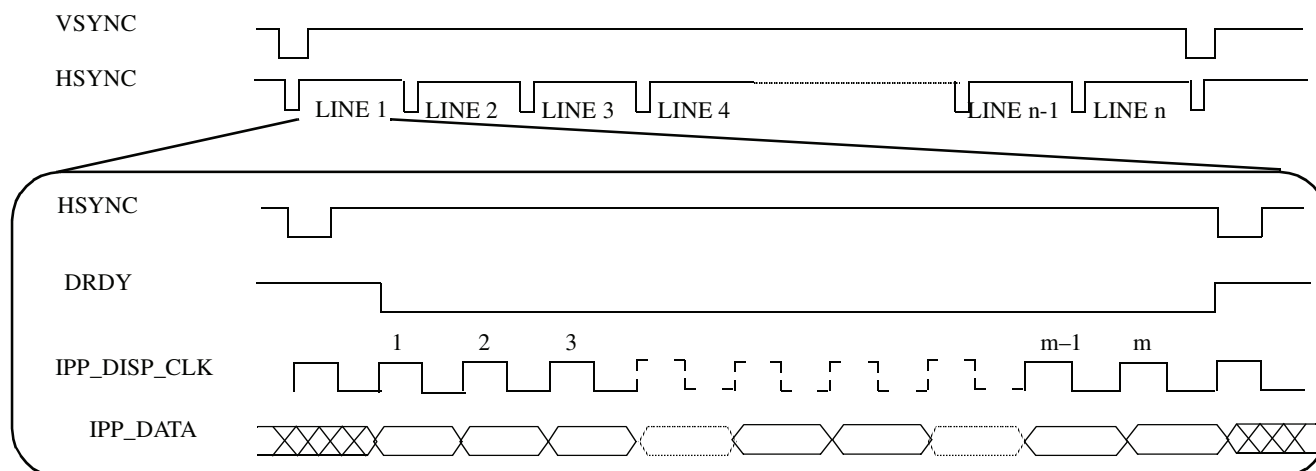


Figure 67. Interface Timing Diagram for TFT (Active Matrix) Panels

4.11.10.6.3 TFT Panel Sync Pulse Timing Diagrams

Figure 68 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All the parameters shown in the figure are programmable. All controls are started by corresponding internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC, and DRDY signals.

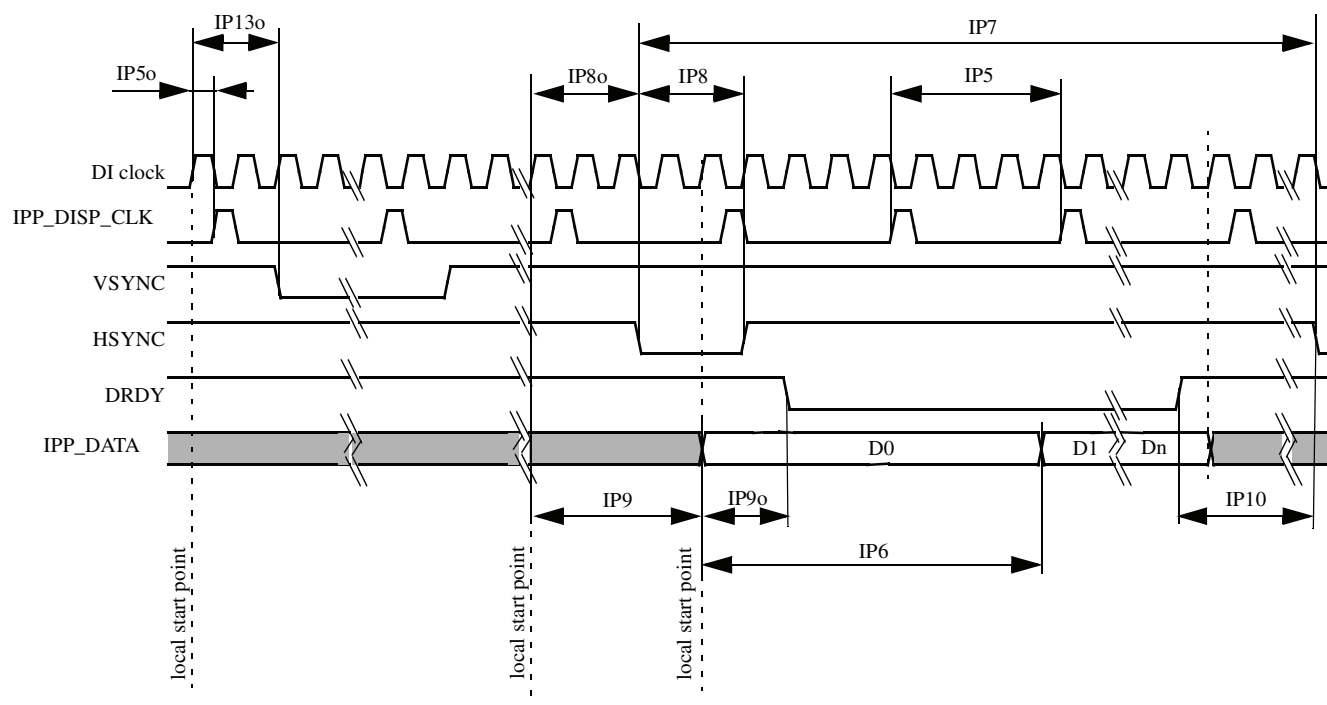


Figure 68. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 69 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

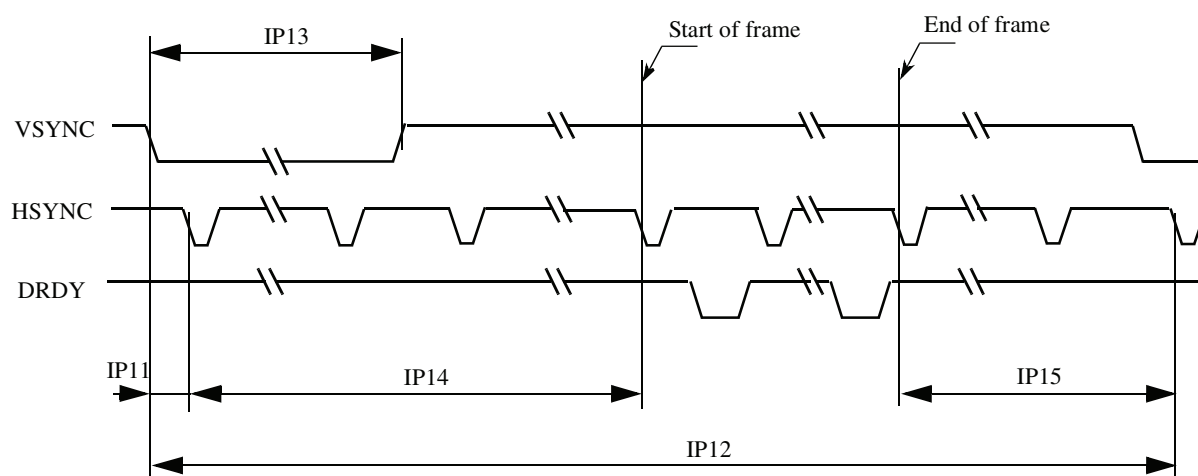


Figure 69. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 67 shows timing characteristics of signals presented in Figure 68 and Figure 69.

Table 67. Synchronous Display Interface Timing Characteristics (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP5	Display interface clock period	Tdicp	(¹)	Display interface clock. IPP_DISP_CLK	ns
IP6	Display pixel clock period	Tdpcp	DISP_CLK_PER_PIXEL × Tdicp	Time of translation of one pixel to display, DISP_CLK_PER_PIXEL—number of pixel components in one pixel (1.n). The DISP_CLK_PER_PIXEL is virtual parameter to define display pixel clock period. The DISP_CLK_PER_PIXEL is received by DC/DI one access division to n components.	ns
IP7	Screen width time	Tsw	(SCREEN_WIDTH) × Tdicp	SCREEN_WIDTH—screen width in, interface clocks. horizontal blanking included. The SCREEN_WIDTH should be built by suitable DI's counter ² .	ns
IP8	HSYNC width time	Thsw	(HSYNC_WIDTH)	HSYNC_WIDTH—Hsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP9	Horizontal blank interval 1	Thbi1	BGXP × Tdicp	BGXP—width of a horizontal blanking before a first active data in a line (in interface clocks). The BGXP should be built by suitable DI's counter.	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH – BGXP – FW) × Tdicp	Width a horizontal blanking after a last active data in a line (in interface clocks) FW—with of active line in interface clocks. The FW should be built by suitable DI's counter.	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT) × Tsw	SCREEN_HEIGHT— screen height in lines with blanking. The SCREEN_HEIGHT is a distance between 2 VSYNCs. The SCREEN_HEIGHT should be built by suitable DI's counter.	ns
IP13	VSYNC width	Tvsw	VSYNC_WIDTH	VSYNC_WIDTH—Vsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP14	Vertical blank interval 1	Tvbi1	BGYP × Tsw	BGYP—width of first Vertical blanking interval in line. The BGYP should be built by suitable DI's counter.	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT – BGYP – FH) × Tsw	Width of second vertical blanking interval in line. The FH should be built by suitable DI's counter.	ns

Table 67. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution). Defined by DISP_CLK counter.	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET—offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution). The DRDY_OFFSET should be built by suitable DI's counter.	ns

¹ Display interface clock period immediate value.

$$T_{dicp} = \begin{cases} T_{diclk} \times \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD}, & \text{for integer } \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD} \\ T_{diclk} \left(\left\lfloor \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD} \right\rfloor + 0.5 \pm 0.5 \right), & \text{for fractional } \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.

DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency

Display interface clock period average value.

$$\bar{T}_{dicp} = T_{diclk} \times \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD}$$

² DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximal accuracy of UP/DOWN edge of controls is:

$$\text{Accuracy} = (0.5 \times T_{diclk}) \pm 0.62\text{ns}$$

The maximal accuracy of UP/DOWN edge of IPP_DATA is:

$$\text{Accuracy} = T_{\text{dclk}} \pm 0.62\text{ns}$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are register-controlled.

Figure 70 depicts the synchronous display interface timing for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are register-controlled. Table 68 lists the synchronous display interface timing characteristics.

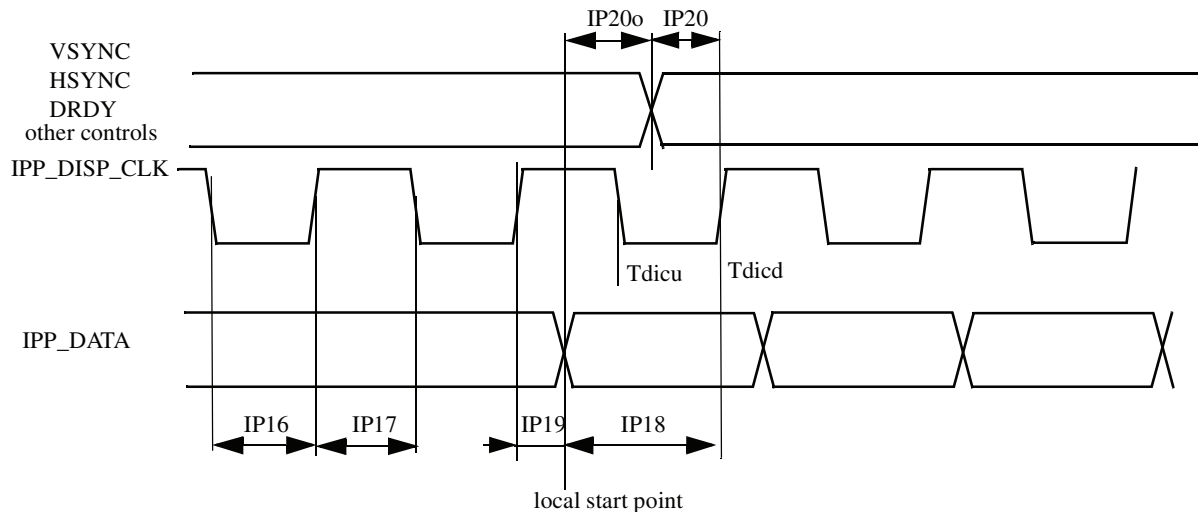


Figure 70. Synchronous Display Interface Timing Diagram—Access Level

Table 68. Synchronous Display Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ ¹	Max	Unit
IP16	Display interface clock low time	Tckl	$T_{\text{dcd}} - T_{\text{dicu}} - 1.24$	$T_{\text{dcd}}^2 - T_{\text{dicu}}^3$	$T_{\text{dcd}} - T_{\text{dicu}} + 1.24$	ns
IP17	Display interface clock high time	Tckh	$T_{\text{dcp}} - T_{\text{dcd}} + T_{\text{dicu}} - 1.24$	$T_{\text{dcp}} - T_{\text{dcd}} + T_{\text{dicu}}$	$T_{\text{dcp}} - T_{\text{dcd}} + T_{\text{dicu}} + 1.2$	ns
IP18	Data setup time	Tdsu	$T_{\text{dcd}} - 1.24$	T_{dicu}	—	ns
IP19	Data holdup time	Tdhd	$T_{\text{dcp}} - T_{\text{dcd}} - 1.24$	$T_{\text{dcp}} - T_{\text{dicu}}$	—	ns
IP20o	Control signals offset times (defined for each pin)	Tocsu	$T_{\text{ocsu}} - 1.24$	T_{ocsu}	$T_{\text{ocsu}} + 1.24$	ns
IP20	Control signals setup time to display interface clock (defined for each pin)	Tcsu	$T_{\text{dcd}} - 1.24 - T_{\text{ocsu}} \% T_{\text{dcp}}$	T_{dicu}	—	ns

¹The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

Electrical Characteristics

² Display interface clock down time

$$T_{dcd} = \frac{1}{2} \left(T_{diclk} \times \text{ceil} \left[\frac{2 \times \text{DISP_CLK_DOWN}}{\text{DI_CLK_PERIOD}} \right] \right)$$

³ Display interface clock up time where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

$$T_{dcd} = \frac{1}{2} \left(T_{diclk} \times \text{ceil} \left[\frac{2 \times \text{DISP_CLK_UP}}{\text{DI_CLK_PERIOD}} \right] \right)$$

4.11.11 LVDS Display Bridge (LDB) Module Parameters

The LVDS interface complies with TIA/EIA 644-A standard. For more details, see TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits.”

Table 69. LVDS Display Bridge (LDB) Electrical Specification

Parameter	Symbol	Test Condition	Min	Max	Units
Differential Voltage Output Voltage	V_{OD}	100 Ω Differential load	250	450	mV
Output Voltage High	V_{OH}	100 Ω differential load (0 V Diff—Output High Voltage static)	1.25	1.6	mV
Output Voltage Low	V_{OL}	100 Ω differential load (0 V Diff—Output Low Voltage static)	0.9	1.25	mV
Offset Static Voltage	V_{OS}	Two 49.9 Ω resistors in series between N-P terminal, with output in either Zero or One state, the voltage measured between the 2 resistors.	1.15	1.375	V
VOS Differential	V_{OSDIFF}	Difference in V_{OS} between a One and a Zero state	-50	50	mV
Output short circuited to GND	ISA ISB	With the output common shorted to GND	-24	24	mA
VT Full Load Test	VTLoad	100 Ω Differential load with a 3.74 k Ω load between GND and I/O supply voltage	247	454	mV

4.11.12 MIPI D-PHY Timing Parameters

This section describes MIPI D-PHY electrical specifications, compliant with MIPI CSI-2 version 1.0, D-PHY specification Rev. 1.0 (for MIPI sensor port x4 lanes) and MIPI DSI Version 1.01, and D-PHY specification Rev. 1.0 (and also DPI version 2.0, DBI version 2.0, DSC version 1.0a at protocol layer) (for MIPI display port x2 lanes).

4.11.12.1 Electrical and Timing Information

Table 70. Electrical and Timing Information

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
Input DC Specifications - Apply to CLKP/N and DATAP/N inputs						
V_I	Input signal voltage range	Transient voltage range is limited from -300 mV to 1600 mV	-50	—	1350	mV

Table 70. Electrical and Timing Information (continued)

V_{LEAK}	Input leakage current	$V_{GND\text{SH}}(\text{min}) = V_I = V_{GND\text{SH}}(\text{max}) + V_{OH}(\text{absmax})$ Lane module in LP Receive Mode	-10	—	10	mA
$V_{GND\text{SH}}$	Ground Shift		-50	—	50	mV
$V_{OH}(\text{absmax})$	Maximum transient output voltage level		—	—	1.45	V
$t_{voh}(\text{absmax})$	Maximum transient time above $V_{OH}(\text{absmax})$		—	—	20	ns
HS Line Drivers DC Specifications						
$ V_{OD} $	HS Transmit Differential output voltage magnitude	$80\ \Omega \leq R_L < 125\ \Omega$	140	200	270	mV
$\Delta V_{OD} $	Change in Differential output voltage magnitude between logic states	$80\ \Omega \leq R_L < 125\ \Omega$			10	mV
V_{CMTX}	Steady-state common-mode output voltage.	$80\ \Omega \leq R_L < 125\ \Omega$	150	200	250	mV
$\Delta V_{CMTX}(1,0)$	Changes in steady-state common-mode output voltage between logic states	$80\ \Omega \leq R_L < 125\ \Omega$			5	mV
$V_{OH\text{HS}}$	HS output high voltage	$80\ \Omega \leq R_L < 125\ \Omega$			360	mV
Z_{OS}	Single-ended output impedance.		40	50	62.5	Ω
ΔZ_{OS}	Single-ended output impedance mismatch.				10	%
LP Line Drivers DC Specifications						
V_{OL}	Output low-level SE voltage		-50		50	mV
V_{OH}	Output high-level SE voltage		1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance.		110			Ω
$\Delta Z_{OLP}(01-10)$	Single-ended output impedance mismatch driving opposite level				20	%
$\Delta Z_{OLP}(00-11)$	Single-ended output impedance mismatch driving same level				5	%
HS Line Receiver DC Specifications						
$V_{ID\text{TH}}$	Differential input high voltage threshold				70	mV
$V_{ID\text{TL}}$	Differential input low voltage threshold		-70			mV

Table 70. Electrical and Timing Information (continued)

V_{IHHS}	Single ended input high voltage				460	mV
V_{ILHS}	Single ended input low voltage		-40			mV
V_{CMRXDC}	Input common mode voltage		70		330	mV
Z_{ID}	Differential input impedance		80		125	Ω
LP Line Receiver DC Specifications						
V_{IL}	Input low voltage				550	mV
V_{IH}	Input high voltage		920			mV
V_{HYST}	Input hysteresis		25			mV
Contention Line Receiver DC Specifications						
V_{ILF}	Input low fault threshold		200		450	mV

4.11.12.2 D-PHY Signaling Levels

The signal levels are different for differential HS mode and single-ended LP mode. Figure 71 shows both the HS and LP signal levels on the left and right sides, respectively. The HS signaling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

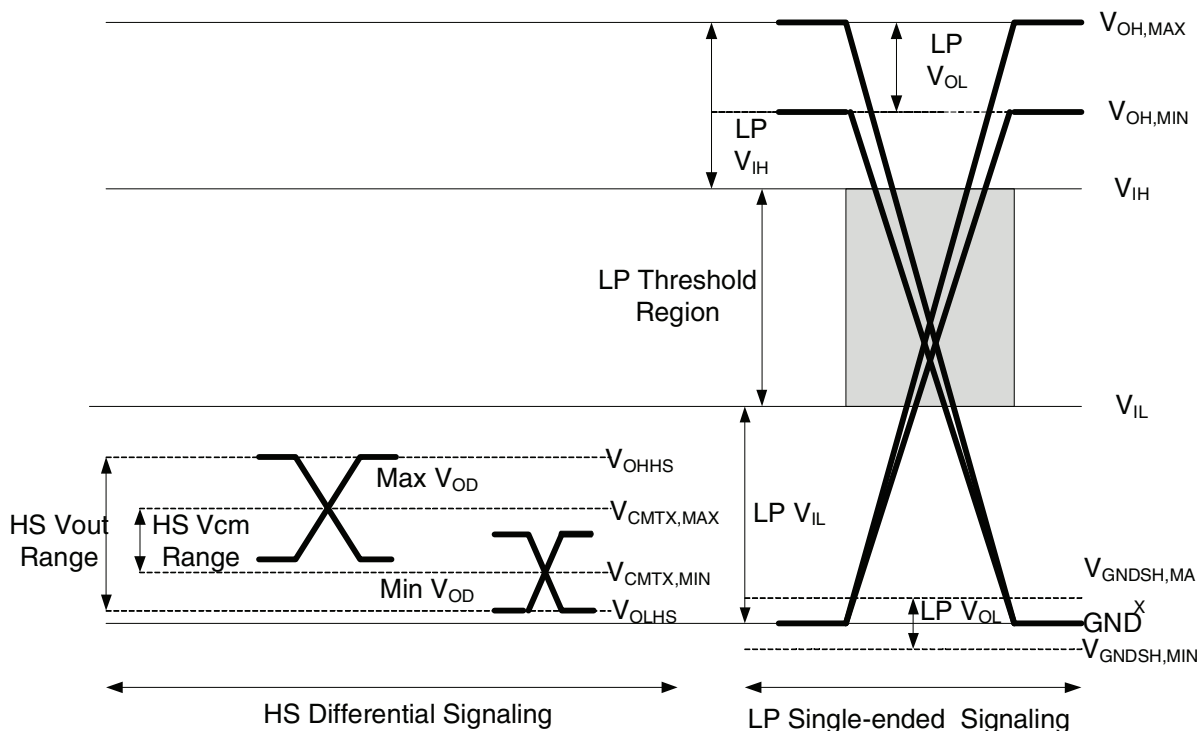


Figure 71. D-PHY Signaling Levels

4.11.12.3 HS Line Driver Characteristics

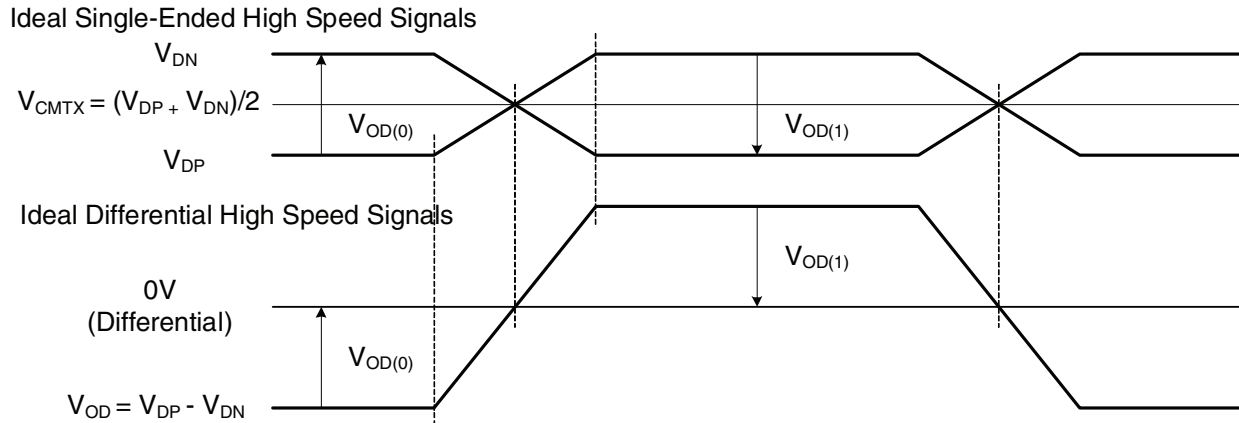


Figure 72. Ideal Single-ended and Resulting Differential HS Signals

4.11.12.4 Possible ΔV_{CMTX} and ΔV_{OD} Distortions of the Single-ended HS Signals

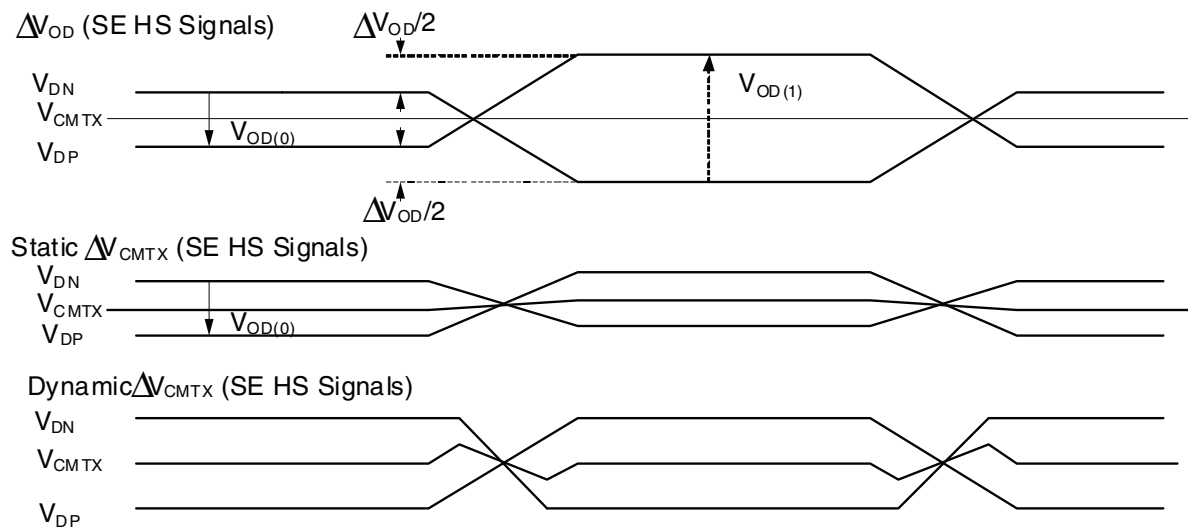


Figure 73. Possible ΔV_{CMTX} and ΔV_{OD} Distortions of the Single-ended HS Signals

4.11.12.5 D-PHY Switching Characteristics

Table 71. Electrical and Timing Information

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
HS Line Drivers AC Specifications						
—	Maximum serial data rate (forward direction)	On DATAP/N outputs. $80\ \Omega \leq R_L \leq 125\ \Omega$	80	—	1000	Mbps

Table 71. Electrical and Timing Information

F _{DDRCLK}	DDR CLK frequency	On DATAP/N outputs.	40	—	500	MHz
P _{DDRCLK}	DDR CLK period	80 Ω ≤ RL ≤ 125 Ω	2	—	25	ns
t _{CDC}	DDR CLK duty cycle	t _{CDC} = t _{CPH} / P _{DDRCLK}	—	50	—	%
t _{CPH}	DDR CLK high time		—	1	—	UI
t _{CPL}	DDR CLK low time		—	1	—	UI
—	DDR CLK / DATA Jitter		—	75	—	ps pk-pk
t _{SKEW[PN]}	Intra-Pair (Pulse) skew			0.075		UI
t _{SKEW[TX]}	Data to Clock Skew		0.350		0.650	UI
t _{SETUP[RX]}	Data to Clock Receiver Setup time		0.15			UI
t _{HOLD[RX]}	Clock to Data Receiver Hold time		0.15			UI
t _r	Differential output signal rise time	20% to 80%, RL = 50 Ω	150		0.3UI	ps
t _f	Differential output signal fall time	20% to 80%, RL = 50 Ω	150		0.3UI	ps
ΔV _{CMTX(HF)}	Common level variation above 450 MHz	80 Ω ≤ RL ≤ 125 Ω			15	mV _{rms}
ΔV _{CMTX(LF)}	Common level variation between 50 MHz and 450 MHz	80 Ω ≤ RL ≤ 125 Ω			25	mV _p
LP Line Drivers AC Specifications						
t _{rip} , t _{flp}	Single ended output rise/fall time	15% to 85%, C _L < 70 pF			25	ns
t _{reo}		30% to 85%, C _L < 70 pF			35	ns
δV/δt _{SR}	Signal slew rate	15% to 85%, C _L < 70 pF			120	mV/ns
C _L	Load capacitance		0		70	pF
HS Line Receiver AC Specifications						
ΔV _{CMRX(HF)}	Common mode interference beyond 450 MHz				200	mVpp
ΔV _{CMRX(LF)}	Common mode interference between 50 MHz and 450 MHz		-50		50	mVpp
C _{CM}	Common mode termination				60	pF
LP Line Receiver AC Specifications						
e _{SPIKE}	Input pulse rejection				300	Vps
T _{MIN}	Minimum pulse response		50			ns
V _{INT}	Pk-to-Pk interference voltage				400	mV
f _{INT}	Interference frequency		450			MHz
Model Parameters used for Driver Load switching performance evaluation						
C _{PAD}	Equivalent Single ended I/O PAD capacitance.				1	pF
C _{PIN}	Equivalent Single ended Package + PCB capacitance.				2	pF

Table 71. Electrical and Timing Information

L_S	Equivalent wire bond series inductance				1.5	nH
R_S	Equivalent wire bond series resistance				0.15	Ω
R_L	Load Resistance		80	100	125	Ω

4.11.12.6 High-Speed Clock Timing

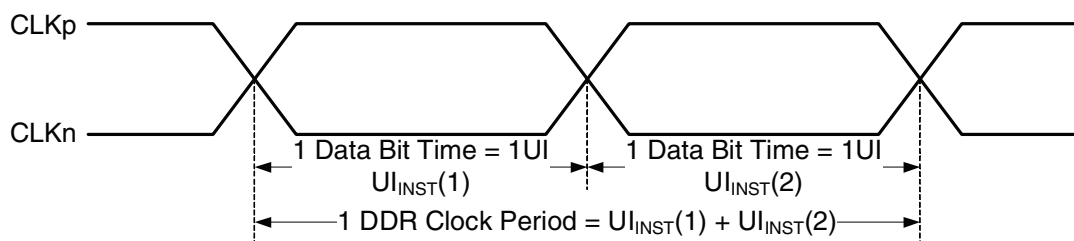


Figure 74. DDR Clock Definition

4.11.12.7 Forward High-Speed Data Transmission Timing

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 75:

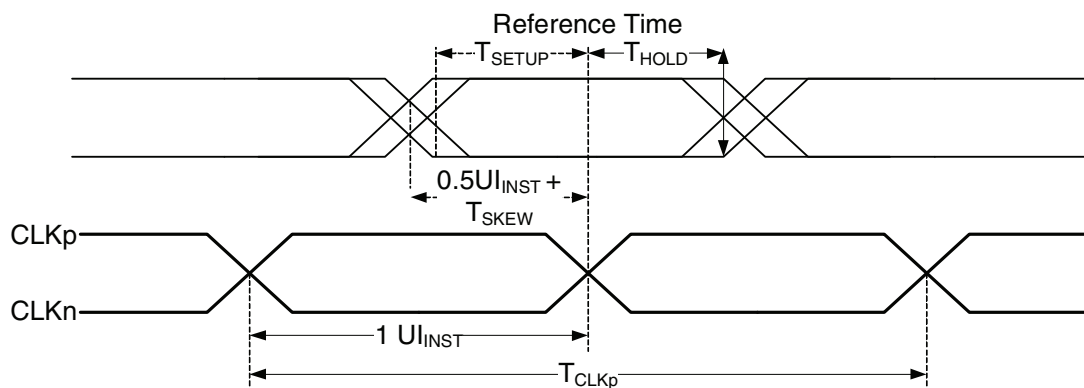


Figure 75. Data to Clock Timing Definitions

4.11.12.8 Reverse High-Speed Data Transmission Timing

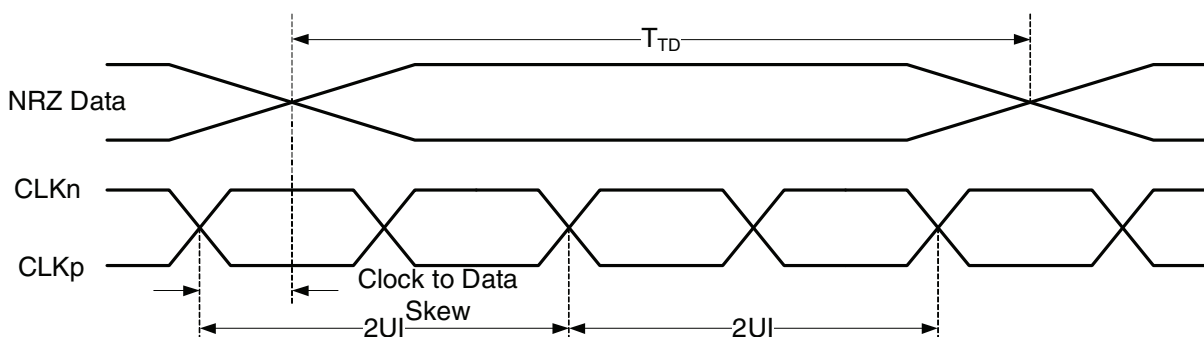


Figure 76. Reverse High-Speed Data Transmission Timing at Slave Side

4.11.12.9 Low-Power Receiver Timing

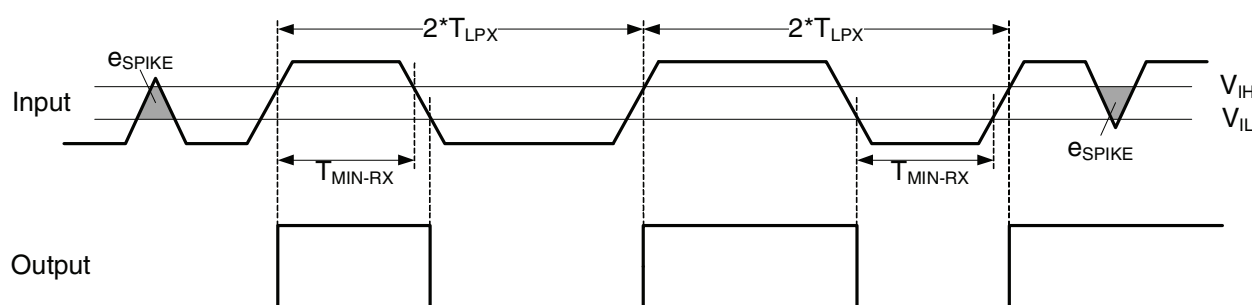


Figure 77. Input Glitch Rejection of Low-Power Receivers

4.11.13 HSI Host Controller Timing Parameters

This section describes the timing parameters of the HSI Host Controller which are compliant with High-Speed Synchronous Serial Interface (HSI) Physical Layer specification version 1.01.

4.11.13.1 Synchronous Data Flow

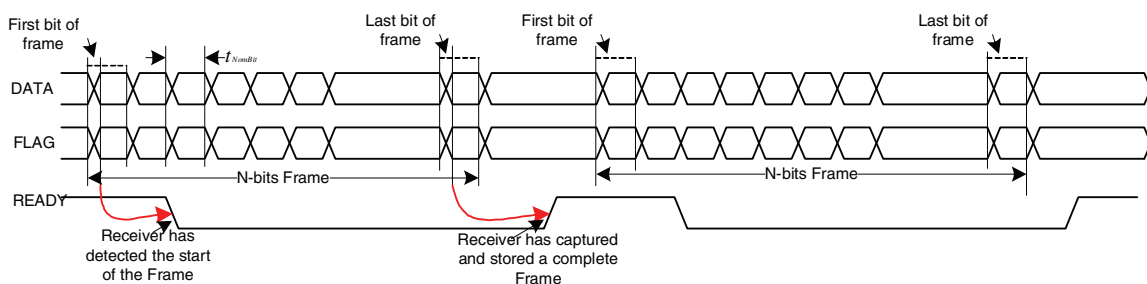


Figure 78. Synchronized Data Flow READY Signal Timing (Frame and Stream Transmission)

4.11.13.2 Pipelined Data Flow

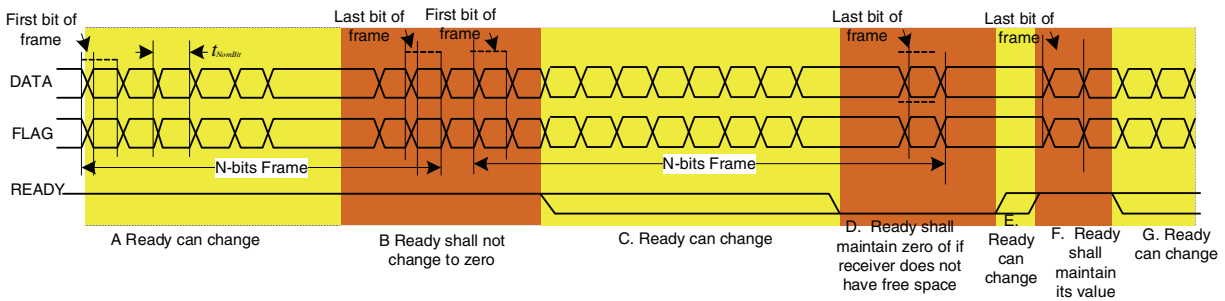


Figure 79. Pipelined Data Flow Ready Signal Timing (Frame Transmission Mode)

4.11.13.3 Receiver Real-Time Data Flow

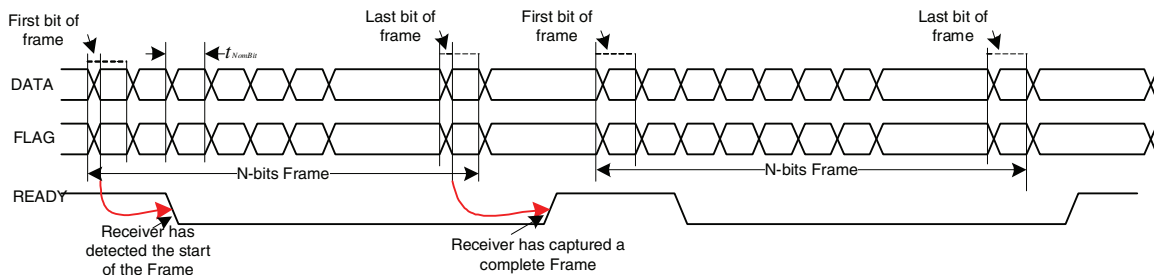


Figure 80. Receiver Real-Time Data Flow READY Signal Timing

4.11.13.4 Synchronized Data Flow Transmission with Wake

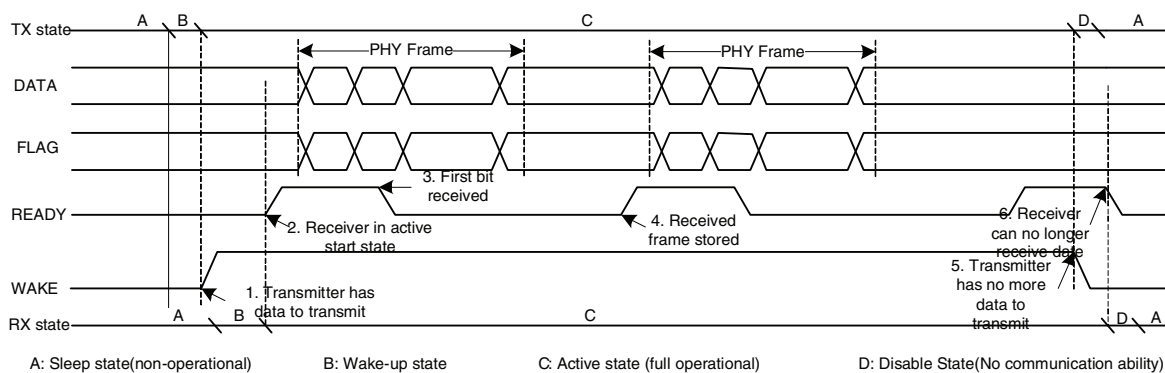


Figure 81. Synchronized Data Flow Transmission with WAKE

4.11.13.5 Stream Transmission Mode Frame Transfer

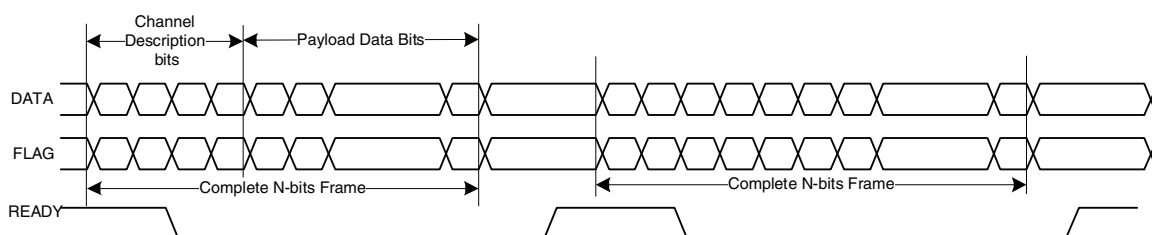


Figure 82. Stream Transmission Mode Frame Transfer (Synchronized Data Flow)

4.11.13.6 Frame Transmission Mode (Synchronized Data Flow)

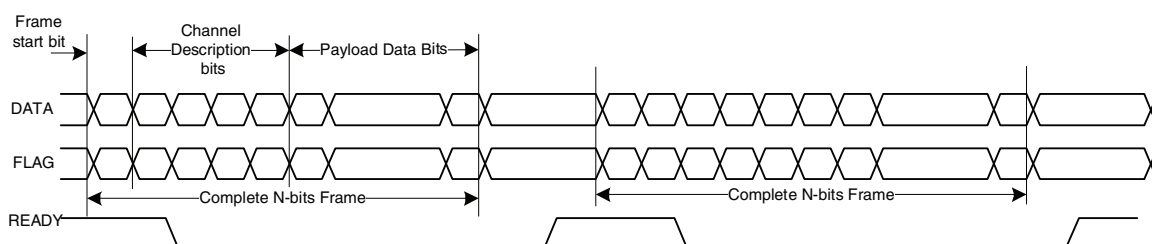


Figure 83. Frame Transmission Mode Transfer of Two Frames (Synchronized Data Flow)

4.11.13.7 Frame Transmission Mode (Pipelined Data Flow)

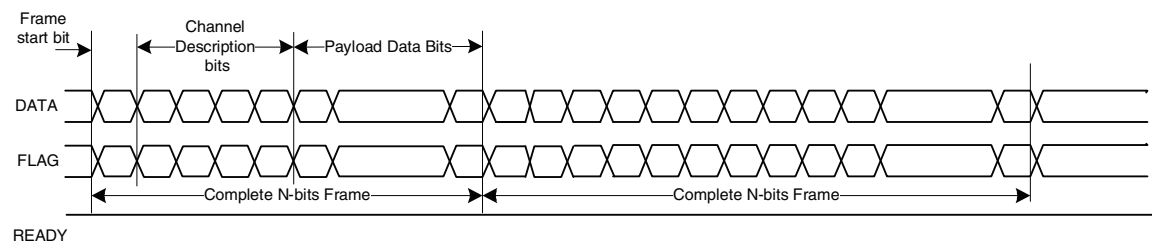


Figure 84. Frame Transmission Mode Transfer of Two Frames (Pipelined Data Flow)

4.11.13.8 DATA and FLAG Signal Timing Requirement for a 15 pF Load

Table 72. DATA and FLAG Timing

Parameter	Description	1 Mbit/s	100 Mbit/s
$t_{\text{Bit, nom}}$	Nominal bit time	1000 ns	10 ns
$t_{\text{Rise, min}}$ and $t_{\text{Fall, min}}$	Minimum allowed rise and fall time	2 ns	2 ns
$t_{\text{TxToRxSkew, max}}$	Maximum skew between transmitter and receiver package pins	50 ns	0.5 ns

Table 72. DATA and FLAG Timing (continued)

Parameter	Description	1 Mbit/s	100 Mbit/s
$t_{\text{EageSepTx, min}}$	Minimum allowed separation of signal transitions at transmitter package pins, including all timing defects, for example, jitter and skew, inside the transmitter.	400 ns	4 ns
$t_{\text{EageSepRx, min}}$	Minimum separation of signal transitions, measured at the receiver package pins, including all timing defects, for example, jitter and skew, inside the receiver.	350 ns	3.5 ns

4.11.13.9 DATA and FLAG Signal Timing

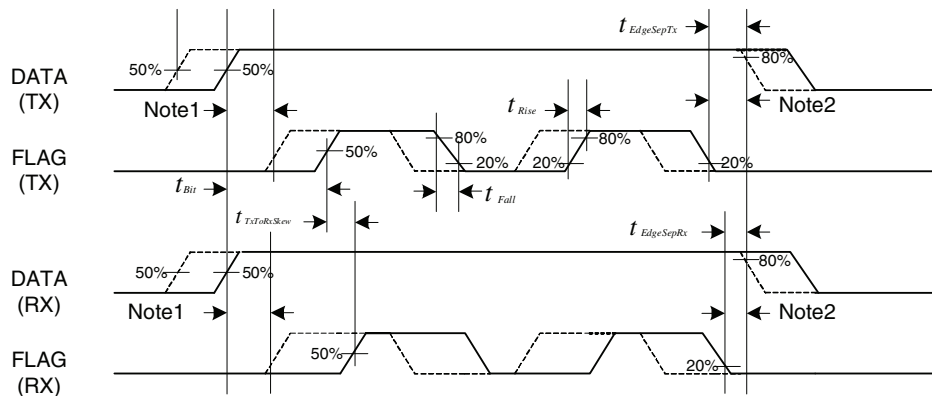


Figure 85. DATA and FLAG Signal Timing

4.11.14 PCIe PHY Parameters

The PCIe interface complies with PCIe specification Gen2 x1 lane and supports the PCI Express 1.1/2.0 standard.

4.11.14.1 PCIE_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 200 Ω . 1% precision resistor on PCIE_REXT pads to ground. It is used for termination impedance calibration.

4.11.15 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 86 depicts the timing of the PWM, and Table 73 lists the PWM timing parameters.

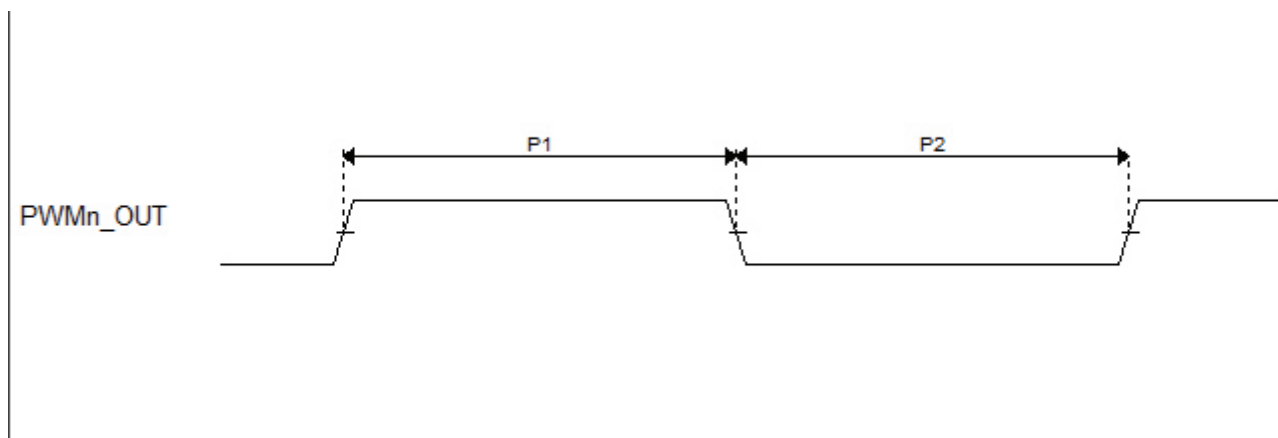


Figure 86. PWM Timing

Table 73. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	ipg_clk	MHz
P1	PWM output pulse width high	15		ns
P2	PWM output pulse width low	15		ns

4.11.16 SATA PHY Parameters

This section describes SATA PHY electrical specifications.

4.11.16.1 Transmitter and Receiver Characteristics

The SATA PHY meets or exceeds the electrical compliance requirements defined in the SATA specifications.

NOTE

The tables in the following sections indicate any exceptions to the SATA specification or aspects of the SATA PHY that exceed the standard, as well as provide information about parameters not defined in the standard.

The following subsections provide values obtained from a combination of simulations and silicon characterization.

4.11.16.1.1 SATA PHY Transmitter Characteristics

Table 74 provides specifications for SATA PHY transmitter characteristics.

Table 74. SATA2 PHY Transmitter Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Transmit common mode voltage	V_{CTM}	0.4	—	0.6	V
Transmitter pre-emphasis accuracy (measured change in de-emphasized bit)	—	−0.5	—	0.5	dB

4.11.16.1.2 SATA PHY Receiver Characteristics

Table 75 provides specifications for SATA PHY receiver characteristics.

Table 75. SATA PHY Receiver Characteristics

Parameters	Symbol	Min	Typ	Max	Unit
Minimum Rx eye height (differential peak-to-peak)	$V_{MIN_RX_EYE_HEIGHT}$	175	—	—	mV
Tolerance	PPM	−400	—	400	ppm

4.11.16.2 SATA_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 191 Ω 1% precision resistor on SATA_REXT pad to ground.

Resistor calibration consists of learning which state of the internal Resistor Calibration register causes an internal, digitally trimmed calibration resistor to best match the impedance applied to the SATA_REXT pin. The calibration register value is then supplied to all Tx and Rx termination resistors.

During the calibration process (for a few tens of microseconds), up to 0.3 mW can be dissipated in the external SATA_REXT resistor. At other times, no power is dissipated by the SATA_REXT resistor.

4.11.17 SCAN JTAG Controller (SJC) Timing Parameters

Figure 87 depicts the SJC test clock input timing. Figure 88 depicts the SJC boundary scan timing. Figure 89 depicts the SJC test access port. Signal parameters are listed in Table 76.

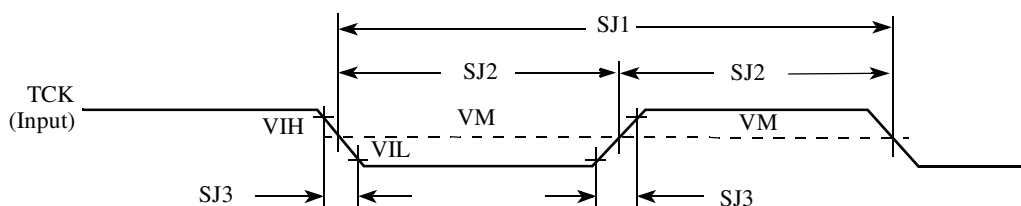


Figure 87. Test Clock Input Timing Diagram

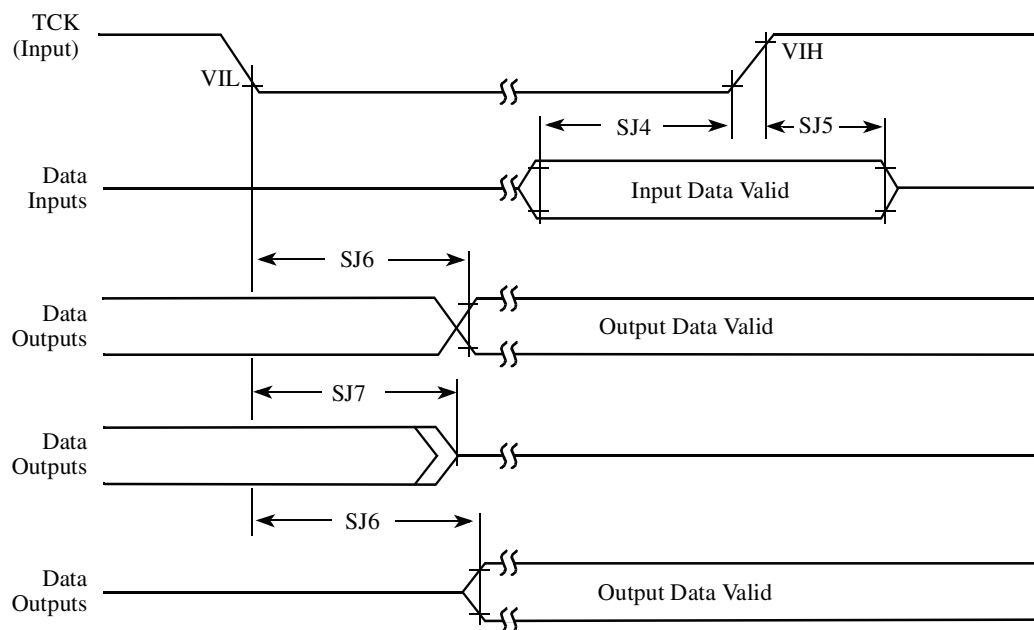


Figure 88. Boundary Scan (JTAG) Timing Diagram

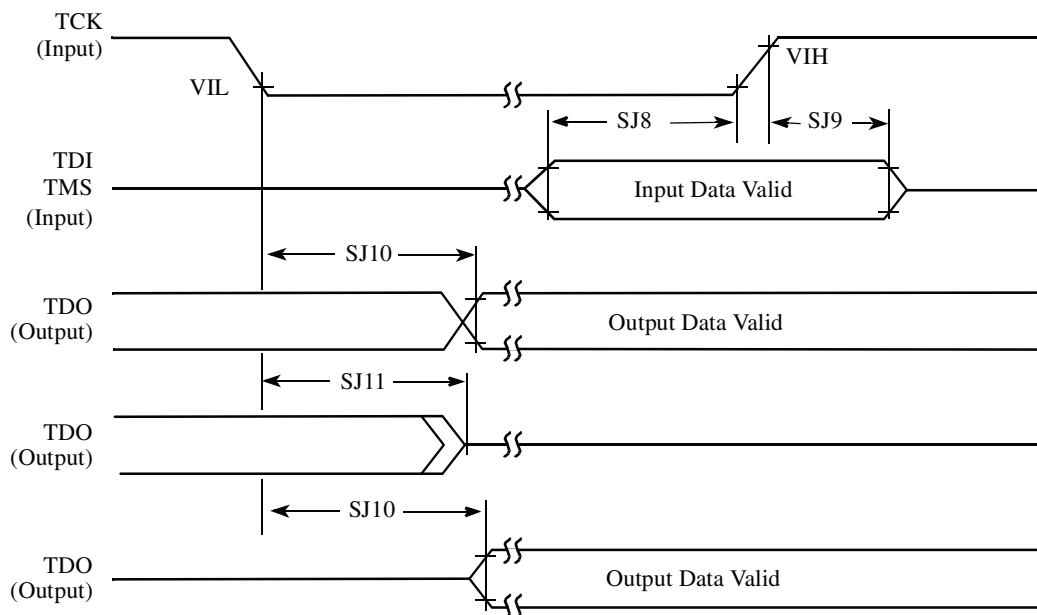


Figure 89. Test Access Port Timing Diagram

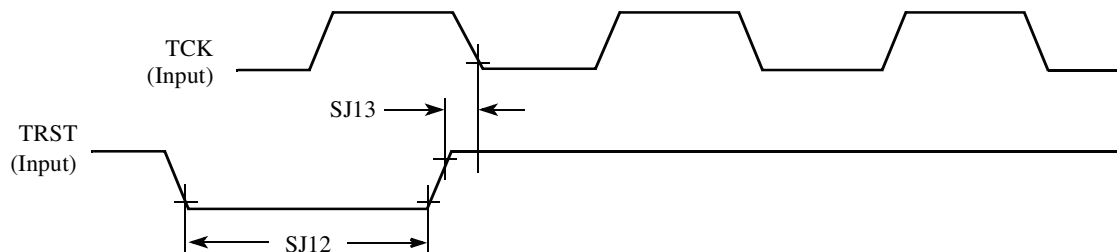
Figure 90. $\overline{\text{TRST}}$ Timing Diagram

Table 76. JTAG Timing

ID	Parameter ^{1,2}	All Frequencies		Unit
		Min	Max	
SJ0	TCK frequency of operation $1/(3 \times T_{DC})^1$	0.001	22	MHz
SJ1	TCK cycle time in crystal mode	45	—	ns
SJ2	TCK clock pulse width measured at V_M^2	22.5	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	TCK low to output data valid	—	40	ns
SJ7	TCK low to output high impedance	—	40	ns
SJ8	TMS, TDI data set-up time	5	—	ns
SJ9	TMS, TDI data hold time	25	—	ns
SJ10	TCK low to TDO data valid	—	44	ns
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

¹ T_{DC} = target frequency of SJC² V_M = mid-point voltage

4.11.18 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 77 and Figure 91 and Figure 92 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK) for SPDIF in Tx mode.

Table 77. SPDIF Timing Parameters

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIFIN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIFOUT output (Load = 50pf)	—	—	1.5	ns
• Skew	—	—	24.2	ns
• Transition rising	—	—	31.3	ns
• Transition falling	—	—	31.3	ns
SPDIFOUT1 output (Load = 30pf)	—	—	1.5	ns
• Skew	—	—	13.6	ns
• Transition rising	—	—	18.0	ns
• Transition falling	—	—	18.0	ns
Modulating Rx clock (SRCK) period	srckp	40.0	—	ns
SRCK high period	srckph	16.0	—	ns
SRCK low period	srckpl	16.0	—	ns
Modulating Tx clock (STCLK) period	stclkp	40.0	—	ns
STCLK high period	stclkph	16.0	—	ns
STCLK low period	stckpl	16.0	—	ns

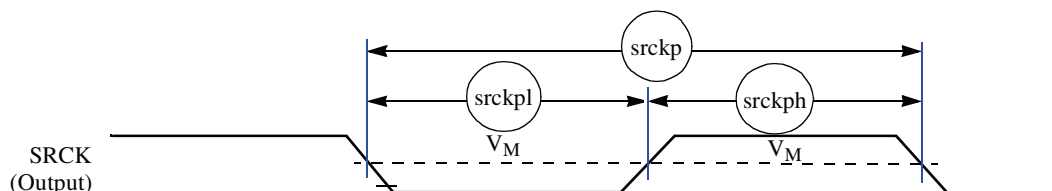


Figure 91. SRCK Timing Diagram

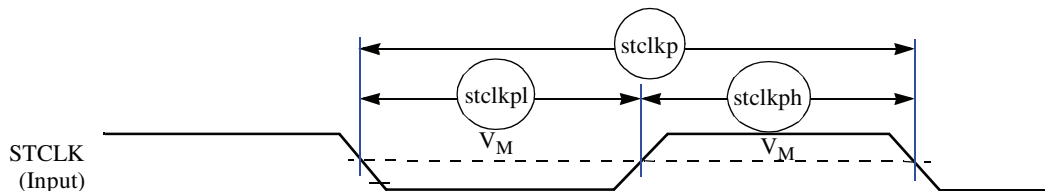


Figure 92. STCLK Timing Diagram

4.11.19 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in [Table 78](#).

Table 78. AUDMUX Port Allocation

Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External – AUD3 I/O
AUDMUX port 4	AUD4	External – EIM or CSPI1 I/O through IOMUXC
AUDMUX port 5	AUD5	External – EIM or SD1 I/O through IOMUXC
AUDMUX port 6	AUD6	External – EIM or DISP2 through IOMUXC
AUDMUX port 7	SSI 3	Internal

NOTE

- The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).
- The SSI timing diagrams use generic signal names wherein the names used in the i.MX 6Dual/6Quad reference manual are channel specific signal names. For example, a channel clock referenced in the IOMUXC chapter as AUD3_TXC appears in the timing diagram as RGMII_TXC.

4.11.19.1 SSI Transmitter Timing with Internal Clock

Figure 93 depicts the SSI transmitter internal clock timing and Table 79 lists the timing parameters for the SSI transmitter internal clock.

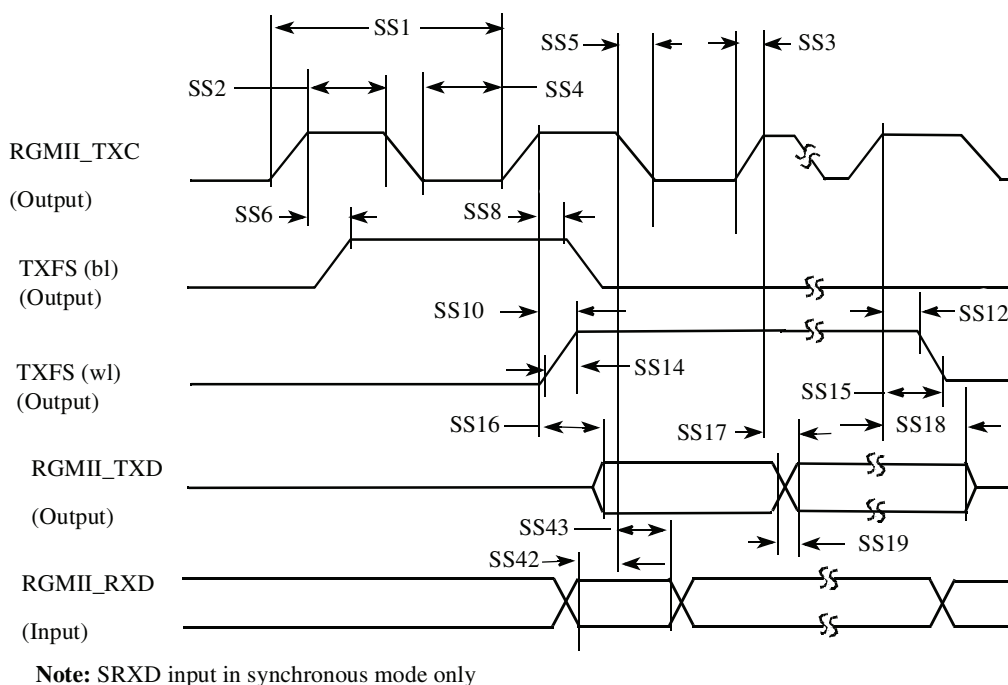


Figure 93. SSI Transmitter Internal Clock Timing Diagram

Table 79. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6.0	ns
SS15	(Tx/Rx) Internal FS fall time	—	6.0	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns

Table 79. SSI Transmitter Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.11.19.2 SSI Receiver Timing with Internal Clock

Figure 94 depicts the SSI receiver internal clock timing and Table 80 lists the timing parameters for the receiver timing with the internal clock.

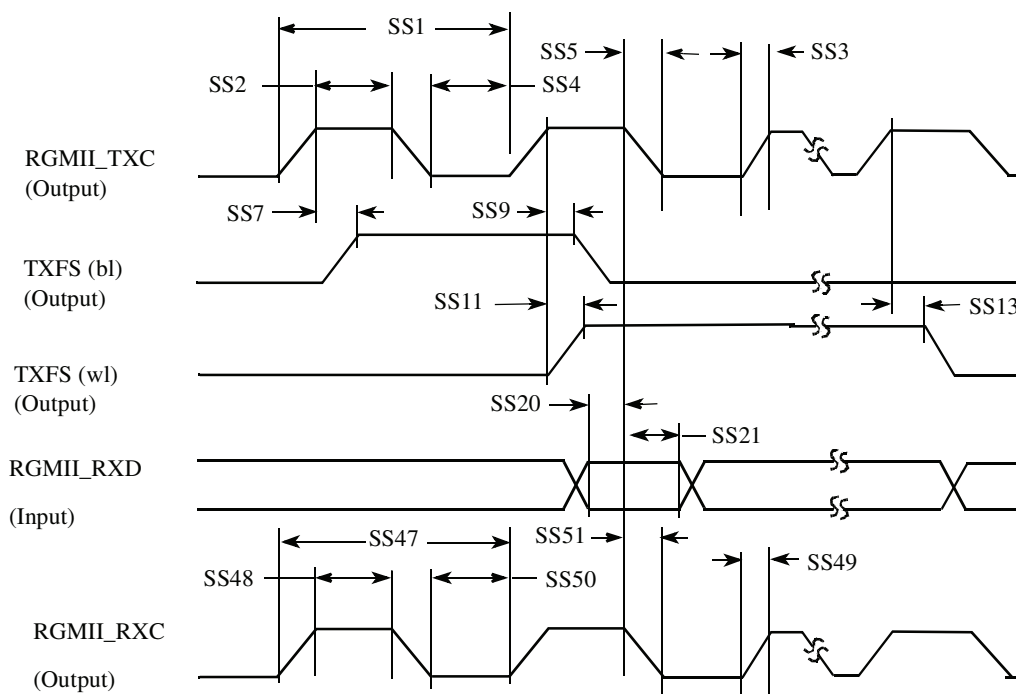


Figure 94. SSI Receiver Internal Clock Timing Diagram

Table 80. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0.0	—	ns
Oversampling Clock Operation				

Table 80. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.11.19.3 SSI Transmitter Timing with External Clock

Figure 95 depicts the SSI transmitter external clock timing and Table 81 lists the timing parameters for the transmitter timing with the external clock.

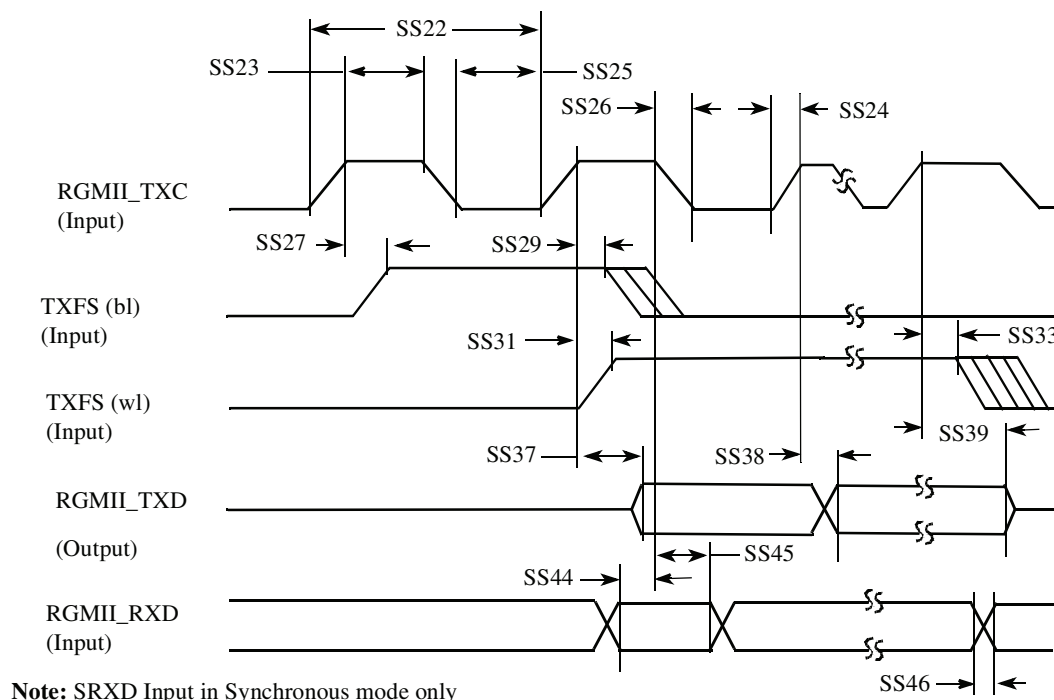


Figure 95. SSI Transmitter External Clock Timing Diagram

Table 81. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	−10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	−10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns

Table 81. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.11.19.4 SSI Receiver Timing with External Clock

Figure 96 depicts the SSI receiver external clock timing and Table 82 lists the timing parameters for the receiver timing with the external clock.

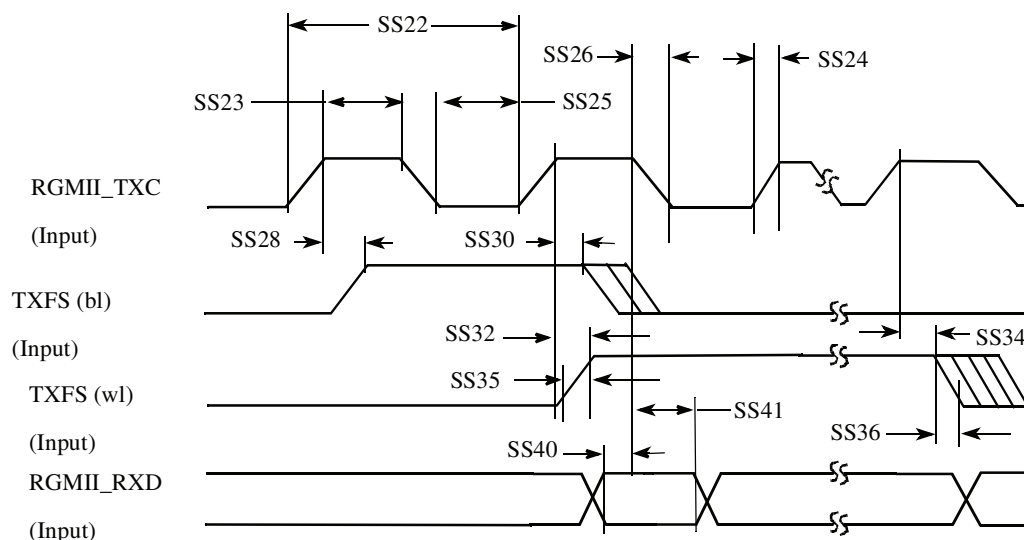


Figure 96. SSI Receiver External Clock Timing Diagram

Table 82. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	(Rx) CK high to FS (bl) high	-10	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10	—	ns
SS32	(Rx) CK high to FS (wl) high	-10	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10	—	ns
SS41	SRXD hold time after (Rx) CK low	2	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.11.20 UART I/O Configuration and Timing Parameters

4.11.20.1 UART RS-232 I/O Configuration in Different Modes

The i.MX 6Dual/6Quad UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0 – DCE mode). [Table 83](#) shows the UART I/O configuration based on the enabled mode.

Table 83. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
RTS	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
CTS	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
DTR	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
DSR	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
DCD	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
RI	Input	RING from DCE to DTE	Output	RING from DCE to DTE
TXD_MUX	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
RXD_MUX	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.11.20.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.11.20.2.1 UART Transmitter

Figure 97 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 84 lists the UART RS-232 serial mode transmit timing characteristics.

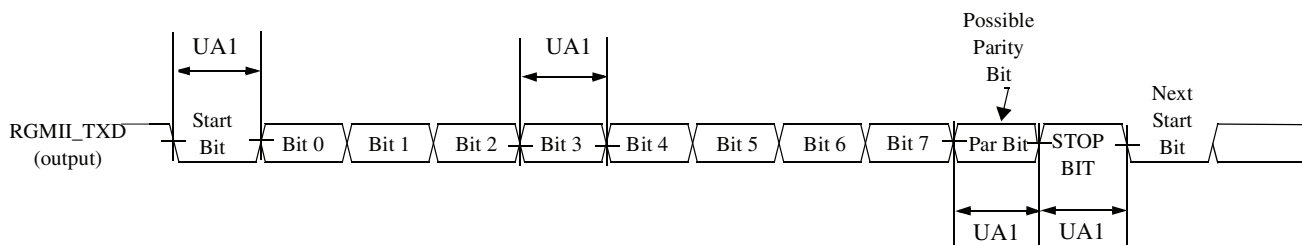


Figure 97. UART RS-232 Serial Mode Transmit Timing Diagram

Table 84. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud_rate}^1 - T_{ref_clk}^2$	$1/F_{baud_rate} + T_{ref_clk}$	—

¹ F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16.

² T_{ref_clk} : The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

4.11.20.2.2 UART Receiver

Figure 98 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 85 lists serial mode receive timing characteristics.

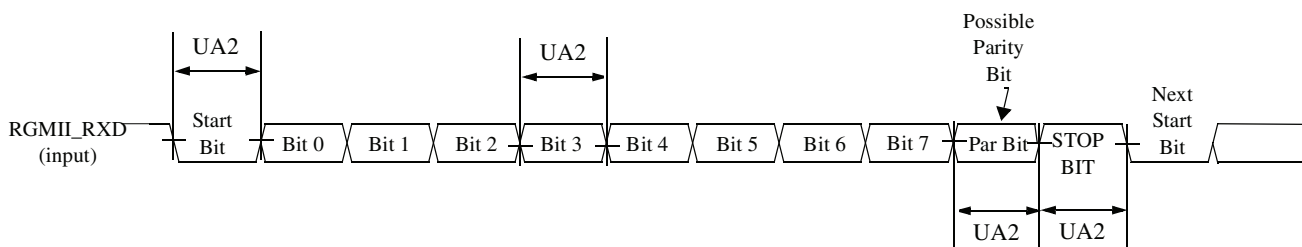


Figure 98. UART RS-232 Serial Mode Receive Timing Diagram

Table 85. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time ¹	t_{Rbit}	$1/F_{baud_rate}^2 - 1/(16 \cdot F_{baud_rate})$	$1/F_{baud_rate} + 1/(16 \cdot F_{baud_rate})$	—

¹ The UART receiver can tolerate $1/(16 \cdot F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \cdot F_{baud_rate})$.

² F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16.

4.11.20.2.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 99 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 86 lists the transmit timing characteristics.

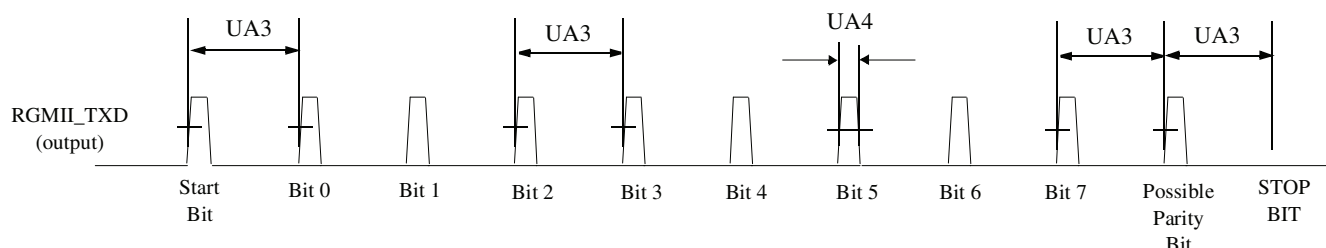


Figure 99. UART IrDA Mode Transmit Timing Diagram

Table 86. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud_rate}^1 - T_{ref_clk}^2$	$1/F_{baud_rate} + T_{ref_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16)*(1/F_{baud_rate}) - T_{ref_clk}$	$(3/16)*(1/F_{baud_rate}) + T_{ref_clk}$	—

¹ F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16.

² T_{ref_clk} : The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

UART IrDA Mode Receiver

Figure 100 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 87 lists the receive timing characteristics.

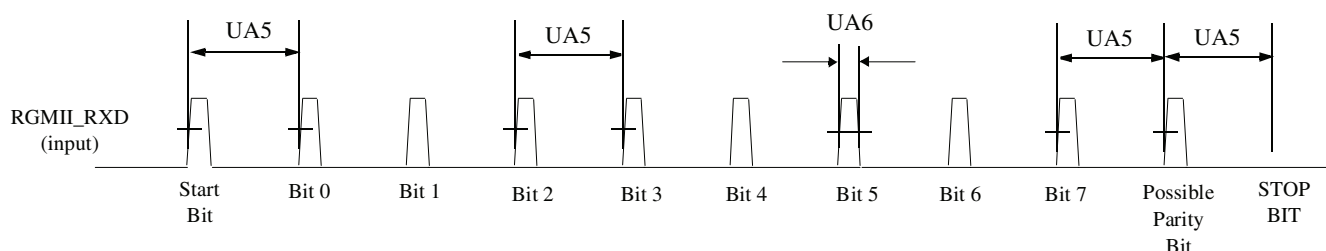


Figure 100. UART IrDA Mode Receive Timing Diagram

Table 87. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time ¹ in IrDA mode	t_{RIRbit}	$1/F_{baud_rate}^2 - 1/(16*F_{baud_rate})$	$1/F_{baud_rate} + 1/(16*F_{baud_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 μs	$(5/16)*(1/F_{baud_rate})$	—

¹ The UART receiver can tolerate $1/(16*F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16*F_{baud_rate})$.

² F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16.

4.11.21 USB HSIC Timings

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is a DDR signal. The following timing specification is for both rising and falling edges.

4.11.21.1 Transmit Timing

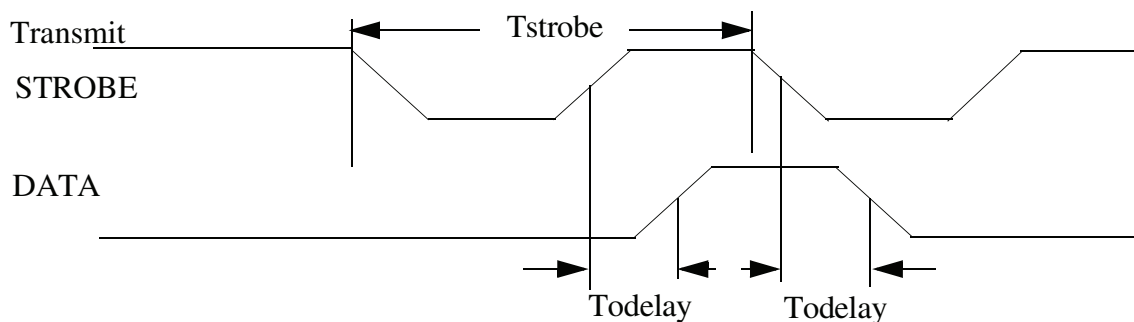


Figure 101. USB HSIC Transmit Waveform

Table 88. USB HSIC Transmit Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	
Todelay	data output delay time	550	1350	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

4.11.21.2 Receive Timing

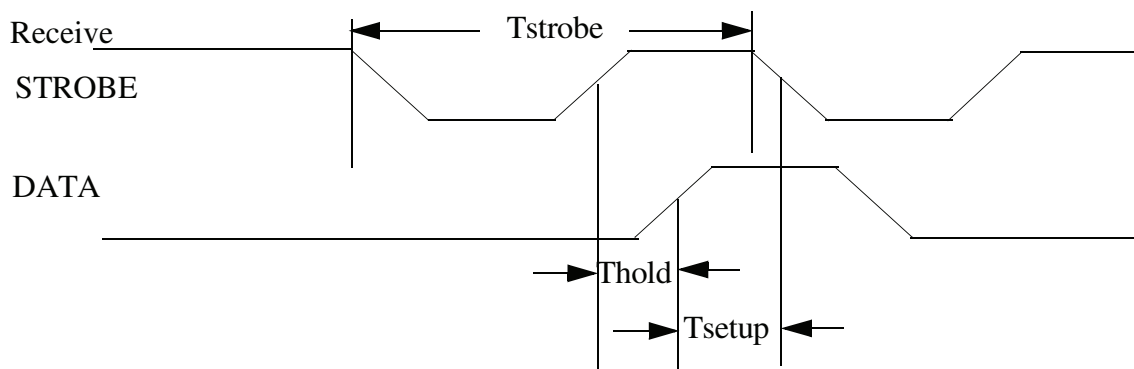


Figure 102. USB HSIC Receive Waveform

Table 89. USB HSIC Receive Parameters¹

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	
Thold	data hold time	300		ps	Measured at 50% point
Tsetup	data setup time	365		ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

¹ The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.11.22 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below ([On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification](#) is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
 - Title: 5V Short Circuit Withstand Requirement Change
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
 - Title: Pull-up/Pull-down resistors
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
 - Title: Suspend Current Limit Changes
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
 - Title: USB 2.0 Phase Locked SOFs
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
 - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
 - Revision 1.2, December 7, 2010

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 90 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6Dual/6Quad Fuse Map document and the System Boot chapter of the i.MX 6Dual/6Quad reference manual.

Table 90. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	eFuse Name	Details
BOOT_MODE1	Input	Boot Mode Selection	Boot Mode selection
BOOT_MODE0	Input	Boot Mode Selection	Boot Mode Selection

Table 90. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name	Details
EIM_DA0	Input	BOOT_CFG1[0]	Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
EIM_DA1	Input	BOOT_CFG1[1]	
EIM_DA2	Input	BOOT_CFG1[2]	
EIM_DA3	Input	BOOT_CFG1[3]	
EIM_DA4	Input	BOOT_CFG1[4]	
EIM_DA5	Input	BOOT_CFG1[5]	
EIM_DA6	Input	BOOT_CFG1[6]	
EIM_DA7	Input	BOOT_CFG1[7]	
EIM_DA8	Input	BOOT_CFG2[0]	
EIM_DA9	Input	BOOT_CFG2[1]	
EIM_DA10	Input	BOOT_CFG2[2]	
EIM_DA11	Input	BOOT_CFG2[3]	
EIM_DA12	Input	BOOT_CFG2[4]	
EIM_DA13	Input	BOOT_CFG2[5]	
EIM_DA14	Input	BOOT_CFG2[6]	
EIM_DA15	Input	BOOT_CFG2[7]	
EIM_A16	Input	BOOT_CFG3[0]	
EIM_A17	Input	BOOT_CFG3[1]	
EIM_A18	Input	BOOT_CFG3[2]	
EIM_A19	Input	BOOT_CFG3[3]	
EIM_A20	Input	BOOT_CFG3[4]	
EIM_A21	Input	BOOT_CFG3[5]	
EIM_A22	Input	BOOT_CFG3[6]	
EIM_A23	Input	BOOT_CFG3[7]	
EIM_A24	Input	BOOT_CFG4[0]	
EIM_WAIT	Input	BOOT_CFG4[1]	
EIM_LBA	Input	BOOT_CFG4[2]	
EIM_EB0	Input	BOOT_CFG4[3]	
EIM_EB1	Input	BOOT_CFG4[4]	
EIM_RW	Input	BOOT_CFG4[5]	
EIM_EB2	Input	BOOT_CFG4[6]	
EIM_EB3	Input	BOOT_CFG4[7]	

5.2 Boot Devices Interfaces Allocation

Table 91 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 91. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-1	EIM_D17, EIM_D18, EIM_D16, EIM_EB2, EIM_D19, EIM_D24, EIM_D25	
SPI	ECSPI-2	CSIO_DAT10, CSIO_DAT9, CSIO_DAT8, CSIO_DAT11, EIM_LBA, EIM_D24, EIM_D25	
SPI	ECSPI-3	DISP0_DAT2, DISP0_DAT1, DISP0_DAT0, DISP0_DAT3, DISP0_DAT4, DISP0_DAT5, DISP0_DAT6	
SPI	ECSPI-4	EIM_D22, EIM_D28, EIM_D21, EIM_D20, EIM_A25, EIM_D24, EIM_D25	
SPI	ECSPI-5	SD1_DAT0, SD1_CMD, SD1_CLK, SD1_DAT1, SD1_DAT2, SD1_DAT3, SD2_DAT3	
EIM	EIM	EIM_DA[15:0], EIM_D[31:16], CSIO_DAT[19:4], CSIO_DATA_EN, CSIO_VSYNC	Used for NOR, OneNAND boot Only CS0 is supported
NAND Flash	GPMI	NANDF_CLE, NANDF_ALE, NANDF_WP_B, SD4_CMD, SD4_CLK, NANDF_RB0, SD4_DAT0, NANDF_CS0, NANDF_CS1, NANDF_CS2, NANDF_CS3, NANDF_D[7:0]	8 bit Only CS0 is supported
SD/MMC	USDHC-1	SD1_CLK, SD1_CMD, SD1_DAT0, SD1_DAT1, SD1_DAT2, SD1_DAT3, NANDF_D0, NANDF_D1, NANDF_D2, NANDF_D3, KEY_COL1	1, 4, or 8 bit
SD/MMC	USDHC-2	SD2_CLK, SD2_CMD, SD2_DAT0, SD2_DAT1, SD2_DAT2, SD2_DAT3, NANDF_D5, NANDF_D6, NANDF_D7, NANDF_D8, KEY_ROW1	1, 4, or 8 bit
SD/MMC	USDHC-3	SD3_CLK, SD3_CMD, SD3_DAT0, SD3_DAT1, SD3_DAT2, SD3_DAT3, SD3_DAT4, SD3_DAT5, SD3_DAT6, SD3_DAT7, GPIO_18	1, 4, or 8 bit
SD/MMC	USDHC-4	SD4_CLK, SD4_CMD, SD4_DAT0, SD4_DAT1, SD4_DAT2, SD4_DAT3, SD4_DAT4, SD4_DAT5, SD4_DAT6, SD4_DAT7, NANDF_CS1	1, 4, or 8 bit
I2C	I2C-1	EIM_D28, EIM_D21	—
I2C	I2C-2	EIM_D16, EIM_EB2	—
I2C	I2C-3	EIM_D18, EIM_D17	—
SATA	SATA_PHY	SATA_TXM, SATA_TXP, SATA_RXP, SATA_RXM, SATA_REXT, SATA_REFCLKM, SATA_REFCLKP	—
USB	USB-OTG PHY	USB_OTG_DP USB_OTG_DN USB_OTG_VBUS	—

6 Package Information and Contact Assignments

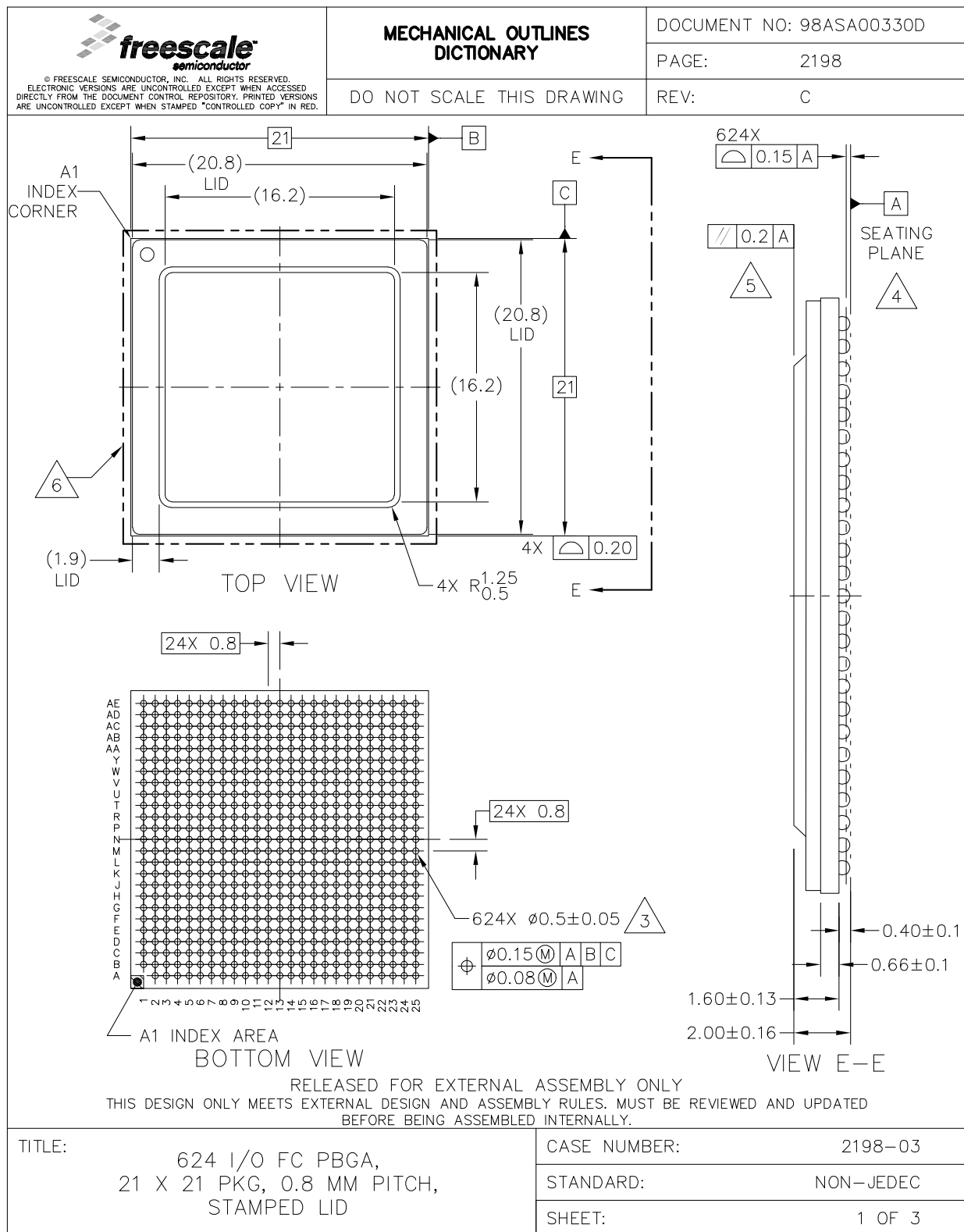
This section includes the contact assignment information and mechanical package drawing.

6.1 21 x 21 mm Package Information

6.1.1 Case FCPBGA, 21 x 21 mm, 0.8 mm Pitch, 25 x 25 Ball Matrix

6.1.1.1 21 x 21 mm Lidded Package

Figure 103 shows the top, bottom, and side views of the 21 × 21 mm lidded package.




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		PAGE: 2198
	DO NOT SCALE THIS DRAWING	REV: C
<p>NOTES:</p> <ol style="list-style-type: none"> ALL DIMENSIONS IN MILLIMETERS. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE. 29.2MM MAXIMUM PACKAGE ASSEMBLY (LID + LAMINATE) X AND Y. 		
TITLE: 624 I/O FC PBGA, 21 X 21 PKG, 0.8 MM PITCH, STAMPED LID		CASE NUMBER: 2198–03
		STANDARD: NON–JEDEC
		SHEET: 2

Figure 103. 21 x 21 mm Lidded Package Top, Bottom, and Side Views

6.1.2 21 x 21 mm Ground, Power, Sense, and Reference Contact Assignments

Table 92 shows the device connection list for ground, power, sense, and reference contact signals.

Table 92. 21 x 21 mm Supplies Contact Assignment

Supply Rail Name	Ball(s) Position(s)	Remark
CSI_REXT	D4	
DRAM_VREF	AC2	
DSI_REXT	G4	
FA_ANA	A5	
GND	A13, A25, A4, A8, AA10, AA13, AA16, AA19, AA22, AD4, D3, F8, J15, L10, M15, P15, T15, U8, W17, AA7, AD7, D6, G10, J18, L12, M18, P18, T17, V19, W18, AB24, AE1, D8, G19, J2, L15, M8, P8, T19, V8, W19, AB3, AE25, E5, G3, J8, L18, N10, R12, T8, W10, W3, AD10, B4, E6, H12, K10, L2, N15, R15, U11, W11, W7, AD13, C1, E7, H15, K12, L5, N18, R17, U12, W12, W8, AD16, C10, F5, H18, K15, L8, N8, R8, U15, W13, W9, AD19, C4, F6, H8, K18, M10, P10, T11, U17, W15, Y24, AD22, C6, F7, J12, K8, M12, P12, T12, U19, W16, Y5	
GPANAIO	C8	
HDMI_REF	J1	
HDMI_VP	L7	
HDMI_VPH	M7	
NVCC_CSI	N7	Supply of the camera sensor interface
NVCC_DRAM	R18, T18, U18, V10, V11, V12, V13, V14, V15, V16, V17, V18, V9	Supply of the DDR interface
NVCC_EIM0	K19	Supply of the EIM interface
NVCC_EIM1	L19	Supply of the EIM interface
NVCC_EIM2	M19	Supply of the EIM interface
NVCC_ENET	R19	Supply of the ENET interface
NVCC_GPIO	P7	Supply of the GPIO interface
NVCC_JTAG	J7	Supply of the JTAG tap controller interface
NVCC_LCD	P19	Supply of the LCD interface
NVCC_LVDS2P5	V7	Supply of the LVDS display interface and DDR pre-drivers. Even if the LVDS interface is not used, this supply must remain powered.
NVCC_MIPI	K7	Supply of the MIPI interface

Table 92. 21 x 21 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
NVCC_NANDF	G15	Supply of the RAW NAND Flash Memories interface
NVCC_PLL_OUT	E8	
NVCC_RGMII	G18	Supply of the ENET interface
NVCC_SD1	G16	Supply of the SD card interface
NVCC_SD2	G17	Supply of the SD card interface
NVCC_SD3	G14	Supply of the SD card interface
PCIE_VP	H7	
PCIE_REXT	A2	
PCIE_VPH	G7	PCI PHY supply
PCIE_VPTX	G8	PCI PHY supply
SATA_REXT	C14	
SATA_VP	G13	
SATA_VPH	G12	
VDD_CACHE_CAP	N12	Cache supply input. This input should be connected to (driven by) VDD_SOC_CAP. The external capacitor used for VDD_SOC_CAP is sufficient for this supply.
VDD_FA	B5	
VDD_SNVS_CAP	G9	Secondary supply for the SNVS (internal regulator output—requires capacitor if internal regulator is used)
VDD_SNVS_IN	G11	Primary supply for the SNVS regulator
VDDARM_CAP	H13, J13, K13, L13, M13, N13, P13, R13	Secondary supply for the ARM0 and ARM1 cores (internal regulator output—requires capacitor if internal regulator is used)
VDDARM_IN	H14, J14, K14, L14, M14, N14, P14, R14	Primary supply for the ARM0 and ARM1 core regulator
VDDARM23_CAP	H11, J11, K11, L11, M11, N11, P11, R11	Secondary supply for the ARM2 and ARM3 cores (internal regulator output—requires capacitor if internal regulator is used)
VDDARM23_IN	K9, L9, M9, N9, P9, R9, T9, U9	Primary supply for the ARM2 and ARM3 core regulator
VDDHIGH_CAP	H10, J10	Secondary supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)

Table 92. 21 x 21 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
VDDHIGH_IN	H9, J9	Primary supply for the 2.5 V regulator
VDDPU_CAP	H17, J17, K17, L17, M17, N17, P17	Secondary supply for the VPU and GPU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_CAP	R10, T10, T13, T14, U10, U13, U14	Secondary supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_IN	H16, J16, K16, L16, M16, N16, P16, R16, T16, U16	Primary supply for the SoC and PU regulators
VDDUSB_CAP	F9	Secondary supply for the 3 V domain (internal regulator output—requires capacitor if internal regulator is used)
ZQPAD	AE17	

Table 93 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 93. 21 x 21 mm Functional Contact Assignments

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
BOOT_MODE0	C12	VDD_SNVS_IN	GPIO	ALT0	src_BOOT_MODE[0]	Input	PD (100K)
BOOT_MODE1	F12	VDD_SNVS_IN	GPIO	ALT0	src_BOOT_MODE[1]	Input	PD (100K)
CLK1_N	C7	VDDHIGH_CAP			CLK1_N	—	—
CLK1_P	D7	VDDHIGH_CAP			CLK1_P	—	—
CLK2_N	C5	VDDHIGH_CAP			CLK2_N	—	—
CLK2_P	D5	VDDHIGH_CAP			CLK2_P	—	—
CSI_CLK0M	F4	NVCC_MIPI			CSI_CLK0M	—	—
CSI_CLK0P	F3	NVCC_MIPI			CSI_CLK0P	—	—
CSI_D0M	E4	NVCC_MIPI			CSI_D0M	—	—
CSI_D0P	E3	NVCC_MIPI			CSI_D0P	—	—
CSI_D1M	D1	NVCC_MIPI			CSI_D1M	—	—
CSI_D1P	D2	NVCC_MIPI			CSI_D1P	—	—
CSI_D2M	E1	NVCC_MIPI			CSI_D2M	—	—
CSI_D2P	E2	NVCC_MIPI			CSI_D2P	—	—
CSI_D3M	F2	NVCC_MIPI			CSI_D3M	—	—

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
CSI_D3P	F1	NVCC_MIPI			CSI_D3P	—	—
CSI0_DAT10	M1	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[28]	Input	PU (100K)
CSI0_DAT11	M3	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[29]	Input	PU (100K)
CSI0_DAT12	M2	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[30]	Input	PU (100K)
CSI0_DAT13	L1	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[31]	Input	PU (100K)
CSI0_DAT14	M4	NVCC_CSI	GPIO	ALT5	gpio6_GPIO[0]	Input	PU (100K)
CSI0_DAT15	M5	NVCC_CSI	GPIO	ALT5	gpio6_GPIO[1]	Input	PU (100K)
CSI0_DAT16	L4	NVCC_CSI	GPIO	ALT5	gpio6_GPIO[2]	Input	PU (100K)
CSI0_DAT17	L3	NVCC_CSI	GPIO	ALT5	gpio6_GPIO[3]	Input	PU (100K)
CSI0_DAT18	M6	NVCC_CSI	GPIO	ALT5	gpio6_GPIO[4]	Input	PU (100K)
CSI0_DAT19	L6	NVCC_CSI	GPIO	ALT5	gpio6_GPIO[5]	Input	PU (100K)
CSI0_DAT4	N1	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[22]	Input	PU (100K)
CSI0_DAT5	P2	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[23]	Input	PU (100K)
CSI0_DAT6	N4	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[24]	Input	PU (100K)
CSI0_DAT7	N3	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[25]	Input	PU (100K)
CSI0_DAT8	N6	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[26]	Input	PU (100K)
CSI0_DAT9	N5	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[27]	Input	PU (100K)
CSI0_DATA_EN	P3	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[20]	Input	PU (100K)
CSI0_MCLK	P4	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[19]	Input	PU (100K)
CSI0_PIXCLK	P1	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[18]	Input	PU (100K)
CSI0_VSYNC	N2	NVCC_CSI	GPIO	ALT5	gpio5_GPIO[21]	Input	PU (100K)
DI0_DISP_CLK	N19	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[16]	Input	PU (100K)
DI0_PIN15	N21	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[17]	Input	PU (100K)
DI0_PIN2	N25	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[18]	Input	PU (100K)
DI0_PIN3	N20	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[19]	Input	PU (100K)
DI0_PIN4	P25	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[20]	Input	PU (100K)
DISP0_DAT0	P24	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[21]	Input	PU (100K)
DISP0_DAT1	P22	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[22]	Input	PU (100K)
DISP0_DAT10	R21	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[31]	Input	PU (100K)
DISP0_DAT11	T23	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[5]	Input	PU (100K)

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DISP0_DAT12	T24	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[6]	Input	PU (100K)
DISP0_DAT13	R20	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[7]	Input	PU (100K)
DISP0_DAT14	U25	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[8]	Input	PU (100K)
DISP0_DAT15	T22	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[9]	Input	PU (100K)
DISP0_DAT16	T21	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[10]	Input	PU (100K)
DISP0_DAT17	U24	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[11]	Input	PU (100K)
DISP0_DAT18	V25	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[12]	Input	PU (100K)
DISP0_DAT19	U23	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[13]	Input	PU (100K)
DISP0_DAT2	P23	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[23]	Input	PU (100K)
DISP0_DAT20	U22	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[14]	Input	PU (100K)
DISP0_DAT21	T20	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[15]	Input	PU (100K)
DISP0_DAT22	V24	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[16]	Input	PU (100K)
DISP0_DAT23	W24	NVCC_LCD	GPIO	ALT5	gpio5_GPIO[17]	Input	PU (100K)
DISP0_DAT3	P21	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[24]	Input	PU (100K)
DISP0_DAT4	P20	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[25]	Input	PU (100K)
DISP0_DAT5	R25	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[26]	Input	PU (100K)
DISP0_DAT6	R23	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[27]	Input	PU (100K)
DISP0_DAT7	R24	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[28]	Input	PU (100K)
DISP0_DAT8	R22	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[29]	Input	PU (100K)
DISP0_DAT9	T25	NVCC_LCD	GPIO	ALT5	gpio4_GPIO[30]	Input	PU (100K)
DRAM_A0	AC14	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[0]	Output	0
DRAM_A1	AB14	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[1]	Output	0
DRAM_A10	AA15	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[10]	Output	0
DRAM_A11	AC12	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[11]	Output	0
DRAM_A12	AD12	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[12]	Output	0
DRAM_A13	AC17	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[13]	Output	0
DRAM_A14	AA12	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[14]	Output	0
DRAM_A15	Y12	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[15]	Output	0
DRAM_A2	AA14	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[2]	Output	0
DRAM_A3	Y14	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[3]	Output	0

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DRAM_A4	W14	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[4]	Output	0
DRAM_A5	AE13	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[5]	Output	0
DRAM_A6	AC13	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[6]	Output	0
DRAM_A7	Y13	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[7]	Output	0
DRAM_A8	AB13	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[8]	Output	0
DRAM_A9	AE12	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_A[9]	Output	0
DRAM_CAS	AE16	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CAS	Output	0
DRAM_CS0	Y16	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CS[0]	Output	0
DRAM_CS1	AD17	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_CS[1]	Output	0
DRAM_D0	AD2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[0]	Input	PU (100K)
DRAM_D1	AE2	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[1]	Input	PU (100K)
DRAM_D10	AA6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[10]	Input	PU (100K)
DRAM_D11	AE7	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[11]	Input	PU (100K)
DRAM_D12	AB5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[12]	Input	PU (100K)
DRAM_D13	AC5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[13]	Input	PU (100K)
DRAM_D14	AB6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[14]	Input	PU (100K)
DRAM_D15	AC7	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[15]	Input	PU (100K)
DRAM_D16	AB7	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[16]	Input	PU (100K)
DRAM_D17	AA8	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[17]	Input	PU (100K)
DRAM_D18	AB9	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[18]	Input	PU (100K)
DRAM_D19	Y9	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[19]	Input	PU (100K)
DRAM_D2	AC4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[2]	Input	PU (100K)
DRAM_D20	Y7	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[20]	Input	PU (100K)
DRAM_D21	Y8	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[21]	Input	PU (100K)
DRAM_D22	AC8	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[22]	Input	PU (100K)
DRAM_D23	AA9	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[23]	Input	PU (100K)
DRAM_D24	AE9	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[24]	Input	PU (100K)
DRAM_D25	Y10	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[25]	Input	PU (100K)
DRAM_D26	AE11	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[26]	Input	PU (100K)
DRAM_D27	AB11	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[27]	Input	PU (100K)

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DRAM_D28	AC9	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[28]	Input	PU (100K)
DRAM_D29	AD9	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[29]	Input	PU (100K)
DRAM_D3	AA5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[3]	Input	PU (100K)
DRAM_D30	AD11	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[30]	Input	PU (100K)
DRAM_D31	AC11	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[31]	Input	PU (100K)
DRAM_D32	AA17	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[32]	Input	PU (100K)
DRAM_D33	AA18	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[33]	Input	PU (100K)
DRAM_D34	AC18	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[34]	Input	PU (100K)
DRAM_D35	AE19	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[35]	Input	PU (100K)
DRAM_D36	Y17	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[36]	Input	PU (100K)
DRAM_D37	Y18	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[37]	Input	PU (100K)
DRAM_D38	AB19	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[38]	Input	PU (100K)
DRAM_D39	AC19	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[39]	Input	PU (100K)
DRAM_D4	AC1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[4]	Input	PU (100K)
DRAM_D40	Y19	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[40]	Input	PU (100K)
DRAM_D41	AB20	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[41]	Input	PU (100K)
DRAM_D42	AB21	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[42]	Input	PU (100K)
DRAM_D43	AD21	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[43]	Input	PU (100K)
DRAM_D44	Y20	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[44]	Input	PU (100K)
DRAM_D45	AA20	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[45]	Input	PU (100K)
DRAM_D46	AE21	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[46]	Input	PU (100K)
DRAM_D47	AC21	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[47]	Input	PU (100K)
DRAM_D48	AC22	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[48]	Input	PU (100K)
DRAM_D49	AE22	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[49]	Input	PU (100K)
DRAM_D5	AD1	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[5]	Input	PU (100K)
DRAM_D50	AE24	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[50]	Input	PU (100K)
DRAM_D51	AC24	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[51]	Input	PU (100K)
DRAM_D52	AB22	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[52]	Input	PU (100K)
DRAM_D53	AC23	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[53]	Input	PU (100K)
DRAM_D54	AD25	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[54]	Input	PU (100K)

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DRAM_D55	AC25	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[55]	Input	PU (100K)
DRAM_D56	AB25	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[56]	Input	PU (100K)
DRAM_D57	AA21	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[57]	Input	PU (100K)
DRAM_D58	Y25	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[58]	Input	PU (100K)
DRAM_D59	Y22	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[59]	Input	PU (100K)
DRAM_D6	AB4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[6]	Input	PU (100K)
DRAM_D60	AB23	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[60]	Input	PU (100K)
DRAM_D61	AA23	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[61]	Input	PU (100K)
DRAM_D62	Y23	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[62]	Input	PU (100K)
DRAM_D63	W25	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[63]	Input	PU (100K)
DRAM_D7	AE4	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[7]	Input	PU (100K)
DRAM_D8	AD5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[8]	Input	PU (100K)
DRAM_D9	AE5	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_D[9]	Input	PU (100K)
DRAM_DQM0	AC3	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[0]	Output	0
DRAM_DQM1	AC6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[1]	Output	0
DRAM_DQM2	AB8	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[2]	Output	0
DRAM_DQM3	AE10	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[3]	Output	0
DRAM_DQM4	AB18	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[4]	Output	0
DRAM_DQM5	AC20	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[5]	Output	0
DRAM_DQM6	AD24	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[6]	Output	0
DRAM_DQM7	Y21	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_DQM[7]	Output	0
DRAM_RAS	AB15	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_RAS	Output	0
DRAM_RESET	Y6	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_RESET	Output	0
DRAM_SDBA0	AC15	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDBA[0]	Output	0
DRAM_SDBA1	Y15	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDBA[1]	Output	0
DRAM_SDBA2	AB12	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDBA[2]	Output	0
DRAM_SDCKE0	Y11	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDCKE[0]	Output	0
DRAM_SDCKE1	AA11	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDCKE[1]	Output	0
DRAM_SDCLK_0	AD15	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDCLK0	Input	Hi-Z
DRAM_SDCLK_0_B	AE15	NVCC_DRAM	DDRCLK		DRAM_SDCLK_0_B	—	—

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DRAM_SDCLK_1	AD14	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDCLK1	Input	Hi-Z
DRAM_SDCLK_1_B	AE14	NVCC_DRAM	DDRCLK		DRAM_SDCLK_1_B	—	—
DRAM_SDOT0	AC16	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_ODT[0]	Output	0
DRAM_SDOT1	AB17	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_ODT[1]	Output	0
DRAM_SDQS0	AE3	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[0]	Input	Hi-Z
DRAM_SDQS0_B	AD3	NVCC_DRAM	DDRCLK		DRAM_SDQS0_B	—	—
DRAM_SDQS1	AD6	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[1]	Input	Hi-Z
DRAM_SDQS1_B	AE6	NVCC_DRAM	DDRCLK		DRAM_SDQS1_B	—	—
DRAM_SDQS2	AD8	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[2]	Input	Hi-Z
DRAM_SDQS2_B	AE8	NVCC_DRAM	DDRCLK		DRAM_SDQS2_B	—	—
DRAM_SDQS3	AC10	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[3]	Input	Hi-Z
DRAM_SDQS3_B	AB10	NVCC_DRAM	DDRCLK		DRAM_SDQS3_B	—	—
DRAM_SDQS4	AD18	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[4]	Input	Hi-Z
DRAM_SDQS4_B	AE18	NVCC_DRAM	DDRCLK		DRAM_SDQS4_B	—	—
DRAM_SDQS5	AD20	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[5]	Input	Hi-Z
DRAM_SDQS5_B	AE20	NVCC_DRAM	DDRCLK		DRAM_SDQS5_B	—	—
DRAM_SDQS6	AD23	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[6]	Input	Hi-Z
DRAM_SDQS6_B	AE23	NVCC_DRAM	DDRCLK		DRAM_SDQS6_B	—	—
DRAM_SDQS7	AA25	NVCC_DRAM	DDRCLK	ALT0	mmdc_DRAM_SDQS[7]	Input	Hi-Z
DRAM_SDQS7_B	AA24	NVCC_DRAM	DDRCLK		DRAM_SDQS7_B	—	—
DRAM_SDWE	AB16	NVCC_DRAM	DDR	ALT0	mmdc_DRAM_SDWE	Output	0
DSI_CLK0M	H3	NVCC_MIPI			DSI_CLK0M	—	—
DSI_CLK0P	H4	NVCC_MIPI			DSI_CLK0P	—	—
DSI_D0M	G2	NVCC_MIPI			DSI_D0M	—	—
DSI_D0P	G1	NVCC_MIPI			DSI_D0P	—	—
DSI_D1M	H2	NVCC_MIPI			DSI_D1M	—	—
DSI_D1P	H1	NVCC_MIPI			DSI_D1P	—	—
EIM_A16	H25	NVCC_EIM1	GPIO	ALT0	eim_EIM_A[16]	Output	0
EIM_A17	G24	NVCC_EIM1	GPIO	ALT0	eim_EIM_A[17]	Output	0
EIM_A18	J22	NVCC_EIM1	GPIO	ALT0	eim_EIM_A[18]	Output	0

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
EIM_A19	G25	NVCC_EIM1	GPIO	ALT0	eim_EIM_A[19]	Output	0
EIM_A20	H22	NVCC_EIM1	GPIO	ALT0	eim_EIM_A[20]	Output	0
EIM_A21	H23	NVCC_EIM1	GPIO	ALT0	eim_EIM_A[21]	Output	0
EIM_A22	F24	NVCC_EIM1	GPIO	ALT0	eim_EIM_A[22]	Output	0
EIM_A23	J21	NVCC_EIM1	GPIO	ALT0	eim_EIM_A[23]	Output	0
EIM_A24	F25	NVCC_EIM1	GPIO	ALT0	eim_EIM_A[24]	Output	0
EIM_A25	H19	NVCC_EIM0	GPIO	ALT0	eim_EIM_A[25]	Output	0
EIM_BCLK	N22	NVCC_EIM2	GPIO	ALT0	eim_EIM_BCLK	Output	0
EIM_CS0	H24	NVCC_EIM1	GPIO	ALT0	eim_EIM_CS[0]	Output	1
EIM_CS1	J23	NVCC_EIM1	GPIO	ALT0	eim_EIM_CS[1]	Output	1
EIM_D16	C25	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[16]	Input	PU (100K)
EIM_D17	F21	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[17]	Input	PU (100K)
EIM_D18	D24	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[18]	Input	PU (100K)
EIM_D19	G21	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[19]	Input	PU (100K)
EIM_D20	G20	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[20]	Input	PU (100K)
EIM_D21	H20	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[21]	Input	PU (100K)
EIM_D22	E23	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[22]	Input	PD (100K)
EIM_D23	D25	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[23]	Input	PU (100K)
EIM_D24	F22	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[24]	Input	PU (100K)
EIM_D25	G22	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[25]	Input	PU (100K)
EIM_D26	E24	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[26]	Input	PU (100K)
EIM_D27	E25	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[27]	Input	PU (100K)
EIM_D28	G23	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[28]	Input	PU (100K)
EIM_D29	J19	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[29]	Input	PU (100K)
EIM_D30	J20	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[30]	Input	PU (100K)
EIM_D31	H21	NVCC_EIM0	GPIO	ALT5	gpio3_GPIO[31]	Input	PD (100K)
EIM_DA0	L20	NVCC_EIM2	GPIO	ALT0	eim_EIM_DA_A[0]	Input	PU (100K)
EIM_DA1	J25	NVCC_EIM2	GPIO	ALT0	eim_EIM_DA_A[1]	Input	PU (100K)
EIM_DA2	L21	NVCC_EIM2	GPIO	ALT0	eim_EIM_DA_A[2]	Input	PU (100K)
EIM_DA3	K24	NVCC_EIM2	GPIO	ALT0	eim_EIM_DA_A[3]	Input	PU (100K)

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
EIM_DA4	L22	NVCC_EIM2	GPIO	ALT0	eim_EIM_DA_A[4]	Input	PU (100K)
EIM_DA5	L23	NVCC_EIM2	GPIO	ALT0	eim_EIM_DA_A[5]	Input	PU (100K)
EIM_DA6	K25	NVCC_EIM2	GPIO	ALT0	eim_EIM_DA_A[6]	Input	PU (100K)
EIM_DA7	L25	NVCC_EIM2	GPIO	ALT0	eim_EIM_DA_A[7]	Input	PU (100K)
EIM_DA8	L24	NVCC_EIM2	GPIO	ALT0	eim_EIM_DA_A[8]	Input	PU (100K)
EIM_DA9	M21	NVCC_EIM2	GPIO	ALT0	eim_EIM_DA_A[9]	Input	PU (100K)
EIM_DA10	M22	NVCC_EIM2	GPIO	ALT0	eim_EIM_DA_A[10]	Input	PU (100K)
EIM_DA11	M20	NVCC_EIM2	GPIO	ALT0	eim_EIM_DA_A[11]	Input	PU (100K)
EIM_DA12	M24	NVCC_EIM2	GPIO	ALT0	eim_EIM_DA_A[12]	Input	PU (100K)
EIM_DA13	M23	NVCC_EIM2	GPIO	ALT0	eim_EIM_DA_A[13]	Input	PU (100K)
EIM_DA14	N23	NVCC_EIM2	GPIO	ALT0	eim_EIM_DA_A[14]	Input	PU (100K)
EIM_DA15	N24	NVCC_EIM2	GPIO	ALT0	eim_EIM_DA_A[15]	Input	PU (100K)
EIM_EB0	K21	NVCC_EIM2	GPIO	ALT0	eim_EIM_EB[0]	Output	1
EIM_EB1	K23	NVCC_EIM2	GPIO	ALT0	eim_EIM_EB[1]	Output	1
EIM_EB2	E22	NVCC_EIM0	GPIO	ALT5	gpio2_GPIO[30]	Input	PU (100K)
EIM_EB3	F23	NVCC_EIM0	GPIO	ALT5	gpio2_GPIO[31]	Input	PU (100K)
EIM_LBA	K22	NVCC_EIM1	GPIO	ALT0	eim_EIM_LBA	Output	1
EIM_OE	J24	NVCC_EIM1	GPIO	ALT0	eim_EIM_OE	Output	1
EIM_RW	K20	NVCC_EIM1	GPIO	ALT0	eim_EIM_RW	Output	1
EIM_WAIT	M25	NVCC_EIM2	GPIO	ALT0	eim_EIM_WAIT	Input	PU (100K)
ENET_CRSDV	U21	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[25]	Input	PU (100K)
ENET_MDC	V20	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[31]	Input	PU (100K)
ENET_MDIO	V23	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[22]	Input	PU (100K)
ENET_REF_CLK	V22	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[23]	Input	PU (100K)
ENET_RX_ER	W23	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[24]	Input	PU (100K)
ENET_RXD0	W21	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[27]	Input	PU (100K)
ENET_RXD1	W22	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[26]	Input	PU (100K)
ENET_TX_EN	V21	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[28]	Input	PU (100K)
ENET_TXD0	U20	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[30]	Input	PU (100K)
ENET_TXD1	W20	NVCC_ENET	GPIO	ALT5	gpio1_GPIO[29]	Input	PU (100K)

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
GPIO_0	T5	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[0]	Input	PD (100K)
GPIO_1	T4	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[1]	Input	PD (100K)
GPIO_16	R2	NVCC_GPIO	GPIO	ALT5	gpio7_GPIO[11]	Input	PU (100K)
GPIO_17	R1	NVCC_GPIO	GPIO	ALT5	gpio7_GPIO[12]	Input	PU (100K)
GPIO_18	P6	NVCC_GPIO	GPIO	ALT5	gpio7_GPIO[13]	Input	PU (100K)
GPIO_19	P5	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[5]	Input	PU (100K)
GPIO_2	T1	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[2]	Input	PU (100K)
GPIO_3	R7	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[3]	Input	PU (100K)
GPIO_4	R6	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[4]	Input	PU (100K)
GPIO_5	R4	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[5]	Input	PU (100K)
GPIO_6	T3	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[6]	Input	PU (100K)
GPIO_7	R3	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[7]	Input	PU (100K)
GPIO_8	R5	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[8]	Input	PU (100K)
GPIO_9	T2	NVCC_GPIO	GPIO	ALT5	gpio1_GPIO[9]	Input	PU (100K)
HDMI_CLKM	J5	HDMI_VPH			HDMI_VPH_CLKM	—	—
HDMI_CLKP	J6	HDMI_VPH			HDMI_CLKP	—	—
HDMI_D0M	K5	HDMI_VPH			HDMI_D0M	—	—
HDMI_D0P	K6	HDMI_VPH			HDMI_D0P	—	—
HDMI_D1M	J3	HDMI_VPH			HDMI_D1M	—	—
HDMI_D1P	J4	HDMI_VPH			HDMI_D1P	—	—
HDMI_D2M	K3	HDMI_VPH			HDMI_D2M	—	—
HDMI_D2P	K4	HDMI_VPH			HDMI_D2P	—	—
HDMI_DDCCEC	K2	HDMI_VPH			HDMI_DDCCEC	—	—
HDMI_HPD	K1	HDMI_VPH			HDMI_HPD	—	—
JTAG_MOD	H6	NVCC_JTAG	GPIO	ALT0	sjc_MOD	Input	PU (100K)
JTAG_TCK	H5	NVCC_JTAG	GPIO	ALT0	sjc_TCK	Input	PU (47K)
JTAG_TDI	G5	NVCC_JTAG	GPIO	ALT0	sjc_TDI	Input	PU (47K)
JTAG_TDO	G6	NVCC_JTAG	GPIO	ALT0	sjc_TDO	Output	Keeper
JTAG_TMS	C3	NVCC_JTAG	GPIO	ALT0	sjc_TMS	Input	PU (47K)
JTAG_TRSTB	C2	NVCC_JTAG	GPIO	ALT0	sjc_TRSTB	Input	PU (47K)

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
KEY_COL0	W5	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[6]	Input	PU (100K)
KEY_COL1	U7	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[8]	Input	PU (100K)
KEY_COL2	W6	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[10]	Input	PU (100K)
KEY_COL3	U5	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[12]	Input	PU (100K)
KEY_COL4	T6	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[14]	Input	PU (100K)
KEY_ROW0	V6	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[7]	Input	PU (100K)
KEY_ROW1	U6	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[9]	Input	PU (100K)
KEY_ROW2	W4	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[11]	Input	PU (100K)
KEY_ROW3	T7	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[13]	Input	PU (100K)
KEY_ROW4	V5	NVCC_GPIO	GPIO	ALT5	gpio4_GPIO[15]	Input	PD (100K)
LVDS0_CLK_N	V4	NVCC_LVDS2P5	LVDS		LVDS0_CLK_N	—	—
LVDS0_CLK_P	V3	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS0_CLK	Input	Keeper
LVDS0_TX0_N	U2	NVCC_LVDS2P5	LVDS		LVDS0_TX0_N	—	—
LVDS0_TX0_P	U1	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS0_TX0	Input	Keeper
LVDS0_TX1_N	U4	NVCC_LVDS2P5	LVDS		LVDS0_TX1_N	—	—
LVDS0_TX1_P	U3	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS0_TX1	Input	Keeper
LVDS0_TX2_N	V2	NVCC_LVDS2P5	LVDS		LVDS0_TX2_N	—	—
LVDS0_TX2_P	V1	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS0_TX2	Input	Keeper
LVDS0_TX3_N	W2	NVCC_LVDS2P5	LVDS		LVDS0_TX3_N	—	—
LVDS0_TX3_P	W1	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS0_TX3	Input	Keeper
LVDS1_CLK_N	Y3	NVCC_LVDS2P5	LVDS		LVDS1_CLK_N	—	—
LVDS1_CLK_P	Y4	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS1_CLK	Input	Keeper
LVDS1_TX0_N	Y1	NVCC_LVDS2P5	LVDS		LVDS1_TX0_N	—	—
LVDS1_TX0_P	Y2	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS1_TX0	Input	Keeper
LVDS1_TX1_N	AA2	NVCC_LVDS2P5	LVDS		LVDS1_TX1_N	—	—
LVDS1_TX1_P	AA1	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS1_TX1	Input	Keeper
LVDS1_TX2_N	AB1	NVCC_LVDS2P5	LVDS		LVDS1_TX2_N	—	—
LVDS1_TX2_P	AB2	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS1_TX2	Input	Keeper
LVDS1_TX3_N	AA3	NVCC_LVDS2P5	LVDS		LVDS1_TX3_N	—	—
LVDS1_TX3_P	AA4	NVCC_LVDS2P5	LVDS	ALT0	ldb_LVDS1_TX3	Input	Keeper

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
MLB_CN ²	A11	VDDHIGH_CAP	LVDS		MLB_CN	—	—
MLB_CP ²	B11	VDDHIGH_CAP	LVDS		MLB_CP	—	—
MLB_DN ²	B10	VDDHIGH_CAP	LVDS		MLB_DN	—	—
MLB_DP ²	A10	VDDHIGH_CAP	LVDS		MLB_DP	—	—
MLB_SN ²	A9	VDDHIGH_CAP	LVDS		MLB_SN	—	—
MLB_SP ²	B9	VDDHIGH_CAP	LVDS		MLB_SP	—	—
NANDF_ALE	A16	NVCC_NANDF	GPIO	ALT5	gpio6_GPIO[8]	Input	PU (100K)
NANDF_CLE	C15	NVCC_NANDF	GPIO	ALT5	gpio6_GPIO[7]	Input	PU (100K)
NANDF_CS0	F15	NVCC_NANDF	GPIO	ALT5	gpio6_GPIO[11]	Input	PU (100K)
NANDF_CS1	C16	NVCC_NANDF	GPIO	ALT5	gpio6_GPIO[14]	Input	PU (100K)
NANDF_CS2	A17	NVCC_NANDF	GPIO	ALT5	gpio6_GPIO[15]	Input	PU (100K)
NANDF_CS3	D16	NVCC_NANDF	GPIO	ALT5	gpio6_GPIO[16]	Input	PU (100K)
NANDF_D0	A18	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[0]	Input	PU (100K)
NANDF_D1	C17	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[1]	Input	PU (100K)
NANDF_D2	F16	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[2]	Input	PU (100K)
NANDF_D3	D17	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[3]	Input	PU (100K)
NANDF_D4	A19	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[4]	Input	PU (100K)
NANDF_D5	B18	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[5]	Input	PU (100K)
NANDF_D6	E17	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[6]	Input	PU (100K)
NANDF_D7	C18	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[7]	Input	PU (100K)
NANDF_RB0	B16	NVCC_NANDF	GPIO	ALT5	gpio6_GPIO[10]	Input	PU (100K)
NANDF_WP_B	E15	NVCC_NANDF	GPIO	ALT5	gpio6_GPIO[9]	Input	PU (100K)
ONOFF	D12	VDD_SNVIS_IN	GPIO		src_ONOFF	Input	PU (100K)
PCIE_RXM	B1	PCIE_VPH			PCIE_RXM	—	—
PCIE_RXP	B2	PCIE_VPH			PCIE_RXP	—	—
PCIE_TXM	A3	PCIE_VPH			PCIE_TXM	—	—
PCIE_TXP	B3	PCIE_VPH			PCIE_TXP	—	—
PMIC_ON_REQ	D11	VDD_SNVIS_IN	GPIO	ALT0	snvs_lp_wrapper_SNVIS_WAKEUP_ALARM	Output	Open Drain with PU (100K)

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
PMIC_STBY_REQ	F11	VDD_SNVS_IN	GPIO	ALT0	ccm_PMIC_VSTBY_REQ	Output	0
POR_B	C11	VDD_SNVS_IN	GPIO	ALT0	src_POR_B	Input	PU (100K)
RGMII_RD0	C24	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[25]	Input	PU (100K)
RGMII_RD1	B23	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[27]	Input	PU (100K)
RGMII_RD2	B24	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[28]	Input	PU (100K)
RGMII_RD3	D23	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[29]	Input	PU (100K)
RGMII_RX_CTL	D22	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[24]	Input	PD (100K)
RGMII_RXC	B25	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[30]	Input	PD (100K)
RGMII_TD0	C22	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[20]	Input	PU (100K)
RGMII_TD1	F20	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[21]	Input	PU (100K)
RGMII_TD2	E21	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[22]	Input	PU (100K)
RGMII_TD3	A24	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[23]	Input	PU (100K)
RGMII_TX_CTL	C23	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[26]	Input	PD (100K)
RGMII_TXC	D21	NVCC_RGMII	DDR	ALT5	gpio6_GPIO[19]	Input	PD (100K)
RTC_XTALI	D9	VDD_SNVS_CAP			RTC_XTALI	—	—
RTC_XTALO	C9	VDD_SNVS_CAP			RTC_XTALO	—	—
SATA_RXM	A14	SATA_VPH			SATA_RXM	—	—
SATA_RXP	B14	SATA_VPH			SATA_RXP	—	—
SATA_TXM	B12	SATA_VPH			SATA_TXM	—	—
SATA_TXP	A12	SATA_VPH			SATA_TXP	—	—
SD1_CLK	D20	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[20]	Input	PU (100K)
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[18]	Input	PU (100K)
SD1_DAT0	A21	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[16]	Input	PU (100K)
SD1_DAT1	C20	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[17]	Input	PU (100K)
SD1_DAT2	E19	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[19]	Input	PU (100K)
SD1_DAT3	F18	NVCC_SD1	GPIO	ALT5	gpio1_GPIO[21]	Input	PU (100K)
SD2_CLK	C21	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[10]	Input	PU (100K)
SD2_CMD	F19	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[11]	Input	PU (100K)
SD2_DAT0	A22	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[15]	Input	PU (100K)
SD2_DAT1	E20	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[14]	Input	PU (100K)

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
SD2_DAT2	A23	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[13]	Input	PU (100K)
SD2_DAT3	B22	NVCC_SD2	GPIO	ALT5	gpio1_GPIO[12]	Input	PU (100K)
SD3_CLK	D14	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[3]	Input	PU (100K)
SD3_CMD	B13	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[2]	Input	PU (100K)
SD3_DAT0	E14	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[4]	Input	PU (100K)
SD3_DAT1	F14	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[5]	Input	PU (100K)
SD3_DAT2	A15	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[6]	Input	PU (100K)
SD3_DAT3	B15	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[7]	Input	PU (100K)
SD3_DAT4	D13	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[1]	Input	PU (100K)
SD3_DAT5	C13	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[0]	Input	PU (100K)
SD3_DAT6	E13	NVCC_SD3	GPIO	ALT5	gpio6_GPIO[18]	Input	PU (100K)
SD3_DAT7	F13	NVCC_SD3	GPIO	ALT5	gpio6_GPIO[17]	Input	PU (100K)
SD3_RST	D15	NVCC_SD3	GPIO	ALT5	gpio7_GPIO[8]	Input	PU (100K)
SD4_CLK	E16	NVCC_NANDF	GPIO	ALT5	gpio7_GPIO[10]	Input	PU (100K)
SD4_CMD	B17	NVCC_NANDF	GPIO	ALT5	gpio7_GPIO[9]	Input	PU (100K)
SD4_DAT0	D18	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[8]	Input	PU (100K)
SD4_DAT1	B19	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[9]	Input	PU (100K)
SD4_DAT2	F17	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[10]	Input	PU (100K)
SD4_DAT3	A20	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[11]	Input	PU (100K)
SD4_DAT4	E18	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[12]	Input	PU (100K)
SD4_DAT5	C19	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[13]	Input	PU (100K)
SD4_DAT6	B20	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[14]	Input	PU (100K)
SD4_DAT7	D19	NVCC_NANDF	GPIO	ALT5	gpio2_GPIO[15]	Input	PU (100K)
TAMPER	E11	VDD_SNVS_IN	GPIO	ALT0	snvs_lp_wrapper_ SNVS_TD1	Input	PD (100K)
TEST_MODE	E12	VDD_SNVS_IN			Reserved—Factory Use Only	Input	PD (100K)
USB_H1_DN	F10	VDDUSB_CAP			USB_H1_DN	—	—
USB_H1_DP	E10	VDDUSB_CAP			USB_H1_DP	—	—
USB_H1_VBUS	D10	VDDUSB_CAP			USB_H1_VBUS	—	—

Table 93. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ¹			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
USB_OTG_CHD_B	B8	VDDUSB_CAP			USB_OTG_CHD_B	—	—
USB_OTG_DN	B6	VDDUSB_CAP			USB_OTG_DN	—	—
USB_OTG_DP	A6	VDDUSB_CAP			USB_OTG_DP	—	—
USB_OTG_VBUS	E9	VDDUSB_CAP			USB_OTG_VBUS	—	—
XTALI	A7	NVCC_PLL_OUT			XTALI	—	—
XTALO	B7	NVCC_PLL_OUT			XTALO	—	—

¹ The state immediately after reset and before ROM firmware or software has executed.

² MLB is only supported in automotive graded parts. These balls should be considered as not connected in industrial graded parts.

For most of the signals, the state during reset is same as the state after reset, given in Out of Reset Condition column of [Table 93](#). However, there are few signals for which the state during reset is different from the state after reset. These signals along with their state during reset are given in [Table 94](#).

Table 94. Signals with Differing Before Reset and After Reset States

Ball Name	Before Reset State	
	Input/Output	Value
EIM_A16	Input	PD (100K)
EIM_A17	Input	PD (100K)
EIM_A18	Input	PD (100K)
EIM_A19	Input	PD (100K)
EIM_A20	Input	PD (100K)
EIM_A21	Input	PD (100K)
EIM_A22	Input	PD (100K)
EIM_A23	Input	PD (100K)
EIM_A24	Input	PD (100K)
EIM_A25	Input	PD (100K)
EIM_DA0	Input	PD (100K)
EIM_DA1	Input	PD (100K)
EIM_DA2	Input	PD (100K)
EIM_DA3	Input	PD (100K)
EIM_DA4	Input	PD (100K)

Table 94. Signals with Differing Before Reset and After Reset States (continued)

Ball Name	Before Reset State	
	Input/Output	Value
EIM_DA5	Input	PD (100K)
EIM_DA6	Input	PD (100K)
EIM_DA7	Input	PD (100K)
EIM_DA8	Input	PD (100K)
EIM_DA9	Input	PD (100K)
EIM_DA10	Input	PD (100K)
EIM_DA11	Input	PD (100K)
EIM_DA12	Input	PD (100K)
EIM_DA13	Input	PD (100K)
EIM_DA14	Input	PD (100K)
EIM_DA15	Input	PD (100K)
EIM_EB0	Input	PD (100K)
EIM_EB1	Input	PD (100K)
EIM_EB2	Input	PD (100K)
EIM_EB3	Input	PD (100K)
EIM_LBA	Input	PD (100K)
EIM_RW	Input	PD (100K)
EIM_WAIT	Input	PD (100K)
GPIO_17	Output	Drive state unknown (x)
GPIO_19	Output	Drive state unknown (x)
KEY_COL0	Output	Drive state unknown (x)

6.1.3 21 x 21 mm, 0.8 mm Pitch Ball Map

Table 95 shows the FCPBGA 21 x 21 mm, 0.8 mm pitch ball map.

Table 95. 21 x 21 mm, 0.8 mm Pitch Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
A		PCIE_REXT	PCIE_TXM	GND	FA_ANA	USB_OTG_DP	XTALI	GND	MLB_SN ¹	MLB_DP ¹	MLB_CN ¹	SATA_TXP	GND	SATA_RXM	SD3_DAT2	NANDF_ALE	NANDF_CS2	NANDF_D0	NANDF_D4	SD4_DAT3	SD1_DAT0	SD2_DAT0	SD2_DAT2	RGMII_TD3	GND

Table 95. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

H	G	F	E	D	C	B
DSI_D1P	DSI_D0P	CSI_D3P	CSI_D2M	CSI_D1M	GND	PCIE_RXM
DSI_D1M	DSI_D0M	CSI_D3M	CSI_D2P	CSI_D1P	JTAG_TRSTB	PCIE_RXP
DSI_CLK0M	GND	CSI_CLK0P	CSI_D0P	GND	JTAG_TMS	PCIE_TXP
DSI_CLK0P	DSI_REXT	CSI_CLK0M	CSI_D0M	CSI_REXT	GND	GND
JTAG_TCK	JTAG_TDI	GND	GND	CLK2_P	CLK2_N	VDD_FA
JTAG_MOD	JTAG_TDO	GND	GND	GND	GND	USB_OTG_DN
PCIE_VP	PCIE_VPH	GND	GND	CLK1_P	CLK1_N	XTALO
GND	PCIE_VPTX	GND	NVCC_PLL_OUT	GND	GPANAIO	USB_OTG_CHD_B
VDDHIGH_IN	VDD_SNV5_CAP	VDDUSB_CAP	USB_OTG_VBUS	RTC_XTALI	RTC_XTALO	MLB_SP1
VDDHIGH_CAP	GND	USB_H1_DN	USB_H1_DP	USB_H1_VBUS	GND	MLB_DN1
VDDARM23_CAP	VDD_SNV5_IN	PMIC_STBY_REQ	TAMPER	PMIC_ON_REQ	POR_B	MLB_CP1
GND	SATA_VPH	BOOT_MODE1	TEST_MODE	ONOFF	BOOT_MODE0	SATA_TXM
VDDARM_CAP	SATA_VP	SD3_DAT7	SD3_DAT6	SD3_DAT4	SD3_DAT5	SD3_CMD
VDDARM_IN	NVCC_SD3	SD3_DAT1	SD3_DAT0	SD3_CLK	SATA_REXT	SATA_RXP
GND	NVCC_NANDF	NANDF_CS0	NANDF_WP_B	SD3_RST	NANDF_CLE	SD3_DAT3
VDDSOC_IN	NVCC_SD1	NANDF_D2	SD4_CLK	NANDF_CS3	NANDF_CS1	NANDF_RB0
VDDPU_CAP	NVCC_SD2	SD4_DAT2	NANDF_D6	NANDF_D3	NANDF_D1	SD4_CMD
GND	NVCC_RGMII	SD1_DAT3	SD4_DAT4	SD4_DAT0	NANDF_D7	NANDF_D5
EIM_A25	GND	SD2_CMD	SD1_DAT2	SD4_DAT7	SD4_DAT5	SD4_DAT1
EIM_D21	EIM_D20	RGMII_TD1	SD2_DAT1	SD1_CLK	SD1_DAT1	SD4_DAT6
EIM_D31	EIM_D19	EIM_D17	RGMII_TD2	RGMII_TXC	SD2_CLK	SD1_CMD
EIM_A20	EIM_D25	EIM_D24	EIM_EB2	RGMII_RX_CTL	RGMII_TD0	SD2_DAT3
EIM_A21	EIM_D28	EIM_EB3	EIM_D22	RGMII_RD3	RGMII_TX_CTL	RGMII_RD1
EIM_CS0	EIM_A17	EIM_A22	EIM_D26	EIM_D18	RGMII_RD0	RGMII_RD2
EIM_A16	EIM_A19	EIM_A24	EIM_D27	EIM_D23	EIM_D16	RGMII_RXC

Table 95. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

R	P	N	M	L	K	J
GPIO_17	CSIO_PIXCLK	CSIO_DATA4	CSIO_DAT10	CSIO_DAT13	HDMI_HP_D	HDMI_REF
GPIO_16	CSIO_DATA5	CSIO_VSYNC	CSIO_DAT12	GND	HDMI_DDCCEC	GND
GPIO_7	CSIO_DATA_EN	CSIO_DATA7	CSIO_DAT11	CSIO_DAT17	HDMI_D2M	HDMI_D1M
GPIO_5	CSIO_MCLK	CSIO_DATA6	CSIO_DAT14	CSIO_DAT16	HDMI_D2P	HDMI_D1P
GPIO_8	GPIO_19	CSIO_DATA9	CSIO_DAT15	GND	HDMI_D0M	HDMI_CLKM
GPIO_4	GPIO_18	CSIO_DATA8	CSIO_DAT18	CSIO_DAT19	HDMI_D0P	HDMI_CLKP
GPIO_3	NVCC_GPIO	NVCC_CSI	HDMI_VPH	HDMI_VP	NVCC_MIPI	NVCC_JTAG
GND	GND	GND	GND	GND	GND	GND
VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDARM23_IN	VDDHIGH_IN
VDDSOC_CAP	GND	GND	GND	GND	GND	VDDHIGH_CAP
VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP	VDDARM23_CAP
GND	GND	VDD_CACHE_CAP	GND	GND	GND	GND
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN
GND	GND	GND	GND	GND	GND	GND
VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN
GND	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP
NVCC_DRAM	GND	GND	GND	GND	GND	GND
NVCC_ENET	NVCC_LCD	DIO_DISP_CLK	NVCC_EIM2	NVCC_EIM1	NVCC_EIM0	EIM_D29
DISP0_DAT13	DISP0_DATA4	DIO_PIN3	EIM_DA11	EIM_DA0	EIM_RW	EIM_D30
DISP0_DAT10	DISP0_DATA3	DIO_PIN15	EIM_DA9	EIM_DA2	EIM_EB0	EIM_A23
DISP0_DATA8	DISP0_DATA1	EIM_BCLK	EIM_DA10	EIM_DA4	EIM_LBA	EIM_A18
DISP0_DATA6	DISP0_DATA2	EIM_DA14	EIM_DA13	EIM_DA5	EIM_EB1	EIM_CS1
DISP0_DATA7	DISP0_DATA0	EIM_DA15	EIM_DA12	EIM_DA8	EIM_DA3	EIM_OE
DISP0_DATA5	DIO_PIN4	DIO_PIN2	EIM_WAIT	EIM_DA7	EIM_DA6	EIM_DA1

Table 95. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

AC	AB	AA	Y	W	V	U	T
DRAM_D4	LVDS1_TX2_N	LVDS1_TX1_P	LVDS1_TX0_N	LVDS0_TX3_P	LVDS0_TX2_P	LVDS0_TX0_P	GPIO_2
DRAM_VREF	LVDS1_TX2_P	LVDS1_TX1_N	LVDS1_TX0_P	LVDS0_TX3_N	LVDS0_TX2_N	LVDS0_TX0_N	GPIO_9
DRAM_DQM0	GND	LVDS1_TX3_N	LVDS1_CLK_N	GND	LVDS0_CLK_P	LVDS0_TX1_P	GPIO_6
DRAM_D2	DRAM_D6	LVDS1_TX3_P	LVDS1_CLK_P	KEY_ROW2	LVDS0_CLK_N	LVDS0_TX1_N	GPIO_1
DRAM_D13	DRAM_D12	DRAM_D3	GND	KEY_COL0	KEY_ROW4	KEY_COL3	GPIO_0
DRAM_DQM1	DRAM_D14	DRAM_D10	DRAM_RESET	KEY_COL2	KEY_ROW0	KEY_ROW1	KEY_COL4
DRAM_D15	DRAM_D16	GND	DRAM_D20	GND	NVCC_LVDS2P5	KEY_COL1	KEY_ROW3
DRAM_D22	DRAM_DQM2	DRAM_D17	DRAM_D21	GND	GND	GND	GND
DRAM_D28	DRAM_D18	DRAM_D23	DRAM_D19	GND	NVCC_DRAM	VDDARM23_IN	VDDARM23_IN
DRAM_SDQS3	DRAM_SDQS3_B	GND	DRAM_D25	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP
DRAM_D31	DRAM_D27	DRAM_SDCKE1	DRAM_SDCKE0	GND	NVCC_DRAM	GND	GND
DRAM_A11	DRAM_SDBA2	DRAM_A14	DRAM_A15	GND	NVCC_DRAM	GND	GND
DRAM_A6	DRAM_A8	GND	DRAM_A7	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP
DRAM_A0	DRAM_A1	DRAM_A2	DRAM_A3	DRAM_A4	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP
DRAM_SDBA0	DRAM_RAS	DRAM_A10	DRAM_SDBA1	GND	NVCC_DRAM	GND	GND
DRAM_SDODT0	DRAM_SDWE	GND	DRAM_CS0	GND	NVCC_DRAM	VDDSOC_IN	VDDSOC_IN
DRAM_A13	DRAM_SDODT1	DRAM_D32	DRAM_D36	GND	NVCC_DRAM	GND	GND
DRAM_D34	DRAM_DQM4	DRAM_D33	DRAM_D37	GND	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM
DRAM_D39	DRAM_D38	GND	DRAM_D40	GND	GND	GND	GND
DRAM_DQM5	DRAM_D41	DRAM_D45	DRAM_D44	ENET_TXD1	ENET_MDC	ENET_TXD0	DISP0_DAT21
DRAM_D47	DRAM_D42	DRAM_D57	DRAM_DQM7	ENET_RXD0	ENET_TX_EN	ENET_CRS_DV	DISP0_DAT16
DRAM_D48	DRAM_D52	GND	DRAM_D59	ENET_RXD1	ENET_REF_CLK	DISP0_DAT20	DISP0_DAT15
DRAM_D53	DRAM_D60	DRAM_D61	DRAM_D62	ENET_RX_ER	ENET_MDIO	DISP0_DAT19	DISP0_DAT11
DRAM_D51	GND	DRAM_SDQS7_B	GND	DISP0_DAT23	DISP0_DAT22	DISP0_DAT17	DISP0_DAT12
DRAM_D55	DRAM_D56	DRAM_SDQS7	DRAM_D58	DRAM_D63	DISP0_DAT18	DISP0_DAT14	DISP0_DAT9

Table 95. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

AE	AD
GND	DRAM_D5
DRAM_D1	DRAM_D0
DRAM_SDQS0	DRAM_SDQS0_B
DRAM_D7	GND
DRAM_D9	DRAM_D8
DRAM_SDQS1_B	DRAM_SDQS1
DRAM_D11	GND
DRAM_SDQS2_B	DRAM_SDQS2
DRAM_D24	DRAM_D29
DRAM_DQM3	GND
DRAM_D26	DRAM_D30
DRAM_A9	DRAM_A12
DRAM_A5	GND
DRAM_SDCLK_1_B	DRAM_SDCLK_1
DRAM_SDCLK_0_B	DRAM_SDCLK_0
DRAM_CAS	GND
ZQPAD	DRAM_CS1
DRAM_SDQS4_B	DRAM_SDQS4
DRAM_D35	GND
DRAM_SDQS5_B	DRAM_SDQS5
DRAM_D46	DRAM_D43
DRAM_D49	GND
DRAM_SDQS6_B	DRAM_SDQS6
DRAM_D50	DRAM_DQM6
GND	DRAM_D54

¹ MLB is only supported in automotive graded parts. These balls should be considered as not connected in industrial graded parts.

7 Revision History

Table 98 provides a revision history for this datasheet.

Table 98. i.MX 6Dual/6Quad Datasheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 1	11/2012	Initial public release.

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