Application of Current Mirrors
Design and Simulation of an 8 - bit DAC

A PROJECT BY

Khyathi Nalluri

(19EC30024)

Surya Sai Ram Cheruvu

(19EC30010)

Under the supervision of

PROF. BIBHU DATTA SAHOO

Department of Electronics and Electrical Communication Engineering

Indian Institute of Technology Kharagpur

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Abstract

In this paper, we will go through the analysis, design and simulation of an 8-Bit DAC using current mirrors. Here we used three different design models of current mirrors. They are Simple Current Mirror, Cascode Current Mirror and Low Voltage Sooch Cascode Current Mirror models. At last we also designed a current steering DAC. The 8-bit binary input ranges from -1 to 1 V. The supply voltage is taken to be $V_{DD} = 1.2$ V. Major glitching issues were encountered during the design because of inaccurate mirroring and parasitic capacitances which were overcome through the use of digital flip-flops as well as an RC filter. An overall swing of 600mV was achieved with a resistive load of 50 Ω.

Contents

Objective

The major objective of our project is to build an 8-bit current steering Digital to Analog Converter, commonly known as DAC, using

1. Simple Current Mirror
2. Cascode Current Mirror
3. Low Voltage Sooch Cascode Current Mirror

Eventually we design an 8 - bit current steering DAC, given a digital sine wave as input and show the corresponding FFT analysis.
Here are the design specifications of our project :

Supply Voltage V_{DD}	$1.2\mathrm{V}$
Output Swing	$600\mathrm{mV}$
Load Resistance	50Ω
Topology	Binary Weighted

For this project we assumed that a golden current source of 47μA is available.
All the simulations are done in LTSpice. MATLAB is also used wherever needed.

Design

1 DAC Architecture

As already discussed in previous chapters, our interest is to design an 8-bit current steering DAC using current mirrors. An N-bit binary weighted converter has only N current mirrored sources with sizes of transistors varying from one unit to 2^N units corresponding to one LSB current to 2^N times the LSB current. This kind of design of current source array leads to the use of transistors with very large sizes in case of high resolution DACs. For example, in case of 8-bit DAC, if width of smallest transistor in the current source array is 1 µm, the width of subsequent transistors for higher bits would be 2 µm, 4 µm.. to 128 µm for MSB.

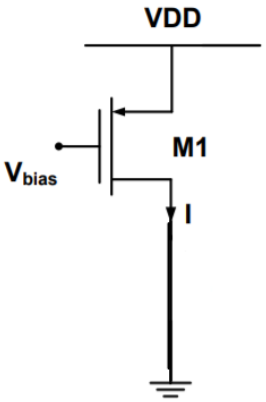
This type of current source architecture occupies lot of on-chip area, more prone to noise and is expensive. To overcome these problems, the number of transistors with the same width, are used in parallel instead of using transistors of different widths. The number of transistors is proportional to the current of the current source. This approach also improves the linearity and reduces the problems arising because of the mismatch of transistors.

Depending upon the input digital word, respective current sources are switched into the output load. When the switched currents from current sources are added, one gets the output proportional to the input digital word. The details of the current sources, the switches and the DAC are discussed in later sections.

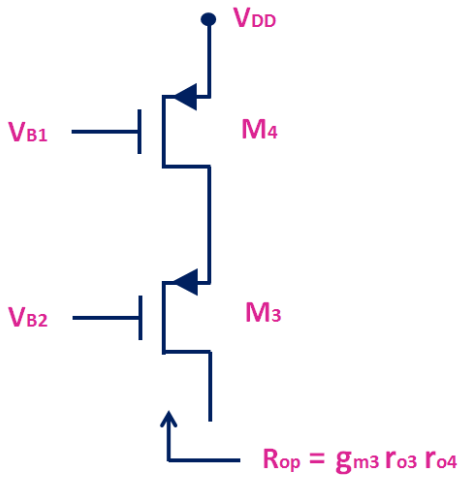
2 Current Sources

A current source is one of the most important elements of the current steering DAC. It generates the required current to be provided at the output of the DAC. Based on the input word, the currents generated by number of current sources are properly switched and summed at the output node. The current source can be realized either by using NMOS or PMOS transistors. The simplest current source which corresponds to a LSB current source as shown in below figures, is

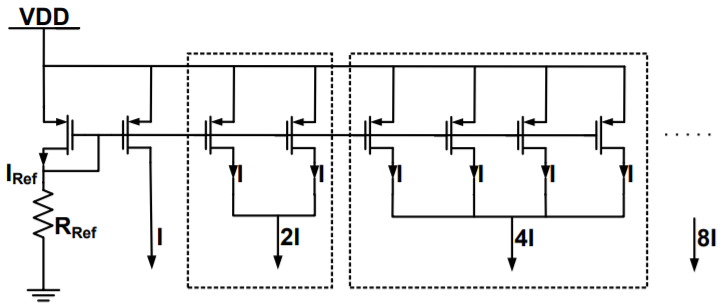
realized by a single transistor or more transistors, biased with a fixed voltage to provide constant current value. The other current sources are simply realized by using the required number of transistors in parallel. For example, a current source which supplies 8 times the current through the LSB source has 8 transistors in parallel.



PMOS Simple current source



PMOS Cascode current source



Current Sources with Parallel Transistors Connection

• There are some disadvantages of using simple PMOS as current source. Because ideal current source should have infinite output resistance, low compliance voltage. Whereas, simple current source has low output resistance and more prone to variations in supply voltage.

• To overcome these problems we used cascode current mirror which has high output resistance and more stable to fluctuations in supply voltage. But we compromised compliance voltage due to degenerating PMOS.

3 I_{LSB} Selection

The selection of current for the LSB is very critical as it decides the output swing of the DAC and also affects the accuracy and linearity of the DAC. As per our design guidelines the output voltage swing is 600 mV with a load resistance of 50 Ω.

$I_{LSB} = \frac{1}{2^N} \times$ Output current swing

where N $= 8$

$$I_{LSB} = \frac{1}{256} \times \frac{600}{50} mA$$

$$I_{LSB} = 47 \mu A$$

Simulation

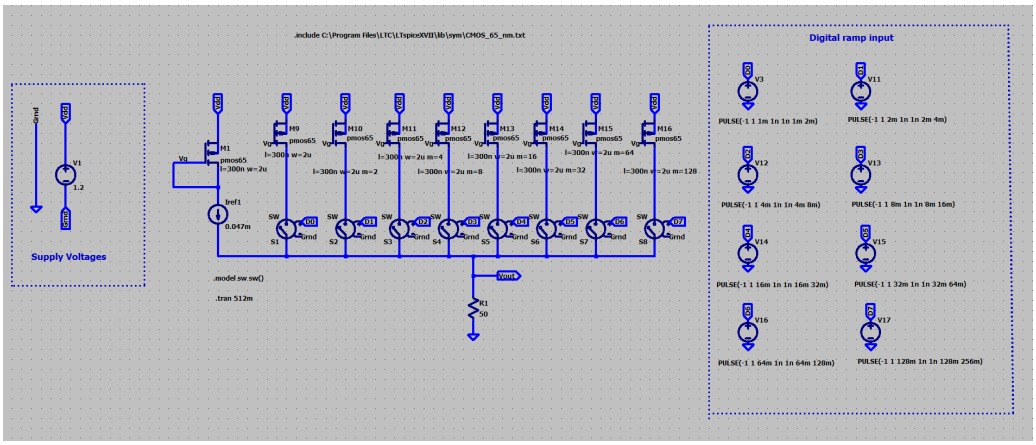
We designed and simulated an 8 - bit DAC in LTSpice using the following types of current mirrors.

4 Ramp Inputs

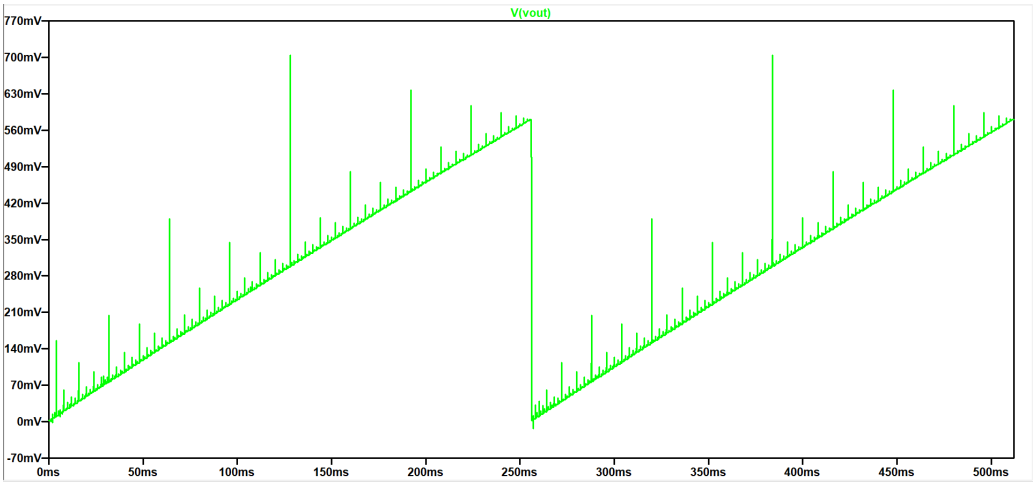
In all the below cases, the digital input can be given either as pulses or through D Flip-flops. Both the kinds of input methods and respective outputs are shown.

4.1 Using Simple Current Mirror

Here is the schematic of the DAC designed using Simple Current Mirror. We imported 65 nm V1.0 models (the corresponding PTM files) and included them in the schematic. We used the default sw() model for voltage controlled switches.

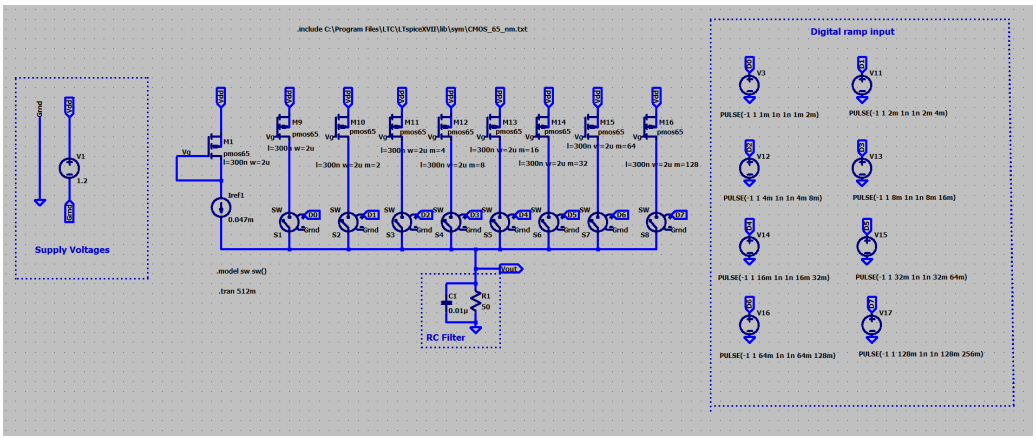


DAC with Simple CM

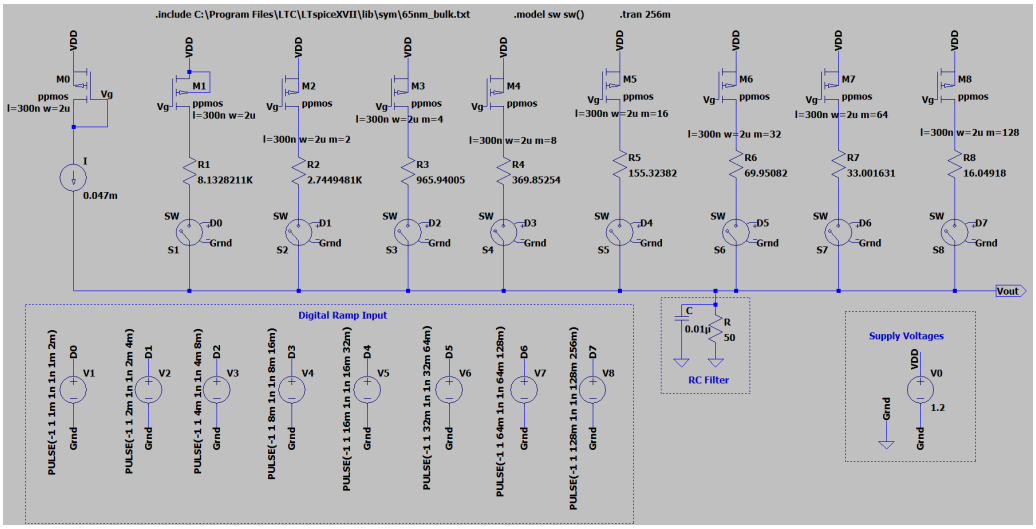


Output of the above schematic

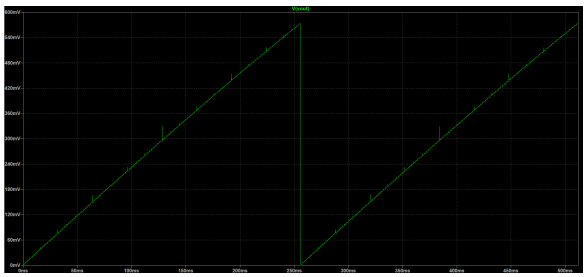
We observe some spikes in the output. These spikes can be filtered out by using an RC filter as shown in the below schematic. Also you can put appropriate resistors in each of the branches to ensure more accuracy in mirroring.



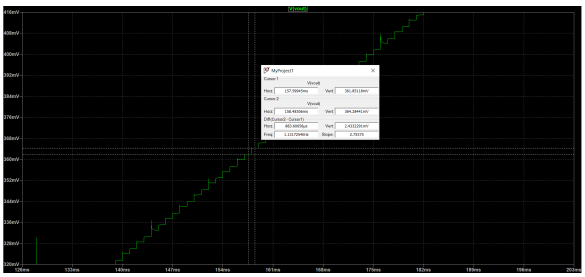
Using an RC Filter



Using appropriate values of resistors



Refined Output



Step Size

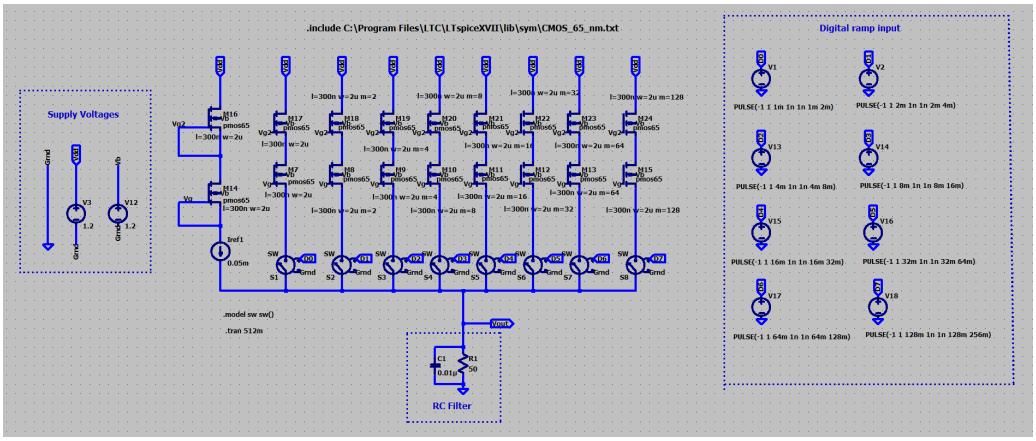
We can see the step size which is close to the expected value 2.35 mV but not equal since simple current mirroring does not give a good accuracy of mirroring. We can also compare the above step size when we do not use any resistors.

We used PMOS for mirroring since we are sourcing current in this case. NMOS can also be used in which case you need to connect the load to supply so that you can generate current sinks.

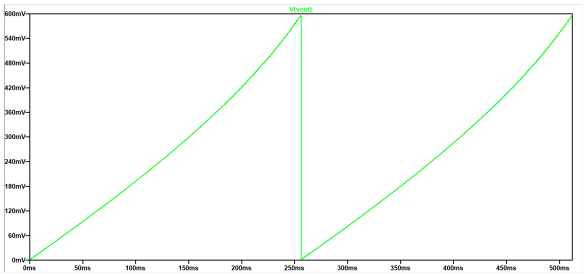
4.2 Using Cascode Current Mirror

Here is the schematic of the DAC designed using Cascode Current Mirror. We know that cascode mirroring is also not accurate.

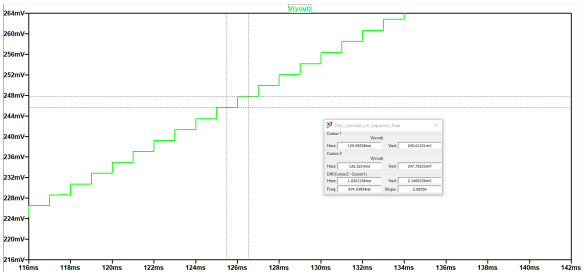
From now on we show the output only when the RC filter is used so that the spikes get removed.



DAC with Cascode CM



Output of above schematic

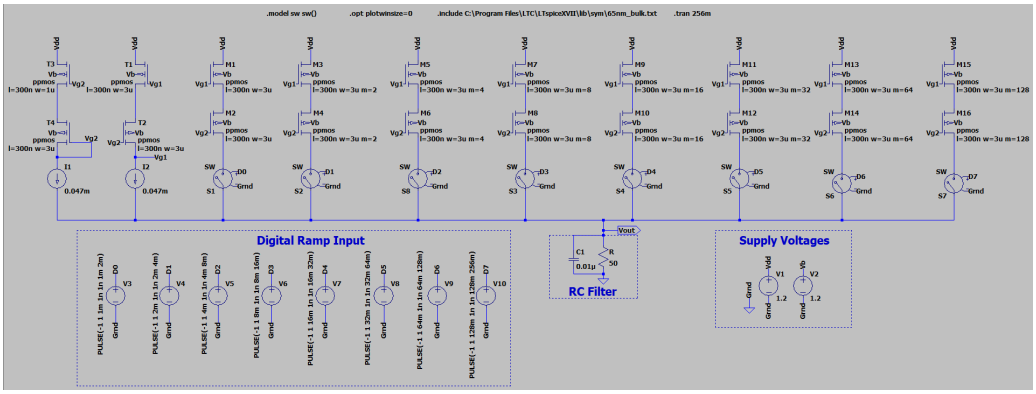


Step size

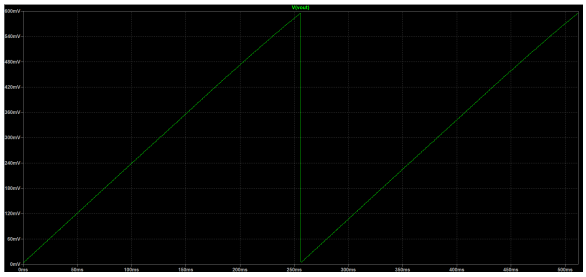
Even in this case we did not get the exact step value. Let's see which mirroring gives us the exact step value.

4.3 Using Low Voltage Sooch Cascode Current Mirror

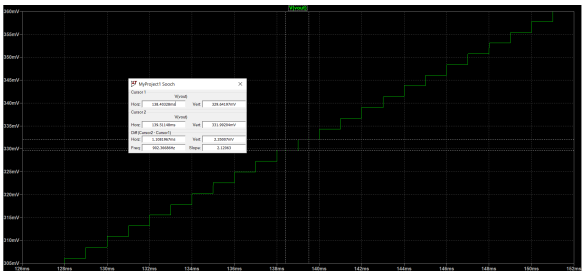
The schematic of the DAC designed using Low Voltage Sooch Cascode Current Mirror is shown below.



DAC with Sooch CM

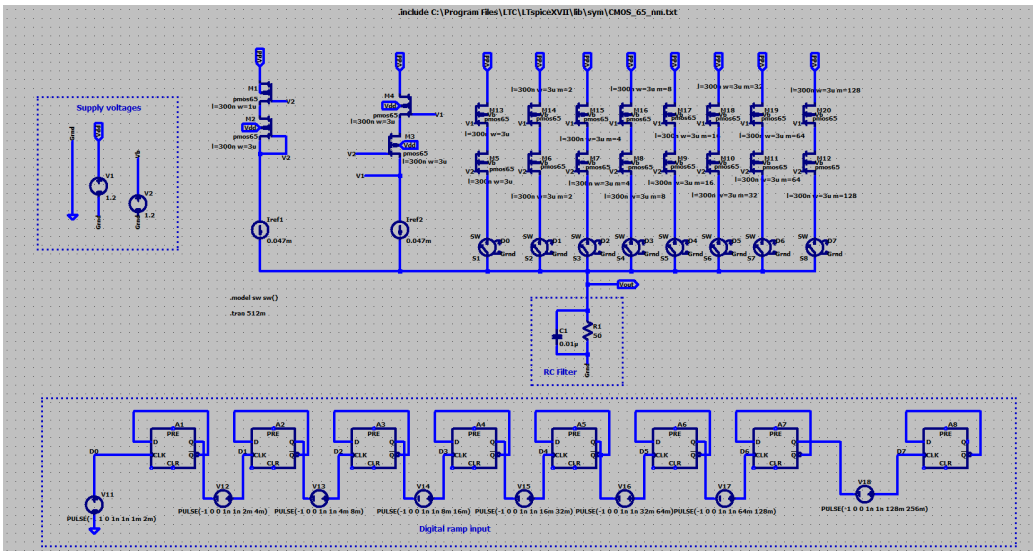


Output of the above schematic

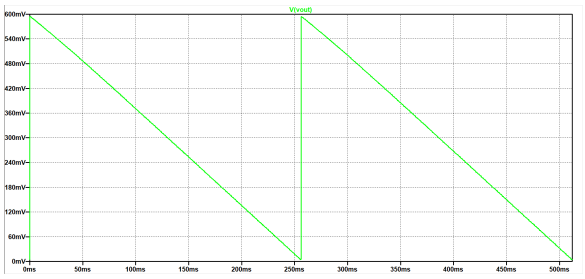


Step Size

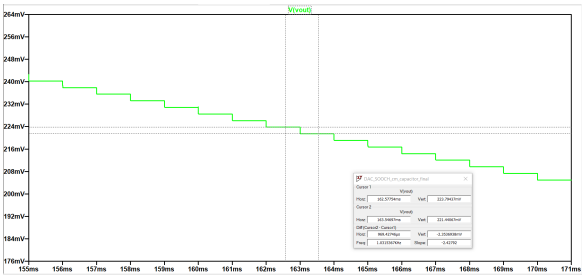
We can see that the step size is exact 2.35 mV. Now let's see the second method of input using D Flip-Flops.



Using D Flip Flops to give input



Respective Output



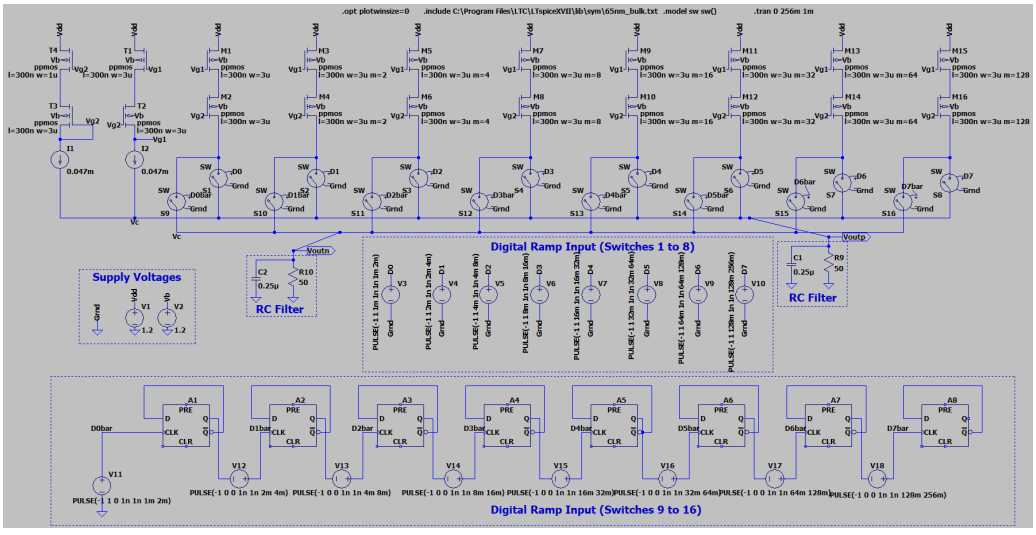
Step Size

We observe that the step size is same even in this case. Due to the kind of input given, the output either appears as increasing steps or decreasing steps. We used voltage sources in between the flip flops so that the expected input goes into every node and also as per our default sw() model.

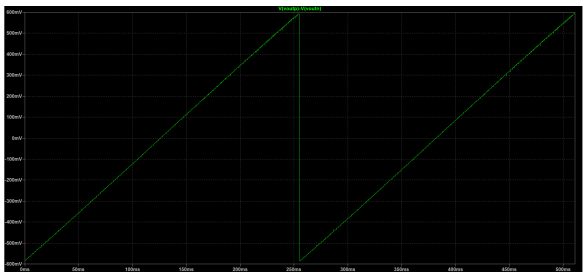
In all the above cases, the currents are scaled by scaling the widths and not the lengths.

4.4 Current Steering DAC

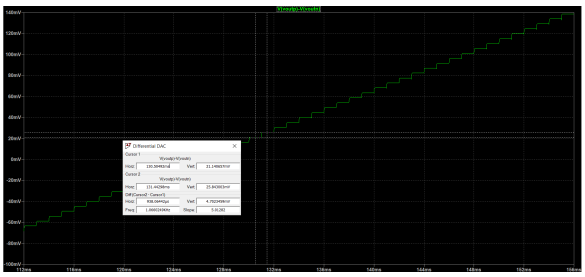
In reality, we always have differential circuits. So a current steering DAC is designed using the below schematic. Here we are interested in the voltage difference of the two nodes namely Voutp and Voutn.



Current Steering DAC



Output



Step Size

The step size is observed to be 4.70 mV i.e. double to that in the normal DAC as expected.

As required, we also obtained an output swing of 600 mV in all the above cases.

5 Digital Sine Wave as Input

Having built our DAC, we would like to test it with a sample digital input. Let's input a digital sine wave. The simulation results for the sine wave input are shown only for the DAC made using Low Voltage Sooch Cascode Current Mirror and the Current Steering DAC.

5.1 Using Low Voltage Sooch Cascode Current Mirror

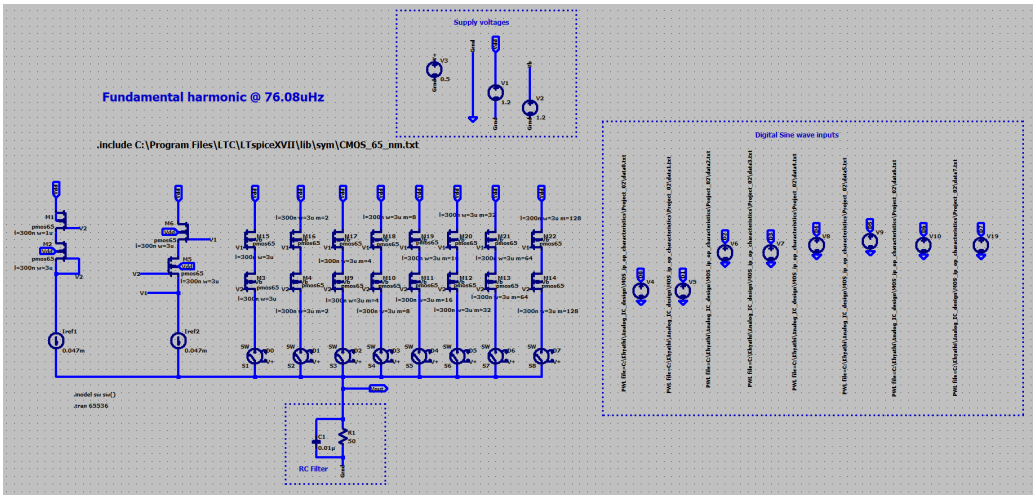
To digitize a sine wave, the following MATLAB code is used whose output can be stored in text files and can be imported into LTSpice through the PWL (Piece Wise Linear) file option.

```
Fs = 100*10^6;                  % Sample rate
N1 = 5;                         % N1 <= NFFT (for Nyquist criteria to be satisfied)
NFFT = 2^16;                    % Larger the NFFT the better the resolution
Fin = (N1/NFFT)*Fs;             % Input Signal Frequency
arr = 0:NFFT-1;                 % Array of numbers from 0 to NFFT-1
Vin = sin(2*pi*Fin*arr/Fs);     % Analog sine wave
din = quant(Vin,2^(-7));        % quantizes NN data Vin so that all values are replaced
                                % by the closest multiple of 2^(-7).
Din = (din+1)*127.5;            % Digital sine wave(din) is scaled and dc shifted so that range is (0:255)
Dfin = dec2bin(Din,8)-'0'       % (NFFT X 8) Matrix of digital sine wave
```

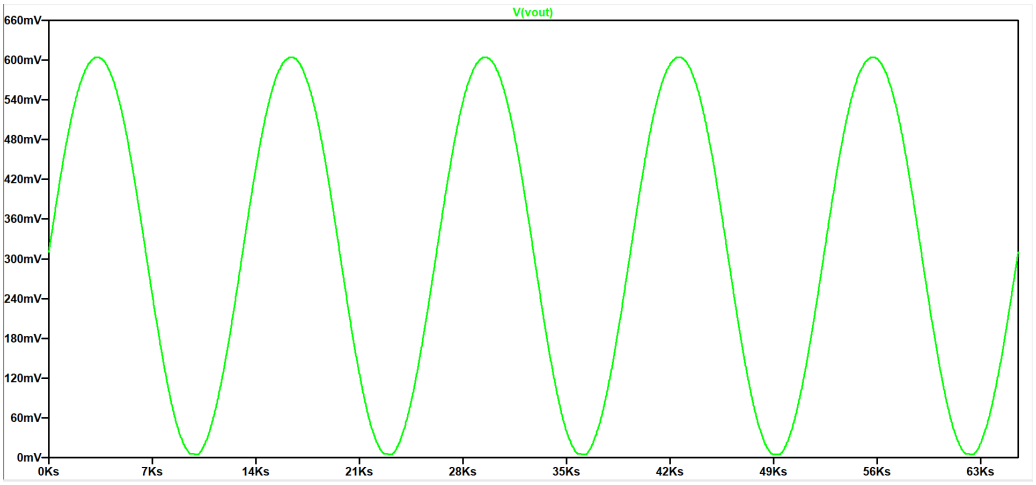
```
Dfin = 65536×8
     0     1     1     1     1     1     1     1
     0     1     1     1     1     1     1     1
     0     1     1     1     1     1     1     1
     0     1     1     1     1     1     1     1
     0     1     1     1     1     1     1     1
     0     1     1     1     1     1     1     1
     0     1     1     1     1     1     1     1
     0     1     1     1     1     1     1     1
     0     1     1     1     1     1     1     1
     0     1     1     1     1     1     1     1
     1     0     0     0     0     0     0     0
     ⋮
```

MATLAB Code for digitizing sine wave

Shown here is the required schematic for Low Voltage Sooch Cascode Current Mirror. The output of our DAC is really good as it can be seen, a perfect analog sine wave.



Sine Wave Input to Sooch CM DAC



Sine Wave Output

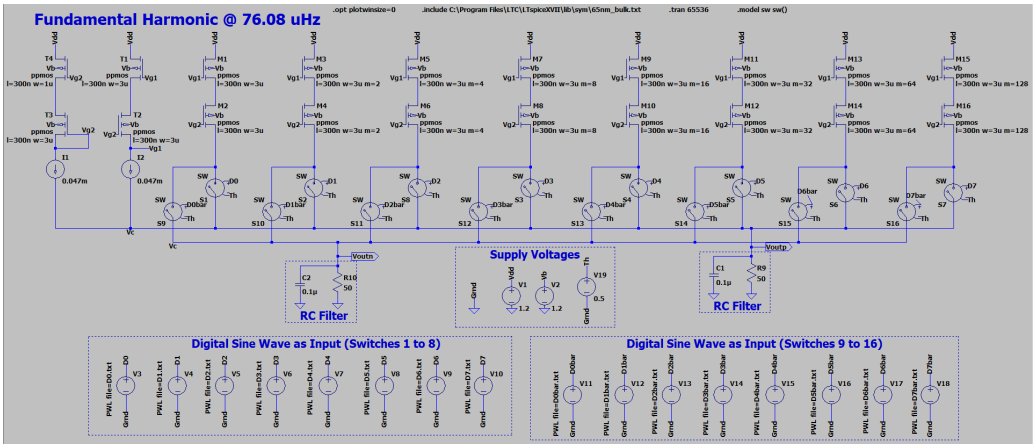
5.2 Current Steering DAC

Now we are going to give the digitized sine wave as input to our current steering DAC. For that, we also need to generate the complementary (logical NOT) values for the above data points and thus the following bit of code might be helpful.

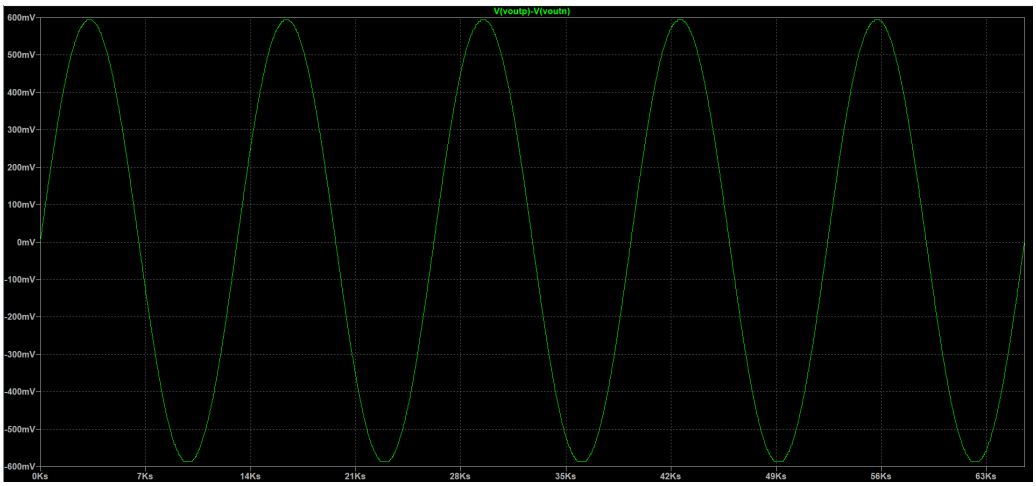
```
M=readmatrix('D0.txt');                    %to read the digital values from D0
N=M;
N(:,2)=~(M(:,2));                          %to obtain the logical not values of those in D0
writematrix(N,'D0bar.txt','Delimiter','tab')  %to write them into another matrix N and store them in a file
```

Required MATLAB Code

Below are the respective schematic and output.



Sine Wave Input to Current Steering DAC



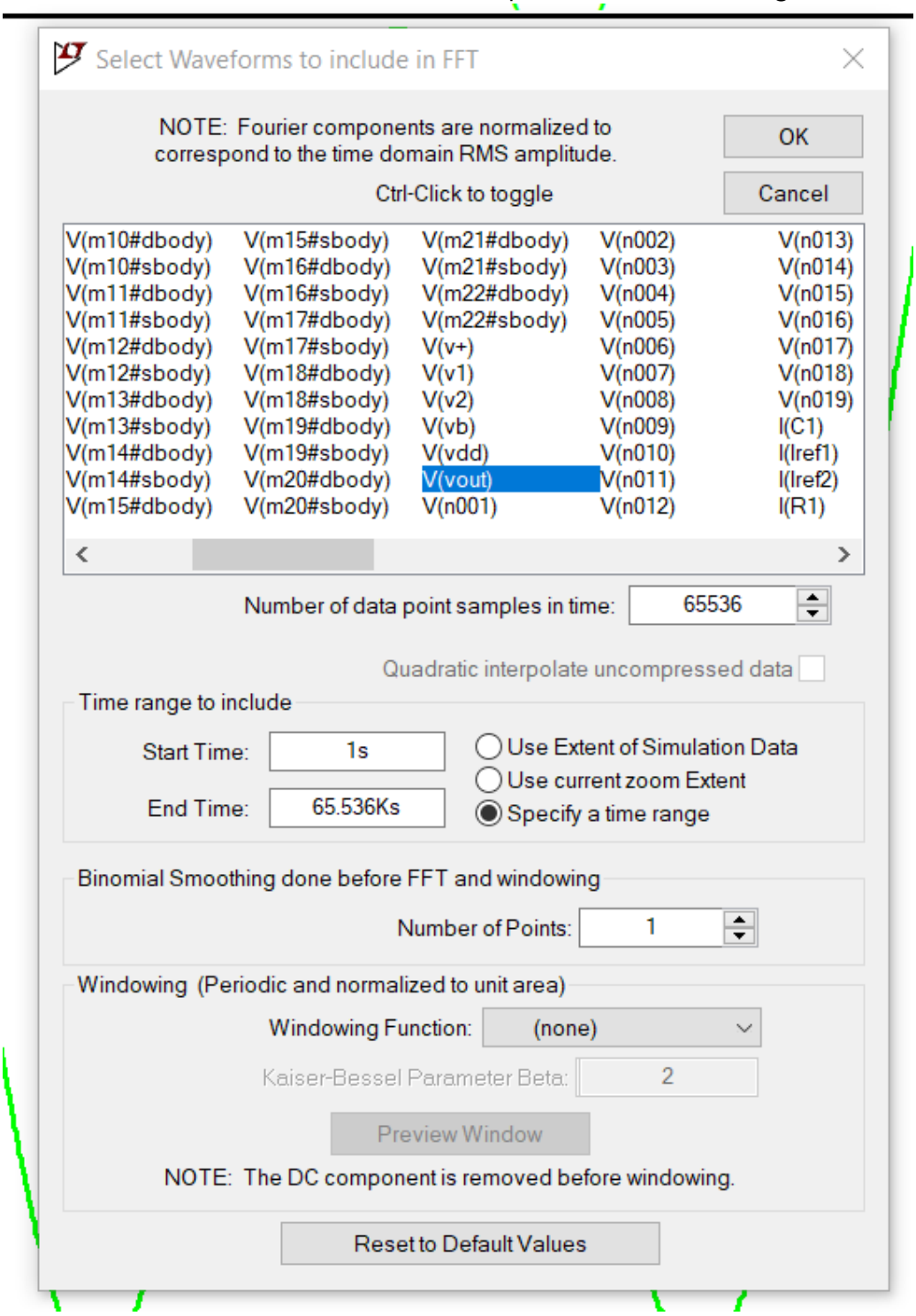
Sine Wave Output

6 FFT Analysis

The FFT (Fast Fourier Transform) analysis gives us a measure of how good our DAC is. We can also know the percentage of other harmonics present through the FFT analysis. Now we will analyse the FFT of the analog sine wave obtained from Low Voltage Sooch Cascode Current Mirror DAC and Current steering DAC.

6.1 Using Low Voltage Sooch Cascode Current Mirror

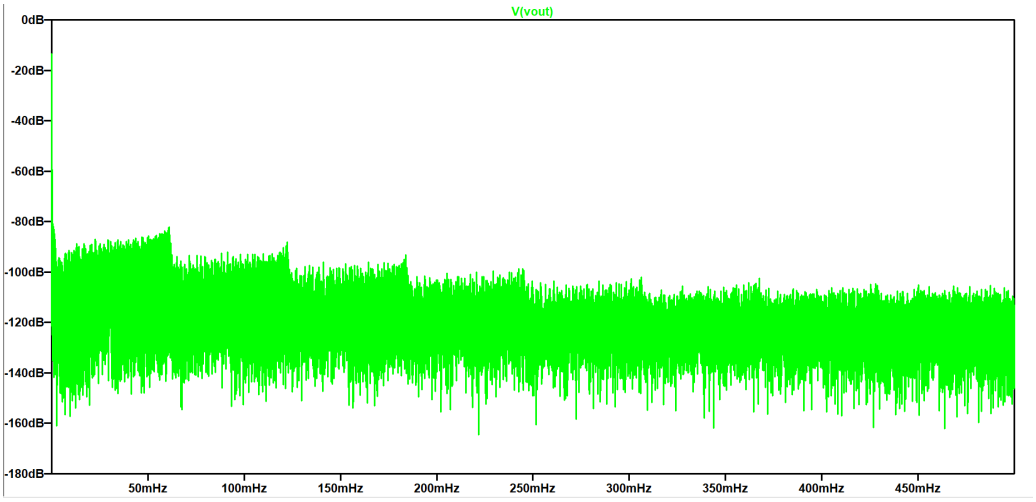
To obtain FFT of sine wave we need to follow the steps as shown in below figure.



Sooch CM DAC

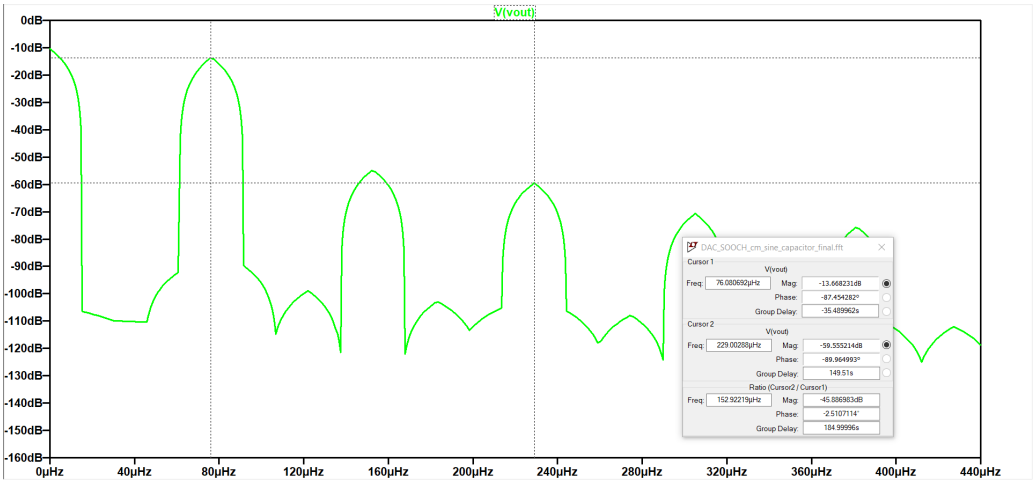
After we have selected all the fields and click OK, new FFT plot opens and the X-axis i.e., the frequency is in logarithmic scale. We have to uncheck the logarithmic field by right clicking on the X-axis and unchecking it. Then we get desired FFT analysis of our sine waveform as shown in

below figure.



FFT analysis

We need to zoom in to see the fundamental, second and third harmonics. We can see that the fundamental harmonic is at 76.08μHz. Below figure shows the remaining harmonics.



Harmonics

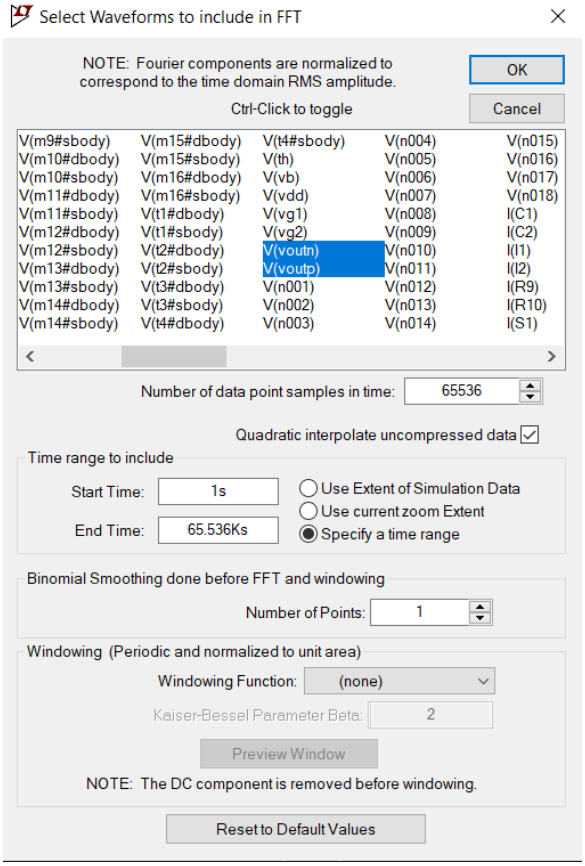
We got decent difference of 39.18dB between fundamental harmonic and second harmonic and a good amount of difference of 45.89dB between fundamental and third harmonic. The difference between fundamental and third harmonic is called linearity of the DAC. We got linearity of our DAC equal to 45.89dB and a point to mention is that linearity greater than 41dB is good.

6.2 Current Steering DAC

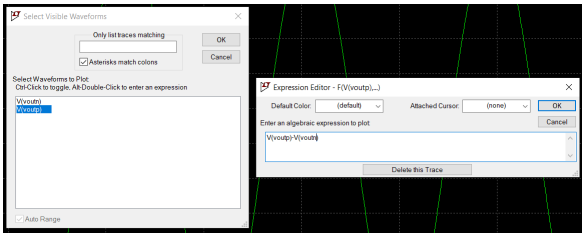
By looking at the output of our current steering DAC, we can say that our current steering DAC is pretty good. However let's carry on the FFT analysis for this too. We observe some interesting

phenomena here.

LTSpice does not plot the FFT of an expression by default. To get the FFT plot of the voltage difference, follow the steps as shown in the below figure but here you need to select both fields V(voutp) and V(voutn). Then another dialog bax appears which you can enter your desired expression by alt + double click.

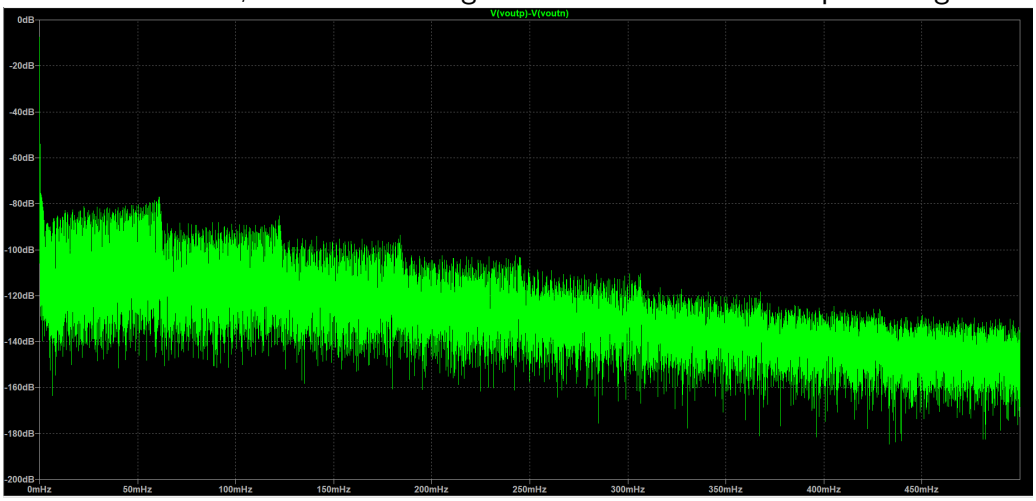


Current Steering DAC



Enter the expression

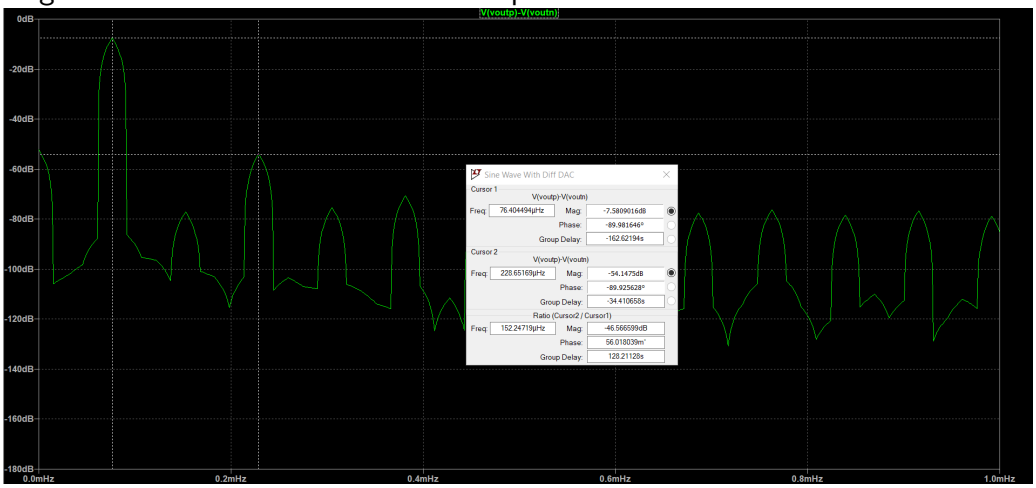
Same as in the above case, uncheck the logarithmic field. The FFT plot we get is as follows.



FFT Analysis

We zoom in to observe the harmonics clearly. We see that the fundamental harmonic is around 76

μHz. The figure below shows us the zoomed in plot.



Harmonics

We get the linearity of the DAC to be 46.57dB but here we can make interesting observations. The second harmonic is greatly suppressed when compared to single ended as you can see in the above figure. Not only the second harmonic but also all the other even harmonics got significantly suppressed in the FFT of our current steering DAC. Only the odd harmonics are clearly visible.

7 Glitches

Glitches are a limitation at high-speed data transfers. They occur during a transition between two output values, as an undesired output value due to different signal propagation delay. For a short period of time a false code could be represented at the output. For example if the code transition is from 0111 to 1000 and if the Most Significant Bit(MSB) is switching faster than the Least Significant Bit(LSB), the code 1111 may be present for a short time. This code represents the maximum value and hence the glitch would be large.

Conclusion

• Using the 65nm technology, both an 8-bit single ended and current steering DACs were appropriately built. We looked at different current mirrors incorporated DACs and analysed their performance.

• We observed that DAC build using Low Voltage Sooch Cascode Current Mirror has best performance.

• Both schematic and simulation results proved appropriate operation of the DAC, with a minor pseudo - glitching issue in the simulation results caused by the inaccurate mirroring and CLM. We also looked how RC filter is used to filter out the glitches.

• We have also seen that in the single ended case, the step value is IR whereas in differential case, the step value is 2IR. This proves our theoretical knowledge.

• Running a Fast Fourier Transform analysis on the result discussed earlier enables us to find the linearity of the DAC. The linearity is evaluated to be approximately 46dB, which is a reasonable value for an 8-bit resolution DAC.

• The plot of the Fast Fourier Transform in the differential case shows the disappearance or atleast suppression of all the even harmonics and only the odd harmonics are visible.

• As is already known, we can use NMOS or PMOS for mirroring depending on whether we want to sink current or source current respectively.

Improvements

For this project, we have taken the following assumptions :

▲ A golden current source of 47 μA is available.

▲ Ideal switches exist.

• In reality, MOSFETS are used in place of switches. The MOSFETS are set appropriately such that they come to cutoff or triode regions in accordance with the digital input. So in our DAC design, the ideal switches can be replaced with NMOS or PMOS transistors so that the practicality gets reflected.

• Also we know that no golden current source exists. The golden current source used for mirroring is generated by a method called bandgap reference. Hence by using bandgap reference, we can generate the 47 μA golden current source and incorporate it into our design. By doing the above things, our DAC design is further left with no more assumptions and all the reality gets in.