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Better PCBs in Eagle

by Nate | November 06, 2008 | 41 comments Skill Level: * Intermediate

Designing a Better PCB:

We are constantly pushing ourselves for better printed circuit boards (PCB). One thing we've learned is that PCB fab houses (such as Advanced Circuits, BatchPCB, PCB123, Gold Phoenix, Bare Bones PCB, anyone really) have a very hard job to do. Creating a PCB is not an easy task and there are many ways for a fab house to mess it up. Unfortunately, fab houses tend to spend less time on prototypes than on production runs. Therefore, we try to design products and PCBs for 'manufacturability'. This tutorial will show you how to minimize the number of ways the fab house can screw up a PCB.

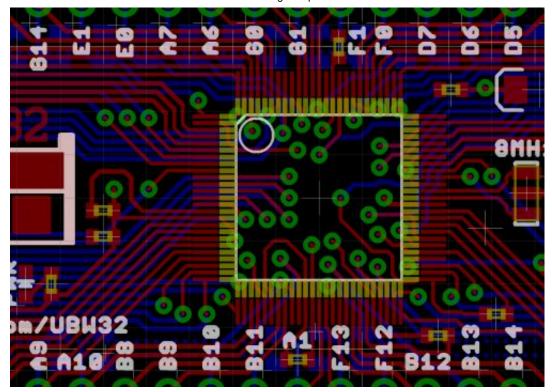
We've messed up piles of PCBs over the years. We want to share with you some of the DFM (design for manufacture) rules and tricks and tips we've learned to get a good PCB, every time. If you're creating a prototype PCB, we highly recommend you use these rules to increase the chances that your proto will work!

Important Files:

- SparkFun Eagle Rules for designing PCBs in Eagle. This is a list of rules that we have forged over the years. You are welcome to use or dismiss them. Some only apply directly to the engineers here at SparkFun, most of the rules apply to everyone.
- SparkFun DRC file for Eagle. Right click on the link, select 'Save Link As' and save this file to your Eagle/dru directory.
- SparkFun CAM file for Eagle. Right click on the link, select 'Save Link As' and save this file to your Eagle/cam directory.

Trace Width and Spacing:

Just because a fab house can handle down to 5mil traces and 6mil space doesn't mean you should design with those sizes. If your board can be routed with 10mil traces and 10mil spaces, do it! The smaller you make things, the more likely you will get a PCB with broken trace (traces less than 10mil) or two traces touching each other (less than 10mil spacing between traces).

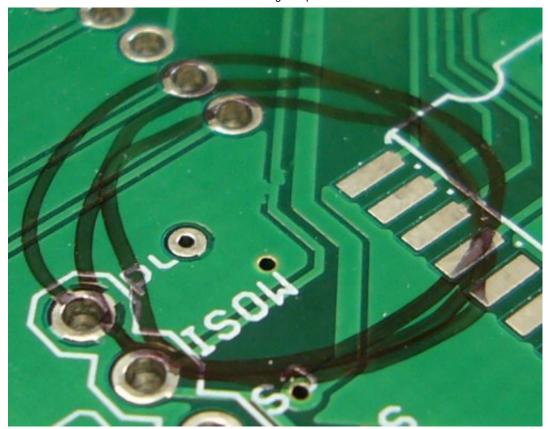


PIC32 development board

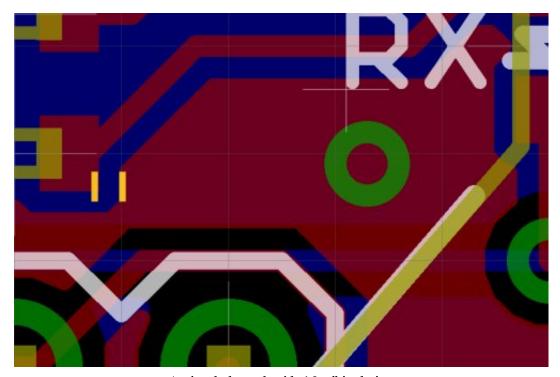
Even complex boards with tight pitch packages and a horrible rat's nest of traces can be routed with 10mil traces and 8mil spacing. Next time you route a board, try it with 10mil traces and see just how far you can go – you'll be suprised. If things get really tough, 8mil is usually ok. The goal of all these tricks and rules is the limit the spots where manufacturing failures could occur.

Isolate:

A ground (or power) plane is a good idea on some projects. But a plane (sometimes called a polygon plane) increases the odds of the plane being mistakenly 'poured' onto a trace.

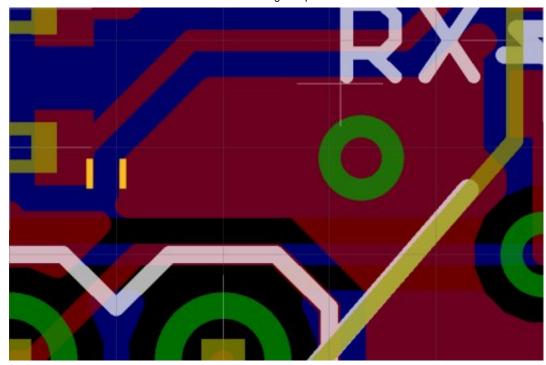


What the?! Bad ground pour. Bad!



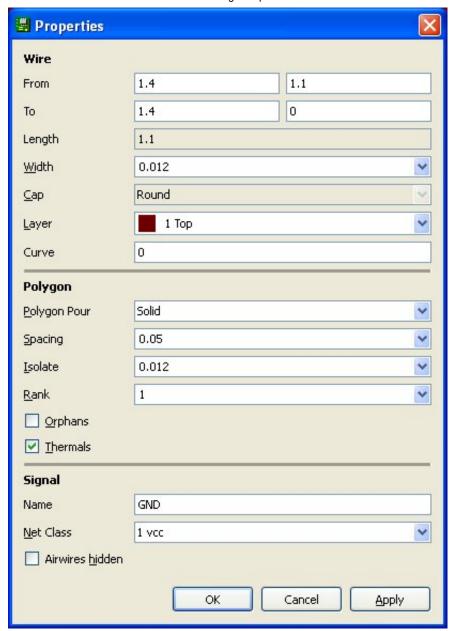
A simple board with 10mil isolation

We recommend you increase the default 10mil isolation in Eagle of a polygon pour to '0.012' or 12mil. This will pull the plane away from the signal traces, thus decreasing the odds of a manufacturing failure. This will however potentially break ground connections so be sure to check your rats nest!



Increased isolation good, ground plane break may be bad.

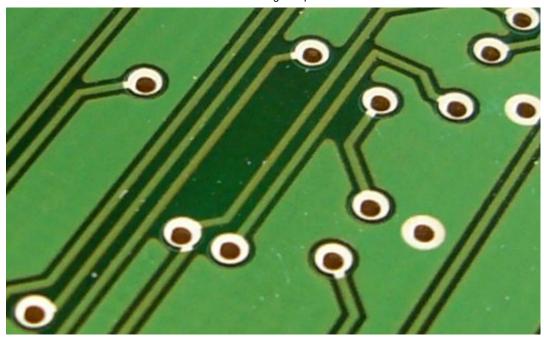
To increase the isolation on an existing polygon, click on the 'i' button for information, then click on the border of the polygon.



Then change the Isolate from a default of 0.010 to 0.012.

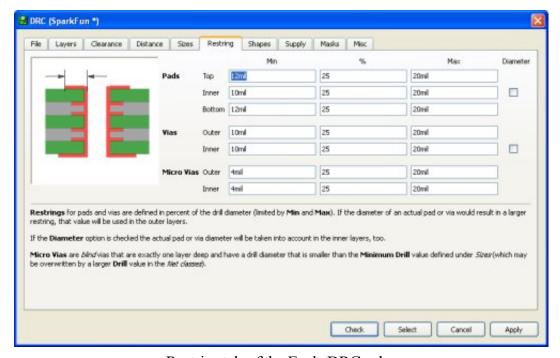
Annular Ring:

Another problem that we have found is sloppy drill hits by a fab house. To connect a trace from one side of the PCB to the other, we use a via. A via is composed of a drilled hole, two circles of copper larger than the hole on either side of the board, and connecting copper inside the hole to connect the circles on either side of the board (these are called plated through holes). Vias make PCBs work. The problem is the size of the copper circles. If the drill hit is not in the middle of the circles, the drill hole can potentially break the via and the trace connected to the via.



Sloppy drill hits in the center of the vias

All of the vias shown above work, but they are marginal. This is one board out of a run of many and the other boards could be even worse. If the drill hit is too far off center, it can cut through the trace connecting to the via. To help protect against this, we increase the size of the annular ring around the vias. To do this, we edit the Eagle DRC rules (click on menu Tools->DRC).



Restring tab of the Eagle DRC rules

Click on the tab labeled 'Restring'. The default for pads on the top and bottom is 10mil. We change this to 12 mil to increase the annular rings by 20%. This will increase the chances that our prototype PCB will work. This DRC setting is set to 12mil in the SparkFun DRC file.

Gerber File Generation:

Generating good gerber files of your PCB is the final step that causes

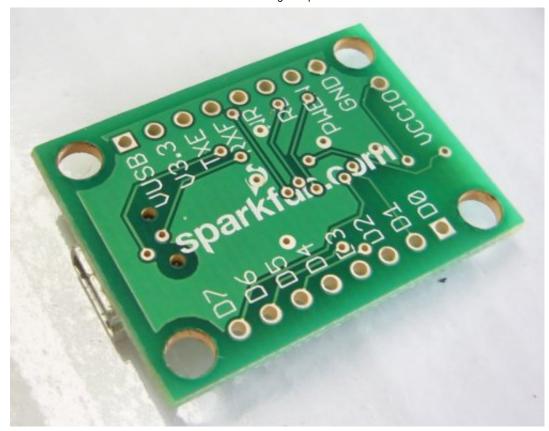
many people to fail. Eagle uses a CAM file to create the gerber files to have a PCB made. We have seen tons of people create horribly defective gerber files. Please start with our CAM file – and modify if you really need to. We've used this CAM file thousands of times without problems.

We've changed the default Eagle CAM file so that it *does not* mirror any of the bottom layers (number one problem with gerber submissions!), it outputs a standard Excellon drill file (second most common error is a missing drill file), and captures only the tPlace layer onto the silkscreen layer (this will cause all part identifiers and values to *not print* on the silkscreen). Put all text and labels onto the tPlace layer that you want to see printed on the board.

Tenting:

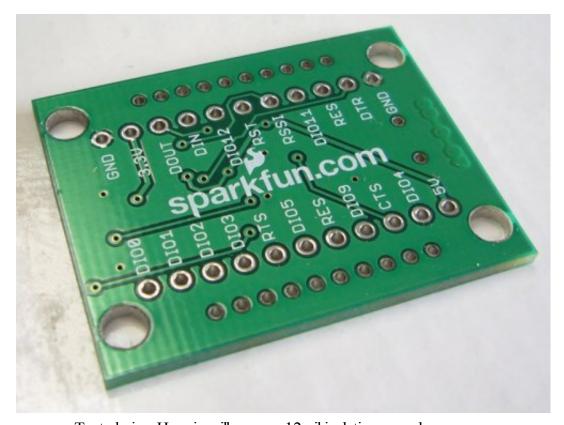
Tenting refers to

the soldermask and vias. The vias on a board may be left exposed or covered up by the soldermask. We've found that covering up the vias (or 'tenting' them) decreases the chances that the silkscreen labels will be broken and gives the overall board a much better look. Don't worry, you can still probe a tented via for voltage and continuity with a multimeter – the soldermask will break down when you insert the probe into the hole. However, it will be much more difficult to solder to a tented via.



Untented vias. Ugly silkscreen. Small 10mil isolation on plane.

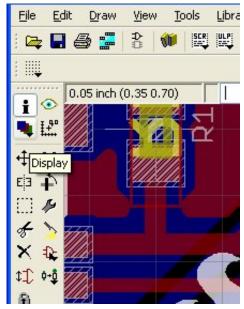
The bottom of the FT245RL breakout is shown above. The pin labels are completely un-readable because an untented via falls right in the middle of 'WR' and 'RE'. Is that 'RE'... I can't remember.



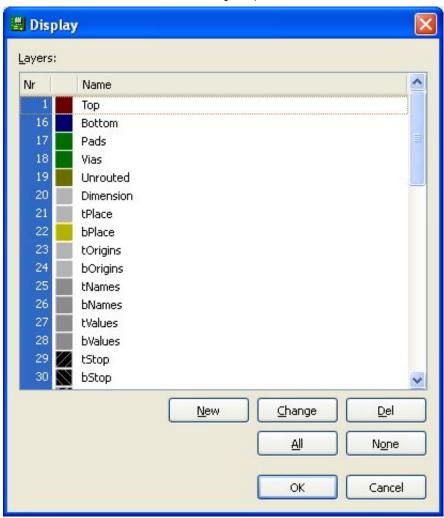
Tented vias. Happier silkscreen. 12mil isolation on polygon pour.

Bottom view of the XBee-Explorer product. I have been known to move a via to avoid a label as well, but that's just me.

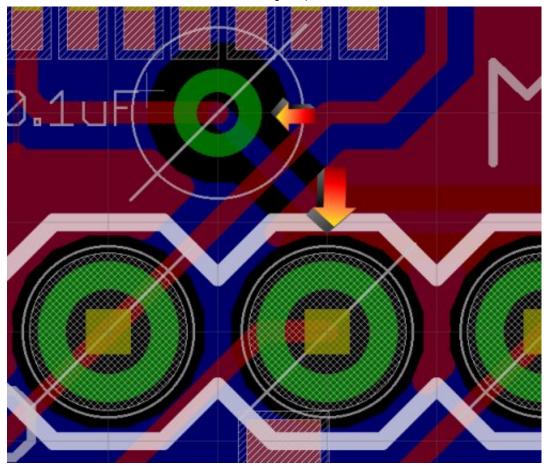
Tenting is taken care of in Eagle by modifying the DRC rules. To see if the vias will be tented or not, turn on all the layers by clicking on the display button:



The Display button is below the 'i' button.

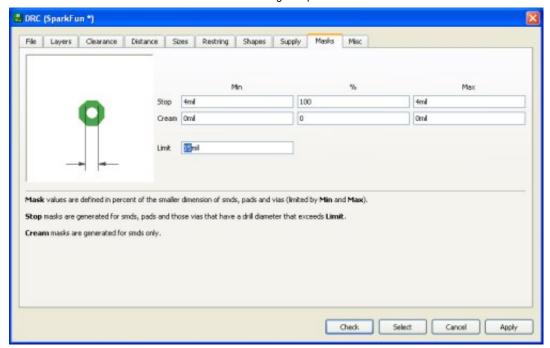


Click on 'All' then OK.



Turning on all the layers will create a lot of noise in the display of the board. What you are looking for is the white hatch marks indicating where the will be a *lack* of solder mask. The upper arrow points to a via that has no hatch marks, indicating there will be *no lack of soldermask* on that via (tenting it). The lower arrow points to a large hole with a white hatch mark on top of it. This is a solder point that needs to be exposed. The white hatch marks indicate there will be a *lack of solder mask* over this hole, exposing it so that we can solder to it.

To tent your vias, open the DRC rules on your current design (Tools->DRC menu).

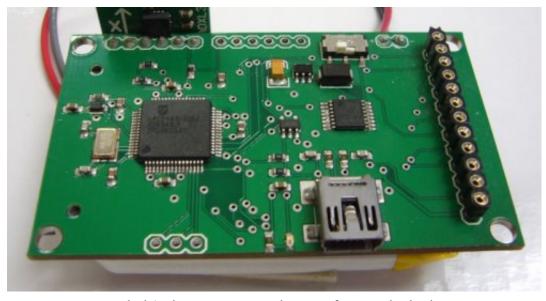


DRC Rules – Masks tab

Then increase the limit value to larger than the vias you are using. For instance, if the vias on your board are the default 0.023mil, then change the limit to 25mil and all drill hits under 25mil (0.025) will be covered in soldermask. Be careful! Don't set this number too high or you will cover important holes, like those meant to solder on connectors. The DRC setting is set to 25mil in the SparkFun DRC file.

Label everything, all the time:

This is another cosmetic issue I see so often it hurts. You should label every button, switch, LED, pin, and especially power connectors on your board. Every one of them!



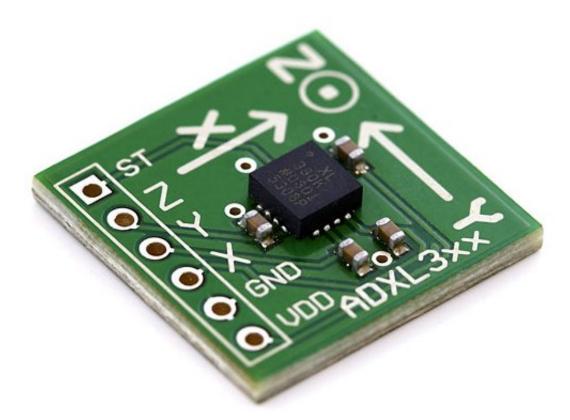
Labels! They are so easy, but so often overlooked.

- 1. What does the LED next to the USB connector mean? Is it a power LED? Or a status LED?
- 2. There's a slide switch, next to the power connector in the upper right corner. Is it a power switch? If so, which way is on?
- 3. There's lots of pins on this board none of which are labeled. Why not? Silkscreen is free!
- 4. The one good thing about this board is the small, but apparent '+' and '-' where the battery connects. This is good! But an acceptable voltage range would have been helpful. '3-7V' or some such indicator is extremely useful.

Sure, you might remember what the LED means today, but what about 3 months from now when you dig it out of your parts bin?

I personally do not put any part indicators on my boards. When assembling the board, sure, I need to know where the 10k resistors go, the 0.1uF caps, and the LED colors. But that's all part of the assembly sheet. Once the device is built, I most likely will never need to know that a given capacitor is '22pF' and certainly I don't need to know that the big IC on the board is labeled 'U1' (what help is that anyway?). If I'm really troubleshooting a board, I will have the schematic and layout open anyways.

On the flip side, it would be nice to know what the pin functions are – right there, clearly labeled, so I don't have to guess. Every time I connect power, it would be really nice *not* to say a prayer and hope I don't hook power up backwards. And if I do hook power up backwards, is that LED supposed to come on? Or is that just a link connection LED? Oh shoot!



The ADXL330 Breakout

Here is a good example of clear pin labels as well as worthy functional labels. When playing with this accelerometer, you will probably want to know what axis is where. Yes, you could look up the datasheet but why not put the information right there on the board?

We hope these basic rules help you prevent as many mistakes as possible! We certainly have our share of coffee coasters and hope you have one less.

Cheers!

Nathan Seidle

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