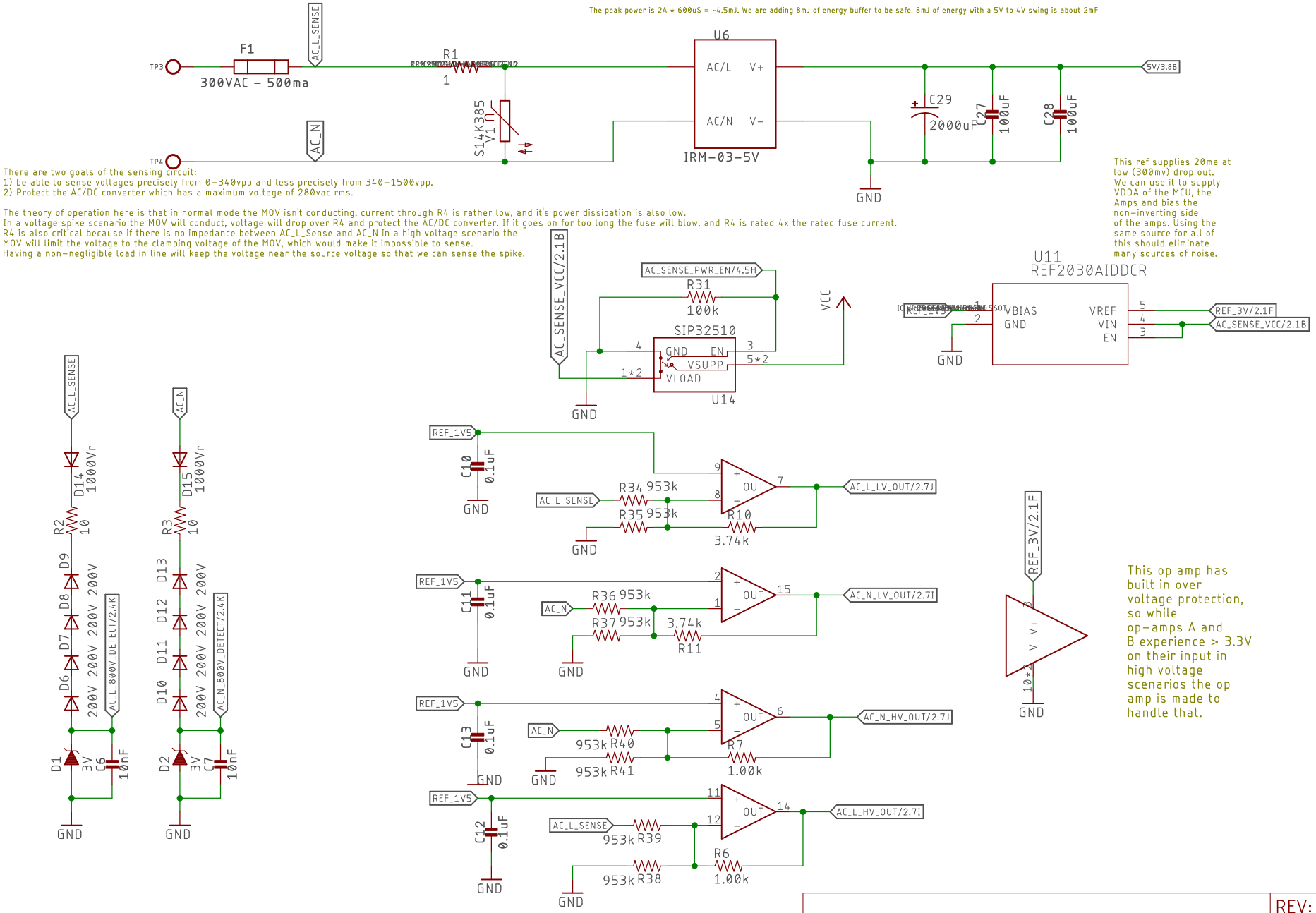

1

PowerWatch	REV: G
Author: Joshua Adkins	
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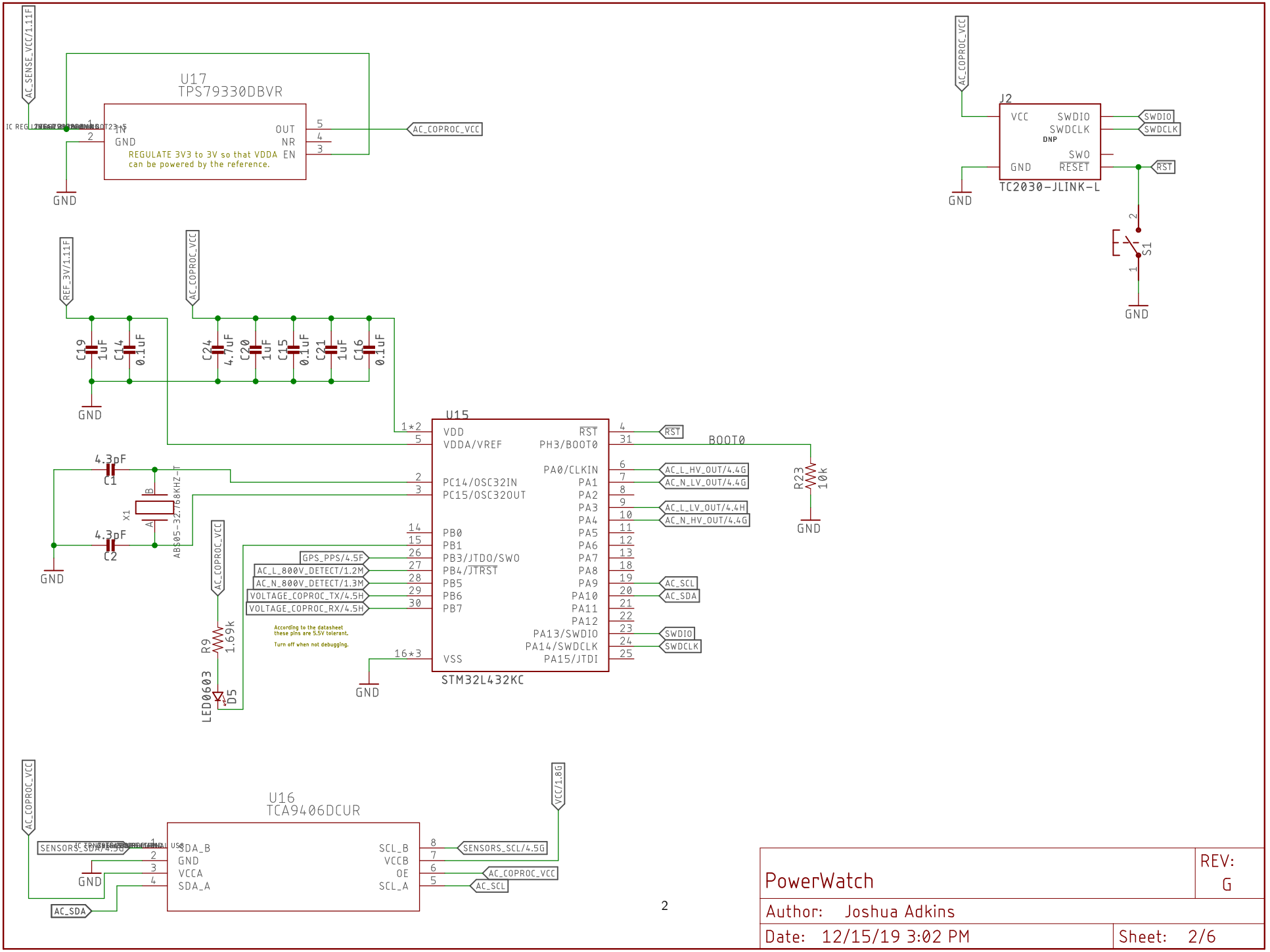
AC_SENSE_VCC/1.11F
U17
TPS79330DBVR
IN
GND
OUT
NR
EN
REGULATE 3V3 to 3V so that VDDA can be powered by the reference.
AC_COPROC_VCC
GND
AC_COPROC_VCC
J2
VCC
SWDIO
SWDCLK
DNP
SWO
GND
RESET
SWDIO
SWDCLK
RST
TC2030-JLINK-L
GND
S1
GND
REF_3V/1.11F
AC_COPROC_VCC
C19 1uF
C14 0.1uF
C24 4.7uF
C20 1uF
C15 0.1uF
C21 1uF
C16 0.1uF
GND
U15
VDD
VDDA/VREF
PC14/OSC32IN
PC15/OSC32OUT
PB0
PB1
PB3/JTDO/SWO
PB4/JTRST
PB5
PB6
PB7
VSS
RST
PH3/BOOT0
PA0/CLKIN
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PA8
PA9
PA10
PA11
PA12
PA13/SWDIO
PA14/SWDCLK
PA15/JTDI
STM32L432KC
BOOT0
R23 10k
GND
4.3pF
C1
4.3pF
C2
X1
ABS05-32.768KHZ-T
GND
GPS_PPS/4.5F
AC_L_800V_DETECT/1.2M
AC_N_800V_DETECT/1.3M
VOLTAGE_COPROC_TX/4.5H
VOLTAGE_COPROC_RX/4.5H
According to the datasheet these pins are 5.5V tolerant.
Turn off when not debugging.
AC_L_HV_OUT/4.4G
AC_N_LV_OUT/4.4G
AC_L_LV_OUT/4.4H
AC_N_HV_OUT/4.4G
AC_SCL
AC_SDA
SWDIO
SWDCLK
AC_COPROC_VCC
R9 1.69k
LED0603
D5
GND
AC_COPROC_VCC
U16
TCA9406DCUR
SDA_B
GND
VCCA
SDA_A
SCL_B
VCCB
OE
SCL_A
VCC/1.8G
SENSORS_SCL/4.5G
AC_COPROC_VCC
AC_SCL
GND
AC_SDA
PowerWatch
REV: G
Author: Joshua Adkins
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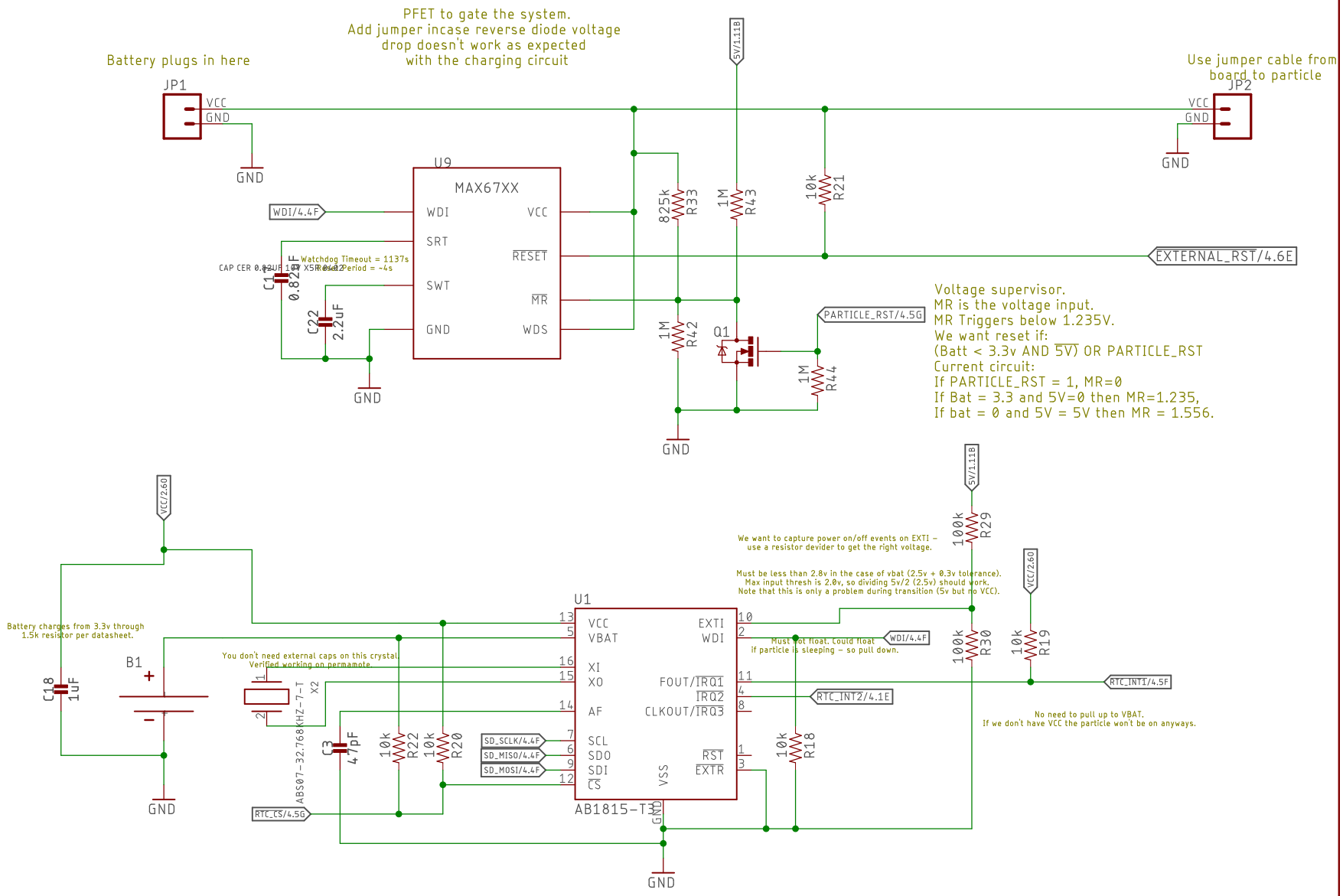

PowerWatch		REV: G
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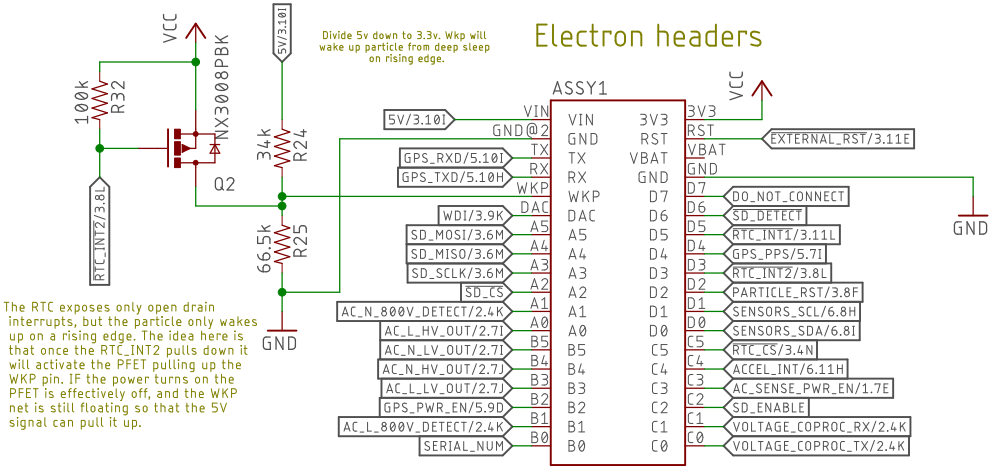
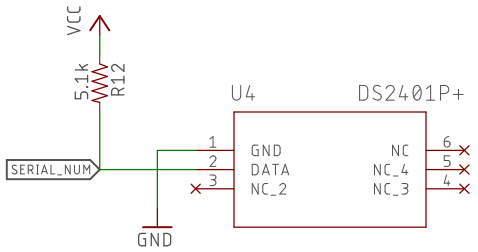
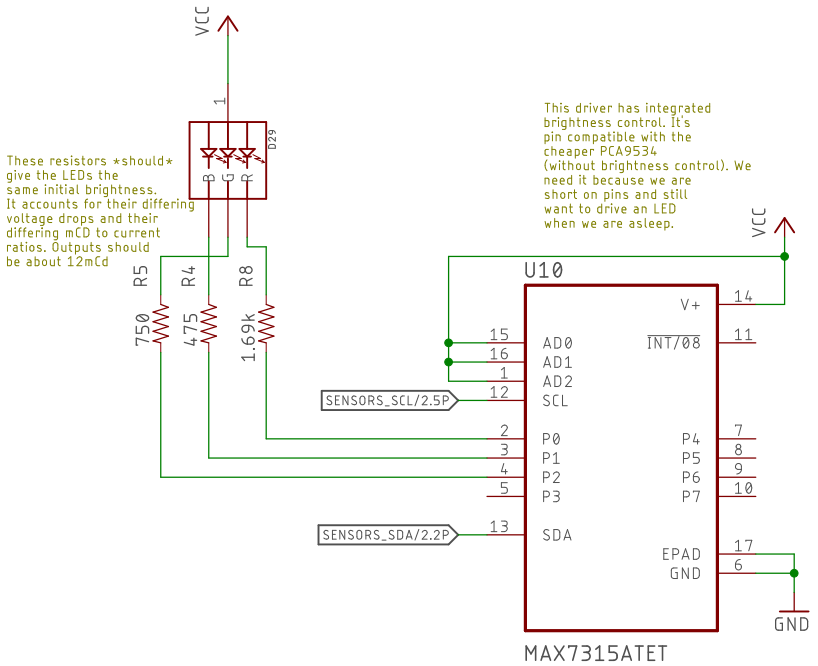
Headers

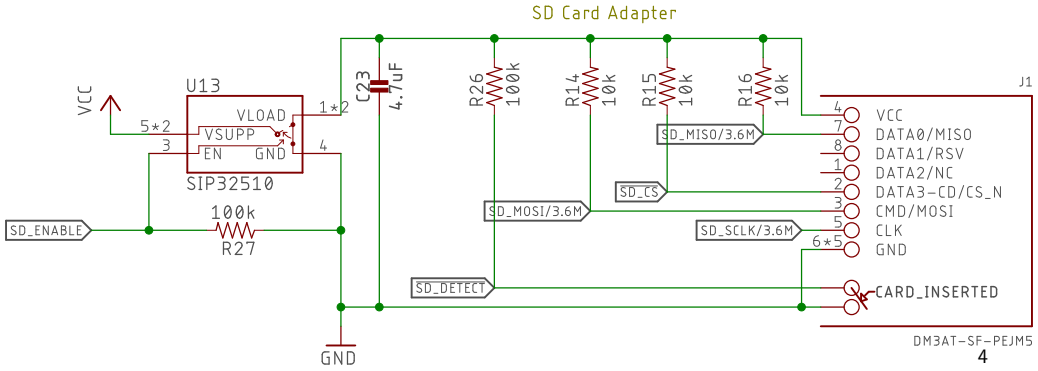
Electron headers



The RTC exposes only open drain interrupts, but the particle only wakes up on a rising edge. The idea here is that once the RTC_INT2 pulls down it will activate the PFET pulling up the WKP pin. IF the power turns on the PFET is effectively off, and the WKP net is still floating so that the 5V signal can pull it up.







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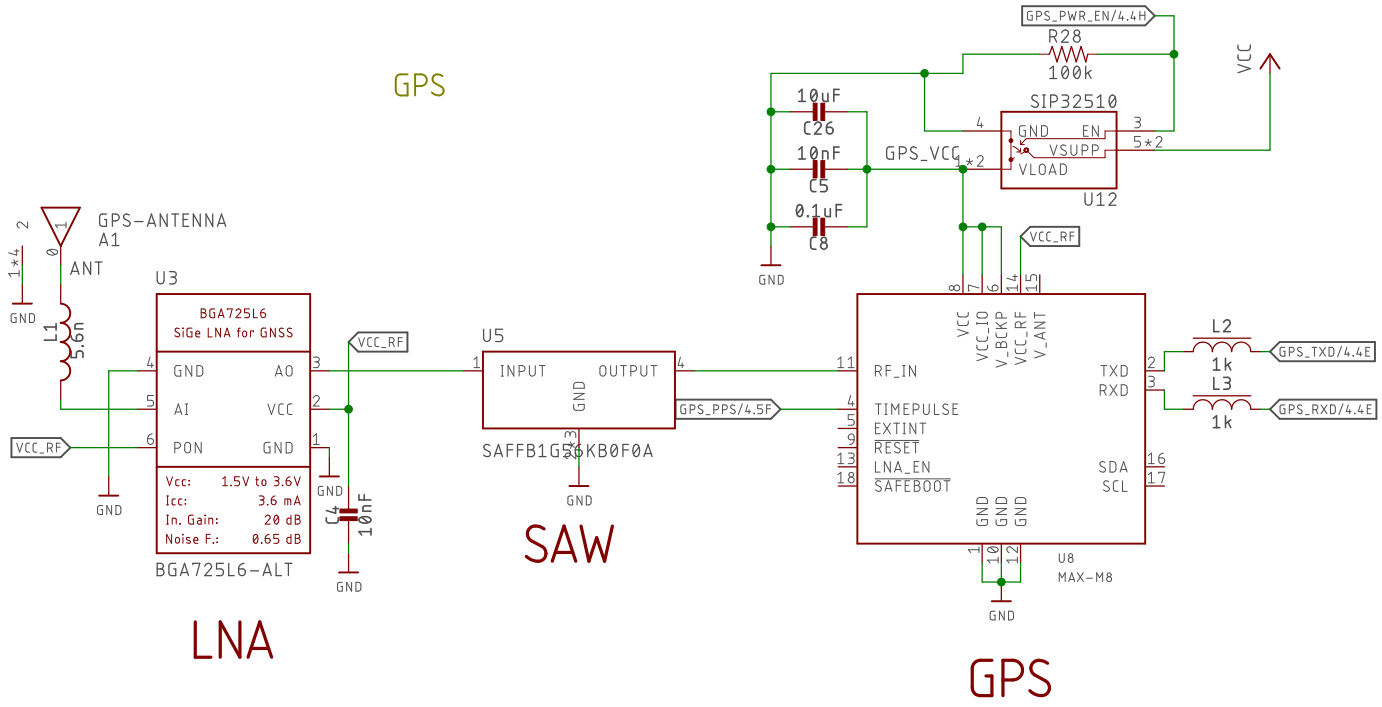
https://www.u-blox.com/sites/default/files/MAX-8-M8-FW3_HardwareIntegrationManual_%28UBX-15030059%29.pdf



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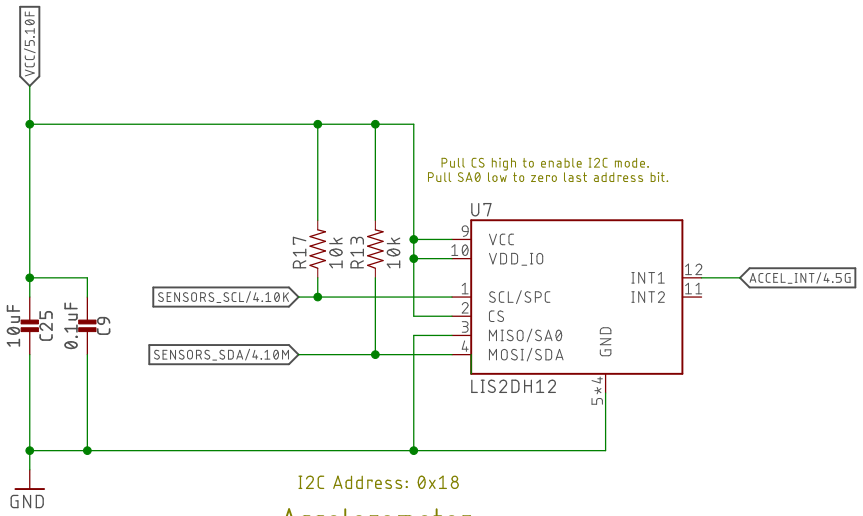
Sensors



Accelerometer

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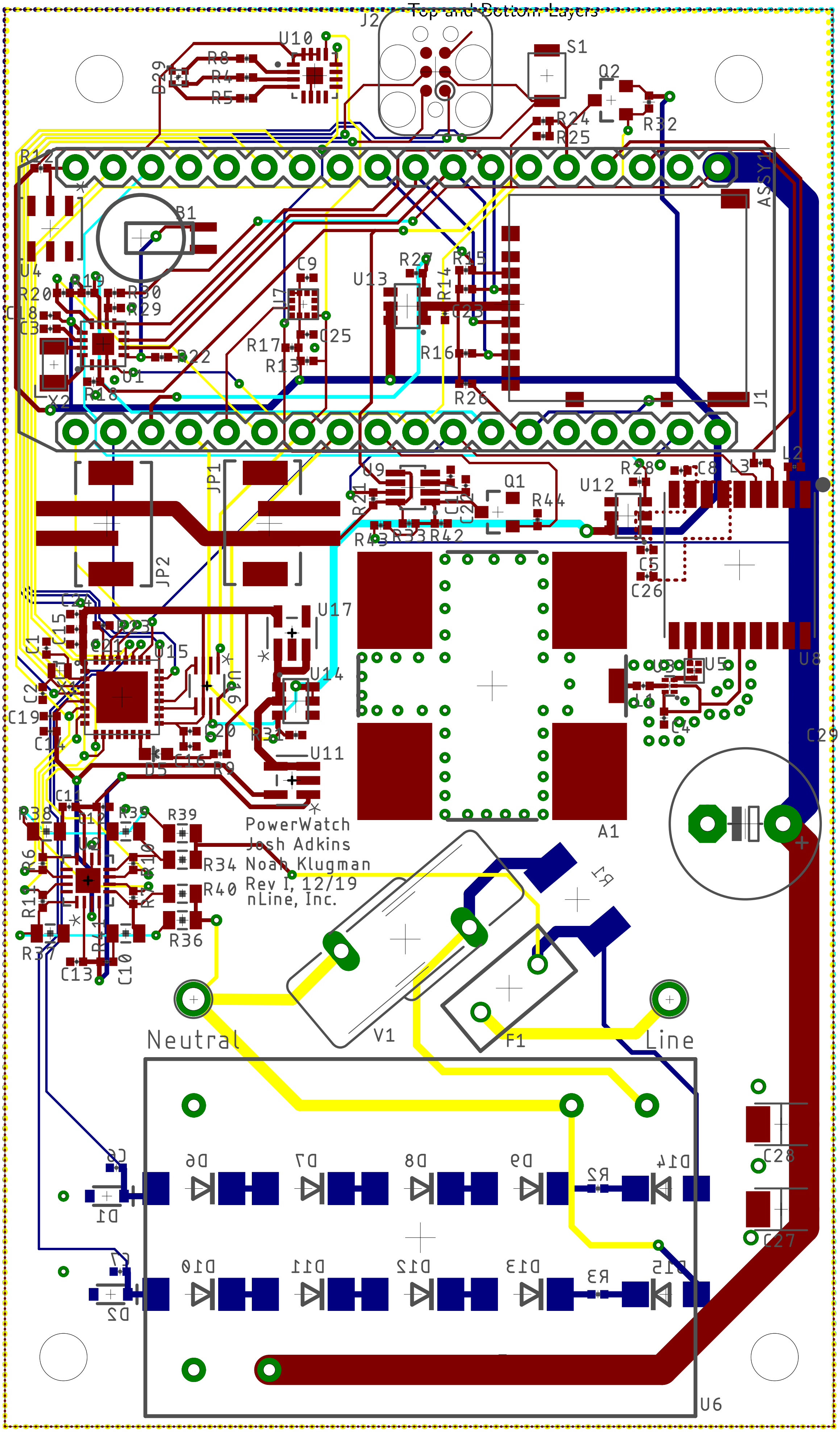
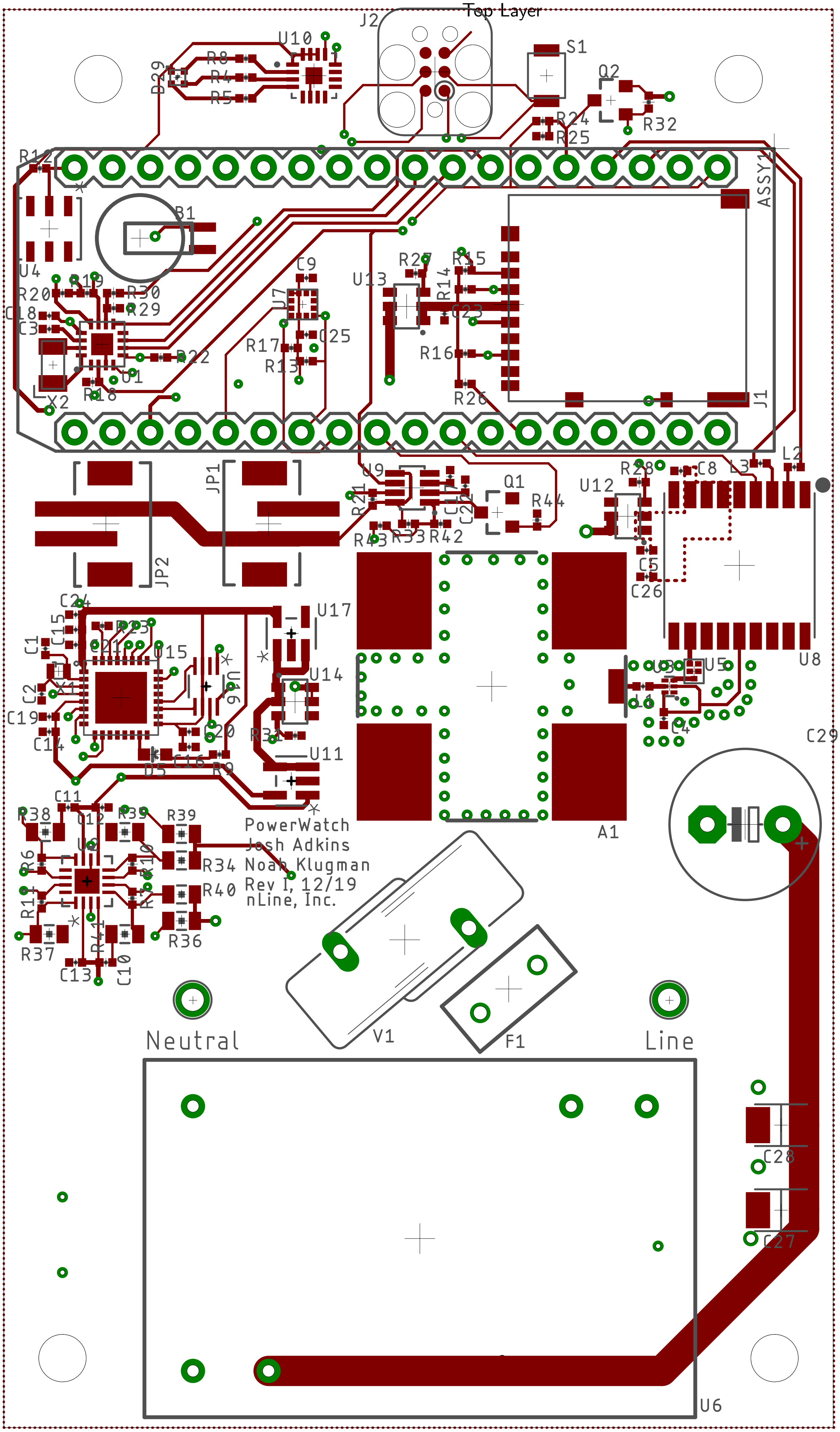
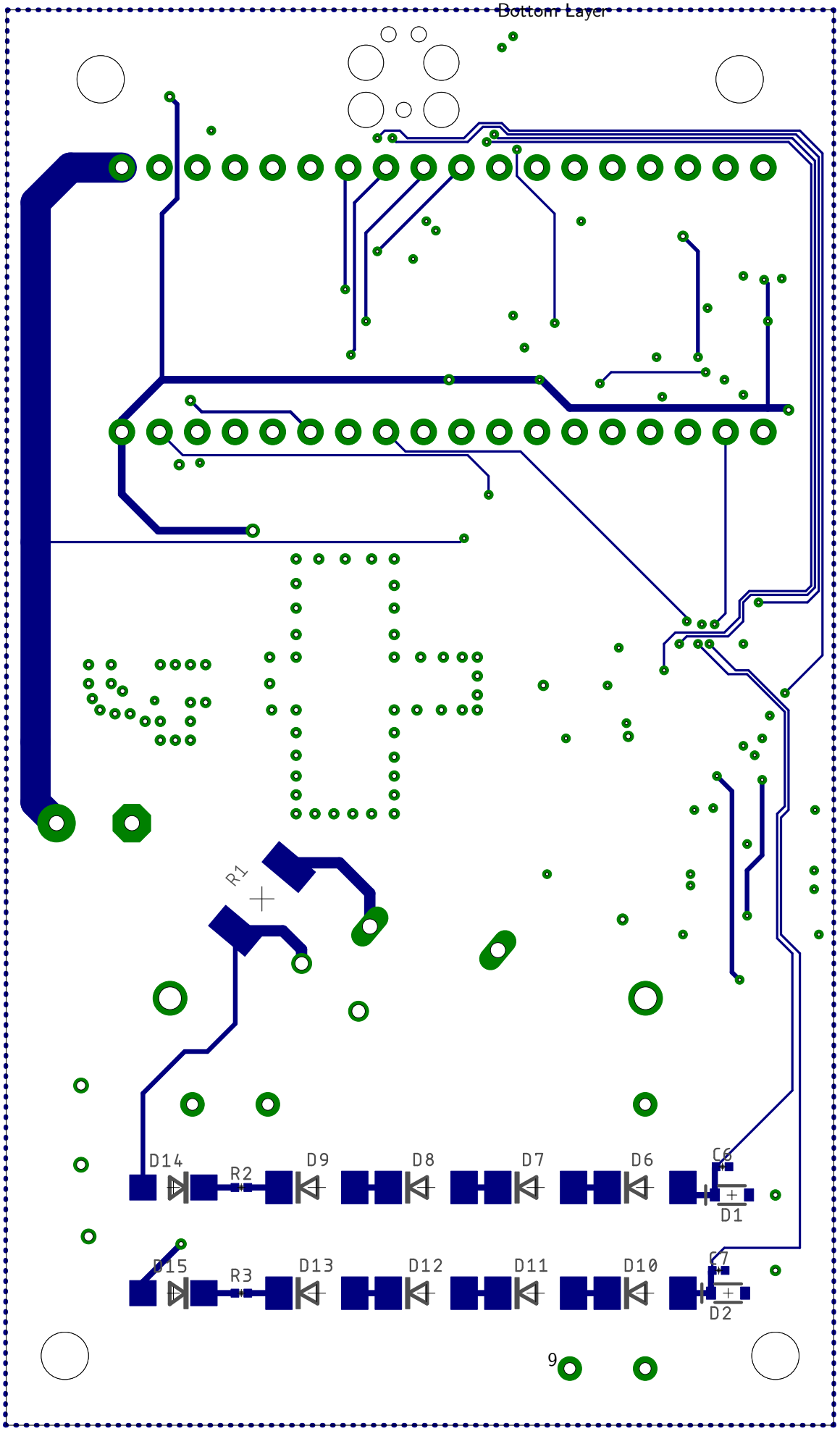
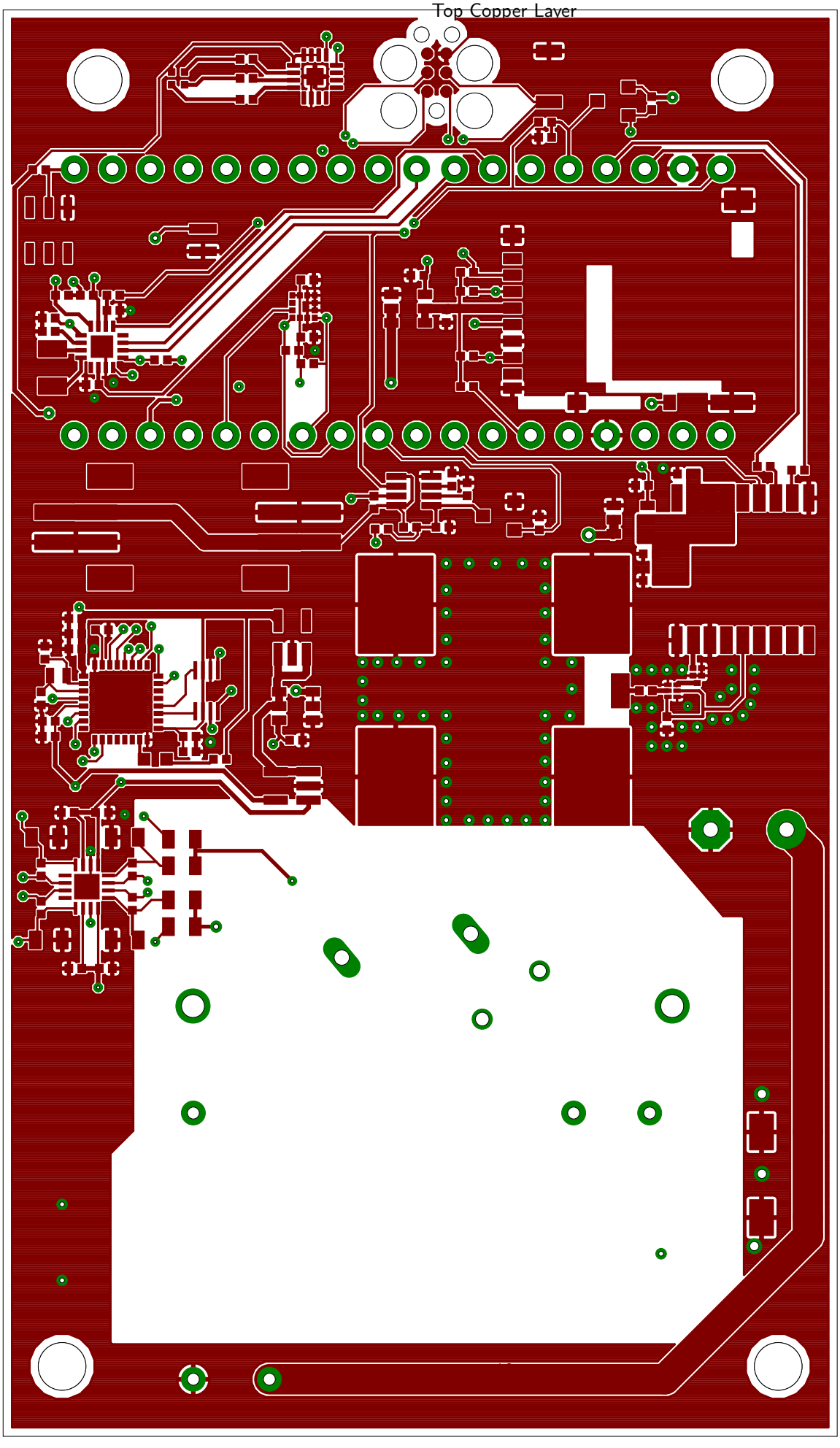
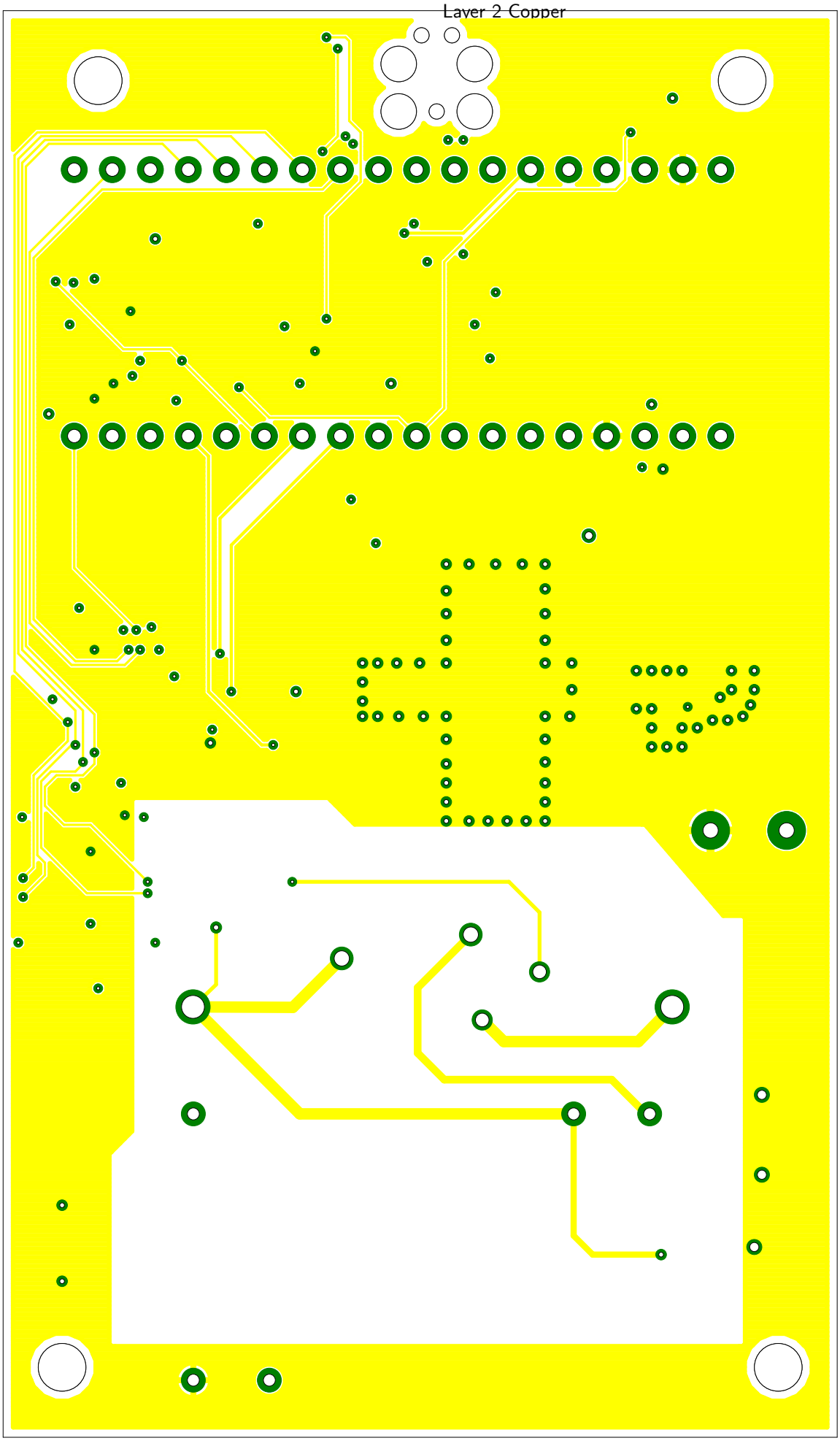
Top and Bottom Layers

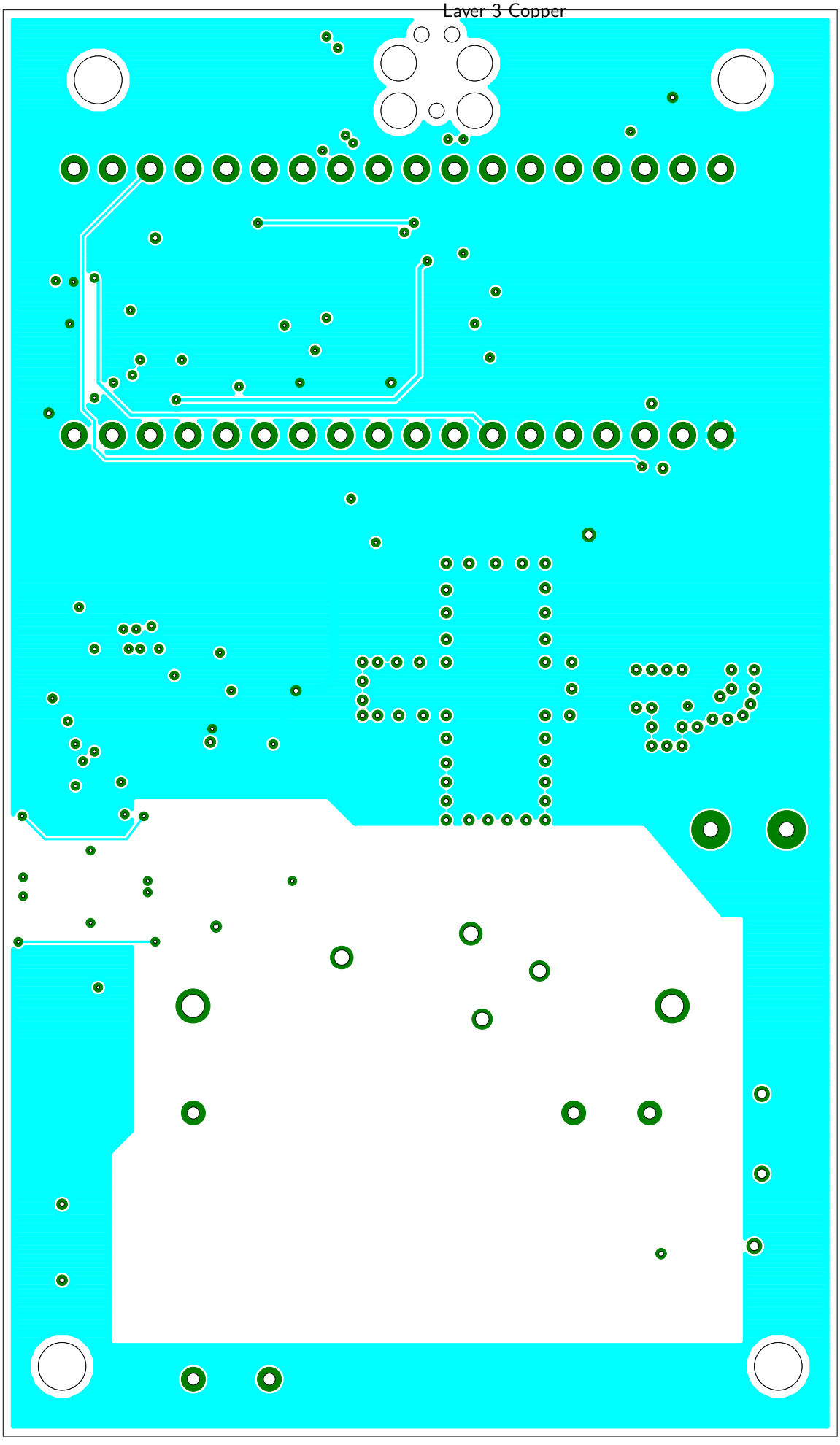


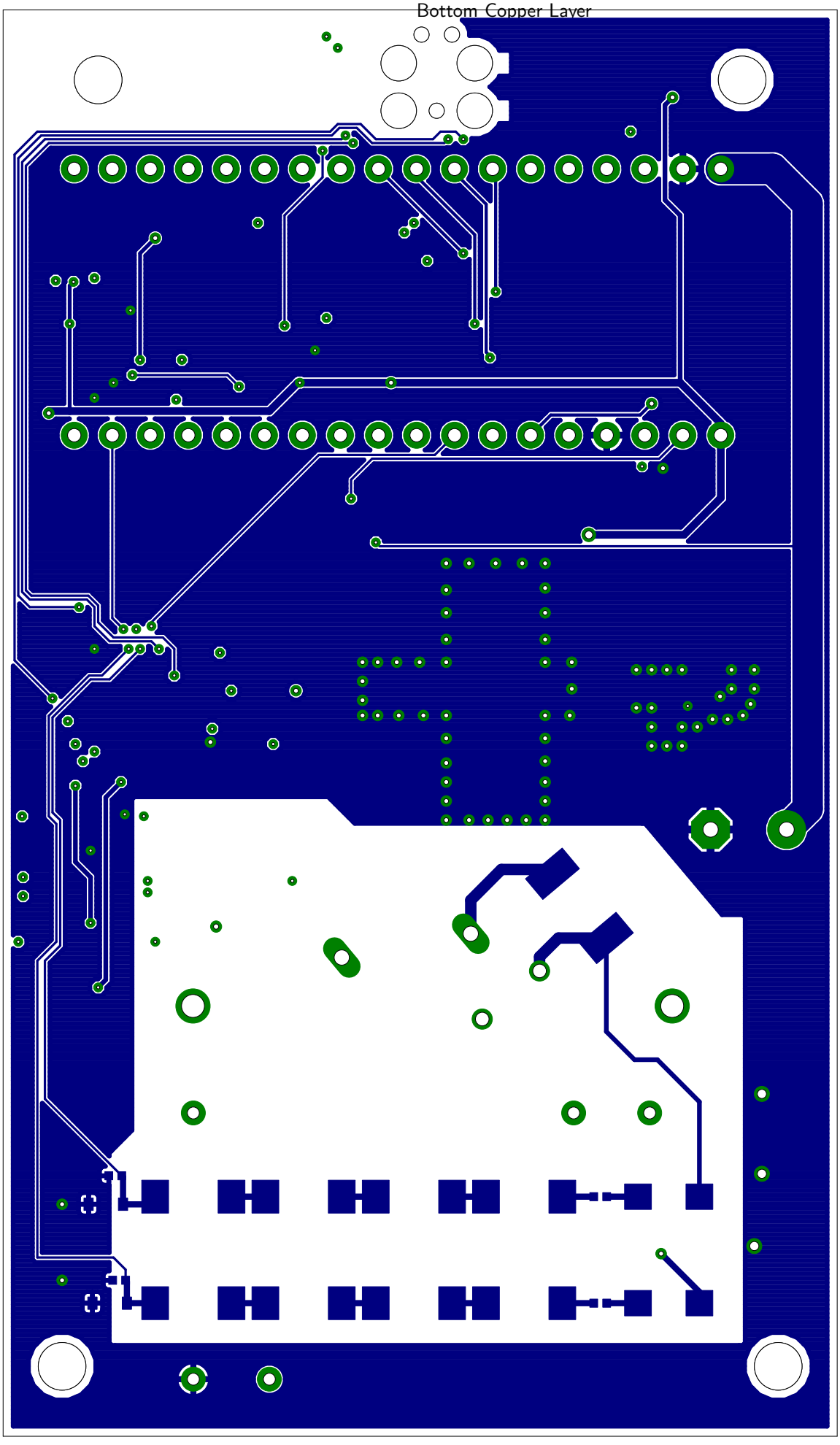

Top Layer
PowerWatch
Josh Adkins
Noah Klugman
Rev I, 12/19
nLine, Inc.
Neutral
Line
J2
U10
S1
Q2
R32
R24
R25
R29
R8
R4
R5
ASSY1
B1
U4
R19
R20
R30
R29
C18
C3
R22
U1
R18
X2
C9
U7
C25
R17
R13
U13
R27
R15
R14
C23
R16
R26
J1
JP1
JP2
U9
R21
Q1
R44
R43
R33
R42
U12
R28
C8
L3
L2
C5
C26
U8
C24
C15
C1
R23
U15
U17
U14
U16
C2
C19
C14
D5
C16
R9
R31
U11
C20
A1
U3
U5
C4
C29
C11
R38
U12
R39
R6
R34
R40
R36
R37
C13
C10
V1
F1
C28
C27
U6


Bottom Layer
R1
D14
R2
D9
D8
D7
D6
C6
D1
D15
R3
D13
D12
D11
D10
C7
D2
9

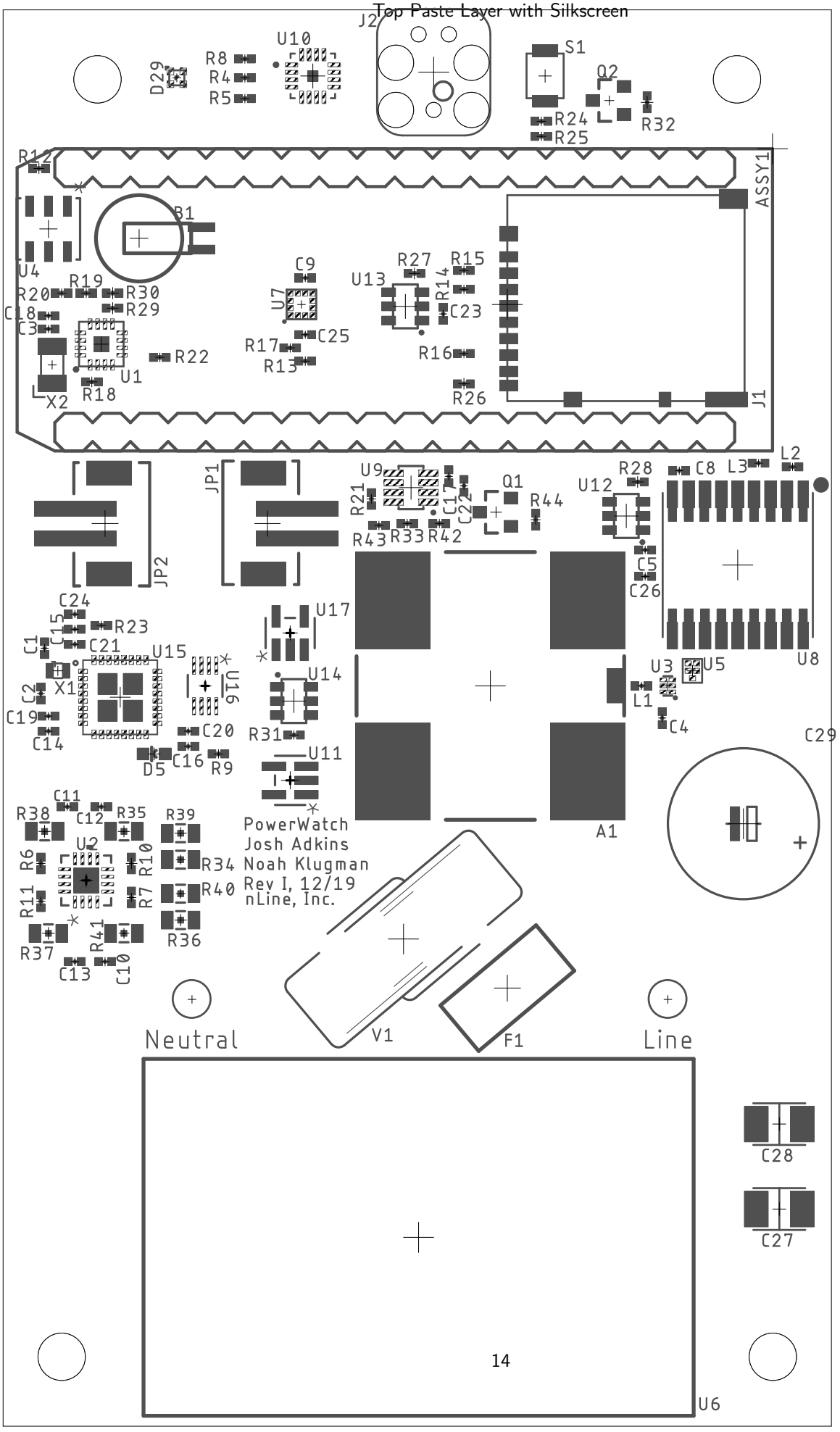

Top Copper Layer

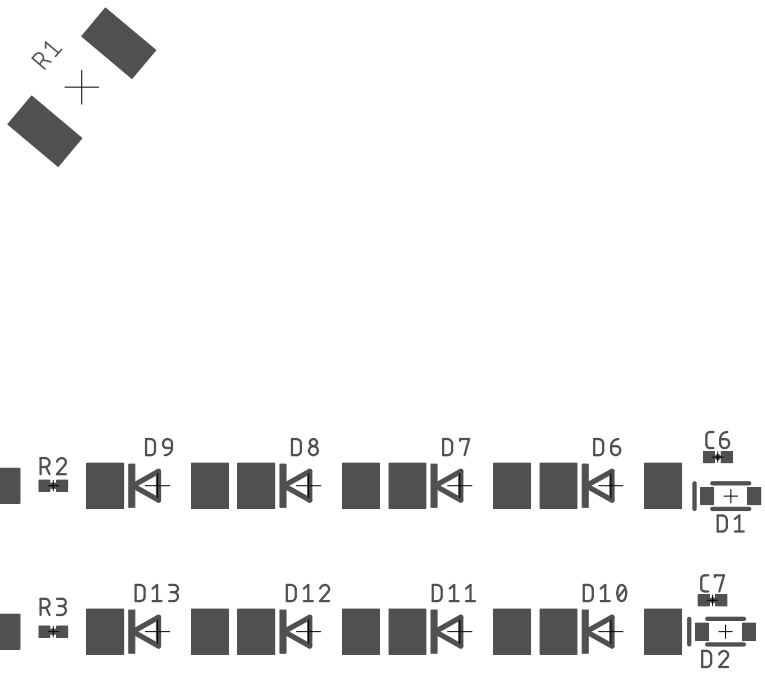

Layer 2 Copper


Layer 3 Copper

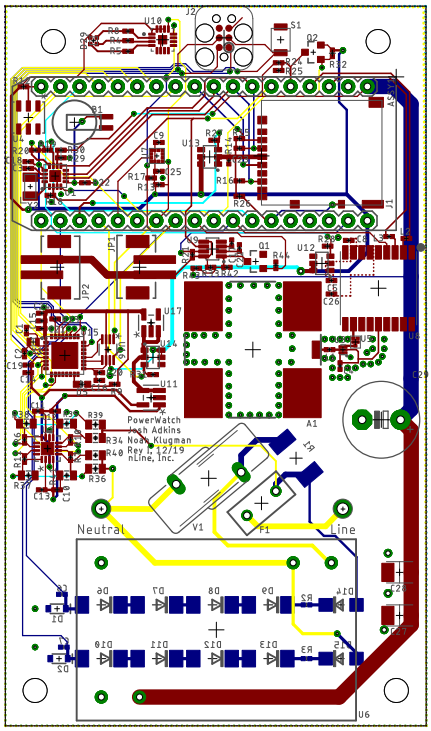

Bottom Copper Layer

Top Paste Layer with Silkscreen

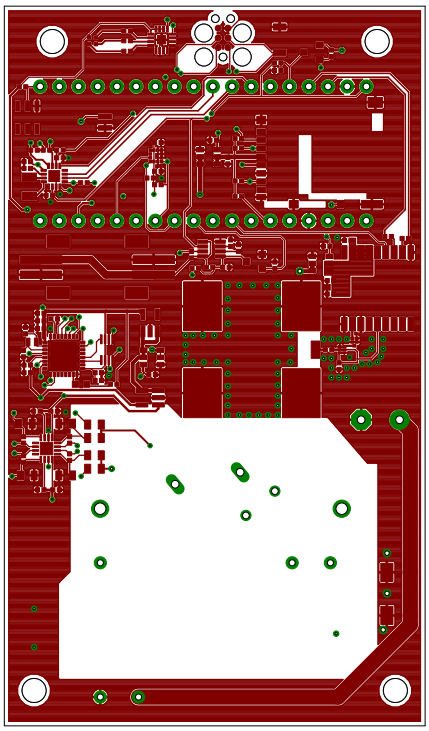



R1
D14
R2
D9
D8
D7
D6
C6
D1
D15
R3
D13
D12
D11
D10
C7
D2

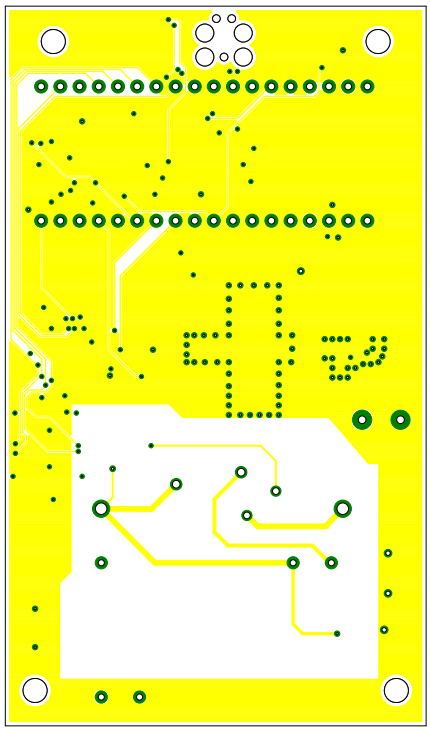
Top and Bottom Layers 1:1 Scale



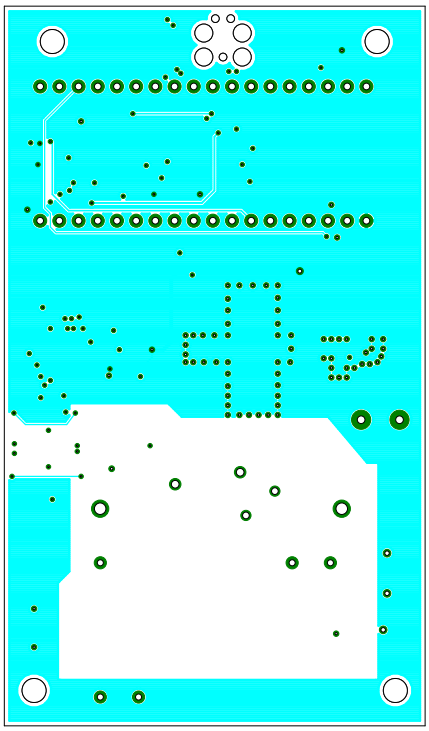
Top Layer 1:1 Scale



Layer 2 Copper 1:1 Scale



Layer 3 Copper 1:1 Scale



Bottom Copper Layer 1:1 Scale