```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity reg is
5   port( clr: in std_logic;
6         clk: in std_logic;
7         ren: in std_logic;
8         rin: in std_logic_vector(31 downto 0);
9         rout: out std_logic_vector(31 downto 0)
10        );
11  end entity reg;
12
13  architecture behavior of reg is
14  begin
15  process (clk,clr,ren,rin)
16     begin
17        if (clr= '1') then
18           rout <= x"00000000";
19        elsif ( clk='1') then
20           if ren = '1' then
21              rout <= rin;
22           end if;
23        end if;
24     end process;
25  END behavior;
```