```
library ieee;
 1
2 use ieee.std logic 1164.all;
3 use ieee.std logic arith.all;
   use ieee.std logic unsigned.all;
5
 6 entity MDMux is
7 port ( ReadIn: in std logic;
8
           BusMuxOut: in std logic vector(31 downto 0);
9
           Mdatain: in std logic vector (31 downto 0);
10
           MDMuxOut: out std_logic_vector(31 downto 0)
11
12
   end MDMux;
13
14
15
   architecture behavior of MDMux is
16 begin
17 process (ReadIn, BusMuxOut, Mdatain)
18
     begin
19
         if (ReadIn= '1') then
20
            MDMuxOut <= Mdatain;</pre>
21
22
             MDMuxOut <= BusMuxOut;</pre>
23
          end if;
    end process;
24
25 END behavior;
```