```
1
      library ieee;
    use ieee.std logic 1164.all;
      use ieee.numeric std.all;
 5
     entity good mux is
 7
      port (data0x : IN STD LOGIC VECTOR (31 DOWNTO 0);
               data1x
                             : IN STD LOGIC VECTOR (31 DOWNTO 0);
 8
9
              data2x
                             : IN STD LOGIC VECTOR (31 DOWNTO 0);
                             : IN STD LOGIC VECTOR (31 DOWNTO 0);
10
              data3x
            data4x : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
data5x : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
data6x : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
data7x : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
data8x : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
data9x : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
11
12
13
14
15
16
17
            data10x
                             : IN STD LOGIC VECTOR (31 DOWNTO 0);
             data11x
                              : IN STD LOGIC VECTOR (31 DOWNTO 0);
18
            data12x : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
data13x : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
data14x : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
data15x : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
data16x : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
19
20
21
22
23
24
            data17x
                             : IN STD LOGIC VECTOR (31 DOWNTO 0);
25
             data18x
                              : IN STD LOGIC VECTOR (31 DOWNTO 0);
            data19x : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
data20x : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
data21x : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
data22x : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
data23x : IN STD_LOGIC_VECTOR (31 DOWNTO 0);
26
27
28
29
30
31
             data24x
                             : IN STD LOGIC VECTOR (31 DOWNTO 0);
32
             data25x
                             : IN STD LOGIC VECTOR (31 DOWNTO 0);
              sel : IN STD_LOGIC_VECTOR (4 DOWNTO 0);
result : OUT STD_LOGIC_VECTOR (31 DOWNTO 0)
33
34
35
36
      end good mux;
37
38
39
      architecture behavioral of good mux is
40
      begin
               process (sel,data0x,data1x,data2x,data3x,data4x,data5x,data6x,data7x,data8x,data9x,⊋
41
      data10x,data11x,data12x,data13x,data14x,data15x,data16x,data17x,data18x,data19x,data20x,⊋
      data21x, data22x, data23x, data24x, data25x)
42
                   begin
43
                       case sel is
                                   when "00001" => result <=</pre>
44
                                                                       data1x;
                                   when "00010" => result <= data2x;</pre>
45
                                   when "00011" => result <=
46
                                                                        data3x;
47
                                   when "00100" => result <=</pre>
                                                                       data4x;
48
                                   when "00101" => result <= data5x;</pre>
                                   when "00110" => result <= data6x;</pre>
49
50
                                   when "00111" => result <=</pre>
                                                                        data7x;
                                   when "01000" => result <= data8x;</pre>
51
52
                                   when "01001" => result <= data9x;</pre>
53
                                   when "01010" => result <= data10x;</pre>
54
                                   when "01011" => result <= data11x;</pre>
55
                                   when "01100" => result <= data12x;</pre>
                                   when "01101" => result <= data13x;</pre>
56
57
                                   when "01110" => result <= data14x;</pre>
                                   when "01111" => result <= data15x;</pre>
58
59
                                   when "10000" => result <= data16x;</pre>
```

when "10001" => result <= data17x;</pre>

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