



		_		_	_	-	_	_	-	
/testbench/rout8_tb 0										
/testbench/rout9_tb (0										
/testbench/routa_tb (0							•	1		
/testbench/routb_tb 0							-	+		
/testbench/routc_tb 0							-	+		
/testbench/routd_tb 0				+		-	-	-		
/testbench/route_tb 0		+		-		-	-	+		
/testbench/routf_tb 0				+		-	-			
/testbench/rout0_tb 0							-			
/testbench/rout1_tb 0	26214								-22	
/testbench/busmuxout_tb 0	26214 0	(21	0 /4	0		\( 4	0 (21	0 (4	0 \( -22	Xo.
/testbench/PCout_tb 0							-			
/testbench/Zhigh_tb 0							-			
/testbench/LOout_tb 0				+			-			
/testbench/HIout_tb 0							-	•		
/testbench/MDRout_tb 0	26214	(21	) \/4	+	(4		-			
/testbench/routy_tb 0				+			(21			
/testbench/Zlow_tb 0				•		•	-	(-22		
/testbench/Present_state default	Reg_load1	Reg_load	2 Reg_loa	ad3 (T0	\(T1	)T2	(T3	(T4	(T5	
0 ps	1 1 1	1 1 1 1			1000	000 ps	1 1 1	150000 ps	1 1 1	200000