```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity reg64 is
5   port( clr: in std_logic;
6         clk: in std_logic;
7         ren: in std_logic;
8         rin: in std_logic_vector(63 downto 0);
9         rh,rlow: out std_logic_vector(31 downto 0)
10        );
11  end entity reg64;
12
13  architecture behavior of reg64 is
14  begin
15  process (clk,clr, rin, ren)
16     begin
17        if (clr = '1') then
18           rh <= x"00000000";
19           rlow <= x"00000000";
20        elsif ( clk='1') then
21           if ren = '1' then
22           rh <= rin(63 downto 32);
23           rlow <= rin(31 downto 0);
24           end if;
25        end if;
26
27     end process;
28  END behavior;
```