High Speed Differential Signal Board Layout

Yuhao Lin, Nick Liu, Kim Wong

*Abstract*—The project requires a 4-layer Printed Circuit Board with differential signaling. The design should support operation at high speeds while maintaining signal and power integrity. This paper will explore the layout, simulation, and measurements of the project.

# INTRODUCTION

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HIS document is a report for the Project 2 in ECE 4460 – Electronic Packaging. The project consists of designing of designing a 4-layer Printed Circuit Board. The board itself is a channel for 3 differential pairs that are driven through a buffer IC to an output. The dimension of the board, clock frequency, and source voltage are given in Table 1. There were three major parts to the project: layout of the board, simulation, and assembly/measurement. The board was layed out in Mentor PADS with considerations to signal and power integrity. For signal integrity, trace width impedance matching, trace length matching, and crosstalk were taken into consideration. For power integrity, decoupling capacitors were carefully positioned. The board also had to pass connectivity and clearance checks. While the board was sent out for fabrication, the design was then simulated using ADS. The model was made up of two parts: the PCB model, which modeled the power and signal lines, and the circuit model, which modeled the driver IC. With the schematic in ADS, the signal quality and the power supply noise were simulated. The board was then fabricated by Advanced Circuits and the board had to be Surface-mount soldered (SMT). After that, measurements were done by using a Pseudo Random Bit Stream (PRBS) to get the eye-diagram. With the eye-diagram, the signal quality could be evaluated and compared to the simulation results.

TABLE I

Project Parameters

|  |  |
| --- | --- |
| Parameter | Value |
| Dimension (sq. inches) | 30 |
| Clock Frequency (MHz) | 500 |
| Source (V) | 3.5 |

# Design

For the design, the schematic can be seen in Fig. 2. 6 SMA connectors, making 3 differential input pairs, connect to a differential driver which drives 3 differential output pairs. The outputs are terminated by 50 Ω resistors. Decoupling capacitors can also be seen at the supply voltage pins. The stackup of the PCB can be found in Fig. 1. There are four layers to the board. The top and bottom layers are for signal routing while the middle layers are for power and ground planes.

## Trace Width Impedance Matching

One of the considerations for signal integrity is trace width impedance matching. The traces in the PCB are long enough to act as a transmission line. Therefore, reflections need to be accounted for. To mitigate this issue trace impedance needs to be matched with the termination impedance, which is 50 Ω. To get the right trace impedance the proper trace width needs to be calculated for using LineCalc.

## LineCalc

LineCalc is needed to figure out the required width of the traces for matching with the 50 Ω terminating resistor. The stackup can be found in Fig 2. and the parameters used for calculating the required width can be found in Table 2. Looking at the stackup, the two signal layers are found to be microstrip transmission lines. Putting all of the information provided into LineCalc (as seen in Fig. 3.), the required trace width to get a 50 Ω impedance is found to be around 16.4 mils.

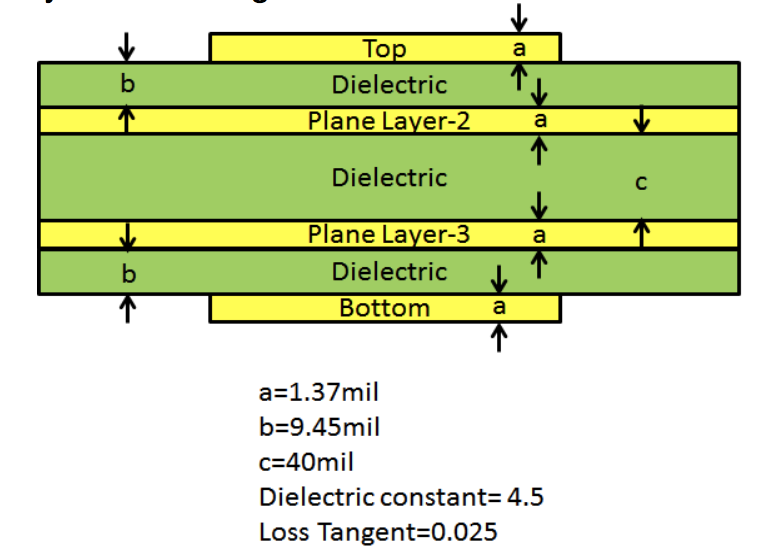


Fig. 1. The package layer stack-up for Project contains 4 metal layers, 2 for power/ground and two for routing. Some parameters of the dielectric are also given.

TABLE 2

Stackup Parameters

|  |  |
| --- | --- |
| Parameter | Value |
| a (mil) | 1.37 |
| b (mil) | 9.45 |
| c (mil) | 40 |
| Dielectric Constant (ε) | 4.5 |
| Loss Tangent (tan δ) | 0.025 |

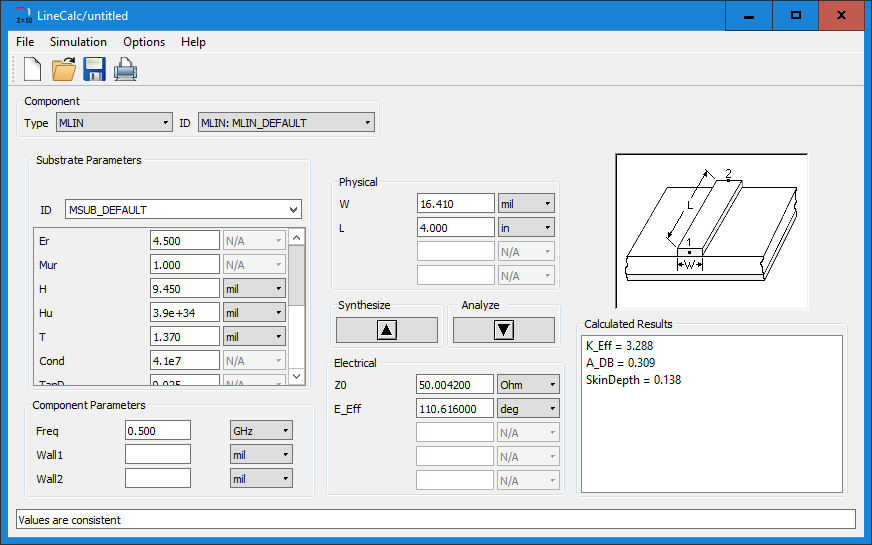
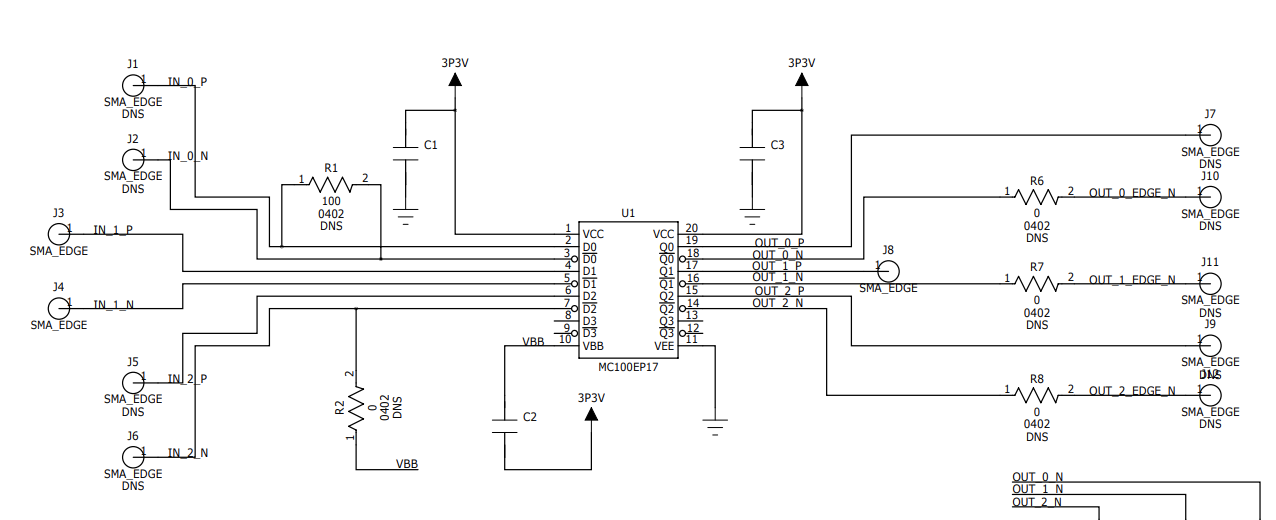


Fig. 2. The schematic for the PCB showing the differential inputs and outputs using SMA connectors, the buffer IC, and the decoupling capacitors.

Fig. 3. The LineCalc calculations used for determining the proper trace width.

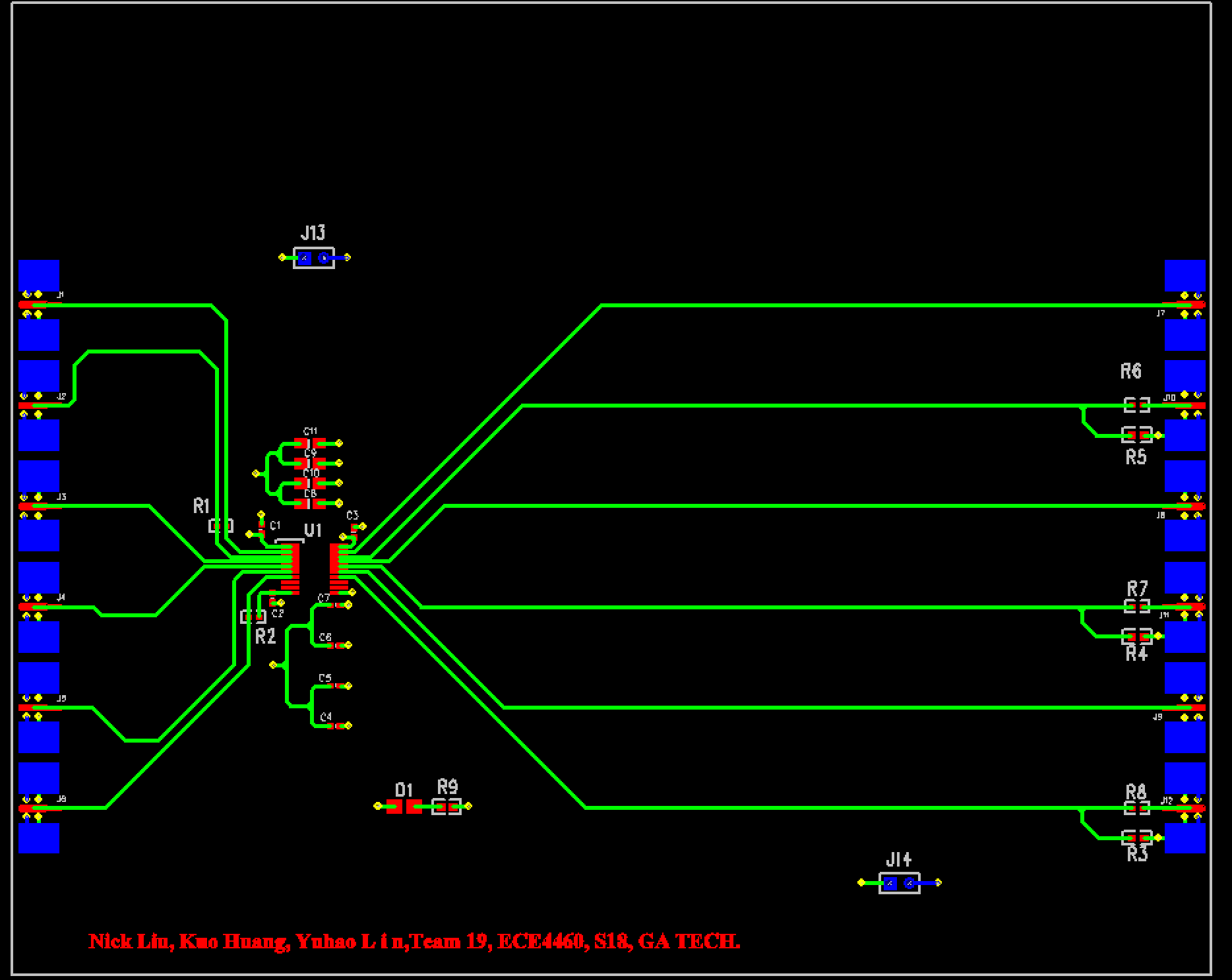
## Differential Signal Length Matching

Differential signals are a way of transmitting information using two complementary signals. One problem that comes with differential signaling is when the two signals have a time difference between one another. This is called differential skew. In order to effectively route differential signals while minimizing differential skew, the lengths of the traces that they go through should be of similar length. This allows for the delay of the complementary signals to be similar. Length matching was only considered for the input side of the buffer. When length matching, the route with the shorter distance had to be made longer in order to match the longer route distance.

## Cross Talk

## Ground Vias

## Decoupling Capacitors



# Simulation

# Measurements

TABLE

Measurement Setup

|  |
| --- |
| Equipment |
| Pulse Generator - 81133A |
| Oscilloscope - DCA-X 86100D |
| Front End Module - 54752A |
| Power Supply - E3610A |
| 20 dB Attenuator - 8439C |
| DC Blocking Adapter - BLK-18-S+ |

# Model to Hardware Correlation

# Conclusion