Nick Liu

Johns Creek, Georgia | nliu41@gatech.edu | 678.642.1508 | US Citizen
Looking for Fall Internship

EDUCATION

GEORGIA INSTITUTE OF TECHNOLOGY

BS in Electrical Engineering
BS in Computer Science
Expected December 2018
Cum. GPA: 3.67 / 4.0

COURSEWORK

ELECTRICAL ENGINEERING

Digital Design
Digital Signal Processing
Electromagnetics
Embedded Systems
Microelectronic Circuits
Power Systems
VLSI

COMPUTER SCIENCE

Computer Architecture
High Performance Computing
Operating Systems
Processor Design

SKILLS

PROGRAMMING

Java • C • C++ (MPI) • Verilog
SystemVerilog (UVM) • VHDL • Matlab
Assembly • Python • Tcl • Bash

SOFTWARE

Linux • Quartus • Vivado • ModelSim
QuestaSim • Spice • Cadence • Eagle
Multisim • Subversion • Git

HARDWARE

FPGA • Microcontroller • Oscilloscope
Function Generator • Logic Analyzer
Multimeter • Power Supply • Soldering

EXPERIENCE

SPACEX | Satellite Development Intern

Expected May 2017 – August 2017 | Irvine, CA

- Accepted offer for a Summer 2017 internship on the Satellite Development team involving FPGAs and RF systems

TESLA | Firmware Validation Intern

January 2017 – April 2017 | Palo Alto, CA

- Perform system validation of HVAC functionality of vehicles through use of a hardware test automation box
- Using automated testing system interfacing with car gateway and display to read CAN signals, send commands, and read thermocouple values
- Writing test suite for testing thermal systems using Python, ROBOT Framework, and Jenkins

NORTHROP GRUMMAN | Processing Technologies Intern

August 2016 – August 2016 | Baltimore, MD

- Developed project infrastructure with Tcl, Python, Bash, and Make scripts to increase compile and regression speed
- Implemented test cases for constrained random testing of RTL block
- Created SystemVerilog UVM test bench consisting of agent, monitor, driver, scoreboard, sequences, and sparse memory to test DUT

GEORGIA INSTITUTE OF TECHNOLOGY | Undergraduate Research Assistant

August 2015 – Present | Atlanta, GA

- Created initial 3-stage parallel pipelined processor for GPGPU research that supports simple vector instructions using Chisel, an open-source HDL
- Created power routing PCB to connect power system to all parts of CubeSat
- Developed Arduino code to interface with electrical power system of CubeSat using I2C
- Developed feedback system to interface with FPGA involving changing Embedded Linux firmware, a power relay, and EL Wire
- Creating a framework for migrating and testing 3D stacked memories to new FPGA hardware
- Conducting memory characterization on hybrid memory cube using GUPS, a random-access benchmark
- Modified speech recognition code to degrade quality of voice recognition for collecting data on approximate computing

PROJECTS

8-BIT SRAM ADDER SYSTEM | Cadence, HSpice

- Created schematic for 8-Bit Adder and SRAM system, layout for SRAM cell, and simulated with HSpice

MAP BOT | Microcontroller, C++, C#

- Created robot that autonomously moved around and mapped a room from IR sensor data and sent serial data wirelessly to PC through multithreading

PIPELINED PROCESSOR Verilog, FPGA

- Created 5 stage pipelined processor in Verilog with flushing, stalling, and data forwarding simulated with ModelSim and programmed on Altera FPGA.