Lab Assignment-09

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Id : 2019S1186

Section : 2D

Problem 1 :- clock cycle = 62

Instruction status :

	Issue	Real.op	Exec	write Result
LD F_6, 34 R_2	1	2	3	4
LD F_2 34 R_3	5	6	7	8
ADD F_0 F_2 F_4	6	9	11	12
DIVD F_8 F_6 F_2	7	9	49	50
SUBD F_0 F_0 F_6	13	14	16	17
MULD F_6 F_8 F_2	14	51	61	62

①. Ans : 08

② Ans : 62

③ Ans : 12

Problem 2 : clock cycle NO : 40

	Issue	Read.op	Exec	writeResult
LD F_0 0 R_1	1	2	3	4
MULTD F_4 F_0 F_2	2	5	15	16
SD F_4 0 R_1	17	18	19	20
LD F_0 0 R_1	21	22	23	24
MULTD F_4 F_0 F_2	22	25	35	36
SD F_4 0 R_1	37	38	39	40

① Ans : 40

②. Ans : 16

③. Ans : 36

Problem 3 :- clock cycle :- 28

Instruction status :-

	Issue	Real. of	Exec	write Result
LD F_0 6 R_1	1	2	3	4
LD F_2 6 R_1	5	6	7	8
MULTD F_8 F_0 F_2	6	9	19	20
LD F_4 8 R_1	9	10	11	12
LD F_6 10 R_1	13	14	15	16
MULTD F_{10} F_4 F_6	14	17	27	28

① Ans :- 28

② Ans :- write after read hazard is present between the last two instruction. To slove this Registers as soon as they are akaiable

Conclusion :- By this experiment, we can undastand the Process of scoreboard Technique and also dynamically scheduling. And we can also slove Problem based on scoreboard Technique.

Lab Assignment - 10

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Section : 2D.

Problem 1 :-

	Issue	Execute	Write Result
LD F_6 34 R_2	1	2	3
LD F_2 34 R_3	2	3	4
MULTD F_0 F_2 F_4	3	14	15
SUBD F_8 F_6 F_2	4	6	7
DIVD F_{10} F_0 F_6	5	55	56
ADD F_6 F_8 F_2	6	9	10

①. Ans : 4Th cycle

②. Ans : 15Th cycle

③. Ans : 10Th cycle.

Problem 2 :-

	Issue	Execute	Write Result
LD F_0 0 R_1	1	2	3
MULTD F_4 F_0 F_2	2	13	14
SD F_4 0 R_1	3	4	5
LD F_0 0 R_1	4	5	6
MULTD F_4 F_0 F_2	5	24	25
SD F_4 0 R_1	6	7	8

① Ans :- 8^{Th} cycle

② Ans :- 14^{Th} cycle

③ Ans :- 10^{Th} cycle

Problem 3 :

	Issue	Execute	Write Result
LD F0 6 R1	1	2	3
LD F2 6 R1	2	3	4
MULTD F8 F0 F2	3	14	15
LD F4 8 R1	4	5	6
LD F6 10 R1	5	6	7
MULTD F10 F8 F10	6	25	26
ADDD F10 F8 F10	7	28	29
LD F8 10 R1	8	9	10
ADDD F10 F10 F8	9	31	32

①. Ans :- 32

②. Ans :- Yes, re-ordering will inflance the execution Time if we write 6th instn. at last Than our Progkam will Take Less Time

i.e 26 clock cycle This happen Beccaus MULTD have more cycle

③. Ans :- Yes, WAR hazard present at 7th and 8th instruction It is stored by giving a stall write is complete.