(WS2020/21)

Prof. Dr. -Ing Andreas Siggelkow



Nils Schlegel, 32067 & Tara Jaishi, 32289

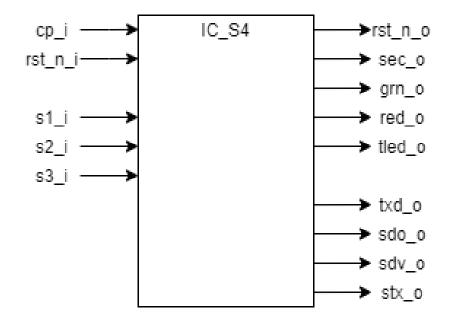
Circuit Design Application

- Matching Covid-19 Restriction
- Monitoring
- Visualizing
- ☐ Security



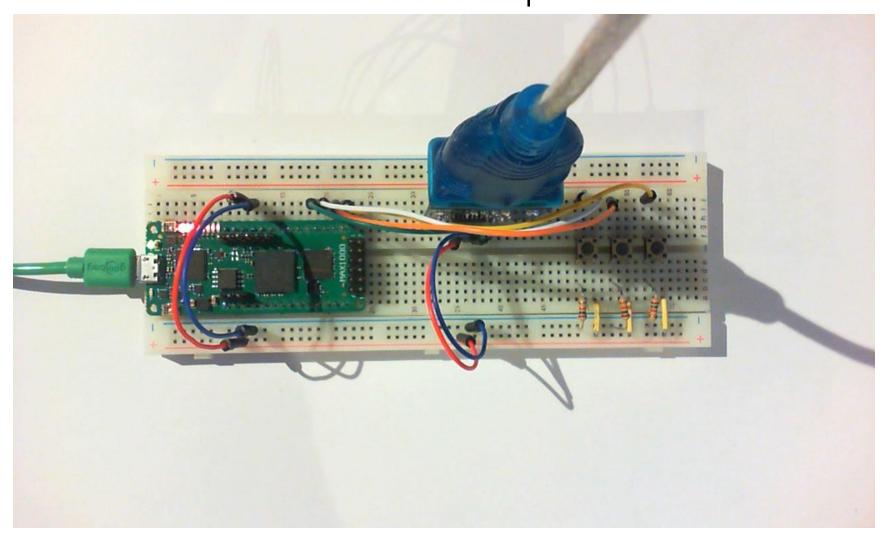
Circuit Design Block Digram





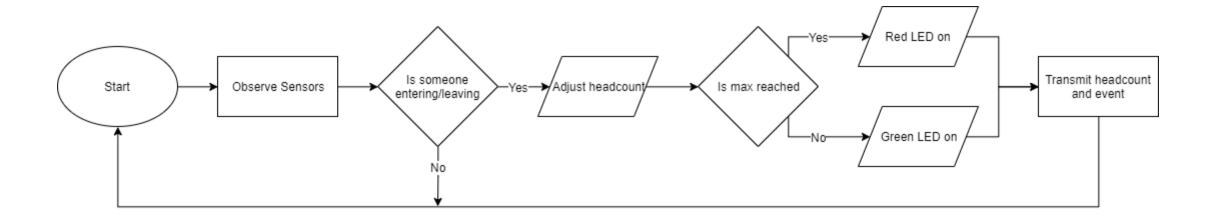
Circuit Design Board Setup





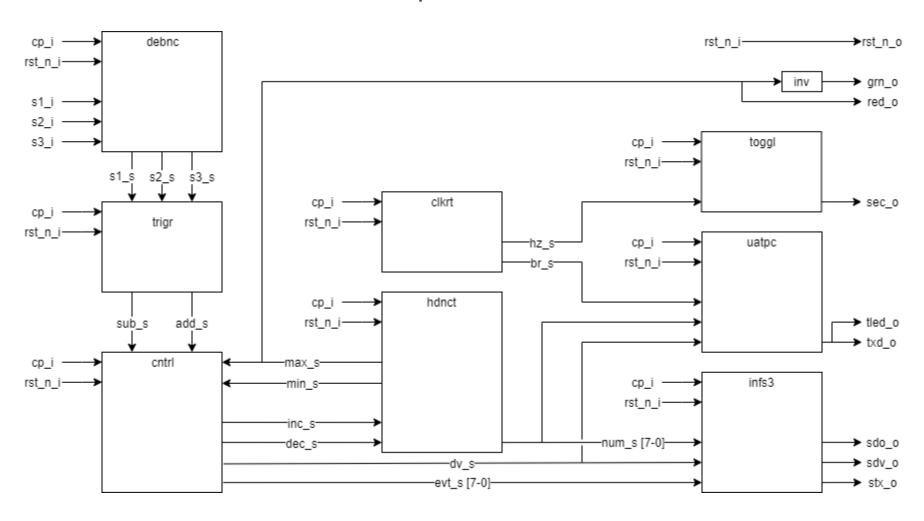
Circuit Design Flow Chart





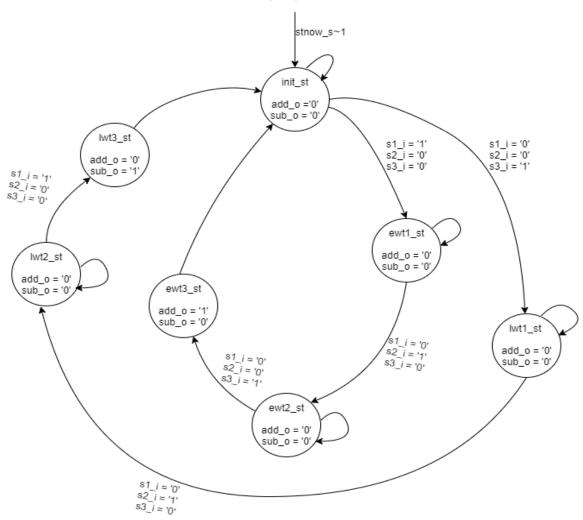
HOCHSCHULE RAVENSBURG-WEINGARTEN UNIVERSITY OF APPLIED SCIENCES

Top-Level



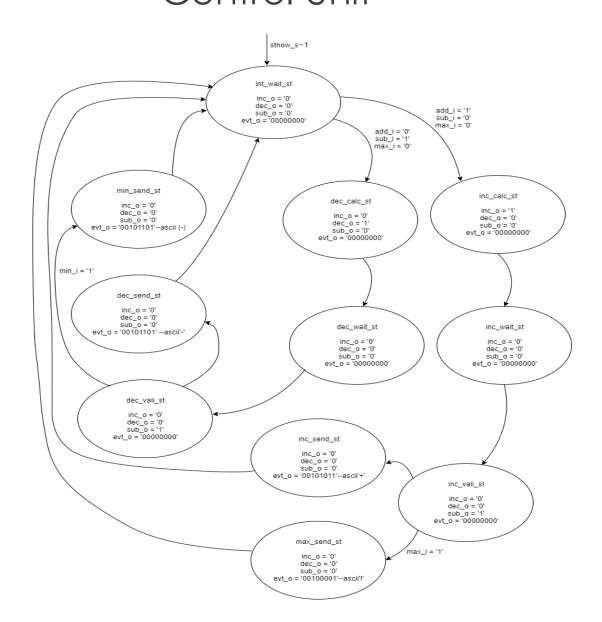
Circuit Design Trigger





Circuit Design Control Unit

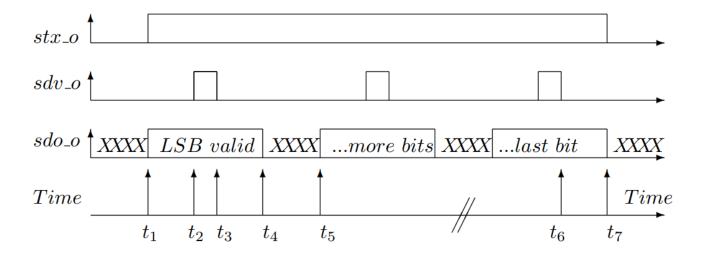








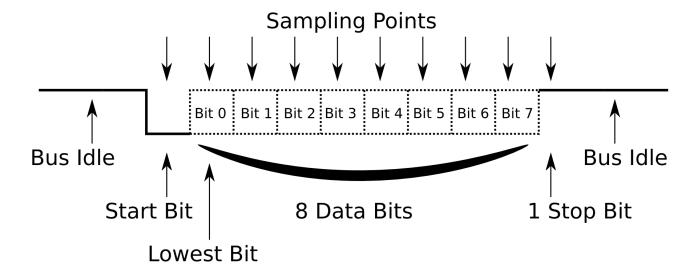
3-Wire-Interface



Circuit Design UART



UART with 8 Databits, 1 Stopbit and no Parity



Program



C:\Users\User\Documents\GitHub\VHDL\C++\VHDLSerialData\Debug\VHDLSerialData.exe

```
Enter COM-PORT Number (standard "COM5"): 5
Opening Port: \\.\COM5
opening serial port successful
1610900919 1
Someone ENTERED
1610900922 2
Someone ENTERED
1610900928 1
Someone LEFT
1610900937 0
Someone LEFT
1610900953 1
Someone ENTERED
1610900956 2
Someone ENTERED
1610900960 3
Someone ENTERED
Max. number of People is reached
```

Circuit Design Implementation



- In real world assumptions:
- ☐ Only one door to enter/exit
- ☐ Everyone completes the enter/leave process completely
- ☐ No one enters, when the room is full
- ☐ No one leaves, when room is already empty



Thank you



Link: https://github.com/nlsy/VHDL