

S4_VHDL Specifications

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1 Requirements

Requirement	ID	Importance	Verifiable	Description	Remarks
General					
Gen.: #persons	G01	High	VHDL Testbench	The number of persons in a room must be known.	
Gen.: max	G02	High	VHDL Testbench	The number of persons in a room must not exceed a given limit.	
Gen.: only one pers.	G03	High	?	Only one person can either enter or leave the room at a time.	Check test.
Gen.: three light sensors	G04	Medium	VHDL Testbench	Along the doorway, there are three light-curtains to allow direction-tracking of possible visitors.	Why not only two?
Gen.: only one door	G05	High	?	Only one door exists.	Check test. Req. given during the lecture.

Sound					
Sound: entered	S01	High	VHDL Testbench	A person entered the room, play a unique sound.	Check, if this is on the FPGA or on the uC.
Sound: left	S02	High	VHDL Testbench	A person left the room, play a unique sound.	Check, if this is on the FPGA or on the uC.
Sound: stop	S03	High	VHDL Testbench	The room is full, play a unique sound.	Check, if this is on the FPGA or on the uC.
LED					
LED: red	LED01	High	VHDL Testbench	The maximal number of persons reached.	
LED: green	LED02	High	VHDL Testbench	The maximal number of persons not reached.	

UART					
UART: 9600 baud	UART01	High	VHDL Testbench	The speed of the serial transmission should be set to 9600 baud.	
UART: 8 bit	UART02	High	VHDL Testbench	The data width of the serial transmission should be set to 8 bit.	
UART: no parity	UART03	High	VHDL Testbench	The serial transmission should not be checked with a parity bit.	
UART: one stop bit	UART04	High	VHDL Testbench	The serial transmission should have only one stop bit.	
UART: time	UART05	High	VHDL Testbench	The time stamp of an event should be delivered to a PC.	
UART: #persons	UART06	High	VHDL Testbench	The #persons should be transmitted to a PC.	

PC					
PC: language	PC01	Medium	C++-program	The information should be displayed on a PC, the language is C++.	Medium: Other languages would do the job also.
IC_S3				Events and headcounts are transferred to IC S3 using a ThreeWire-Interface.	
IC_S3: interface	IC01	Low	VHDL Testbench	Use a three wire IF.	Low: Not needed for the functionality
IC_S3: events	IC02	Low	VHDL Testbench	All events should be transmitted via the three wire IF.	Low: Not needed for the functionality. Not atomic: which events?
3 IC_S3: #persons	IC03	Low	VHDL Testbench	The #persons should be transmitted via the three wire IF.	Low: Not needed for the functionality

2 Product:IC_4

History

Target Spec. Current version: 0.1, 2020-11-9

Previous version:-

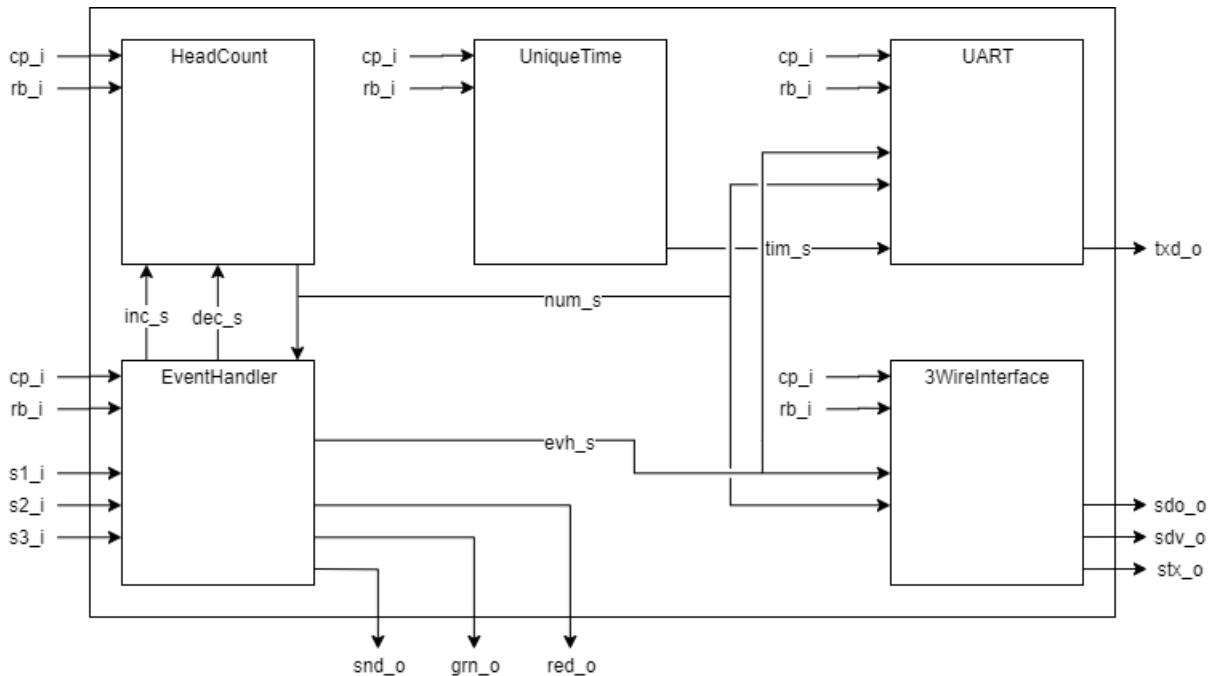
06.11.2020	General description added
06.11.2020	Block diagram added
06.11.2020	Functional description added

2.1 General discription

IC4 is a single chip based application containing processing capabilities to detect and keep track of the amount of people in one room. It is part of a system solution to fullfill the covid-19-restrictions and regulate the amount of people in an area. This solution is only meant for a chamber with only one doorway available to enter or to exit.

The IC4 is designed on a FPGA prototype-board Max1000 with 10M16SAU169C8G device on board.

2.2 Block diagram



rb_i	reset	reset, active low
cp_i	system clock	e.g. 10MHz
s1_i	light_curtain s1	log1: something passes
s2_i	light_curtain s2	log1: something passes
s3_i	light_curtain s3	log1: something passes
grn_o	LED, access garanteed	Green LED, go ahead
red_o	LED, stop, no entry	Red LED, stop, access denied
sdo_o	serial data out	drives S3 or MC
sdv_o	serial data valid	drives S3 or MC
stx_o	serial transfer active	drives S3 or MC
txd_o	serial out	to RS-232-driver, 9k6,8N2,ASCII,to PC
snd_o	sound signal	acoustic signal, to loudspeaker
inc_s	increment	increments head count when triggered
dec_s	decrement	decrements head count when triggered
num_s	number	contains the head count number
evh_s	event	contains the current event

2.3 Functional description

HeadCount

Stores the current number of people in the room. It increments or decrements the number if needed.

EventHandler

It receives the signals from the light curtains and detects which event is triggered. Depending on the event it will play a sound, turn on a LED and create an output signal.

UniqueTime

This element is only counting the clock-cycles, to generate a unique timestamp.

UART

The connection to RS232 is done by the UART. It takes the unique timestamp from the UART as well as the head count from the HeadCount and event type from the EventHandler, when a signal from the EventHandler is received.

3WireInterface

The IC_3 can be connected by using the 3WireInterface. When it receives a signal from the EventHandler it should pass the head count and event type to the IC_3.

3 Top Level View

The ASIC must:

- identify, if a person enters or leaves the room
- activate or deactivate a "STOP- " or a "GO-LED"
- track and count the number of people presently in the room. Events and headcounts are transferred to IC S3 using a three-wire-Interface and via a UART to a PC.
- The transmission to the PC is 9600 baud, 8 bit, no parity, 1 stop bit.

On the PC side, get the information and display it. The programming language is C++.

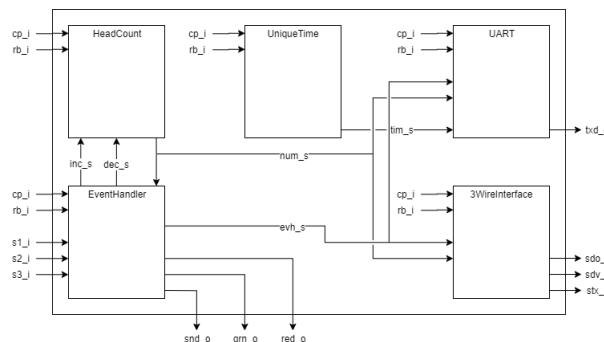


fig: Top level diagram

Table: Top level I/O

Pin	Direction	Width	Explanation
rst_n_i	IN	1	Reset, active low
clk_i	IN	1	Syscp, @ 12MHz
s1_i	IN	3	Sensor 1
s2_i	IN	1	Sensor 2
s3_i	IN	1	Sensor 3
rst_n_o	OUT	1	Reset state LED
sec_o	OUT	1	Pulse LED
grn_o	OUT	1	Green LED
red_o	OUT	1	Red LED
tled_o	OUT	1	Transmission LED
txd_o	OUT	1	Transmission
sdi_o	OUT	1	S3 data value
sdv_o	OUT	1	S3 data valid
stx_o	OUT	1	S3 transmission active

Blocks of Top Level diagram and its Pin and Sifnal are described below.

3.1 Debouncing all Signals

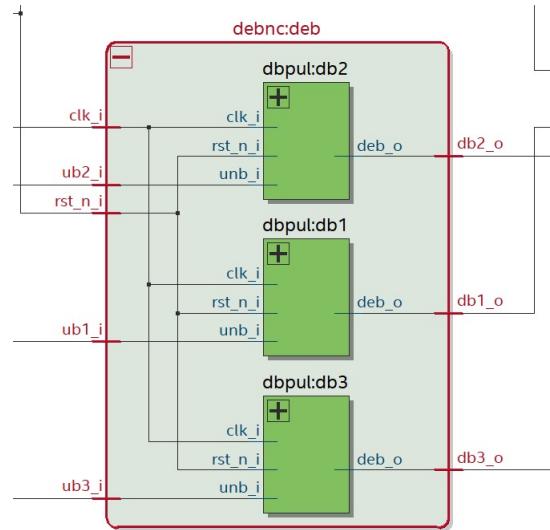


fig: debnc_deb

Pin	Direction	Width	Explanation
rst_n_i	IN	1	Reset, active low
clk_i	IN	1	Syscp, @ 12MHz
ub1_i	IN	1	Unbounced Input 1
ub2_i	IN	1	Unbounced Input 2
ub3_i	IN	1	Unbounced Input 3
db1_o	OUT	1	Debounced Output 1
db2_o	OUT	1	Debounced Output 2
db3_o	OUT	1	Debounced Output 3

3.2 Signal Toggle

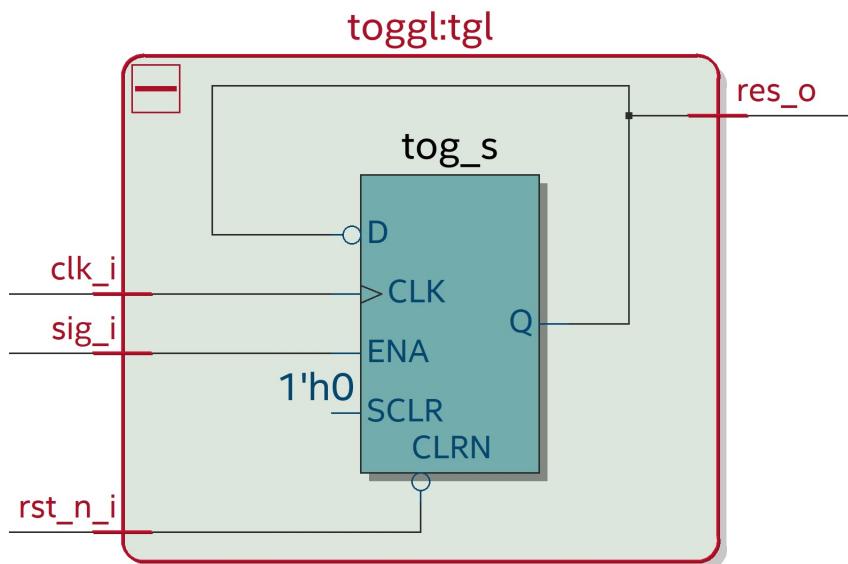


fig: toggle_tgl

Pin	Direction	Width	Explanation
rst_n_i	IN	1	Reset, active low
clk_i	IN	1	Syscp, @ 12MHz
sig_i	IN	1	Pulseing signal
res_o	OUT	1	Toggeled output

3.3 Generates Clock Rates

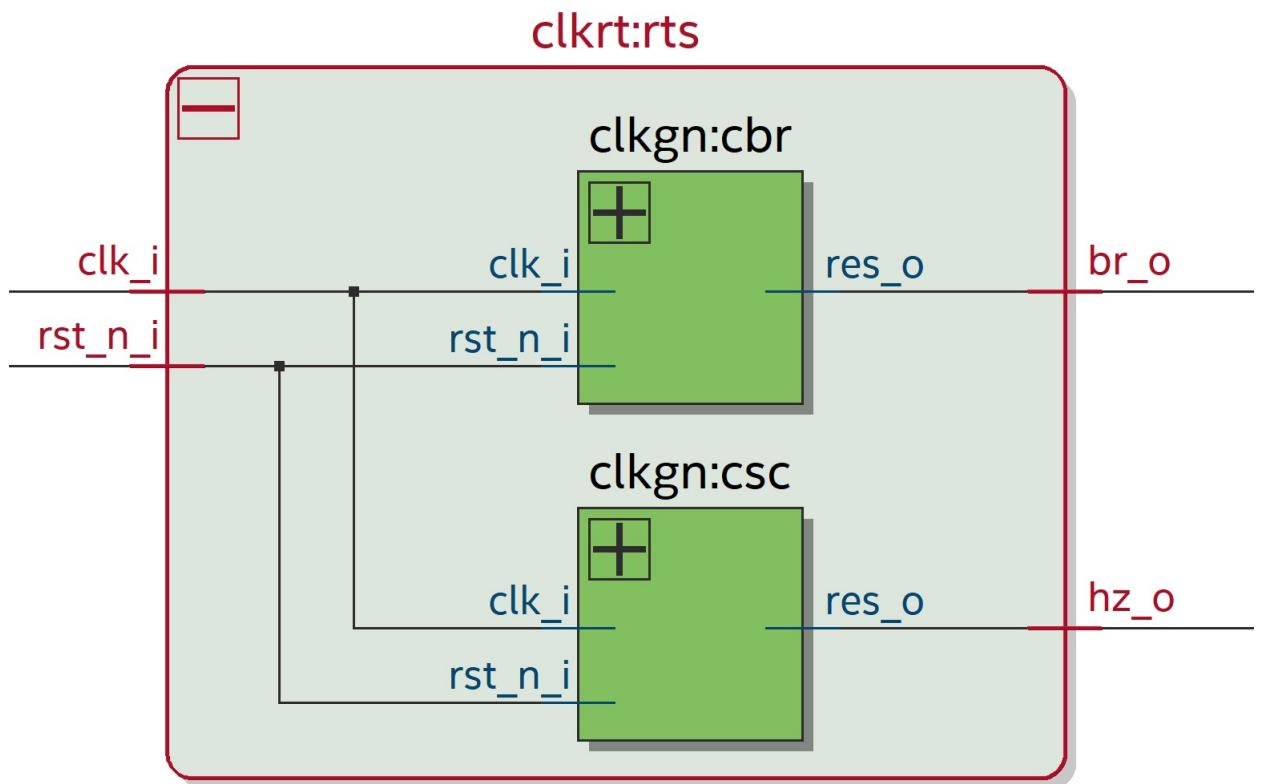


fig : clkrt_rts

Pin	Direction	Width	Explanation
rst_n_i	IN	1	Reset, active low
clk_i	IN	1	Syscp, @ 12MHz
br_o	OUT	1	Baud Rate @9600Hz
hz_o	OUT	1	Alive Pulse @1Hz

3.4 Sensor Handling

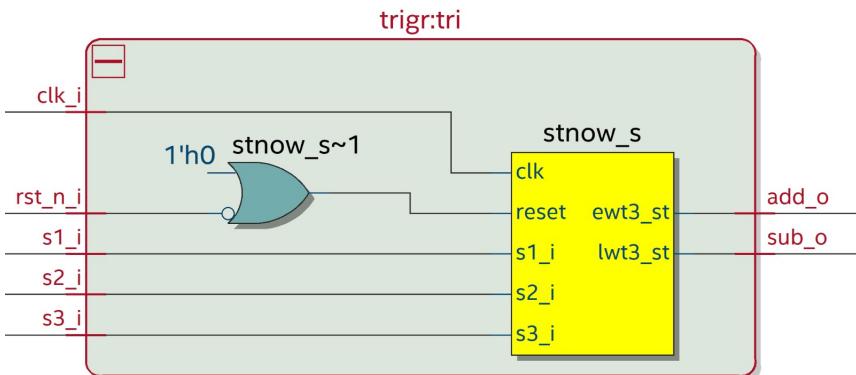


fig: trigr_tri

Pin	Direction	Width	Explanation
rst_n_i	IN	1	Reset, active low
clk_i	IN	1	Syscp, @ 12MHz
s1_i	IN	1	Sensor 1
s2_i	IN	1	Sensor 2
s3_i	IN	1	Sensor 3
add_o	OUT	1	Person entered
sub_o	OUT	1	Person left

3.5 HeadCounter

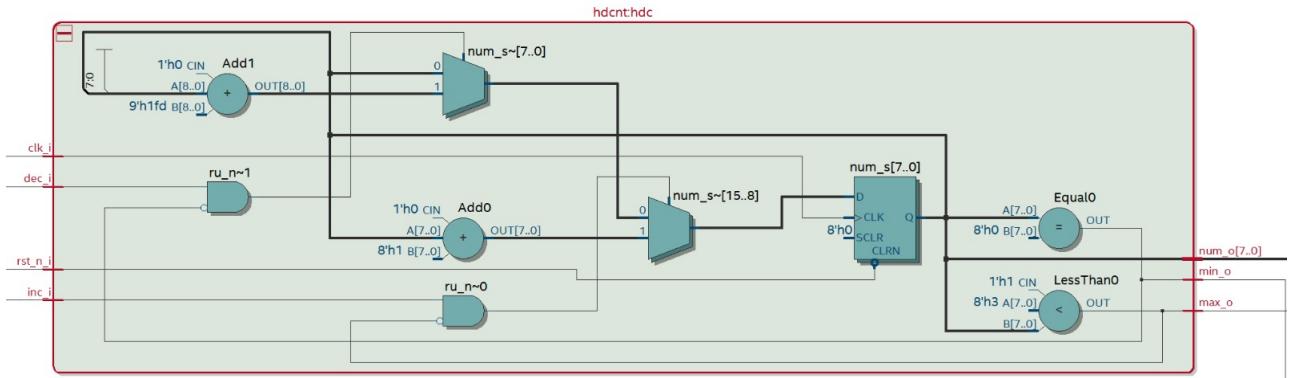


fig: hdcnt_hd

Pin	Direction	Width	Explanation
rst_n_i	IN	1	Reset, active low
clk_i	IN	1	Syscp, @ 12MHz
inc_i	IN	1	Increment Counter Signal
dec_i	IN	1	Decrement Counter Signal
min_o	OUT	1	Min persons in room
max_o	OUT	1	Max persons in room
num_o	OUT		

Generic	Type	Explanation
cnt_width	integer	
max_cnt	integer	

3.6 ControllFSM

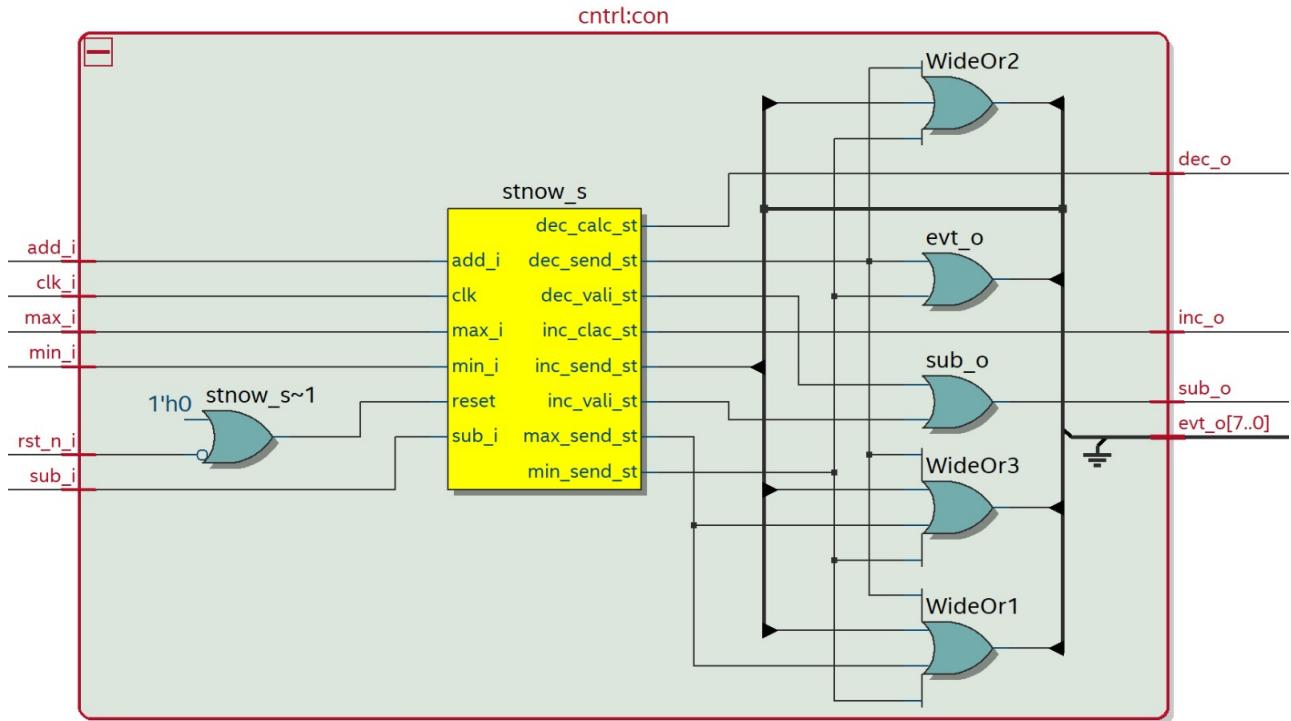


fig: cntrl_con

Pin	Direction	Width	Explanation
<code>rst_n_i</code>	IN	1	Reset, active low
<code>clk_i</code>	IN	1	Syscp, @ 12MHz
<code>add_i</code>	IN	1	Person entered
<code>sub_i</code>	IN	1	Person left
<code>min_i</code>	IN	1	Min persons in room
<code>max_i</code>	IN	1	Max persons in room
<code>inc_o</code>	OUT	1	Increment Counter Signal
<code>dec_o</code>	OUT	1	Decrement Counter Signal
<code>evt_o</code>	OUT		Happened event char
<code>sub_o</code>	OUT	1	Submitt/Send Data

3.7 UART to PC

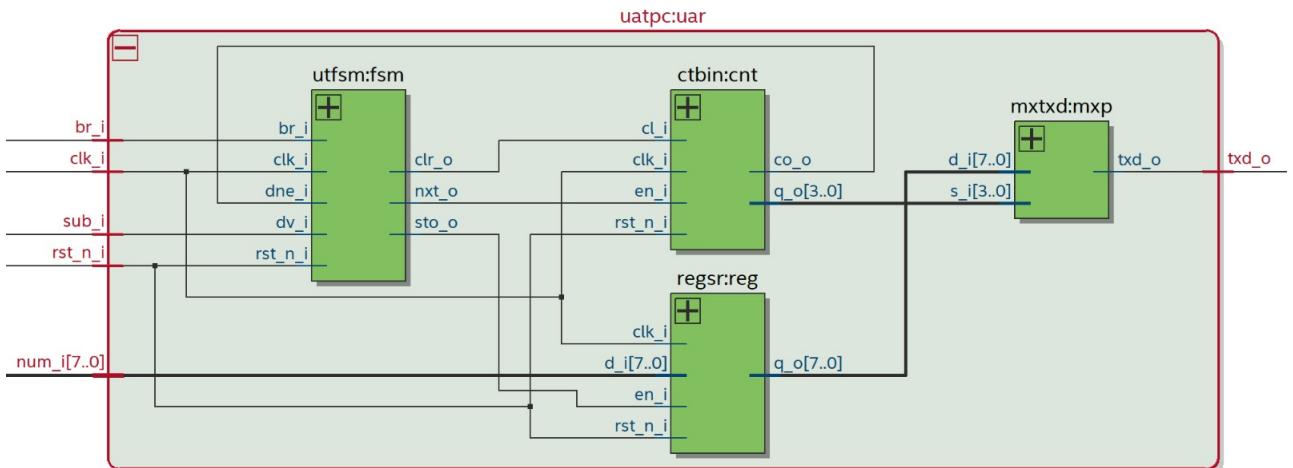


fig: uatpc_uar

Pin	Direction	Width	Explanation
rst_n_i	IN	1	Reset, active low
clk_i	IN	1	Syscp, @ 12MHz
br_i	IN	1	Baud rate
sub_i	IN	1	Submitt/Send Data
num_i	IN		Head count number
txd_o	OUT	1	Serial output

3.8 Interface to S3

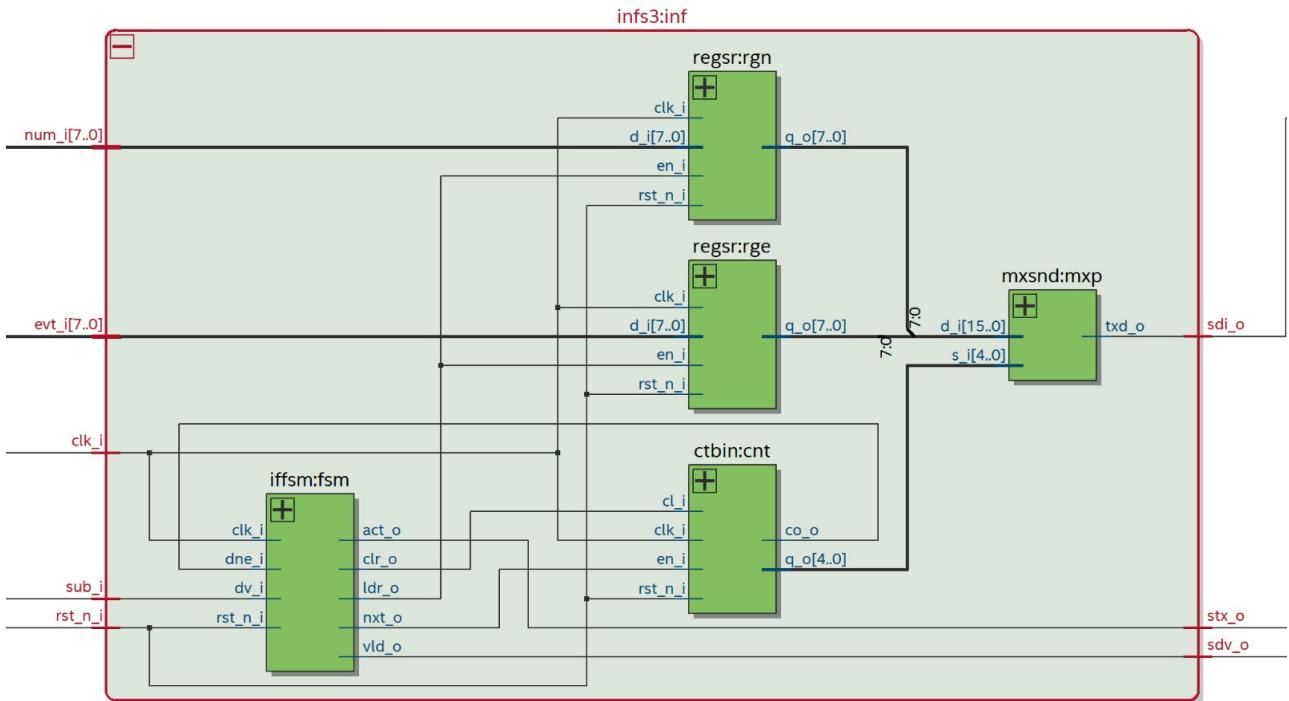


fig: inf3_inf

Pin	Direction	Width	Explanation
rst_n_i	IN	1	Reset, active low
clk_i	IN	1	Syscp, @ 12MHz
sub_i	IN	1	Submitt/Send Data
evt_i	IN	1	Occured event char
num_i	IN	1	Head count number
sdi_o	OUT	1	S3 data value
sdv_o	OUT	1	S3 data valid
stx_o	OUT	1	S3 transmission active

Lower Level Modules are described below.

3.9 Debounc Input resulting in Pulse

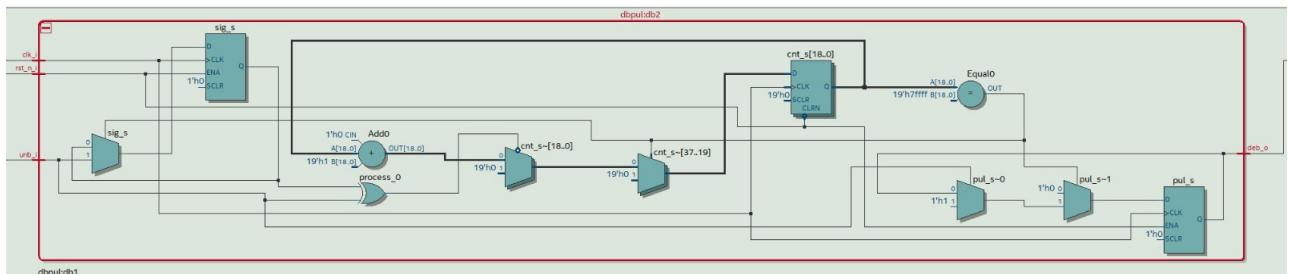


fig: dbpul_db2

Pin	Direction	Explanation
<code>rst_n_i</code>	IN	Reset, active low
<code>clk_i</code>	IN	Syscp, @ 12MHz
<code>unb_i</code>	IN	Unbounced Input
<code>deb_o</code>	OUT	Debounced Output

3.10 Clock Generator

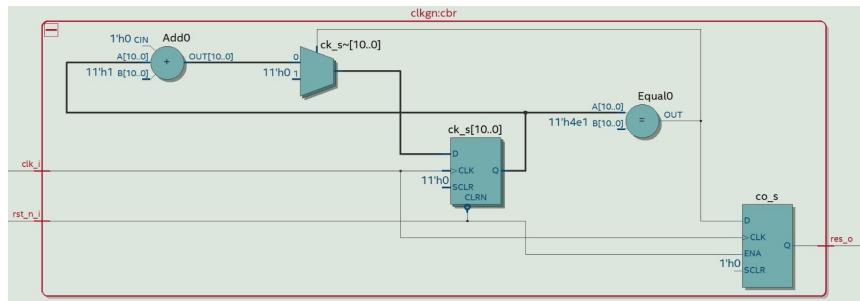


fig: clkgn_cbr

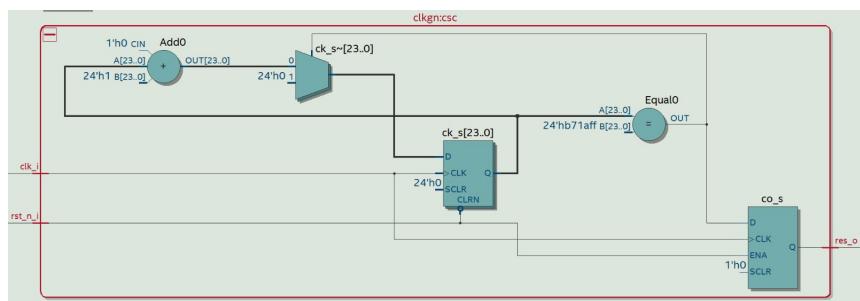


fig: clkgn:csc

Pin	Direction	Explanation
rst_n_i	IN	Reset, active low
clk_i	IN	Syscp, @ 12MHz
res_o	OUT	Resulting Ticks

Generic	Type	Explanation
cnt_width	integer	
div_cnt	integer	

3.11 Finite State Machine for UART

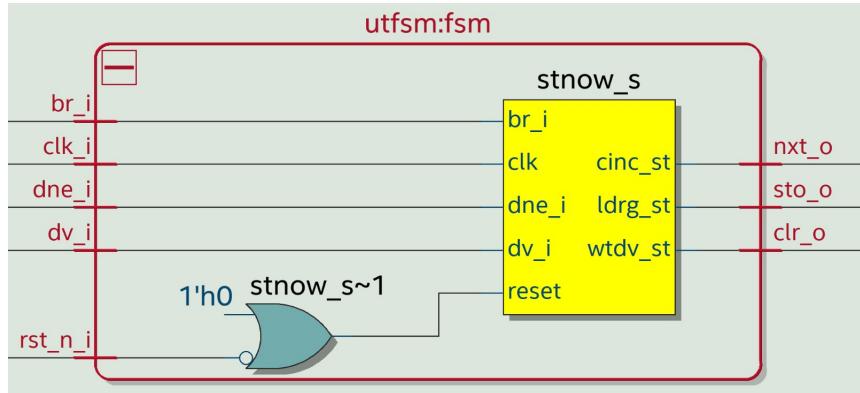


fig: utfsm_fsm

Pin	Direction	Explanation
<code>rst_n_i</code>	IN	Reset, active low
<code>clk_i</code>	IN	Syscp, @ 12MHz
<code>dv_i</code>	IN	Have new RTC or GPS-Data
<code>br_i</code>	IN	Baud-Rate to ena Counter
<code>dne_i</code>	IN	Last Bit transmitted
<code>sto_o</code>	OUT	enable register load
<code>clr_o</code>	OUT	clear Bit-Counters
<code>nxt_o</code>	OUT	next Bit, inc count

3.12 Register to store bits

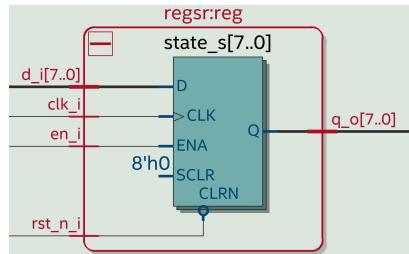


fig: regsr_reg

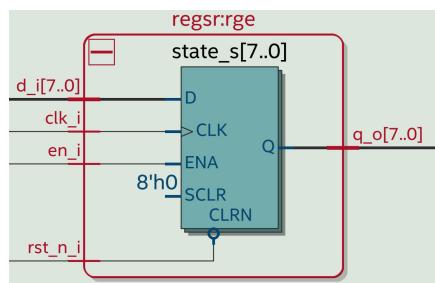


fig: regsr_rge

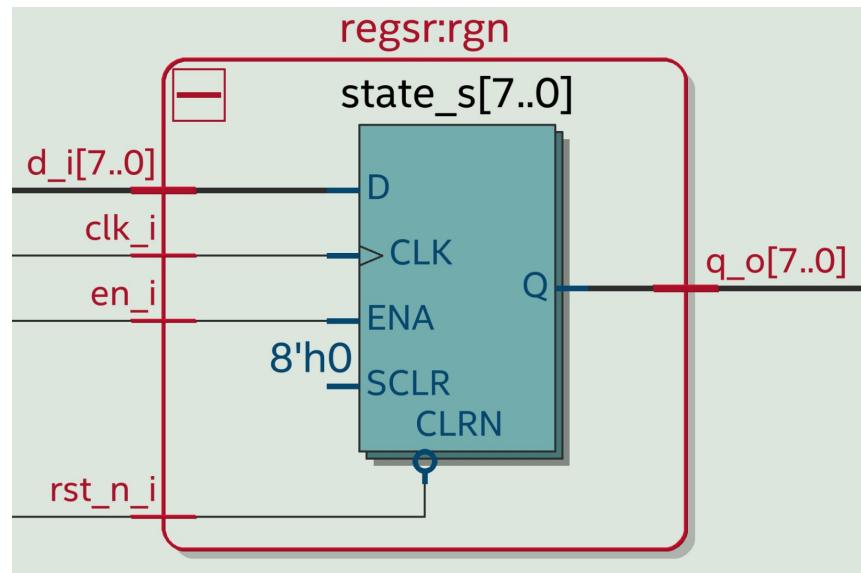


fig: regsr_rgn

dta_width : integer

Pin	Direction	Explanation
rst_n_i	IN	Reset, active low
clk_i	IN	Syscp, @ 12MHz
en_i	IN	Store Data
d_i	IN	Input Data
q_o	OUT	Stored Data

3.13 Binary Counter

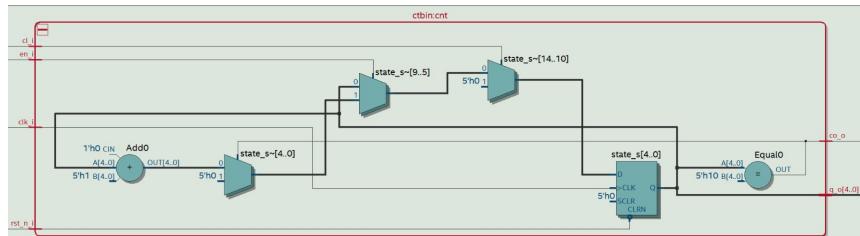


fig:Ctbin_cnt

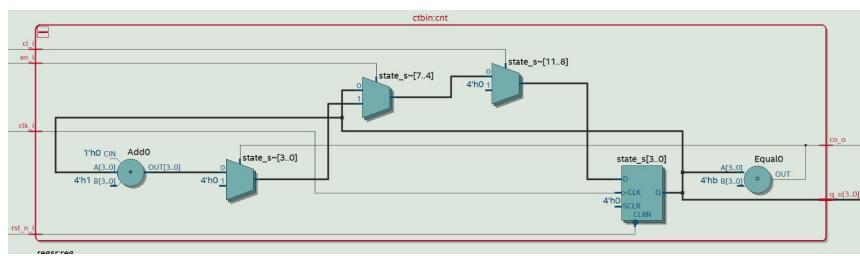


fig:ctbin_cnt

Generic	Type	Explanation
cnt_width	integer	
cnt_max	integer	

Pin	Direction	Explanation
rst_n_i	IN	Reset, active low
clk_i	IN	Syscp, @ 12MHz
en_i	IN	Enable Count
cl_i	IN	Clear Counter
co_o	OUT	Carry Out
q_o	OUT	Counter Value

3.14 Multiplexer for TxD

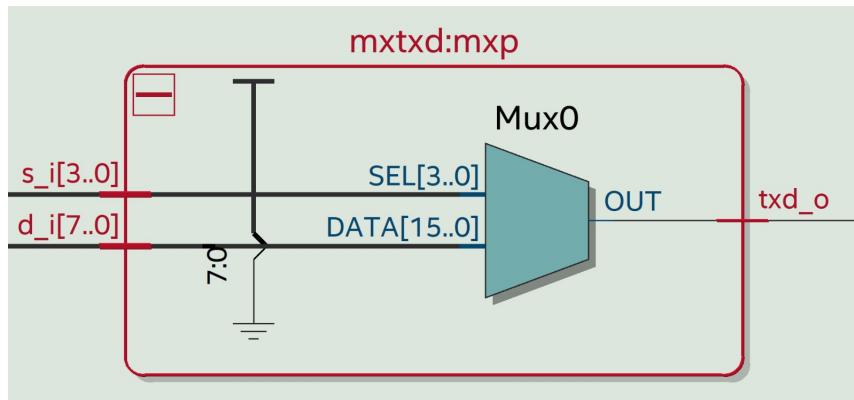


fig:mxtxd_mxp

Pin	Direction	Explanation
<code>s_i</code>	IN	Bit position
<code>d_i</code>	IN	Bit vector
<code>txd_o</code>	OUT	Txd, Serial Output

3.15 Finite State Machine for Interface to S3

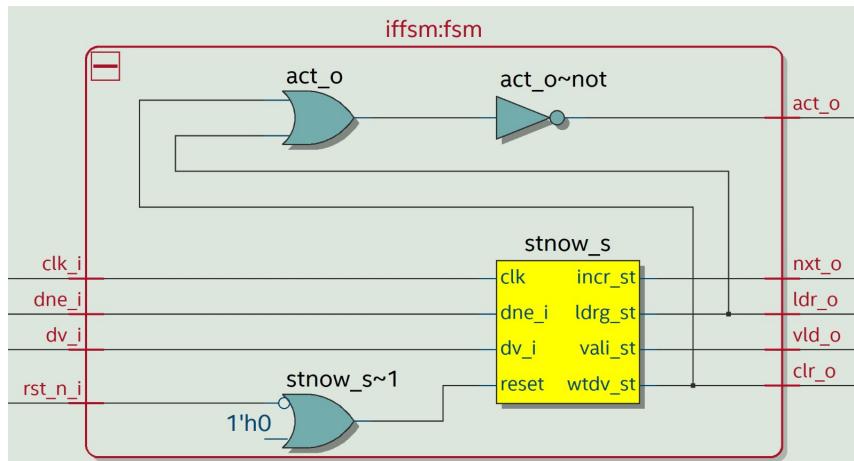


fig:iffsm_fsm

rst_n_i	IN	Reset, active low
clk_i	IN	Syscp, @ 12MHz
dv_i	IN	Have new RTC or GPS-Data
dne_i	IN	Last Bit transmitted
ldr_o	OUT	Enable register load
act_o	OUT	Transmission active
vld_o	OUT	Data Bit valid
clr_o	OUT	Clear Bit-Counters
nxt_o	OUT	Next Bit, inc count

3.16 Multiplexer for Interface to S3

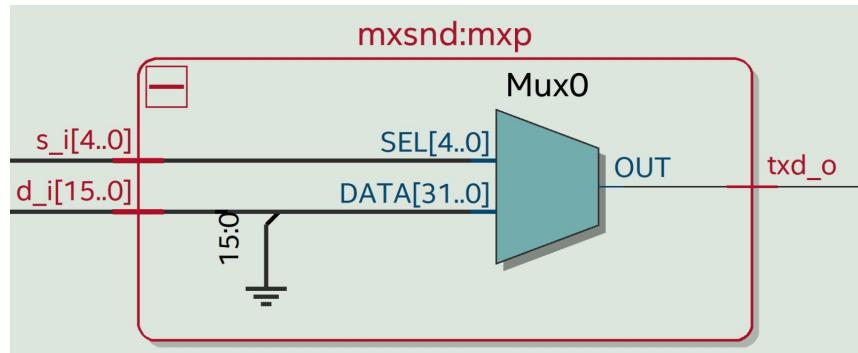


fig:mxsnd_mxp

s_i	IN	Bit position
d_i	IN	Bit vector
txd_o	OUT	txd, Serial Output

4 State Diagrams

The State Transition and the Output states of Uart,Control,Trigger and ifs_3 are given below

Internal Signal	Explanation
ini_wait_st	wait until
inc_clac_st	send increase signal to headcounter
dec_calc_st	send decrease signal to headcounter
inc_wait_st	wait until headcount calculated
dec_wait_st	wait until headcount calculated
inc_vali_st	done calculating, check if max
dec_vali_st	done calculating, check if min
inc_send_st	start sending num and ascii
dec_send_st	start sending num and ascii
min_send_st	start sending num and ascii
max_send_st	start sending num and ascii

4.1 Control Fsm

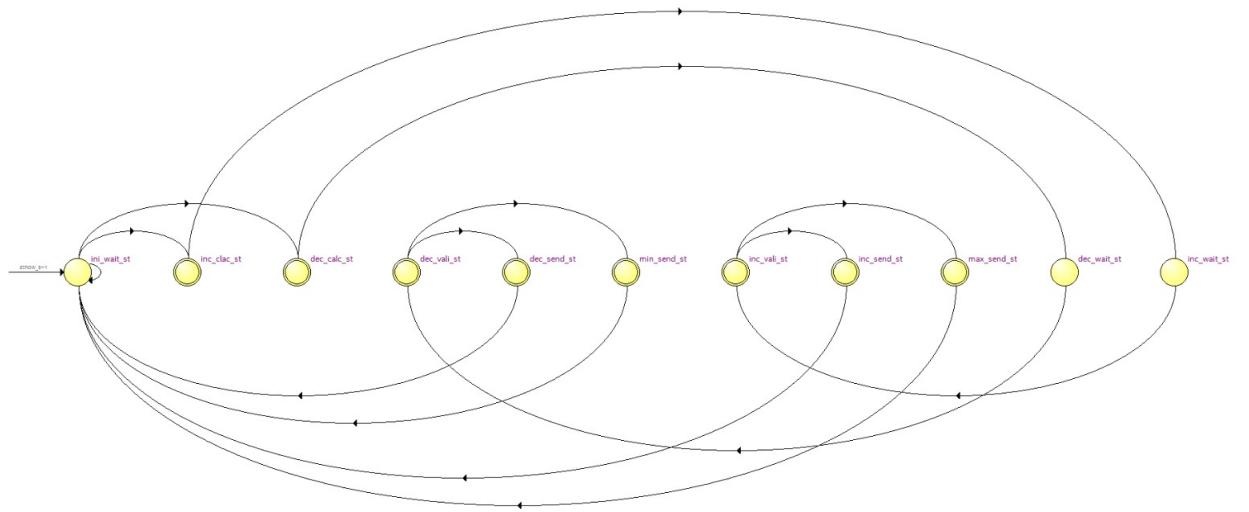


fig: Control FSM

Source State	Destination State	Condition
ewt1_st	ewt2_st	(!s3_i).(!s1_i).(s2_i)
ewt1_st	ewt1_st	(!s3_i).(!s1_i).(!s3_i)+(!s3_i).(s1_i)+(s3_i)
ewt2_st	ewt3_st	(s3_i).(!s1_i).(!s2_i)
ewt2_st	ewt2_st	(!s3_i)+(s3_i).(!s1_i)+(s3_i).(s1_i)
ewt3_st	init_st	
init_st	ewt1_st	(!s3_i).(s1_i).(!s2_i)
init_st	lwt1_st	(s3_i).(!s1_i).(!s2_i)
init_st	init_st	(!s3_i).(!s1_i)+(!s3_i).(s1_i).(s2_i)+(s3_i).(!s3_i).(s2_i)+(s3_i).(s1_i)
lwt1_st	lwt2_st	(!s3_i).(!s1_i).(!s2_i)
lwt1_st	lwt1_st	(!s3_i).(!s1_i).(!s2_i)+(!s3_i).(s1_i)+(s3_i)
lwt2_st	lwt3_st	(!S3_i).(s1_i).(!s2_i)
lwt2_st	lwt2_st	(!s3_i).(!s1_i)+(!s3_i)(s1_i).(s2_i)+(s3_i)
lwt3_st	init_st	

4.2 Trigger Fsm

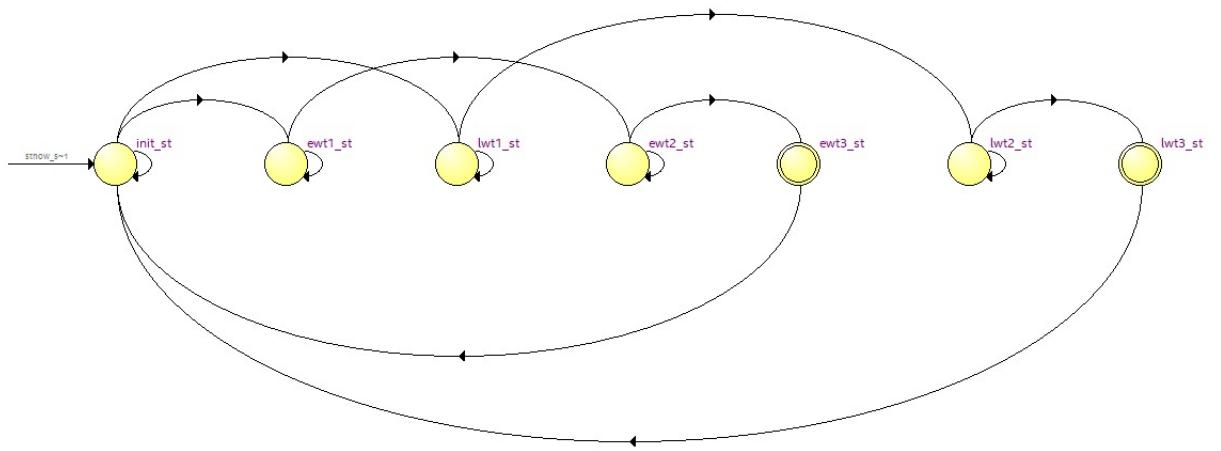


fig: Trigger FSM

Source State	Destination State	Condition

4.3 Uart Fsm

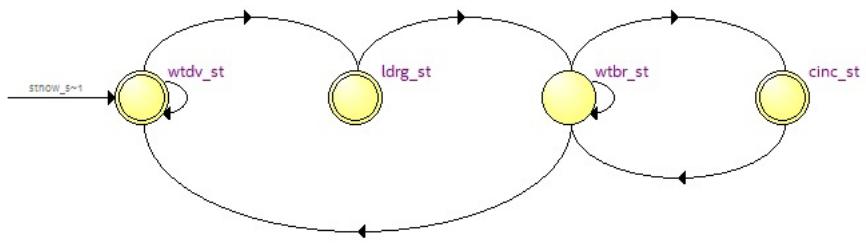


fig: Uart FSM

Source State	Destination State	Condition
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4.4 ifs_3 Fsm

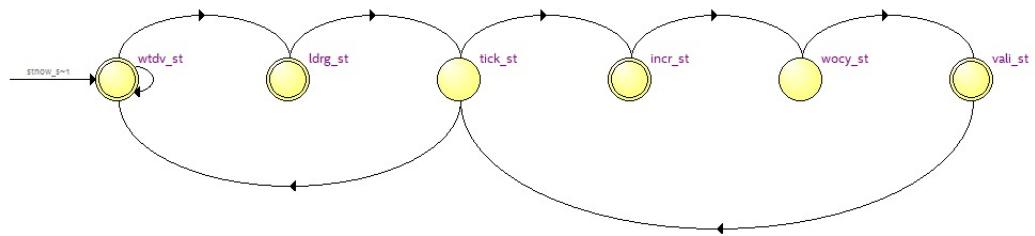


fig: ifs_3 FSM

Source State	Destination State	Condition
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