Industrial Automation
MKT4152

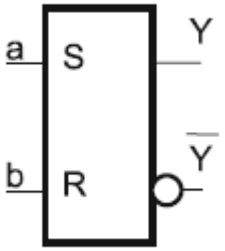
Introduction to
Programmable Logic Controllers
(PLC)

Programming Logic

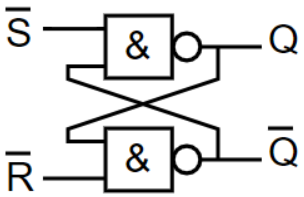
BOOLEAN ARITHMETIC

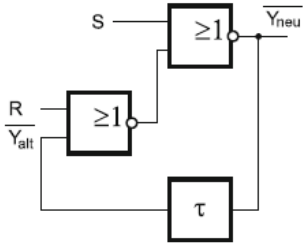
Bi-Stable Gates: RS & SR Flip Flop

RS-FLIP FLOP

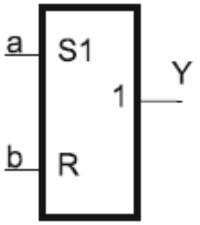


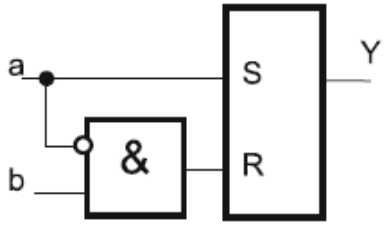
a	b	Y
0	0	Y (no change)
1	0	1 (set)
0	1	0 (reset)
1	1	?? forbidden





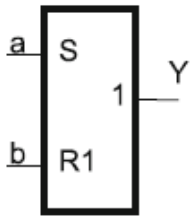
RS-FLIP FLOP – Dominant Set

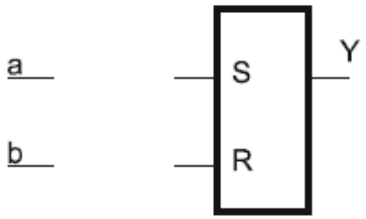




a	b	Y
0	0	Y
1	0	1 (Setzen)
0	1	0 (Rücksetzen)
1	1	**1 (Priorität)**

RS-FLIP FLOP – Dominant Reset

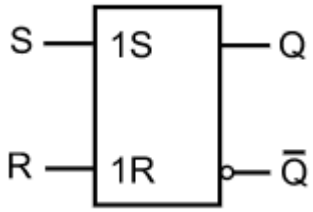


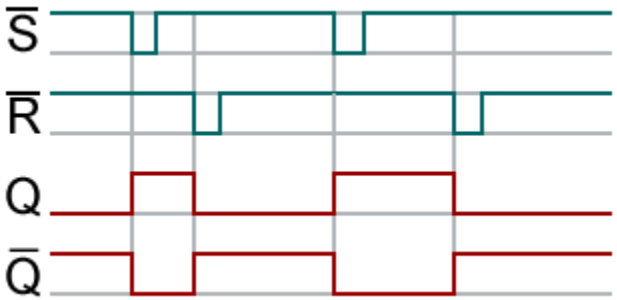


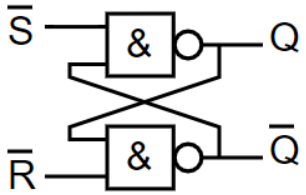
a	b	Y
0	0	Y
1	0	1 (Setzen)
0	1	0 (Rücksetzen)
1	1	**0 (Priorität)**

Trigger Activated Flip Flop I

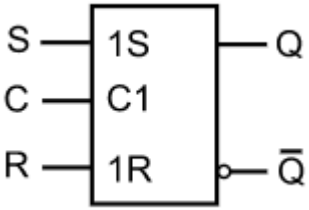
Asynchronous RS Flip Flop

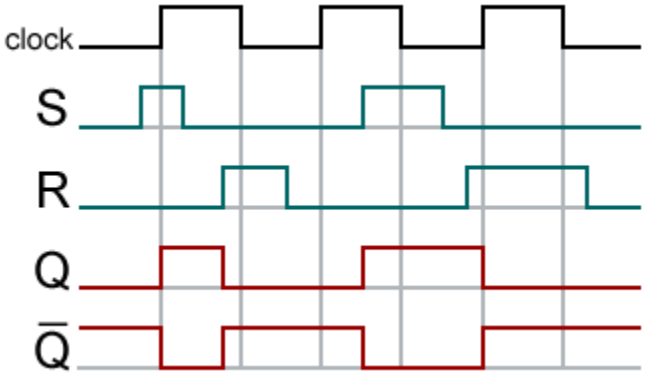


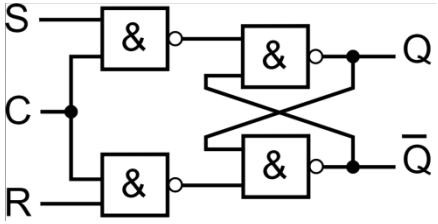




Synchronous RS Flip Flop







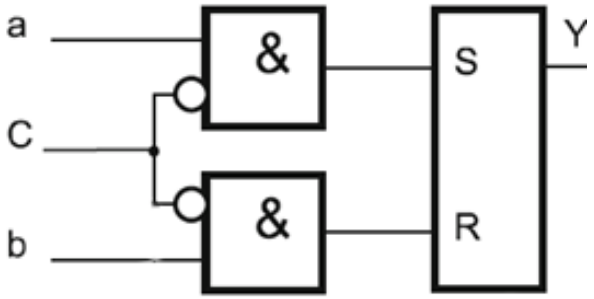
Trigger Activated Flip Flop II

Triggered Flip Flops are operational as long as control input C is active.
This might not always desired. It might be necessary to allow only ONE change in its output state each time the control signal becomes active.

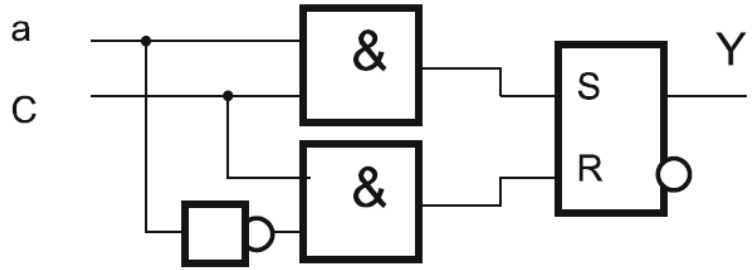
Question:
How can we realize a Flip-Flop, that changes its state only with rising edges, or falling edges?

RS Flip Flop with Dynamic Input

Synchronous RS Flip Flop

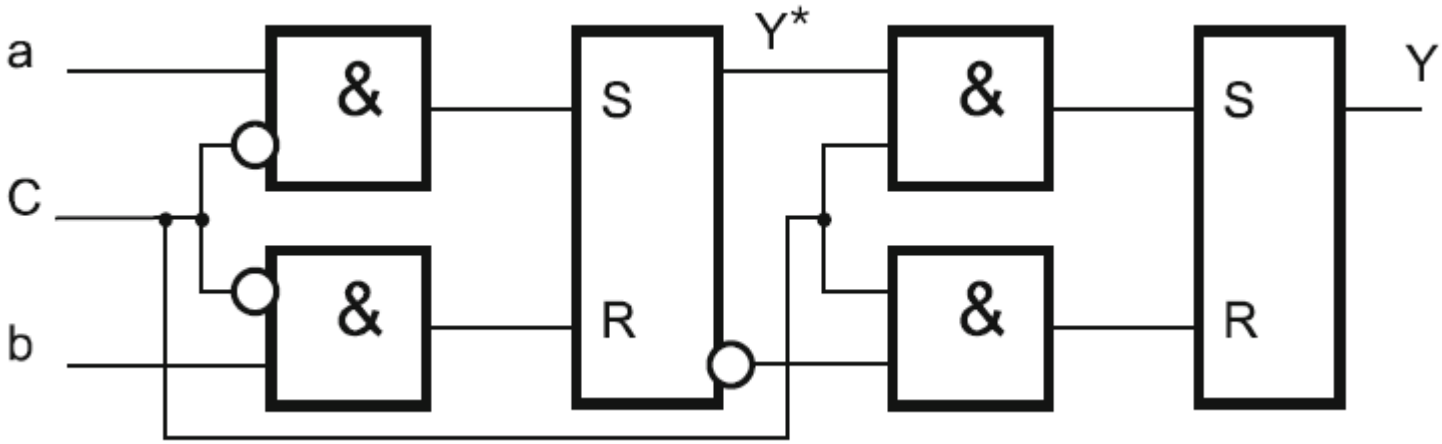


Triggered Memory

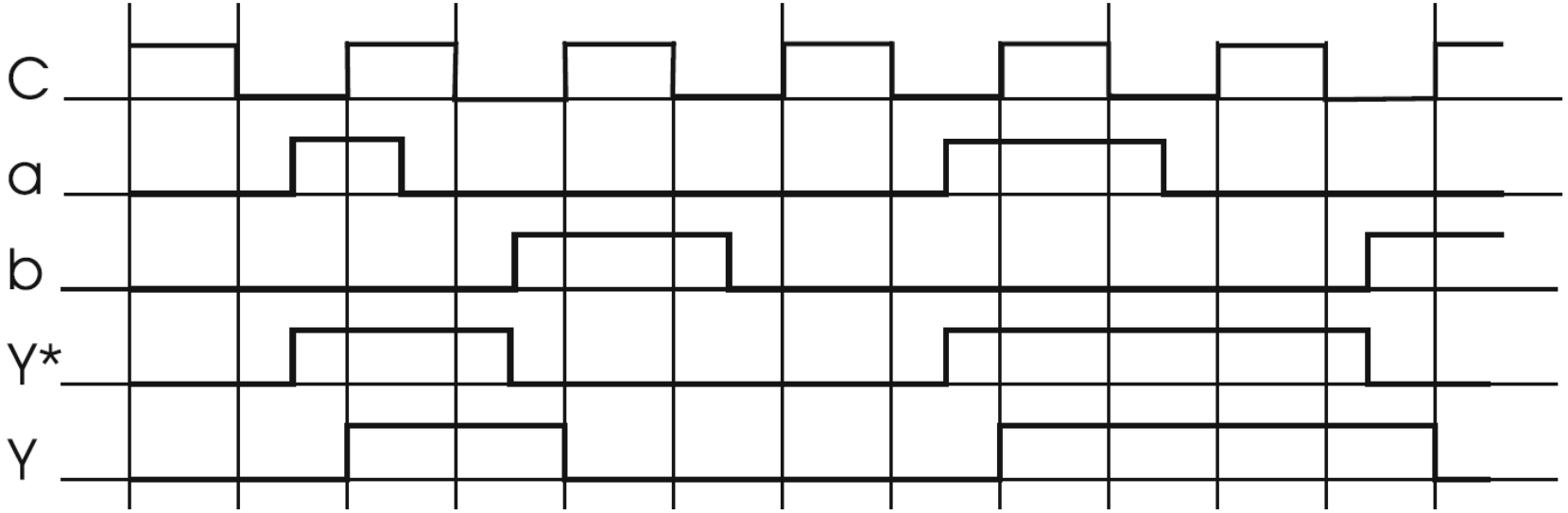


Pre-Storage

Post-Storage



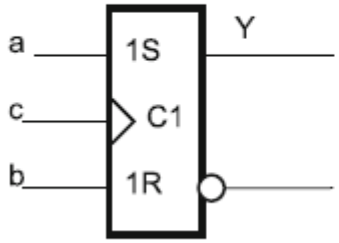
RS Flip Flop with Dynamic Input



But:
a AND b simultaneously is not defined!!!!

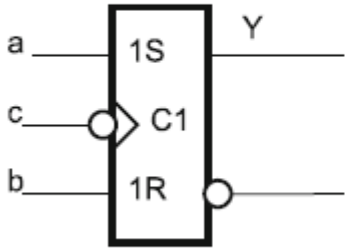
RS Flip Flop with Dynamic Input

Triggered on rising edge



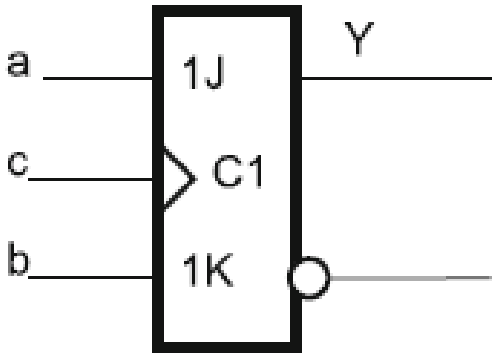
a	b	Y vor Flanke	Y nach Flanke
0	0	No change	
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	forbidden	

Triggered on falling edge



a	b	Y vor Flanke	Y nach Flanke
0	0	No change	
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	forbidden	

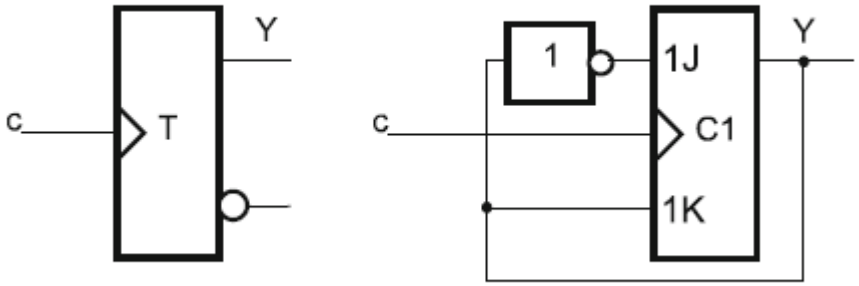
JK FLIP FLOP



a	b	Y vor Flanke	Y nach Flanke
0	0	No change	
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	**1**	**0**	**1**
1	**1**	**1**	**0**

JK Flip Flop
with a AND b, Y changes ist state with each trigger edge!!!

Bistable T-Gate (T Flip Flop)



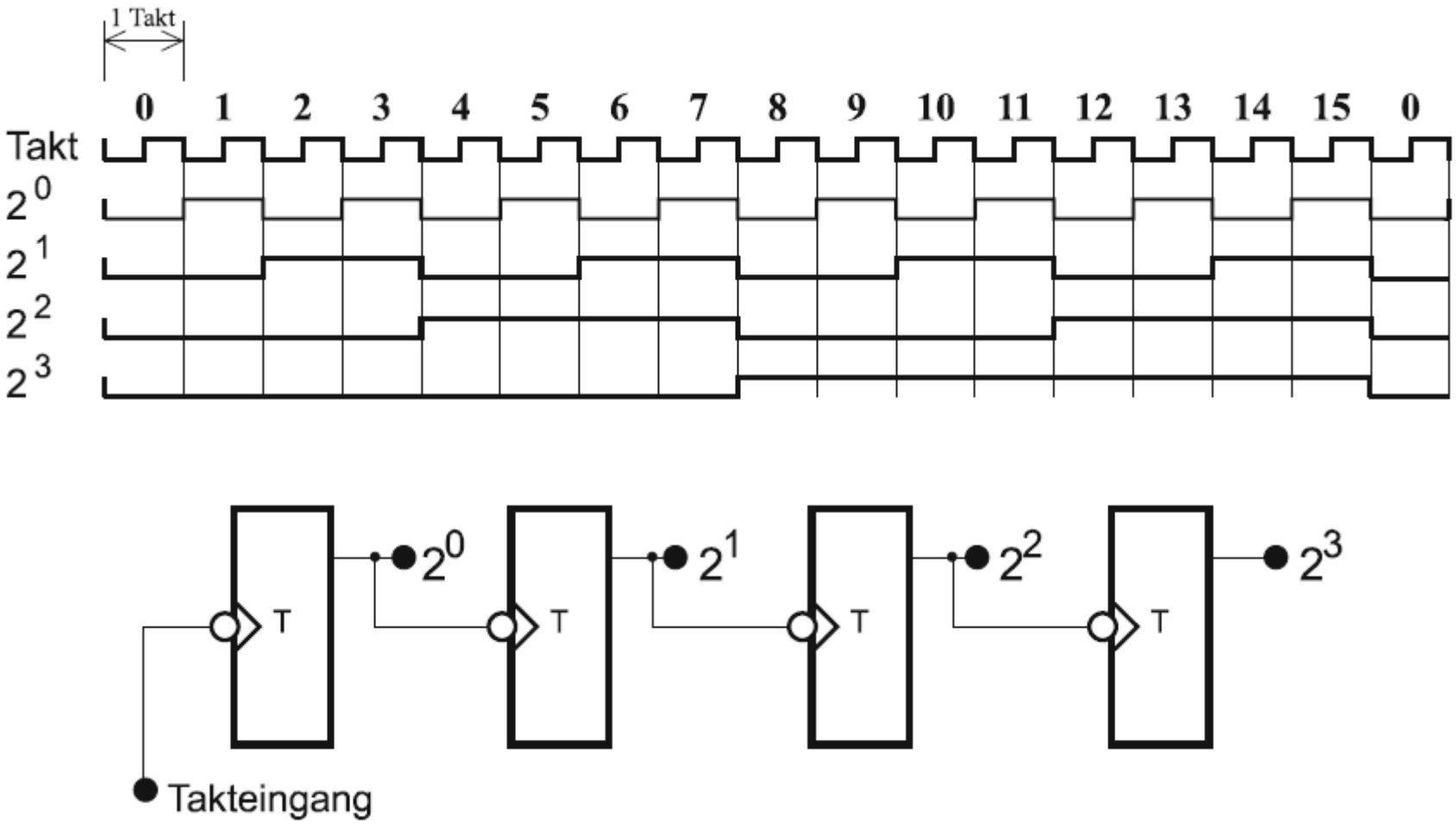
- Single input C
- Y changes its state with each rising edge

Counters

- T-Gate element can be used to realize counting functions
- Counter uses binary numbers

Dez	HEX	Dual			
		2^3	2^2	2^1	2^0
0	0	0	0	0	0
1	1	0	0	0	1
2	2	0	0	1	0
3	3	0	0	1	1
4	4	0	1	0	0
5	5	0	1	0	1
6	6	0	1	1	0
7	7	0	1	1	1
8	8	1	0	0	0
9	9	1	0	0	1
10	A	1	0	1	0
11	B	1	0	1	1
12	C	1	1	0	0
13	D	1	1	0	1
14	E	1	1	1	0
15	F	1	1	1	1

Asynchronous Counter

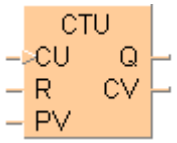


4 Bit asynchronous counter example, counts from 0 through 15

Practical Implementations

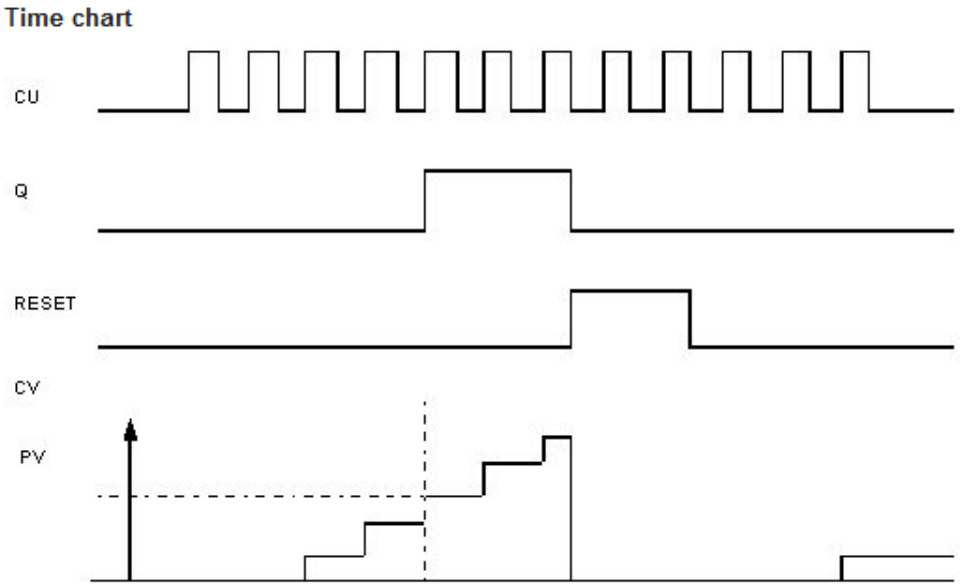
- Logic elements described so far should show basic operation principles of simple digital computers, a.k.a. PLC‘s
- Actual implementations feature ready-to-use function blocks
- Examples:
  - Up counter **CTU**
  - Down counter **CTD**
  - Up/down counter **CTUD**
- **Names are standardized in IEC61131-3**

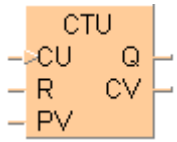
Example:
Up counter in Panasonic‘s FP Win pro



Input variable	Data type	Description
CU	BOOL	clock generator the value 1 is added to **CV** for each rising edge at **CU**, except when RESET is set
R (RESET)		reset **CV** is reset to zero for each rising edge at RESET
PV	INT	Set value if **PV** (preset value) is reached, **Q** is set
Output variable		
Q	BOOL	signal output is set if **CV** is greater than/equal to **PV**
CV	INT	Current value • contains the addition result (**CV** = current value) • The value can be changed during counting operation by writing to the variable from the programming editor.

CTU Timechart





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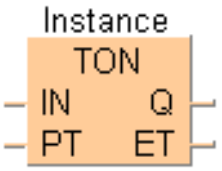
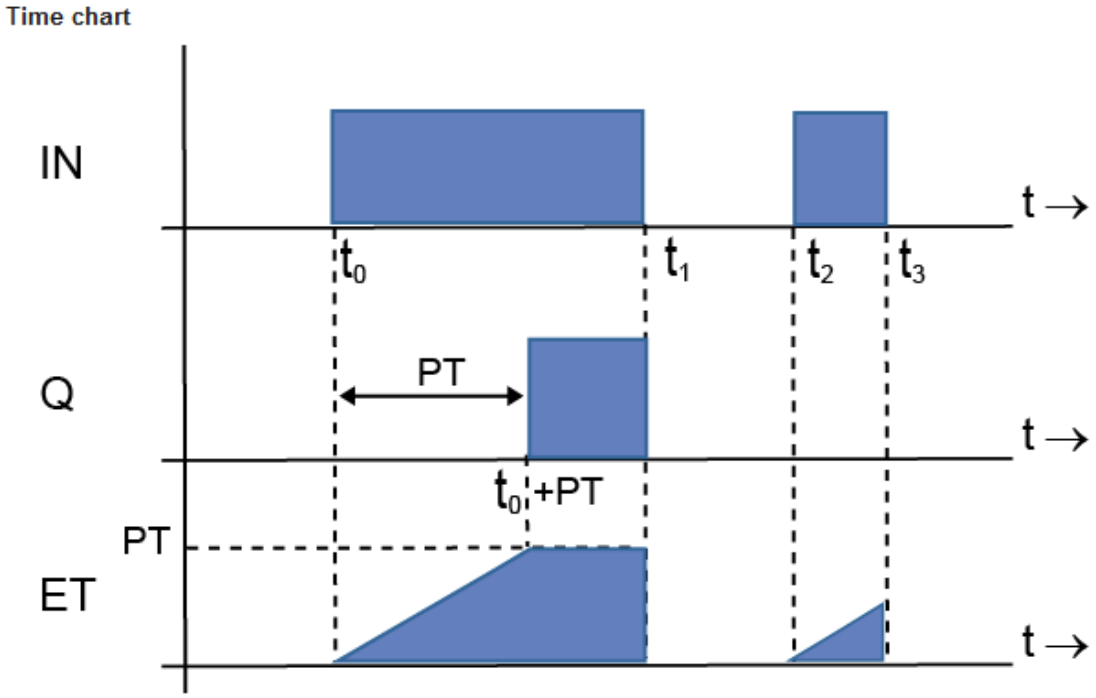
Delay Functions – TON

Timer with switch on delay



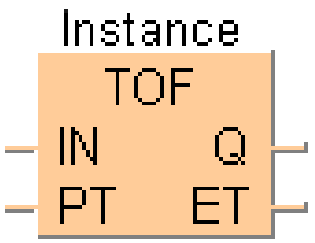
When input IN becomes true, output Q changes to true after period PT.

During this time, the elapsed time EP is shown in output ET.



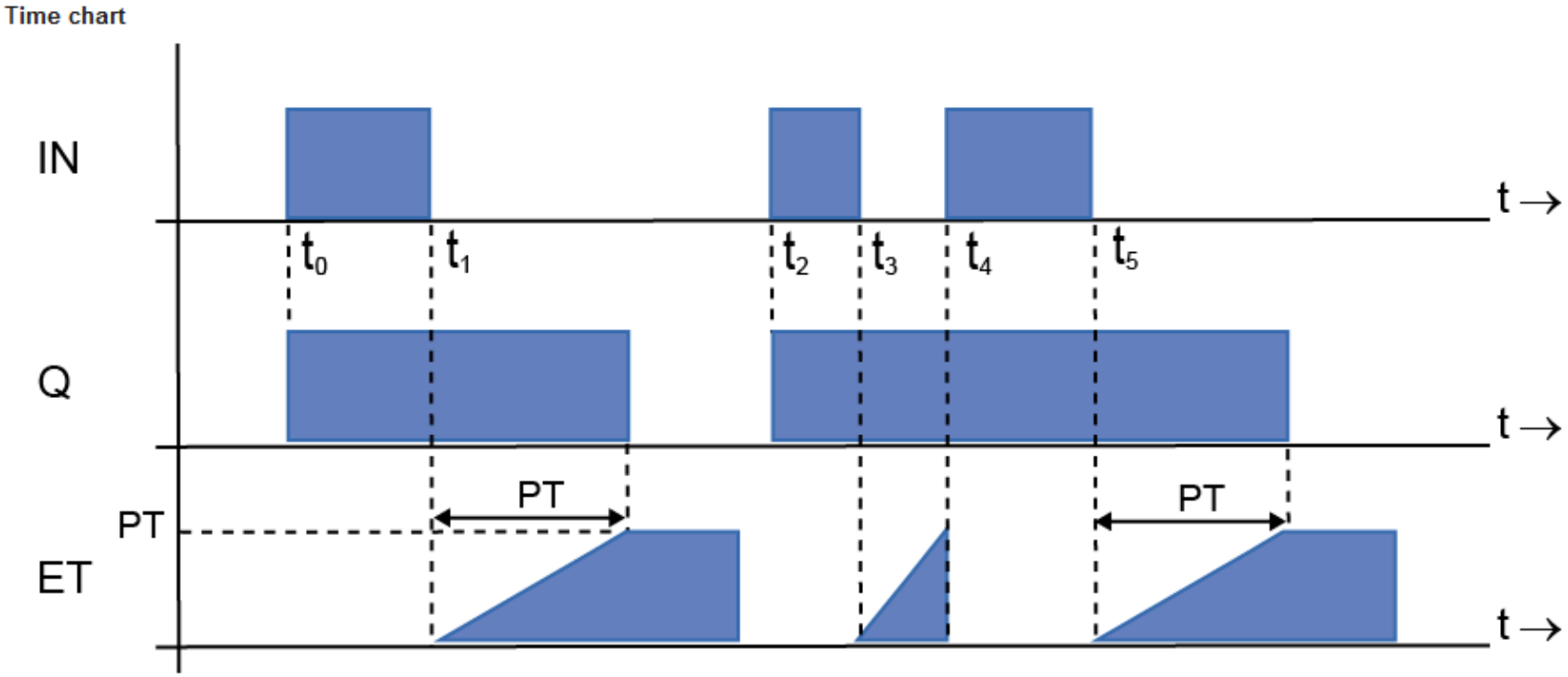
Delay Functions – TOF

Timer with switch off delay



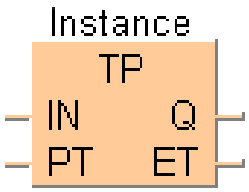
When IN becomes true, Q immediately changes to true. With falling edge of IN, Q remains true for time period PT.

Again, elapsed time is shown in ET

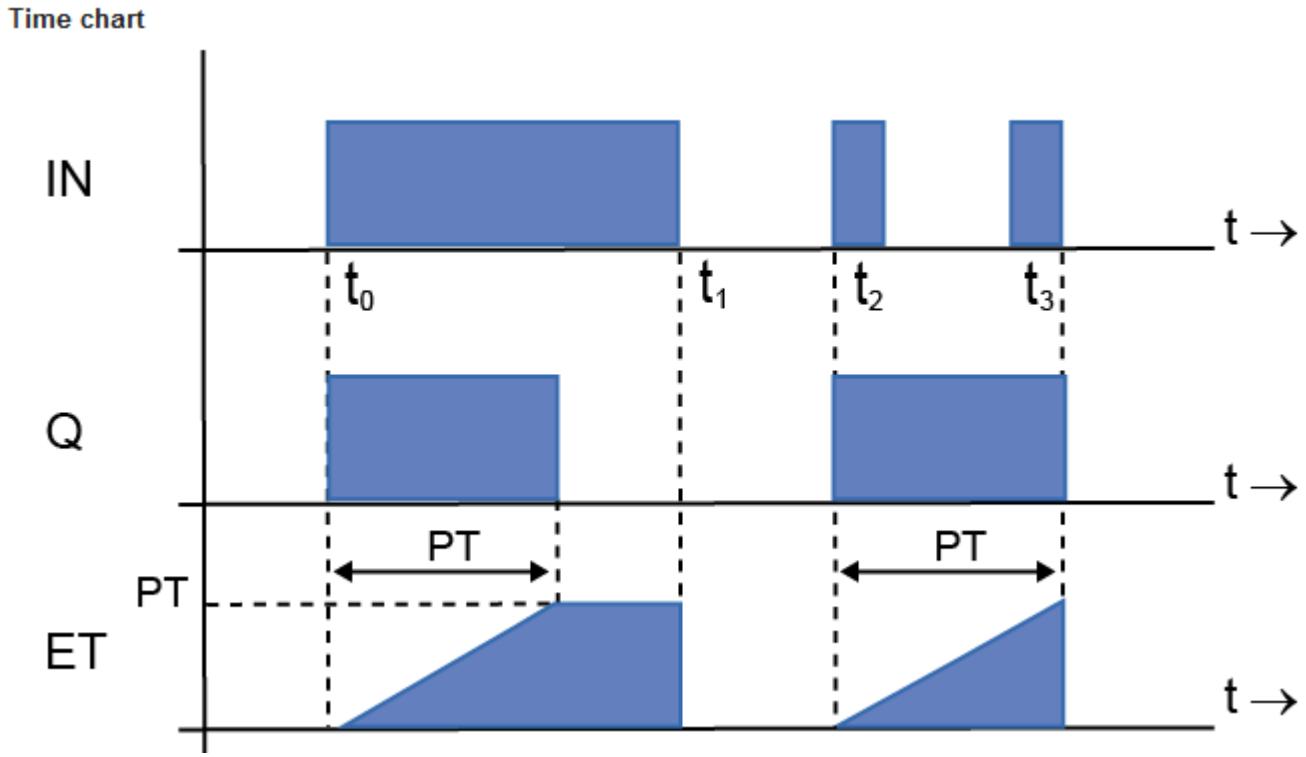


Delay Functions – TP

Timer with defined period



Upon each rising edge of **IN**, **Q** will follow for period **PT**, and then fall back to False.



IEC 61131-3

PLC PROGRAMMING

International Programming Standard IEC61131-3

- open international standard for programmable logic controllers
- First published in 1993
- Part 3 deals with basic software architecture and programming languages within PLC's
- Defines two graphical and two textual programming language standards:
  - **LD**: Ladder Diagrams
  - **FBD**: Function Block Diagram
  - **ST**: Structured Text
  - **IL**: instruction List
  - **SFC**: Sequential Function Chart

- Various implementations:
  - CodeSys
  - TwinCat (Beckhoff)
  - Control FP Win Pro (Panasonic)
- Different Implementations can be compatible, but are not required to
  GUI largly similar across implementations

POU Program organization unit

- Functions
  - Standard: ADD, SQRT, SIN, COS, MIN, …..
  - Custom Functions: user-definable
- Function Blocks
  - Standard: TOF, TON, RS, SR, …..
  - Custom Functions: User-definable
- Programs

Variables

- Global
- Direct
- I/O Mapping
- ….

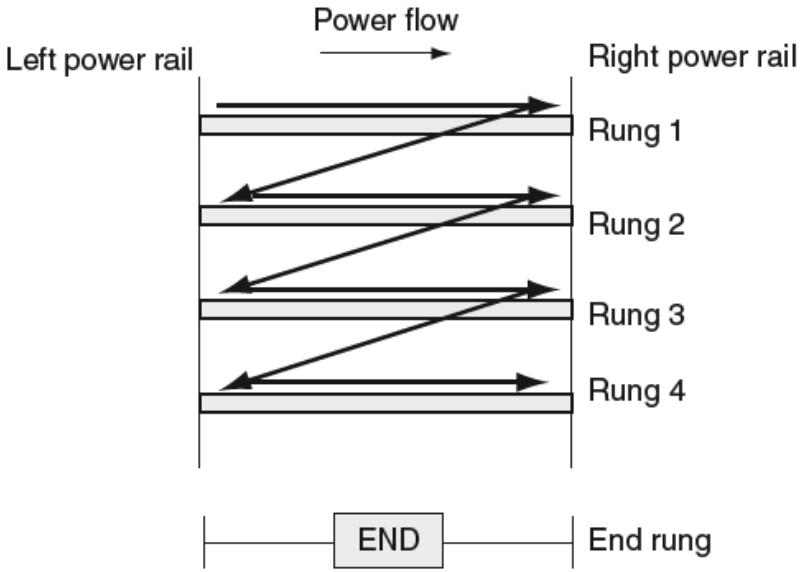
Basic Data Types

- Boolean [Bool] True/False
- Integer
- SINT - signed short integer (1 byte, -128..127)
- INT - signed integer (2byte, -32768..32767)
- DINT – signed double integer (4byte, -2^31 .. (2^31)-1)
- UINT – unsigned integer (2 byte, 0..65536)
- REAL – floating point, 4 byte
- ….

IEC 61131-3

LADDER DIAGRAMS

Ladder Diagrams



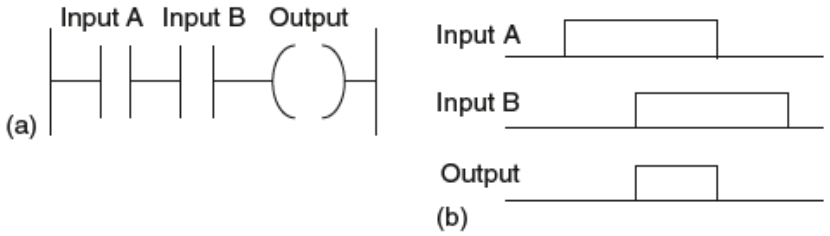
- The vertical lines of the diagram represent the power rails between which circuits are connected. The power flow is taken to be from the left-hand vertical across a rung.
- Each rung on the ladder defines one operation in the control process.
- A ladder diagram is read from left to right and from top to bottom.
  The figure is showing the scanning motion employed by the PLC. The top rung is read from left to right. Then the second rung down is read from left to right and so on.
- When the PLC is in its run mode, it goes through the entire ladder program to the end, the end rung of the program being clearly denoted, and then promptly resumes at the start. This procedure of going through all the rungs of the program is termed **a cycle**. The end rung might be indicated by a block with the word END or RET for return, since the program promptly returns to its beginning.

Ladder Diagrams

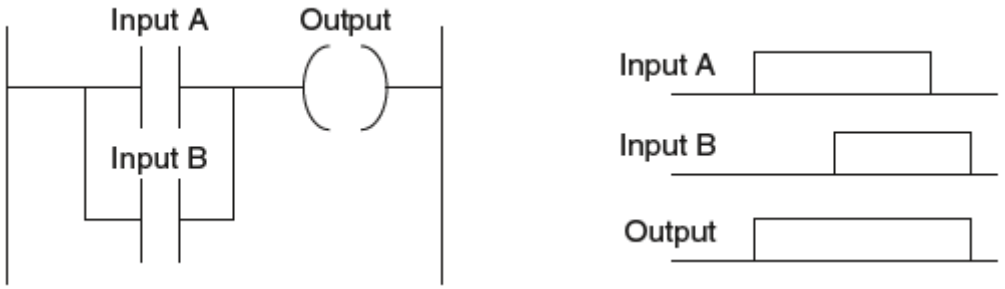
- Each rung must start with an input or inputs and must end with at least one output. The term input is used for a control action, such as closing the contacts of a switch, used as an input to the PLC. The term output is used for a device connected to the output of a PLC, e.g., a motor.
- Electrical devices are shown in their normal condition. Thus a switch, which is normally open until some object closes it, is shown as open on the ladder diagram. A switch that is normally closed is shown closed.
- A particular device can appear in more than one rung of a ladder. For example, we might have a relay that switches on one or more devices. The same letters and/or numbers are used to label the device in each situation.
- The inputs and outputs are all identified by their addresses, the notation used depending on the PLC manufacturer. This is the address of the input or output in the memory of the PLC.

Ladder Logic: Logic Elements: AND, OR, NOT

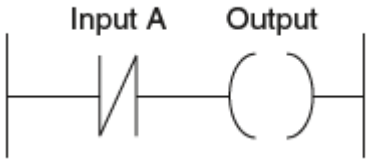
AND Gate



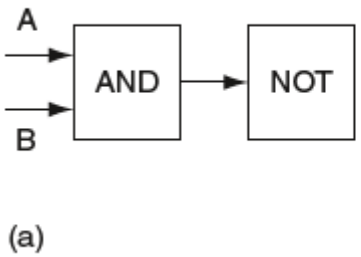
OR Gate



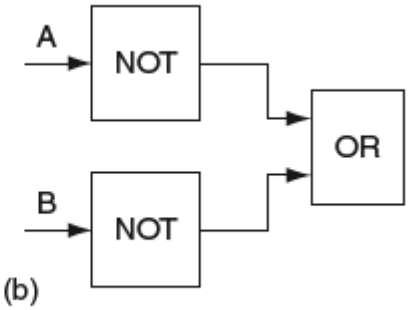
NOT Gate



NAND Gate

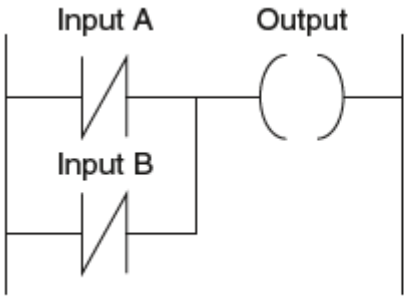


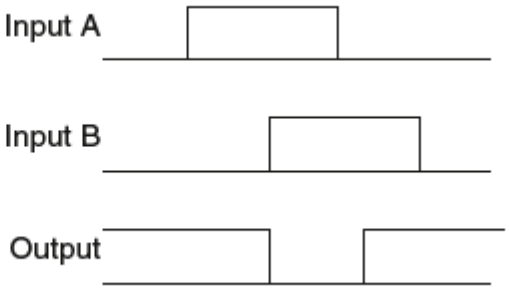
(a)



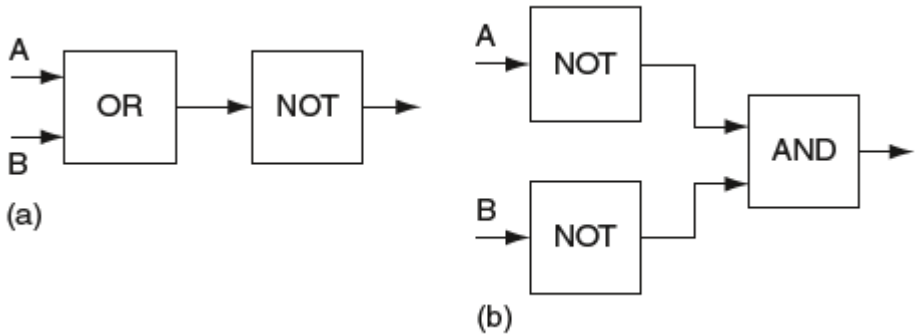
(b)

Inputs		Output
A	B	
0	0	1
0	1	1
1	0	1
1	1	0

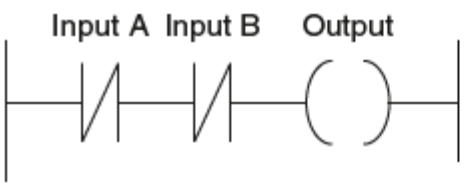


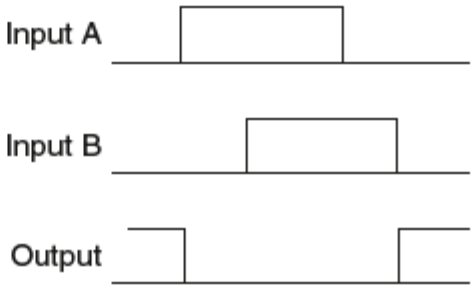


NOR Gate

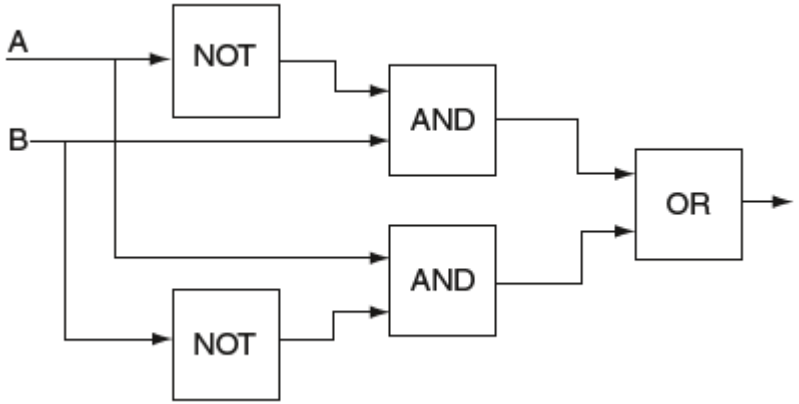


Inputs		Output
A	B	
0	0	1
0	1	0
1	0	0
1	1	0

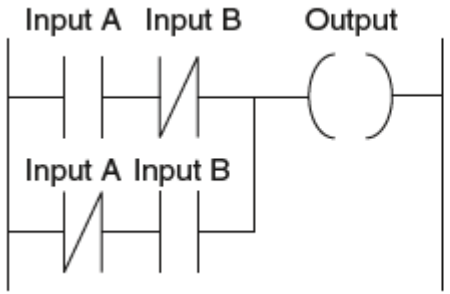


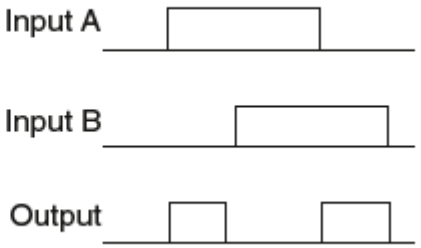


Exlusive OR - XOR Gate



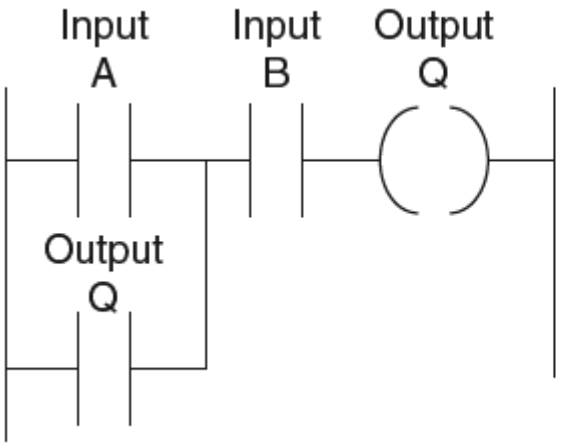
Inputs		Output
A	B	
0	0	0
0	1	1
1	0	1
1	1	0

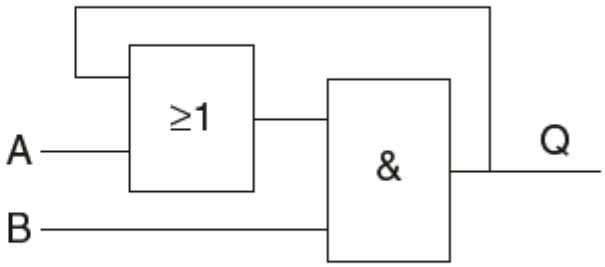




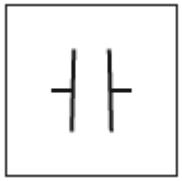
Latching

- There are often situations where it is necessary to hold an output energized, even when the input ceases.
- Simple example: motor, which is started by pressing a push button switch. Though the switch contacts do not remain closed, the motor is required to continue running until a stop push button switch is pressed. The term **latch circuit** is used for the circuit used to carry out such an operation.
- Latch Circuit:
  Self-maintaining circuit that, after being energized, maintains that state until another input is received.

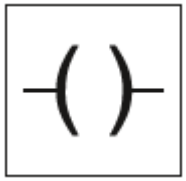




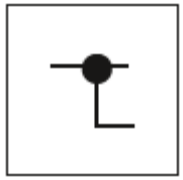
Ladder Symbols



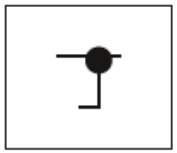
Contact (Input)



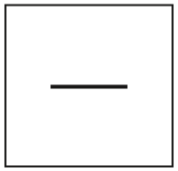
Coil (Output)



Junction Start



Junction End



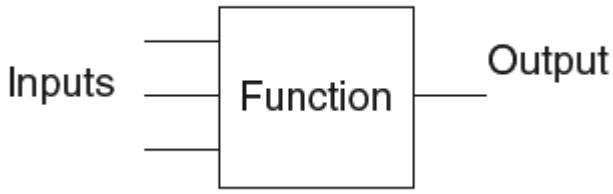
Connection Line

Function Blocks

Function blocks are program instruction units. They can be used within Ladder Diagrams. They have one or more inputs, and one or more outputs.

Examples:

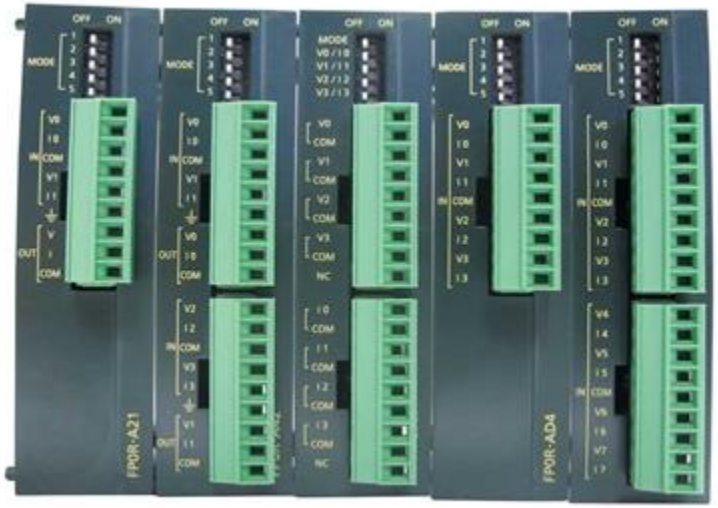
- TON – timer on delay
- TOF - timer off delay
- RS / SR Flip Flops
- User-defined custom functions



Application Example

PANASONIC FP0R

Application Example : Panasonic FP0R



- Modular PLC
- Standard interfaces:
  - digital I/O
  - serial Ports RS232 RS485
- Available Modules:
  - Digital I/O
  - Analog I/O
  - Profibus
  - Temperature Sensor Interfaces
    Thermoelement type K/J, Pt100
- Software:
  FP win Pro
  comforming with IEC 61131-3
  free version limited to 1000 steps

Panasonic FP0R: Specifications I

Product type of FP0R control unit			C10 (Relay output type only)	C14 (Relay output type only)	C16 (Transistor output type only)
Programming method / Control method			Relay symbol / Cyclic operation		
Number of I/O points	No expansion (Control unit only)		10 points [Input: 6, Relay output: 4]	14 points [Input: 8, Relay output: 6]	16 points [Input: 8, Transistor output: 8]
	With expansion 1 Same type of control and expansion units (Note)		Max. 58 points	Max. 62 points	Max. 112 points
	With expansion 2 Mix type of relay and transistor units (Note)		Max. 106 points	Max. 110 points	Max. 112 points
Program memory			EEPROM (no backup battery required)		
Program capacity			16 k steps		
Number of instructions		Basic	110 approx.		
		High-level	210 approx.		
Operation speed		Up to 3,000 steps	Basic instructions: 0.08 µs min. Timer instructions: 2.2 µs min. High-level instructions: 0.32 µs (MV instruction) Min.		
		3,001st and later steps	Basic instructions: 0.58 µs min. Timer instructions: 3.66 µs min. High-level instructions: 1.62 µs (MV instruction) Min.		

Panasonic FP0R: Specifications II

Operation memory	Relay	Internal relay (R)	4,096 points
		Timer / Counter (T / C)	1,024 points
	Memory area	Data register (DT)	12,315 words
		Index register (IX, IY)	14 words (IO to ID)
Master control relay points (MCR)			256 words
Number of labels (JMP and LOOP)			256 labels
Differential points			Equivalent to the program capacity
Number of step ladder			1,000 stages
Number of subroutines			500 subroutines

Panasonic FP0R: Specifications II

Special functions	High speed counter	Single-phase: 6 points (50 kHz max. each) 2-phase: 3 channels (15 kHz max. each)(Note)	
	Pulse output	Not available	4 points (50 kHz max. each) 2 channels can be controlled individually.(Note)
	PWM output	Not available	4 points (6 Hz to 4.8 kHz)
	Pulse catch input / interrupt input	Total 8 points (with high speed counter)	
	Interrupt program	Input: 8 programs (6 programs for C10 only) / Periodic: 1 program / Pulse match: 4 programs/td>	
	Periodical interrupt	In units of 0.5 ms: 0.5 ms to 1.5 sec. / In units of 10 ms: 10 ms to 30 sec.	
	Constant scan	In units of 0.5 ms: 0.5 ms to 600 ms	
	RS232C port	One RS232C port is mounted on each of C10CRS, C10CRM, C14CRS, C14CRM, C16CT, C16CP, C32CT, C32CP, T32CT, T32CP, F32CT and F32CP type (3P terminal block) Transmission speed (Baud rate): 2,400 to 115,200 bits/sec, Transmission distance: 15 m 9.843 ft. Communication method: half duplex	
	RS485 port	One RS485 port is mounted on each of C10MRS, C14MRS, C16MT, C16MP, C32MT, C32MP, T32MT, T32MP, F32MT and F32MP type(3P terminal block) Transmission speed (Baud rate): 115.2 kbps (It is possible to change to 19.2 kbps by the setting.), Transmission distance: 1,200 m 3,937 ft, Communication method: half duplex	

Panasonic FP0R: Specifications IV

Maintenance	Memory backup	Program and system register	Stored program and system register in EEPROM
		Operation memory	Stored fixed area in EEPROM Counter: 16 points Internal relay: 128 points Data register: 315 words
	Self-diagnostic function		Watchdog timer (690 ms approx.), Program syntax check
	Real-time clock function		Not available
	Other functions		Rewriting in RUN mode, Download in RUN mode (incl. comments), 8-character password setting, and Program upload protection

Panasonic FP0R: Specifications V

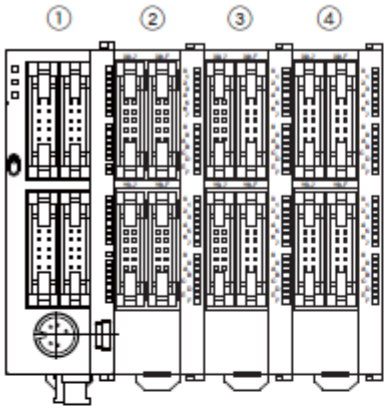
Item		Specifications
Rated voltage		24 V DC
Operating voltage range		20.4 to 28.8 V DC
Allowed momentary power off time	C10, C14, C16	5 ms (at 20.4 V DC), 10 ms (21.6 V DC or higher)
	C32, T32, F32	10 ms (20.4 V DC or higher)
Ambient temperature		0 to +55 °C 32 to +131 °F
Storage temperature		-40 to +70 °C -40 to +158 °F (-20 °C to +70 °C -4 to +158 °F for T32 only)
Ambient humidity		10 to 95% RH (at 25 °C 77 °F, no condensation)
Storage humidity		10 to 95% RH (at 25 °C 77 °F, no condensation)
Breakdown voltage (Detection current: 5 mA)		Input terminals - output terminals, Output terminals – power and functional ground terminals --- Transistor output: 500 V AC for 1 minute (Relay output: 1,500 V AC for 1 minute) / Input terminals – power and functional ground terminals, Functional ground terminal – power terminal --- Transistor output: 500 V AC for 1 minute (Relay output: 500 V AC for 1 minute) / Output terminals – output terminals (different common terminals) --- Relay output: 1,500 V AC for 1 minute
Insulation resistance (Test voltage: 500 V DC)		Input terminals - output terminals, input terminals – power and functional ground terminals, output terminals – power and functional ground terminals, functional ground terminal – power terminal --- Transistor output: 100 MΩ minimum (relay output: 100 MΩ minimum) / Output terminals – output terminals (different common terminals) --- Relay output: 100 MΩ minimum
Vibration resistance		5 to 9 Hz, single amplitude of 3.5 mm, 1 sweep/min; 9 to 150 Hz, constant acceleration of 9.8 m/s^2, 1 sweep/min; for 10 min each in X, Y, and Z directions
Shock resistance		147 m/s^2 or more , 4 times each in X, Y, and Z directions
Noise immunity		1,000 V (p-p) with pulse widths 50 ns and 1 µs (using a noise simulator) (Power supply terminal)
Operating condition		Free from corrosive gasses and excessive dust

Panasonic FP0R: I/O Address Allocation

The I/O allocation of the FP0R CPU is fixed.

CPU type		Number of I/O points	I/O addresses
C10	Input	6	X0–X5
	Output	4	Y0–Y3
C14	Input	8	X0–X7
	Output	6	Y0–Y5
C16	Input	8	X0–X7
	Output	8	Y0–Y7
C32/T32/F32	Input	16	X0–XF
	Output	16	Y0–YF

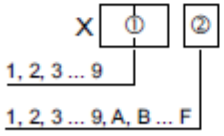
I/O allocation is performed automatically when an expansion unit is added and is determined by the installation location. The I/O allocation of the FP0R CPU is fixed.



Type of unit	Unit number		I/O addresses
FP0R CPU	①	–	X0–XF Y0–YF
FP0/FP0R I/O expansion unit	②	1	X20–X3F Y20–Y3F
	③	2	X40–X5F Y40–Y5F
	④	3	X60–X7F Y60–Y7F

◆NOTE

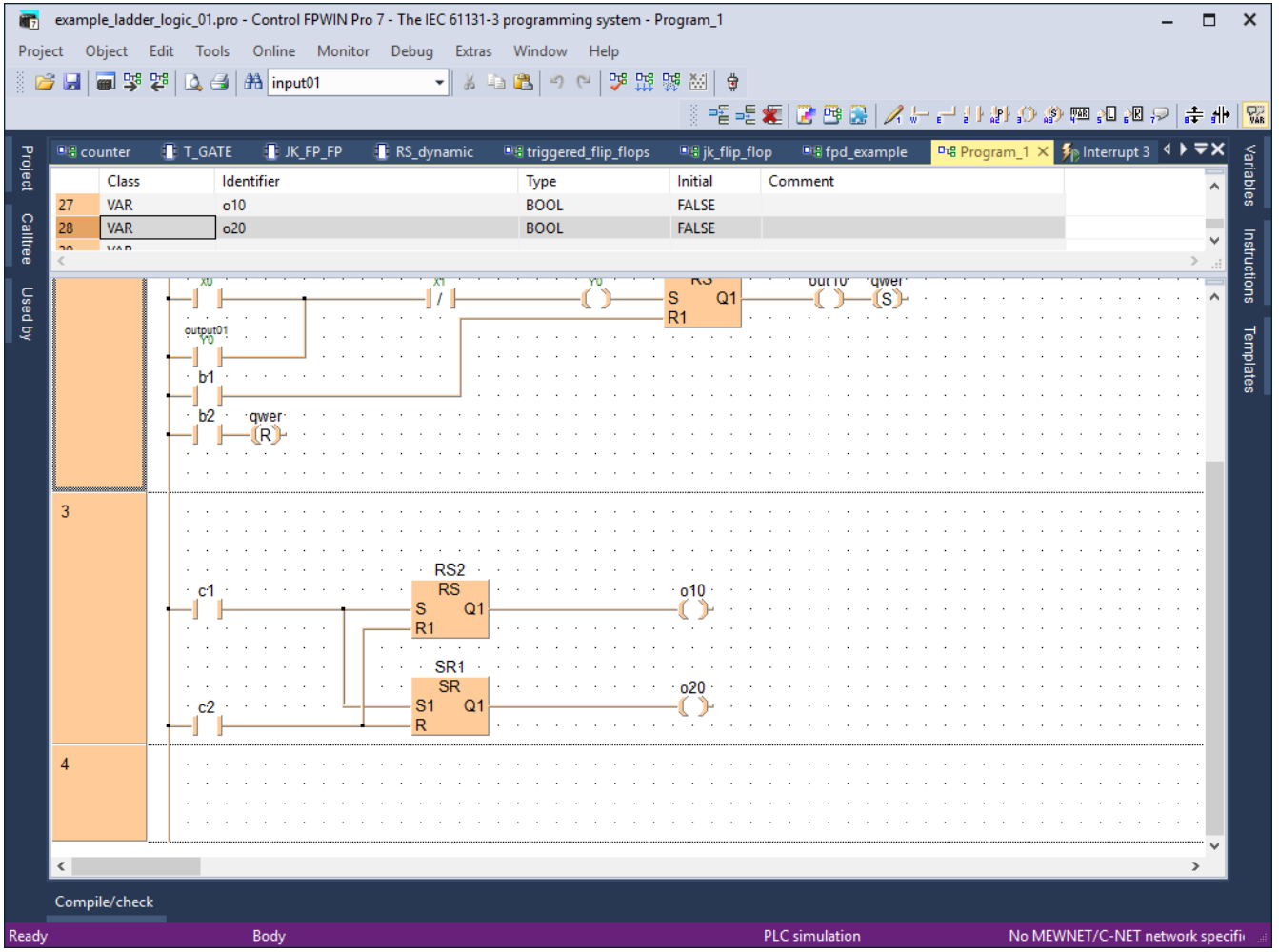
- The input relay "X" and output relay "Y" are expressed as a combination of decimal (①) and hexadecimal (②) numbers:



- On the FP0R and the FP0, the same numbers are used for inputs and outputs, e.g. X20, Y20.
- The usable I/O numbers depend on the unit type. See "FP0/FP0R Expansion Units" on page 64.

FP Win pro

- Panasonic fully implemented IEC 61131-3 as standalone application
- Ready-to-use with Panasonic PLC‘s
- Interface similar to Codesys
- Free version available on panasonics Website www.panasonic-electric-works.com
- Software simulation of panasonic PLC‘s



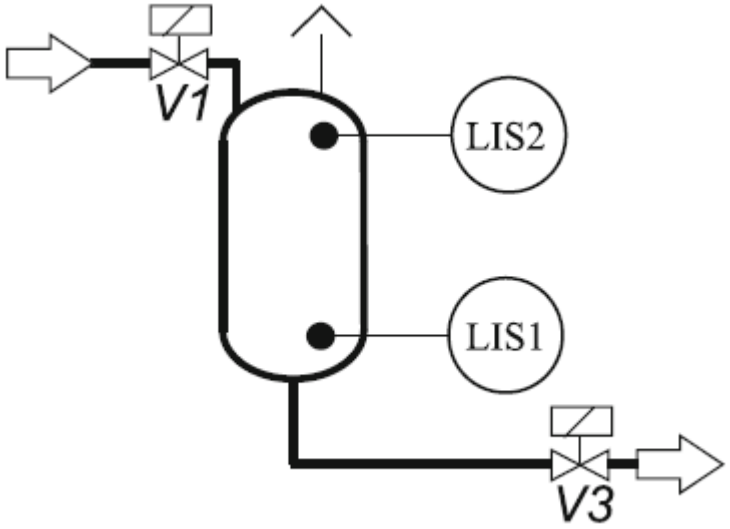
Practical Training

EXAMPLE PROBLEMS

Industrial Volume Measurement

Tank on the right hand side has:

- Valve V1 for filling
  true for open valve
- Valve V3 for emptying
  true for open valve
- Liquid Level Sensor LIS1
  true indicates maximum fluid level has been reached
- Liquid Level Sensor LIS2
  true indicates fluid level greater than minimum



Objectives (A)

- Two buttons F and E (F for fill, E for empty)
- Pressing F should fill the tank
- Pressing E should drain tank
- While filling is active, the tank must not be drained
- While emptying is active, valve V1 must remain closed
- V1 can only open when LIS2 is false
- V3 must close when LIS1 becomes false

Objectives (B)

- Replace buttons F and E with a single push button, which first fills and then drains the tank

Solution