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Narendra M Acharya

- **Hardware architect and designer** with close to 20 years of experience in architecture, micro-architecture, design development, performance analysis, low-power, synthesis, timing closure, emulation and post-silicon bring-up - at **Nvidia**, **EdgeQ** and **Broadcom**.
- **Architected complex HW sub-systems** - 5G Modem Digital Front End at **EdgeQ**, high-performance PCIe controller at **Nvidia** and 4G Modem Demodulator-Decoder engines at **Broadcom**, demonstrating expertise in data-path and control design. Experienced in taking SoCs from initial architecture to productization.
- **Deep understanding of HW/SW co-design** - Responsible for development of virtualisation of Nvidia GPU with SRIOV and PCIe Gen5 in Nvidia Hopper which involved interactions with GPU architecture team. Developed RF driver at EdgeQ which was delivered to customers and ODM partners across Taiwan, UK and US. Did HW/SW partitioning for converged 5G and WiFi modem's AGC scheme with RFIC partner, leading to a design patent.
- **Architect and Lead for Virtual Platform** at EdgeQ, developed SystemC model for the 5G Modem SoC containing custom HW accelerator models integrated with third-party CPU models for ARM and RISCV.
- **Engineering Lead for EdgeQ RF execution** - Owning chipset integration of EdgeQ SoC and RFICs from multiple vendors like Analog Devices. Colloborated with product management to define RF strategy and with SW and board design teams for product design and PCB-level implementation.
- **Well-versed in Project Management** - Led EdgeQ's emulation effort for an SoC 100s of million gates in size, coordinating with SW teams for platform SW bring-up followed by modem SW execution.
- **Managed design, verification, virtual platform, emulation and post-silicon teams** delivering IP and sub-systems designed from scratch into multiple successful tape-outs. A successful **mentor** to my team members.

Work Experience

2020-Current

Senior Principal Engineer in EdgeQ:

- Currently leading the architecture and development of the **5G NR** modem **Digital Front End** module (DFE) and RFIC interfaces.
  End-to-end ownership of a sub-system, ranging from initial architecture to post-silicon bring-up of the OFDM time-domain processing chain including RFIC.
- Developed **HW accelerators** for sampling rate convertors, filters, mixers connecting to an **AXI4** system bus and **JESD204C** RFIC bus.
- Created **performance model** of the modem SoC to determine bandwidth and latency requirements for the NoC and chip IOs.
- Worked with **third-party vendors** to integrate Baseband and RFIC into a gNodeB system, leading to a patent (US11558070B1).

- Responsible for specification, bring-up and debug of complex Baseband and RFIC systems developed by ODMs. Hands-on experience in PCB debug.
- **Co-designed SW** for the DFE and RFIC driver following ORAN P19 specification, delivered to customers and ODMs across Taiwan, US and UK.
- Architect and lead of the **Virtual Platform** for a multi-ISA (ARM, RISCV) gNodeB VP to enable early SW development.
- Led the emulation team and brought up the gNodeB SoC on Synopsys Zebu and Cadence Protium. Collaborated with SW team to boot Linux on the SoC before tapeout.

2013-2019

Senior ASIC Engineer in NVIDIA Graphics:

- Architecture lead for **Hopper PCIe 5.0**[1], a grounds-up design which integrated into the GPU memory sub-system and supported **CXL**. Hopper's GH100 is widely deployed in data centers.
- Led the architecture and development of **GPU virtualization**[2] using **SR-IOV**. Defined and implemented SW driver interface to implement various features of SR-IOV.
- Performed analysis of bandwidth and latency requirements for **PCIe 4.0** in **Ampere** GPU, across HPC, cloud and workstation products.
- Designed the **VirtualLink**[3] connection to VR headsets over PCIe in GPU, providing latency guarantees to isochronous USB traffic concurrent with GPU traffic.
- Designed low-power feature called **RTD3** for notebook GPUs. Coordinated across multiple ASIC and SW teams for the implementation of the feature.
- Developed verification methodology and test-bench implementation for validating **Unified Memory**[4] in **Pascal** GPU.

2005-2012

Senior Staff Engineer in (Beceem) Broadcom Communications:

- Led the design, implementation and verification of a **programmable framer, demodulator, decoder engine** with HARQ features for an **LTE Rel9** modem sub-system.
- Developed micro-architecture and implemented RTL for **synchronization, hand-off and link-adaption HW accelerators** which were part of a WiMax SoC.
- Designed and developed the verification stimulus generator and interface BFMs for a WiMax SoC.

Patents

#11,558,070

Fast AGC convergence using high-speed interface between baseband and RFIC

Education

2001-2005

Completed B.E, Telecommunications engineering in APS College of Engineering, Bangalore.

[1] https://developer.nvidia.com/blog/nvidia-hopper-architecture-in-depth/
[2] https://www.nvidia.com/en-in/technologies/multi-instance-gpu/
[3] https://en.wikipedia.org/wiki/VirtualLink
[4] https://devblogs.nvidia.com/parallelforall/unified-memory-in-cuda-6/