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Narendra M Acharya

- **Hardware architect and designer** with 18+ years of experience in architecture, micro-architecture, design development, performance/power analysis, synthesis, timing closure and post-silicon bring-up.
- **Managed design teams** delivering IP and sub-sytems into multiple successful tape-outs.
- Expert in Verilog/SV, C/C++ and various scripting languages with a **deep understanding of HW/SW co-design**.

Work Experience

2020-Current

Senior Principal Engineer in EdgeQ:

- Currently leading the architecture and development of the **5G NR** gNodeB **Digital Front End** module (DFE) and RFIC interfaces.
  End-to-end ownership ranging from initial architecture to post-silicon bring-up of the OFDM time-domain processing chain.
- Developed **HW accelerators** for sampling rate convertors, filters, mixers and interfacing logic to an **AXI4** system bus and **JESD204C** RFIC interface bus.
- Co-designed **SW interfaces** to the DFE and RFIC control plane following ORAN P19 specification, running on **RISCV** processors.
- Conceived and developed the **Virtual Platform** for a multi-ISA (ARM, RISCV) gNodeB VP to enable early SW development.
- Led the emulation team and brought up the gNodeB SoC on industry standard emulation platforms.

2013-2019

Senior ASIC Engineer in NVIDIA Graphics:

- Led the architecture and development of **PCIe 5.0 endpoint** and integration into the GPU memory sub-system, including support for **CXL**.
- Responsible for architecture and development of **virtualization**[1] features of GPU using **SR-IOV**. Defined and implemented SW driver interface to implement various sub-features of SR-IOV.
- Performed analysis of bandwidth and latency requirements for GPU DMA engines to meet **Gen4 performance**, across HPC, cloud and workstation products.
- Designed the **VirtualLink**[2] connection to VR headsets over PCIe in GPU, providing latency guarantees to isochronous USB traffic concurrent with GPU traffic.
- Designed new low-power feature called **RTD3** for notebook GPUs. Coordinated across multiple ASIC and SW teams for the implementation of the feature.

[1] https://www.nvidia.com/en-in/technologies/multi-instance-gpu/
[2] https://en.wikipedia.org/wiki/VirtualLink

- Developed verification methodology and test-bench implementation for validating **Unified Memory**[3] in the Pascal architecture, at the GPU memory sub-system level.

2005-2012

Senior Staff Engineer in (Beceem) Broadcom Communications:

- Led the design, implementation and verification of a **programmable framer, demodulator, decoder engine** with HARQ features for an **LTE Rel9** modem sub-system.
- Developed micro-architecture and implemented RTL for **synchronization, hand-off and link-adaption HW accelerators** which were part of a WiMax SoC.
- Designed and developed the verification stimulus generator and interface BFMs for a WiMax SoC.

Patents

#11,558,070

Fast AGC convergence using high-speed interface between baseband and RFIC

Skill set

HDLs:

Verilog, Bluespec

EDA tools:

Standard toolchains from Cadence and Synopsys, SpyGlass Lint/CDC, PowerArtist

Hardware interface protocols:

PCIe 3.0/4.0/5.0, AMBA AXI4, APB, JESD204C

Wireless standards:

5G NR, LTE, WLAN, WiMax

Programming languages:

C, C++

Scripting languages:

Python, Perl, Shell, Lua, TCL

OS platforms:

Expert in Unix/Linux environment

Education

2001-2005

Completed B.E, Telecommunications engineering in APS College of Engineering, Bangalore.

2000-2001

Completed pre-university in JSS PU college, Bangalore.

Educational project work

2005

High bit-rate telemetry system - **carried out at ISRO, Bangalore**:
Implemented an onboard telemetry system for satellites operating at higher bit-rates than existing systems.

[3] https://devblogs.nvidia.com/parallelforall/unified-memory-in-cuda-6/

Hobby projects

I am interested in writing software, especially for the web and Android. I have released an Android utility[4] for external storage usage tracking, which has more than a 1000 downloads online. Also contributed to other open-source projects like Home Assistant[5] and Owntracks[6]. More details on my site!

Personal details

Date of birth:
17 October 1983

Marital status:
Married

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MSR City, JP Nagar 8th Phase,
Bangalore - 560076.

Languages:
Kannada, English

Links:
narenma.net, www.linkedin.com/in/narendrama

[4] https://f-droid.org/repository/browse/?fdid=com.nma.util.sdcardtrac
[5] https://home-assistant.io
[6] http://owntracks.org