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Narendra M Acharya

- **Hardware architect and designer** with 18+ years of experience in architecture, micro-architecture, design development, performance analysis, synthesis, timing closure and post-silicon bring-up.
- **Deep understanding of HW/SW co-design,** worked on end-to-end systems.
- **Managed design teams** delivering IP and sub-systems designed from scratch into multiple successful tape-outs.

Work Experience

2020-Current

Senior Principal Engineer in EdgeQ:

- Currently leading the architecture and development of the **5G NR** gNodeB **Digital Front End** module (DFE) and RFIC interfaces.
  End-to-end ownership of a sub-system built from scratch, ranging from initial architecture to post-silicon bring-up of the OFDM time-domain processing chain.
- Developed **HW accelerators** for sampling rate convertors, filters, mixers and interfacing logic to an **AXI4** system bus and **JESD204C** RFIC interface bus.
- Co-designed **SW interfaces** to the DFE and RFIC control plane following ORAN P19 specification, running on **RISCV** processors.
- Conceived and developed the **Virtual Platform** for a multi-ISA (ARM, RISCV) gNodeB VP to enable early SW development.
- Led the emulation team and brought up the gNodeB SoC on Synopsys Zebu and Cadence Protium. Assisted SW bring-up and optimization.

2013-2019

Senior ASIC Engineer in NVIDIA Graphics:

- Architecture lead for **Hopper PCIe 5.0**[1], a from-scratch design which integrated into the GPU memory sub-system and supported **CXL**. Hopper's GH100 is widely deployed in data centers.
- Led the architecture and development of **GPU virtualization**[2] using **SR-IOV**. Defined and implemented SW driver interface to implement various features of SR-IOV.
- Performed analysis of bandwidth and latency requirements for **PCIe 4.0** in **Ampere** GPU, across HPC, cloud and workstation products.
- Designed the **VirtualLink**[3] connection to VR headsets over PCIe in GPU, providing latency guarantees to isochronous USB traffic concurrent with GPU traffic.
- Designed low-power feature called **RTD3** for notebook GPUs. Coordinated across multiple ASIC and SW teams for the implementation of the feature.

[1] https://developer.nvidia.com/blog/nvidia-hopper-architecture-in-depth/
[2] https://www.nvidia.com/en-in/technologies/multi-instance-gpu/
[3] https://en.wikipedia.org/wiki/VirtualLink

- Developed verification methodology and test-bench implementation for validating **Unified Memory**[4] in **Pascal** GPU.

2005-2012
SENIOR STAFF ENGINEER IN (BECEEM) BROADCOM COMMUNICATIONS:

- Led the design, implementation and verification of a **programmable framer, demodulator, decoder engine** with HARQ features for an **LTE Rel9** modem sub-system.
- Developed micro-architecture and implemented RTL for **synchronization, hand-off and link-adaption HW accelerators** which were part of a WiMax SoC.
- Designed and developed the verification stimulus generator and interface BFMs for a WiMax SoC.

Patents

#11,558,070
Fast AGC convergence using high-speed interface between baseband and RFIC

Education

2001-2005
Completed B.E, Telecommunications engineering in APS College of Engineering, Bangalore.

Links:

- narenma.net
- www.linkedin.com/in/narendrama

[4] https://devblogs.nvidia.com/parallelforall/unified-memory-in-cuda-6/