PX14400 Fixed Logic Kit (FLK)
User's Guide

Revision 1.0

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Table of Contents

1 PX14400 Fixed Logic Kit (FLK) Overview

The PX14400 FLK is provided for all 'SP' or FPGA 'signal processing' enabled PX14400 boards. Included within the FLK are capabilities for digital down conversion (DDC), FIR filtering, data decimation filters (in steps of x2), real or I&Q output selection and data averaging. A block diagram below shows how these processing resources are connected within the greater PX14400 system.

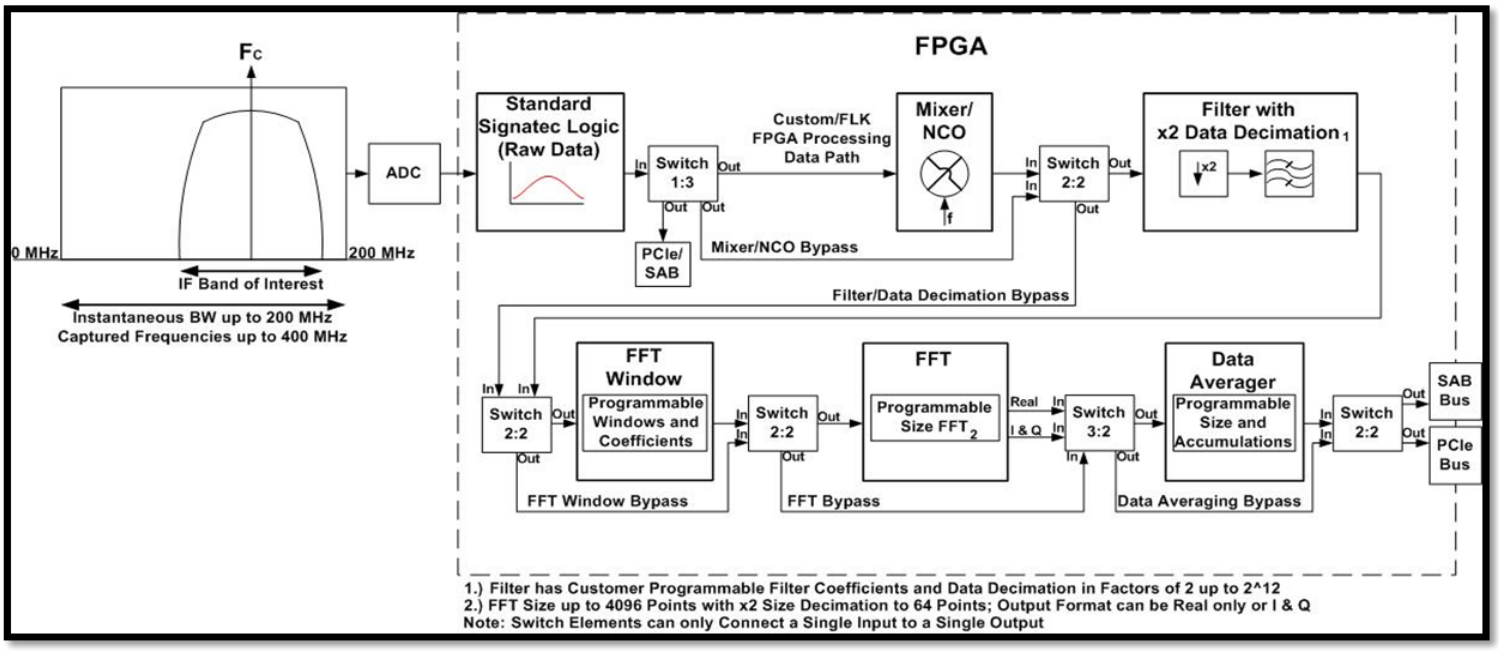


Diagram 1: FLK Processing Elements and Data Flow

The left side of the block diagram is a representative example of a possible spectrum capture scenario. In this example, the PX14400 is digitizing at 400 MHz for a total capture band from near DC to 200 MHz. Inside this greater 200 MHz bandwidth is an intermediate and smaller band of interest positioned at the center frequency 'Fc'. The input signal is digitized by the ADC and passed to the 'Standard Signatec Logic' (SSL) module, which contains all general purpose PX14400 services that are included in the 'DR' version board. Essentially, the SSL is self contained entirely in the first PX14400 FPGA connected directly to the ADCs and PCIe host bus. The remaining elements in the diagram (except the PCIe bus) are contained in the 2nd PX14400 FPGA, which is dedicated to the SAB bus and real-time data processing.

When real-time processing is enabled, the data from the SSL will be transferred to the 2nd FPGA for real-time processing whenever an output data transfer has been initiated. In other words, data does not get routed to the processing logic when the PX14400 is in the 'Ram Acquisition' mode. A transfer to some other external resource (such as PCIe or SAB) must be initiated before data is transferred to the processing FPGA.

When real-time processing is enabled using the FLK, the first element in the processing chain is the digital NCO, which allows for mixing the signal band of interest to some other center frequency (typically baseband). Following the NCO are FIR filter stages that allow for decimating data in steps of x2 from 2^3 up to 2^12.

Though not shown, the output of the filters can be either real or I&Q format. For information on the decimation filter characteristics, refer to the section titled 'Decimation Filter Characteristics'.

Following the filters are the FFT Window and FFT processing stages. The current default FFT window used is a Blackman-Harris of size 1024 elements with FFT sizes of 64 to 4096 points supported. Data from the FFT can be output as either magnitude square or I&Q format. The last processing element is a programmable data averager with up to 2^16 accumulations possible.

Each processing element in the FLK can be either utilized or bypassed, which means data can be processed in-line as shown in the FLK diagram by any number of the processing elements from '0' to all. However, the order in which the data is processed is not programmable and must follow the data processing path.

The FLK and its possible options will likely expand over the product's life-cycle. Attention will be made to not break pre-existing FLK designs and as (and when) needed this FLK User's Guide will be updated to account for these updates.

Customers that purchase the PX14400 'SP' version products will receive their PX14400 with the FLK logic pre-installed. Some customers will also opt to purchase custom programmable logic development kits (LDK), which involves reprogramming the FPGA processing logic (versus the FLK, which only makes changes via programmable register writes). The FLK programmable logic file is provided with the PX14400 product software along with provisions for re-flashing the firmware for instances where users wish to revert back to the provided FLK logic.

2 PX14400 Custom Logic Development Kit (LDK)

In addition to the pre-programmed FLK processing solution that comes standard with all 'SP' version PX14400 boards, Signatec also offers as a separate purchasable option a custom logic development kit (LDK) that allows for customer to create their own FPGA based processing applications embedded onto the PX14400. The same methods used in the Signatec provided PC software for writing to the real-time processing registers in the FLK logic can also be used by LDK users. Additional details concerning the use of the LDK can be found inside the PX14400 LDK Programmer's Manual.

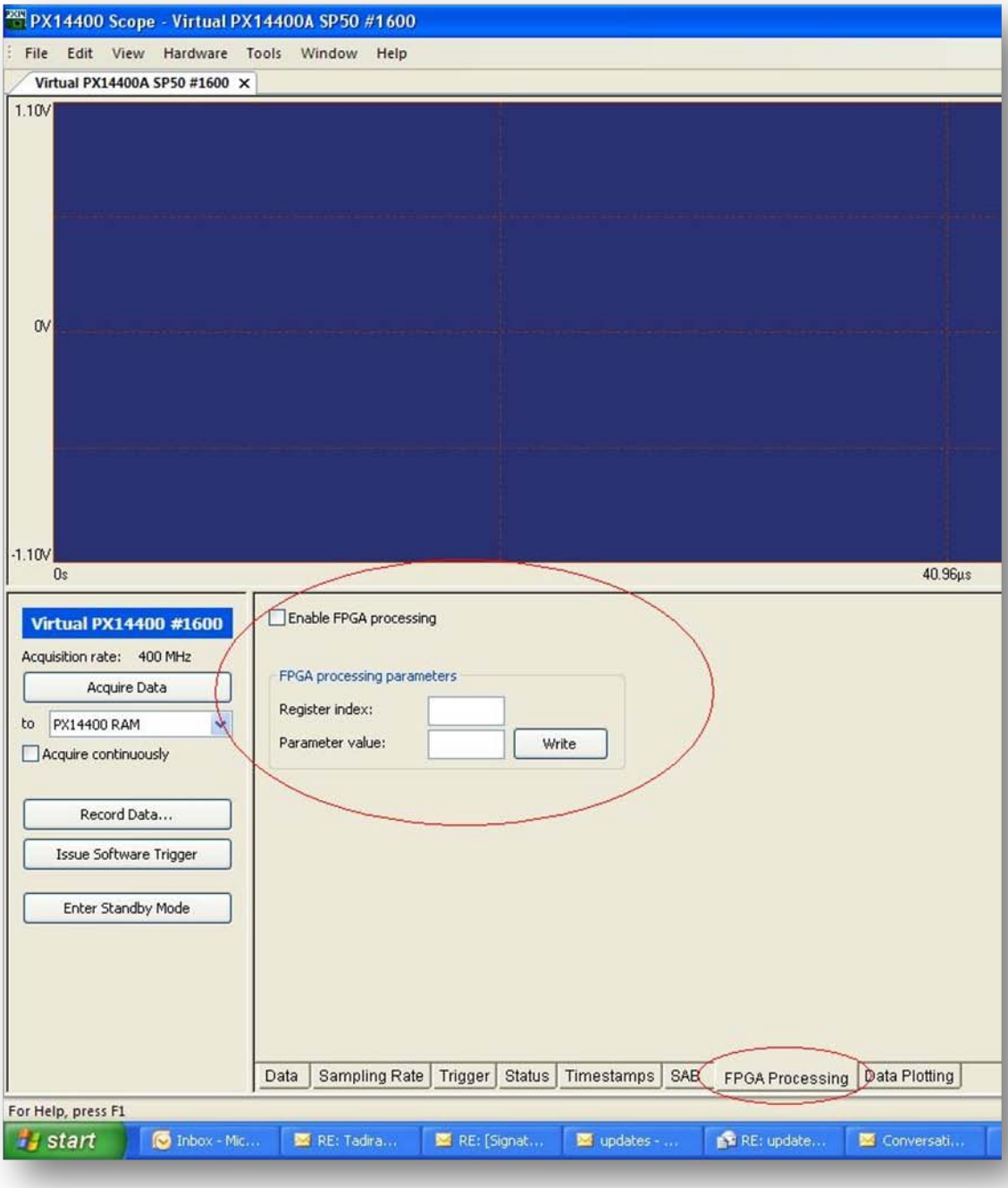
3 FLK use with PX14400 Scope Application

The PX14400 Scope Application ('Scope App') is an application that is installed as part of the freely provided standard PX14400 software installation on Microsoft Windows platforms. This application is used to control one or more Signatec PX14400 data acquisition PCI Express (PCIe) boards.

The PX14400 Scope Application is a virtual oscilloscope application that allows the operator to view or edit all PX14400 hardware settings as well as record and display PX14400 acquisition data. For many users, the Scope App is the primary software tool used to record PX14400 acquisition data.

The PX14400 Scope App has provisions that allow for writing values direct to the FLK registers. The current implementation is a simple register target approach, where a register address and value pair must be provided. Though this is a highly flexible approach, it is quite tedious (especially when entire arrays of data need to be uploaded). The next Scope App update will provide higher level function support for simplifying user settings.

Below is a screen capture of the PX14400 Scope App with the register write interface. The picture details the current system of writing to the FLK 16-bit registers by typing into the edit box a register address and a corresponding register value.

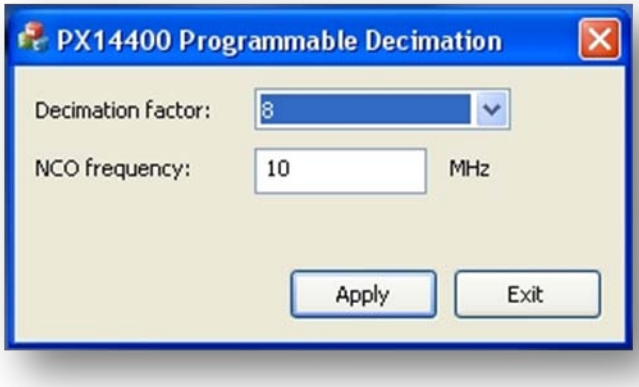


Picture 1: PX14400 Scope Application FPGA Processing Page

To use the FLK processing capabilities, simply check the 'Enable FPGA processing' checkbox and write the corresponding register values to the target register index.

The setting of the NCO frequency is a bit more complicated (see C source code based formula in next section) than the other register settings. A simple EXE (shown below) is available for making the NCO and filter

decimation settings until incorporated in the Scope App. This EXE can be run simultaneously with any other PX14400 application.



Picture 2: PX14400 Temp NCO and Filter Decimation Application

Note: the FIR filters don't flush their data taps when reset so there will be some data in the front of the data record for each new recording that should be ignored. The next logic release will address this issue.

4 FLK use in User Created PC Applications

Users can also set values to the FLK (and LDK too if provided register system is not changed) in their own custom created PC side applications by using the provided register write functions. The next release of the PX14400 windows software will change the implementation from a 'write register' based system of functions to higher level functions (such as 'SetNCOFrequency' for example) that remove the details of working on a register address based system. Until this system is implemented, the following methods can be used.

It should be noted that this temporary programming method will also continue to work in the future. However, it is possible that register addresses could change. Signatec will likely keep the register addresses constant unless a very strong argument is presented in the future for why the addresses should change.

The primary function for writing to the FLK registers is the 'SetBoardProcessingParamPX14' function, which takes a board handle, a 16-bit register address and 16-bit register value as function arguments. This function is not yet documented in the manual, but it is in the current PX14400 function library and header file. Below is the source code for enabling the FPGA processing, setting the filter decimation factors and setting NCO frequencies.

```
// Enable FPGA Processing
SetBoardProcessingEnablePX14 (hBrd, 1);

// Decimation
SetBoardProcessingParamPX14(hBrd, 0x8009, m_decimation);

// NCO frequency
static const UINT64 my_factor_f = 0x00000003FFFFFFFFULL;
GetEffectiveAcqRatePX14(hBrd, &dAcqRateMHz);
qw = static_cast<UINT64>(2.0 * (m_ncoFreqMHz / dAcqRateMHz) * my_factor_f);
SetBoardProcessingParamPX14(hBrd, 0x8001, (USHORT)qw);
```

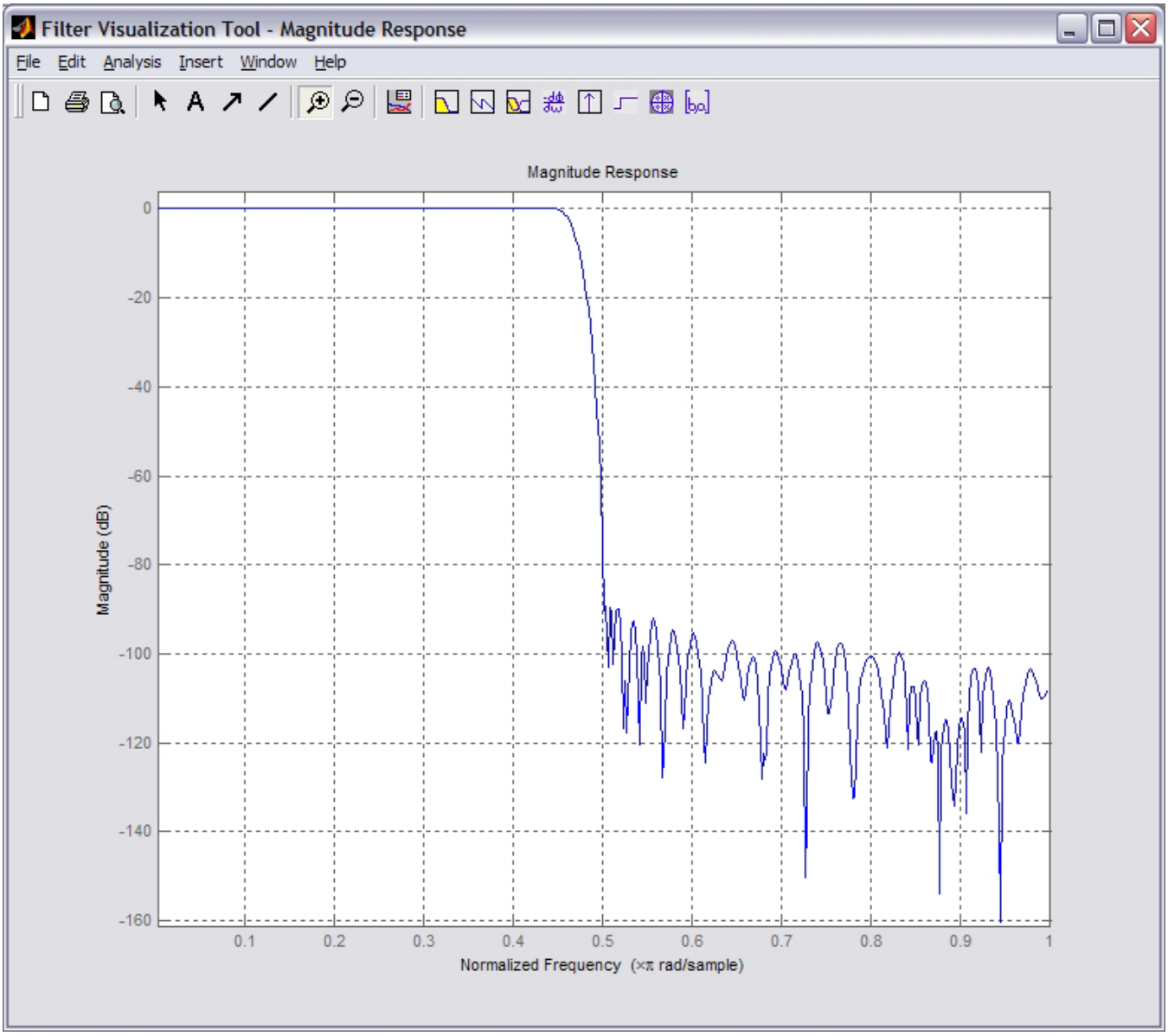
```
SetBoardProcessingParamPX14(hBrd, 0x8002, (USHORT)(qw >> 16));
SetBoardProcessingParamPX14(hBrd, 0x8003, (USHORT)(qw >> 32));
SetBoardProcessingParamPX14(hBrd, 0x8004, (USHORT)(qw >> 48));

// NCO phase
static const UINT64 my_factor_p =   0x00000003FFFFFFFFULL;
qw2 = static_cast<UINT64>(1.0 * (m_ncoFreqMHz / dAcqRateMHz) * my_factor_p);
SetBoardProcessingParamPX14(hBrd, 0x8005, (USHORT)qw2);
SetBoardProcessingParamPX14(hBrd, 0x8006, (USHORT)(qw2 >> 16));
SetBoardProcessingParamPX14(hBrd, 0x8007, (USHORT)(qw2 >> 32));
SetBoardProcessingParamPX14(hBrd, 0x8008, (USHORT)(qw2 >> 48));
```

Function definitions from the PX14.h file:

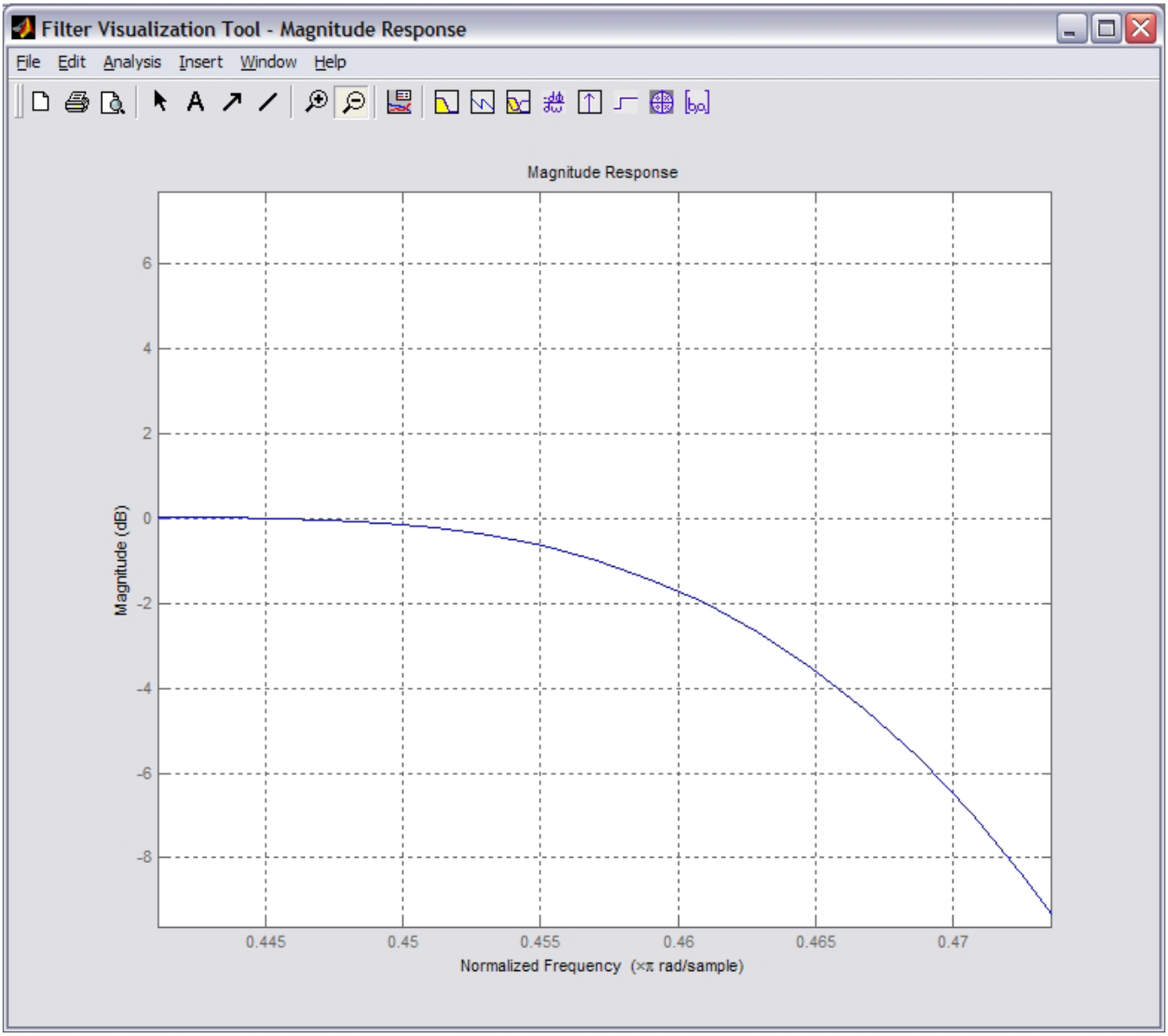
```
// Set FPGA processing enable
PX14API SetBoardProcessingEnablePX14 (HPX14 hBrd, unsigned int bEnable);
// Set a FPGA processing parameter value
PX14API SetBoardProcessingParamPX14 (HPX14 hBrd, unsigned short idx,
                                     unsigned short value);
```

5 Decimation Filter Characteristics

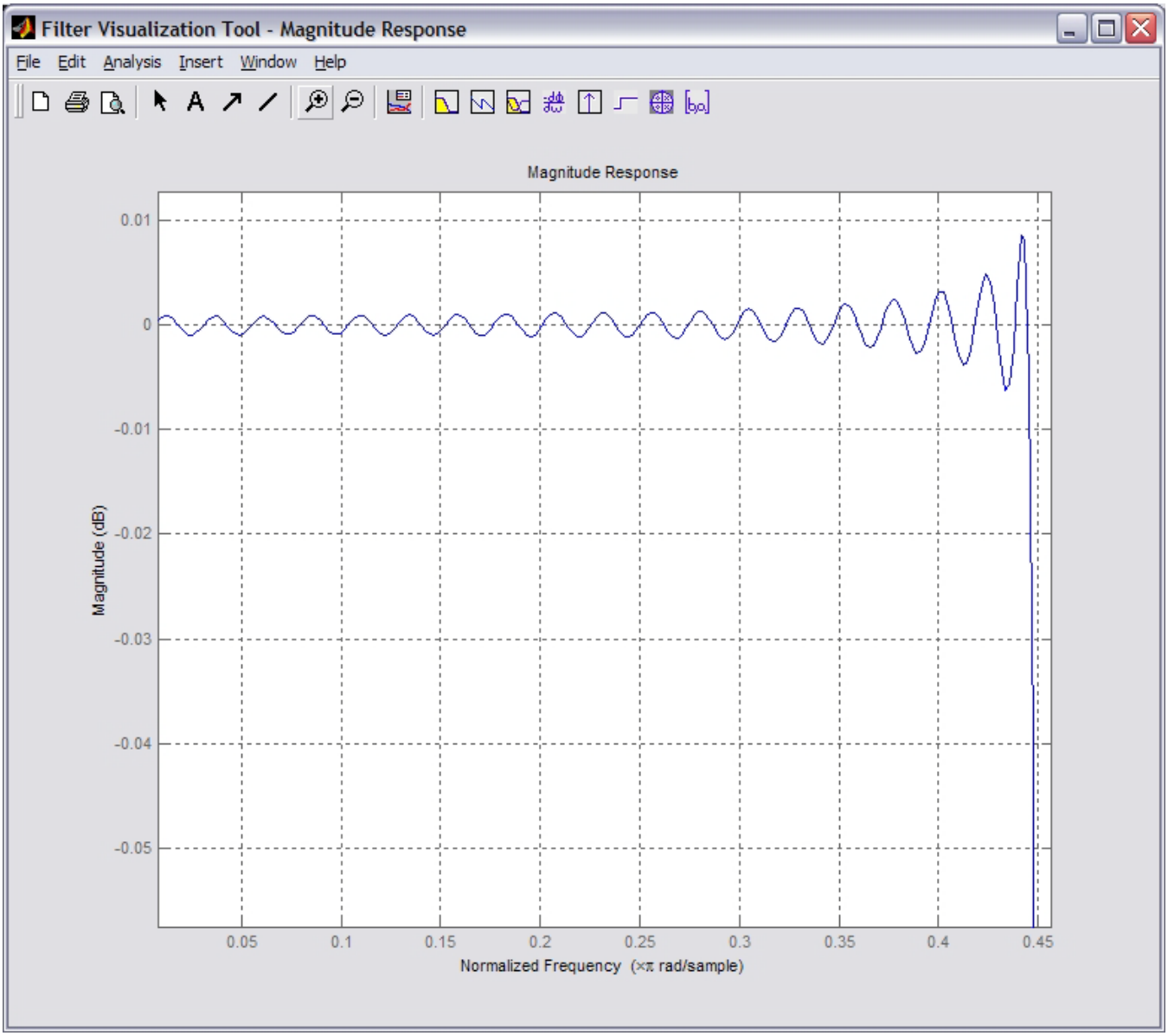
The PX14400 FLK decimation filters use the same filter for all decimation stages with the exception of the final stage. The picture files below (6 total) detail the characteristics of the filters used. The first 3 pictures detail the filter used for all stages except for the last stage and the final 3 pictures detail the filter used for the last filter stage to eliminate aliasing effects.



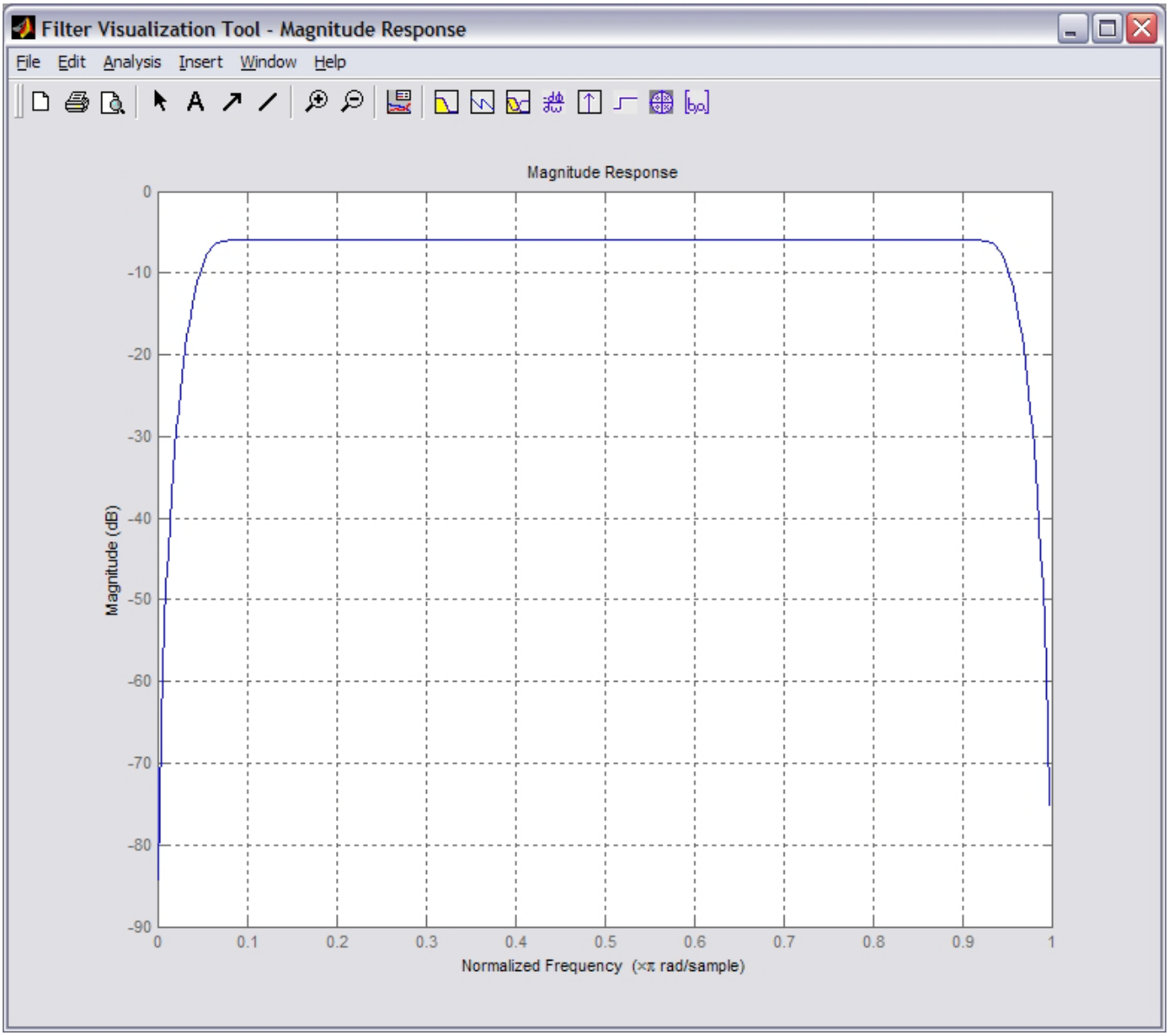
Picture 3: Decimation Filter Characteristics



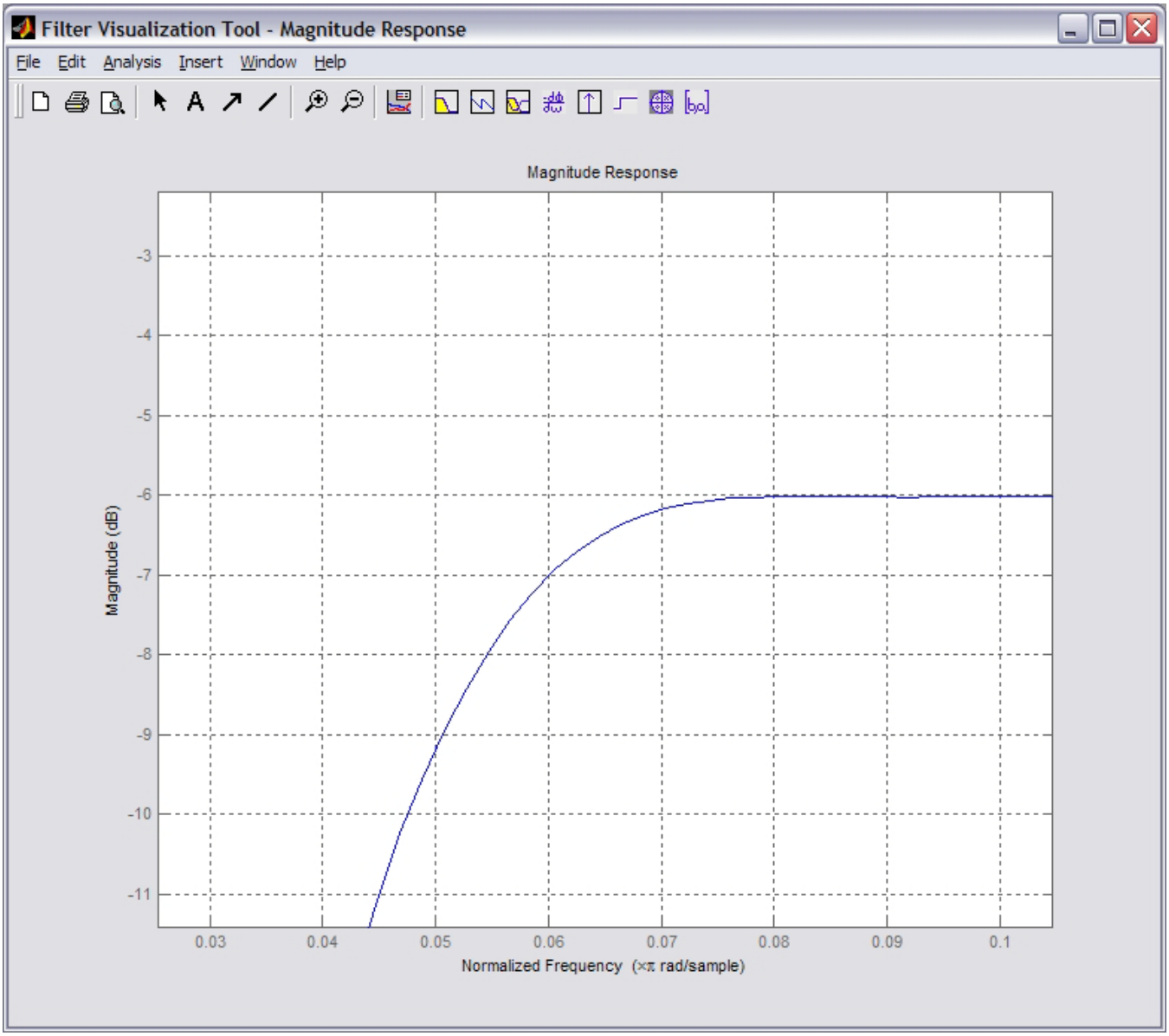
Picture 4: Decimation Filter Transition Band Zoom-In



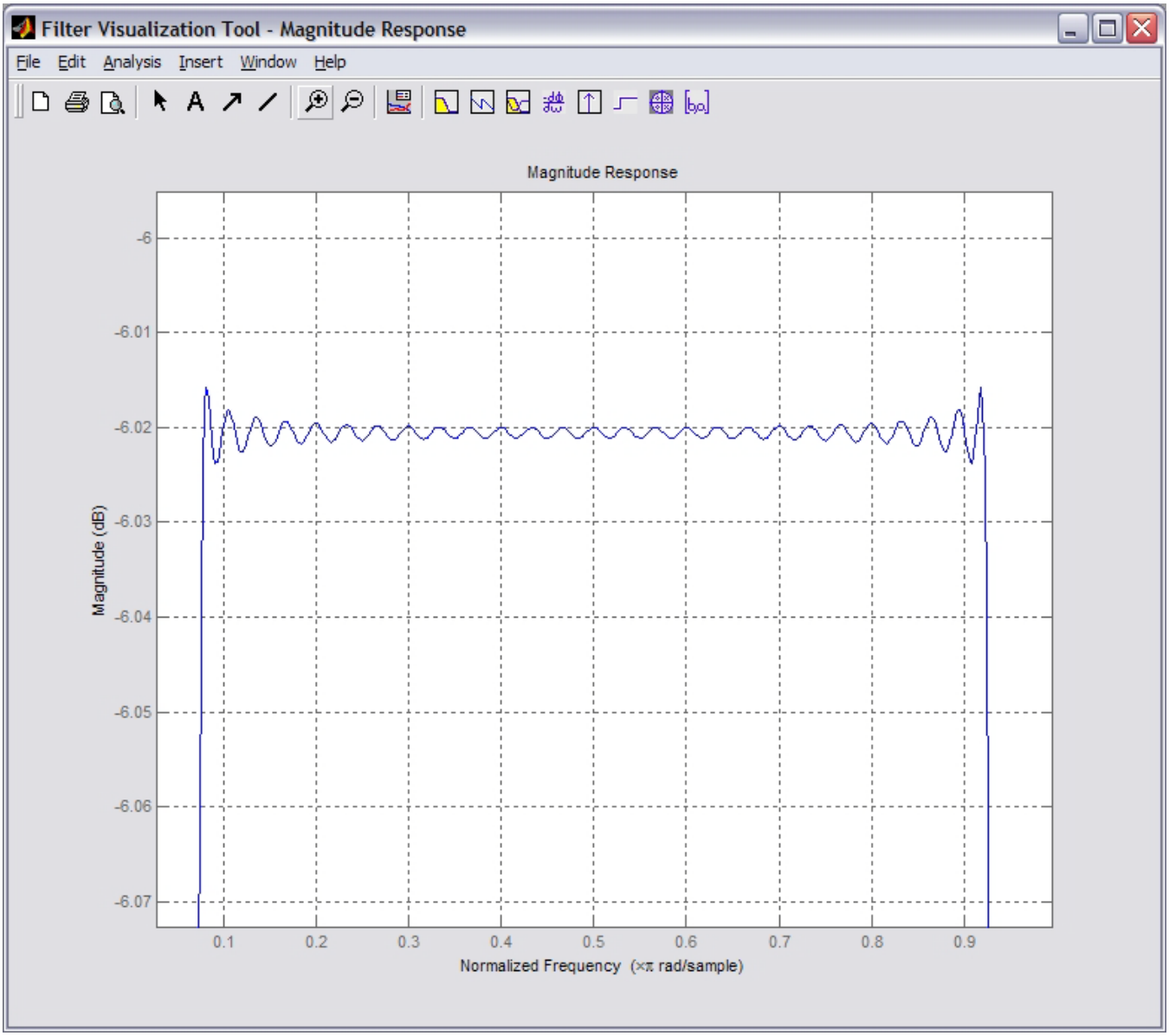
Picture 5: Decimation Filter Pass-Band Ripple



Picture 6: Final Decimation I & Q Filter Characteristics



Picture 7: Final Decimation I & Q Filter Transition Characteristics



Picture 8: Final Decimation I & Q Filter Pass-Band Ripple

6 FLK Registers

NCO Settings:	0x8001 to 0x8008
Decimation:	0x8009, where the value is the base 2 exponent of the desired decimation factor
Filter Coefficients:	Forthcoming
FFT Size:	Forthcoming
FFT Window Coefficients:	Forthcoming
Data Averager Count:	Forthcoming
Data Averager Size:	Forthcoming
FFT Data Format:	Forthcoming
Filter Data Format:	Forthcoming
Bypass Scheme:	Forthcoming