Design of Oversampled ADC Integrators

EE240B Project Report

Emily Naviasky
Department of EECS, UC Berkeley
enaviasky@berkeley.edu

Nathaniel Mailoa
Department of EECS, UC Berkeley
nmailoa@eecs.berkeley.edu

I. Introduction

We will propose a design for the integrator stages of an oversampled ADC. The design is driven by specifications that include input-referred electronic noise, settling time as well as settling accuracy. We have chosen to use the same integrator architecture for both stages but tune the component values for each stage.

II. System-level Considerations

We started the design by modeling the ADC as transfer functions. We noticed that since the circuit implements an integration, the first stage should be a lot more carefully designed than the second stage. The input-referred noise transfer function from the output of the first stage is $N_1 = 2(z-1)$ while the second stage has a contribution that is affected by $N_2 = 0.25(z-1)^2$, assuming a second stage gain of 0.5. These transfer functions are also used later to verify the input-referred electronic noise of the circuit.

We estimated that the noise power contribution of the second stage is approximately 1000 times smaller than the first stage. We also noted that if we split the noise of a stage to each phases' noises (Φ_1 and Φ_2), the noise from Φ_1 is integrated along with the signal and is more important than the Φ_2 noise. We use this analysis to size the sampling and feedback capacitors of both integrator stages separately.

III. Integrator Implementation

Each integrator stage of the oversampled ADC has a gain of 0.5 and has to settle within 0.1% in 1.8ns wih a +/- 1V differential input. Fig. 1 shows the implementation of the integrator stages.

During Φ_1, C_S samples the input and during Φ_2 the input is amplified through charge transfer between C_S and C_F. The Φ_2 switch connecting the two sampling capacitors is a common mode rejection mechanism, transferring only the differential charge to C_F. C_F is connected in the feedback only during the amplification phase Φ_2 and is never reset, thus it integrates the input over time. C_L is the load capacitance; for the first stage this is the the sampling capacitor of the second stage, and for the second stage this is the input capacitance of the comparator.

Since the amplifiers form a second-order integrator, the first amplifier noise dominates the total noise. We begin by

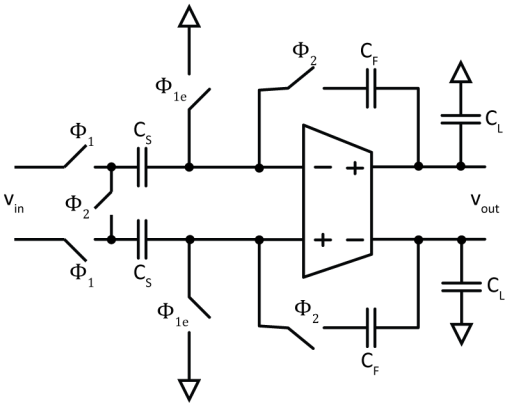

Fig. 1. Switched capacitor integrator

choosing C_S from the noise specification and the equation for noise at Φ_1.

$$N_{\Phi 1} = \frac{kT}{C_S + C_L}$$

$$N_{\Phi 2} = \frac{\alpha}{\beta}\frac{kT}{C_{L,tot}}$$

The value of C_F is easily obtained from the required gain since the gain of the integrator is C_F/C_S. We want to budget $3.5\mu\ V_{RMS}$ to the noise at Φ_1 per differential input, but the signal bandwidth that we care about is only 100-500kHz and our equation for $N_{\phi 1}$ is over the entire spectrum. Therefore, we need to multiply the noise specification by the Oversampling Ratio, which is $\frac{f_S}{2BW}$. The input referred noise that we want therefore is $N_{\Phi 1} = 250 \cdot (3.5)^2 \cdot 10^{-12} V/\sqrt{Hz}$. We rounded the capacitor values up to get some headroom for error.

$$C_S = 1.5pF$$

$$C_F = 3pF$$

Our load capacitor is the sampling capacitor of stage 2. We first started at 100fF and iteratively lumped in parasitic capacitances from the OTA with the load capacitor.

We next calculate the G_m of the OTA which is dictated by the unity gain bandwidth necessary to meet the settling time with those capacitors from the settling time requirement since $\omega_u = \frac{G_m}{C_{L,tot}}$. The equation below expresses the dynamic

settling error specification assuming a zero, where τ is the unity gain bandwidth and $\beta = .67$.

$$t_s = -\tau ln\left(\epsilon_d\left(1 - \beta\frac{C_F}{C_F - C_L}\right)\right)$$

We budget half of the error to static error and half to dynamic, so $\epsilon_d = 0.0005$. In addition, we budgeted .8ns of the settling time to slewing and devices in the second branch being pushed out of saturation so the $t_s = 1ns$. This results in a unity gain bandwidth of 1.4G and a required transconductance of $G_m = 10mS$.

Next we calculated the required open loop gain of the amplifier. Since we are budgeting half of the settling error to static error, we require that

$$\frac{1}{T} = \frac{1}{\beta A} = \epsilon_s = 0.0005$$

With a β of 0.67, the required open loop gain is 3000, or 70 dB. As a quick check, this results in a required output resistance of $300k\Omega$. Which is a bit high and requires at least cascoding.

With the design parameters, we started by building an ideal OTA using a VCCS. We created a testbench for AC, noise, and transient analysis and ran simulations to make sure the settling time, and noise requirements are met. The noise simulation was a performed with a noise current source from a resistor of value $\frac{\alpha}{G_m}$ inside of the OTA and 10Ω ON resistances in series with all of the switches. However, PSS and PNOISE are not really meant for integrators so we exported the noise density at the output of the integrator to Matlab, then multiplied by the input-refered transfer function from the noise source and then integrated over the signal bandwidth.

With a one stage OTA, the transconductance is limited by the g_m of the input device and we already determined that we need $g_m = 10mS$. Assuming a $V* = .2$, the current required is 1mA. We check that the current is close to that required for the slewing. To avoid slewing for extended periods of time, the current in the input device has to be large enough to charge the load capacitance. Since when the closed loop amplifier is subjected to a step input there is a capacitive divider effect from the input to the output node, the output has to slew more than the maximum single-ended output swing of $0.25V$. Designing for a $1V$ slew in $0.8ns$, with a total load capacitance of $C_{Ltot} = C_L + (1 - \beta)C_F = 1.1pF$, the current needed in the input devices is $1.3mA$. Since the required g_m is lower than that, we err on the side of more and use $1.3mA$. Once it was implemented, we found that the slewing was not as bad as we had feared, and we backed off the current to $1.2mA$. This still gives us a higher unity gain BW than required, which means that we need to be sensitive of our phase margin, but the overestimation is not terrible since the unity gain BW is underestimated by assuming only a single pole system. Finally, in order to settle to .1% we needed a phase margin of at least 70 degrees. With these design specifications in mind, we began designing our circuit.

IV. Design Alternatives

We started with a telescopic OTA with an NMOS input but quickly realized that there was not enough head room to maintain a common mode output voltage at 0.6V. We moved on to a folded cascode OTA architecture to obtain the necessary headroom.

The current of the cascode branch is typically about 1.5 time greater than the current flowing through the input devices so the cascode devices stay biased properly, otherwise they could contribute to lower gain for longer while the capacitor is charging. Thus the current through the

After attempting to build the OTA, we found that cascoding was not enough to obtain the $300K\Omega$ necessary. With the bias currents in the design, this output resistance was unachievable. To realize the high output resistances, we added gain boosters to the folded cascode OTA. Fig. 2 shows the gain-boosted folded cascode OTA circuit. The gain booster specs are derived from the un-boosted output resistance and the bandwidth of the OTA. Based on the output resistance looking up from the output node $R_{out,up} = g_{m7}r_{o7}(r_{o5}||r_{o3}||r_{o1})$ which we estimated to be a bit less than $10k\Omega$ so the PMOS gain booster require an open loop gain of $36dB$. The output resistance looking down from the output node is $R_{out,down} = g_{m9}r_{o9}r_{o11}$ which we estimated around $50k\Omega$. This is relatively high compared to $R_{out,up}$, but is still not high enough to meet the total output resistance of $300k\Omega$. We set the same specs for the nmos gain booster since then the top resistance would dominate and the output resistance would be met.

There are several bandwidth requirements for the gainboosters in order to ensure stability. First, the unity gain bandwidth of the gain booster has to be larger than the 3dB point of the closed loop OTA. Second, the gainbooster must have at least 45 degrees of phase margin. This meant that our gain boosted bandwidth needed to be larger than 3GHz.

To build these gain boosters, we attempted to use a simple differential pair, but the input voltage bias and the output voltage bias are not ideal for such an architecture. For example, the PMOS gain boosters have an input voltage of $1V$ and an output voltage of $0.4V$. Using an NMOS input device would result in too much V_{GS}, hence too high $V*$ and it would be power expensive to get the necessary gm. Just like the main OTA, we solved this problem by implementing a folded cascode. We obtained the gate capacitance from the dc simulation to estimate the gain booster load. Thus we used the same design process as above to choose g_m and current for the gain boosters. We were also particularly careful to keep the PMOS gain booster input devices small since they contributed parasitic capacitance to the node of the second pole and worsened the phase margin.

Once the gain boosters were designed, implemented, and verified in dc sim and in stability analysis, we were able to check the OTA again. The OTA needed only a bit of tweaking of biasing tweaking, so that the input to the OTA was now .65V instead of .6V in order to trade a little extra bandwidth for the gain we needed. For the second stage, this tweaking

was done by adjusting the current a bit through the diff pair in order to decrease the much larger unity gain bandwidth and improve the phase margin. The differential phase margin of both OTAs ended up being around 80 degrees for both stages, which is necessary for a small percent error.

Finally, we implemented the common mode feedback. We first tried a differential common mode feedback circuit to compare the output against a constant .6V and control the current of the top two PMOS of the folded cascode. However, when we measured the common mode feedback loop, we found that it was unstable. The common mode feedback needs at least 45 degrees of phase margin, and we calculated that we would need to build a diff pair for the common mode feedback with a gain of .5. Rather than trying to build that, we switched to a triode common mode feedback in the tail of the diff pair as is shown in Figure 2. This had a phase margin of more than 100 degrees and worked immediately.

The entire design was verified successfully for the first stage first. The second stage was similar enough that we maintained all of the same sizing and biasing and simply decreased the current through each branch to maintain a similar unity gain bandwidth and gain. We had some trouble maintaining a 70dB gain while pushing the bandwidth lower without pushing the current of the cascode branch so far down that the biasing was no longer safe when the diff pair was unbalanced. The second stage could have been resized but we ended up running out of time and just adding 100f extra load cap in order to push the bandwidth down and get the necessary phase margin.

V. Circuit Implementation

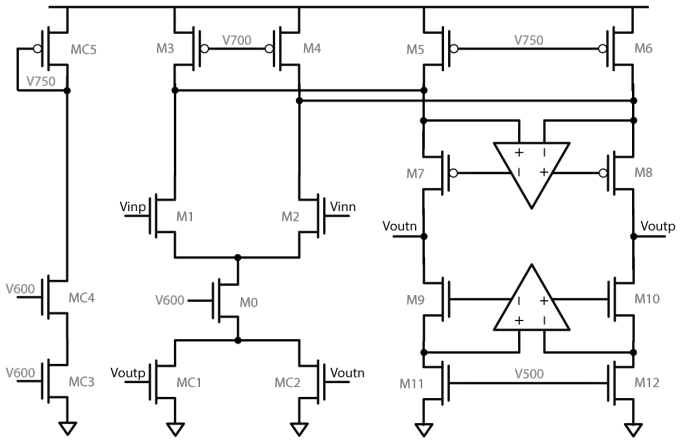

Fig. 2. Gain-boosted folded cascode OTA with CMFB

Device	W (μ)	L (n)	V*	I_D(m)	g_m(m)	f_T(G)
Differential pair						
M0	42.1	90	0.205	3.38	32.9	95.8
M1/2	15.9	60	0.19	1.69	17.8	220
M3/4	154.8	100	0.17	1.75	18.2	12.9
Output branch						
M5/6	172.98	80	0.15	1.73	22.7	19.6
M7/8	79.38	100	0.25	1.8	14.6	18.7
M9/10	71.35	300	0.19	1.8	18.8	9.6
M11/12	88.56	200	0.15	1.8	23.8	17.5
CMFB						
MC1/2	15.13	60	0.7	1.81	5.1	57.3
MC3	12.61	60	0.6	1.52	5.1	68.7
MC4	14.5	90	0.22	1.52	13.7	112
MC5	195.3	140	0.14	1.52	21.4	5.02

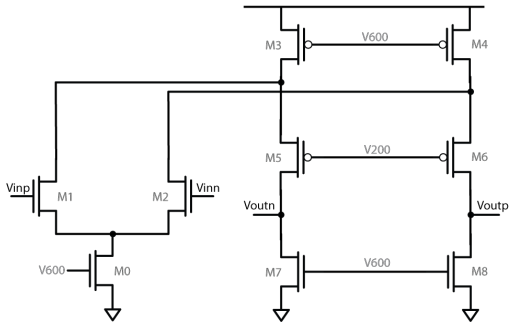

Fig. 3. PMOS Gain Booster

Device	W (μ)	L (n)	V*	I_D(m)	g_m(m)	f_T(G)
Differential pair						
M0	16.4	90	0.29	2	13.9	122.7
M1/2	14	90	0.14	1	14.2	78
Output branch						
M3/4	11.6	90	0.3	1.5	10.1	26.4
M5/6	2.6	90	0.4	0.5	2.53	108
M7/8	4	100	0.28	0.5	3.5	89

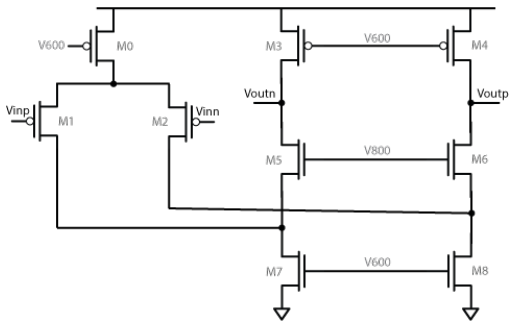

Fig. 4. NMOS Gain Booster

Device	W (μ)	L (n)	V*	I_D(m)	g_m(m)	f_T(G)
Differential pair						
M0	198.4	200	0.27	2.2	16	3.98
M1/2	77.5	60	0.13	1.1	16.3	43
Output branch						
M3/4	68.5	150	0.28	1.1	7.95	7.6
M5/6	49.7	100	0.13	1.1	17.3	58
M7/8	7.13	60	0.44	2.2	10.1	237

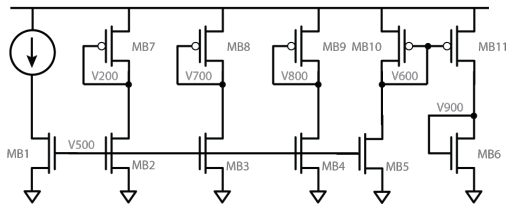

Fig. 5. Biasing Network

Device	W (μ)	L (n)	V*	I_D(m)	g_m(m)	f_T(G)
MB1	5.89	80	0.19	0.5	5.27	128
MB2	7.18	80	0.18	0.5	5.6	115
MB3	5.27	80	0.18	0.5	5.6	115
MB4	4.99	80	0.18	0.5	5.6	115
MB5	5.56	80	0.18	0.5	5.6	115
MB6	2.69	300	0.65	0.5	1.54	17.5
MB7	2.6	140	0.83	0.5	1.2	88.9
MB8	34	140	0.18	0.5	5.6	6.5
MB9	142.59	140	0.12	0.5	8.6	3.82
MB10	13.7	140	0.28	0.5	3.57	9.17
MB11	14.5	140	0.28	0.5	3.57	9.17

As mentioned before, the device sizings for the second stage is scaled by a factor. The differential input of the OTA is sized by a factor of 0.22 while the output branch of the OTA is sized by a factor of 0.3. Every other sizing is the same and the two stages share the same bias network.

VI. Design Verification

The spec specified that the OTA would be used in a delta-sigma ADC with a +/-1V differential square wave from the D/A. Therefore, we assumed that the settling time needed to be met, at worst, for a 1V differential input signal. So with a gain of .5, the output needed to settle to .5V differential in 1.8ns. This is how we determined that our settling and dynamic error met spec in fig. 12.

Running transient on a 1V step after enough time for the common mode feedback was the ultimate verification of our design, but stability analysis was the first check of our design to make sure that the transient would be stable and the settling time would meet. Stability sims were run on the gain boosters, the common mode feedback loop, and the OTA constant time integrator loop of both stages.

Stability analysis in figs. 6 and 8 shows that indeed, the unity gain bandwidth and phase margin requirements are met and surpassed for both the first and second stages. We originally had some trouble with stability from the gain boosters, and the Phase Margin report from the stability analysis was very necessary to verify before using the gain boosters in the larger circuit. The AC response of the gain boosters are shown in figs. 10 and 11. The common mode feedback loop is included in figs. 7 and 9 as well because the integrator is unstable for phase margin of less than 45 degrees, which is not reflected in the differential loop analysis.

The transient simulation was used to verify that the output settled to within 0.1 percent at 1.8ns. We plotted both the differential output and separate outputs. Settling is easily verified from the differential output in figs. 12 and 14, and common mode output is seen in figs. 13 and 15. This figure shows that there is some common mode settling that occurs immediately after switching, which is not reflected in the differential. Both stages are verified in this manner, and meet spec.

In addition, transient was used to examine the effect of slewing on the 1V step settling. As you can see in the final transient simulation in fig. 16, the highlighted line is the output current which is constant as the circuit supplies the entire 1.6mA that is can before it is no longer biased properly. The slewing occurs for the .5ns that is was allotted for settling.

Finally, to determine that the noise spec was met, we ran noise sims over 1600 sidebands and 400 harmonics. We used ideal switches instead of transistors, but used series resistors to simulate noise from switch resistance. We input referred the noise to obtain the values seen in the results.

VII. Final Specification

Gain per stage	0.5
Input Referred Noise	9.18 μ V_{RMS}
Settling	0.1% in 1.27 ns
Sampling Freq	250MHz
Total Power	40.96 mW

	Stage 1	Stage 2
C_S	1.5pF	100fF
C_F	3pF	200fF
Differential input I_D	1.69mA	0.732mA
Output branch I_D	1.8mA	0.55mA
Power consumption	22.68mW	14.68mW
Input Referred Noise	8.86 μV_{RMS}	0.3195 μV_{RMS}

VIII. Design Critique

Our integrator circuit is over designed. We settle faster than the required spec and have lower noise than required. The circuit has a large footprint and burns more power than necessary to do this. We could have traded some power to more closely meet specs, especially in the second stage, where we had to add a load cap in order to get the necessary phase margin. If power was a tight spec, then we would have done this, but considering variation across the die and across chips, we decided that it was better to overshoot and make a circuit that is more easily built and with a better yield. This is especially important for our circuit because we chose very particular widths and lengths for our mosfets, which makes

the circuit harder to actualize in silicon. Variation would have a large effect, so a little over-design is not a huge problem if the power budget can afford it. If we had more time we would have continued to tweak values and biases to see if we could obtain the same performance for lower power.

Second, our design did not take flicker noise into account. If we had, then our larger width and higher power would have been an advantage, but we assumed that since this was for an ADC application it was typical to add a chopper and then flicker would not be a concern.

Our design did not do anything to correct for offset, which might be a concern because our input devices are a bit small and thus variation would have a significant effect. However, considering that the application is an ADC this is not too concerning because the effect of OTA offset from fabrication mismatch is negligible because Delta-Sigma modulators are relatively insensitive to offset [1].

REFERENCES

[1] B. Bernhard, *The Design of Sigma-Delta Modulation Analog-to-Digita1 Converters*, IEEE Journal of Solid-State Circuits, vol.23 ,no.6, 1988.

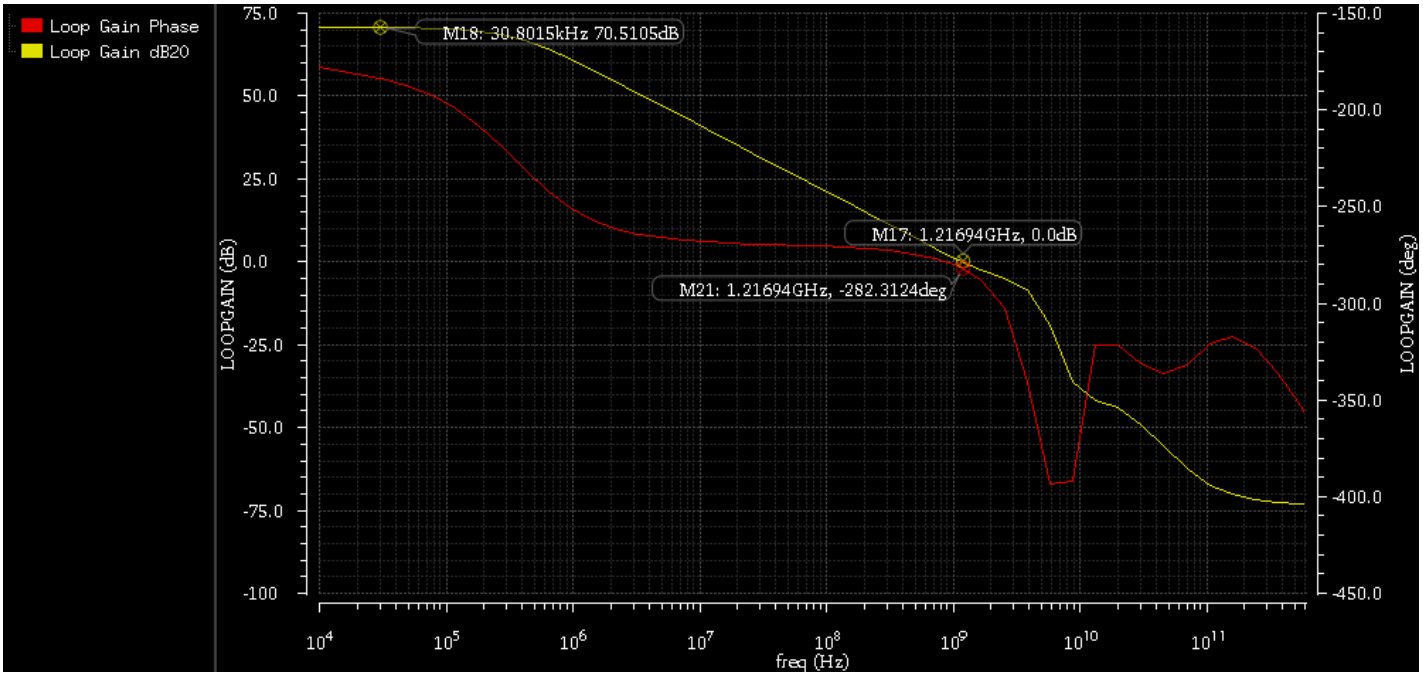

Fig. 6. Stability Analysis simulation of the differential loop for the first stage

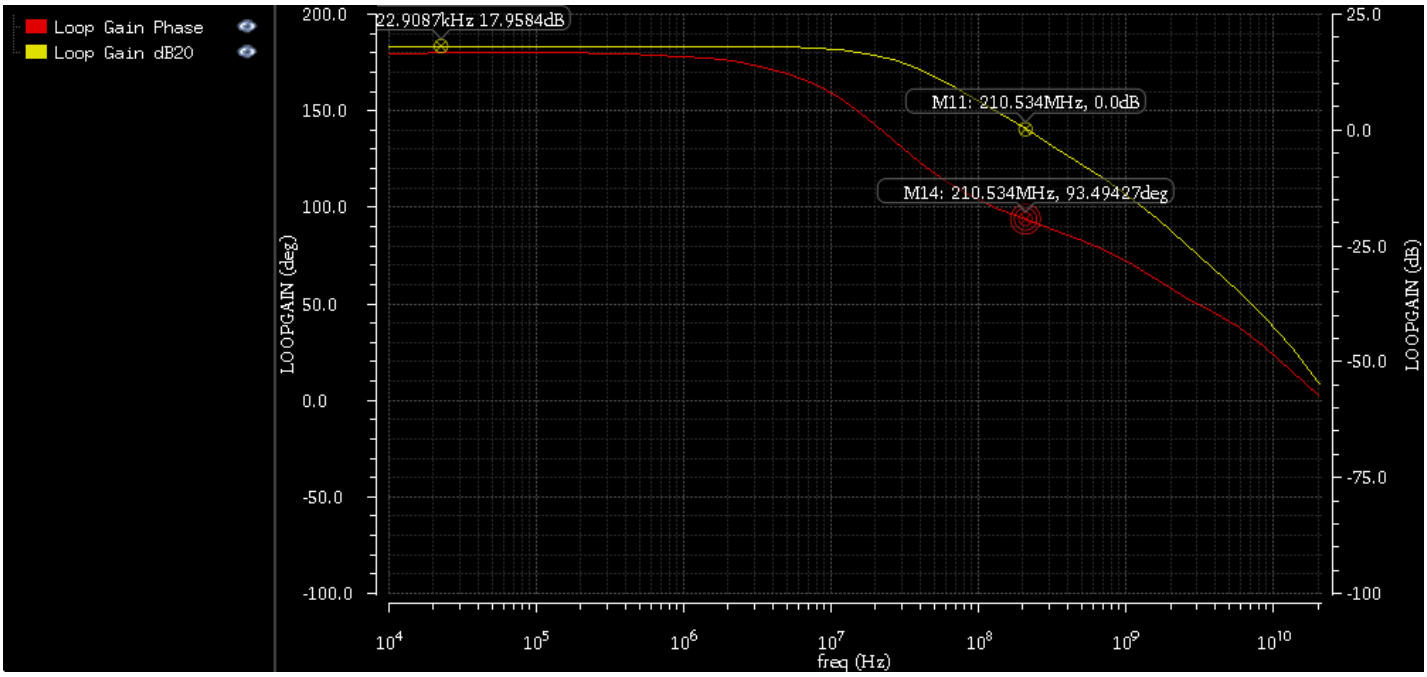

Fig. 7. Stability Analysis simulation of the common mode feedback loop for the first stage

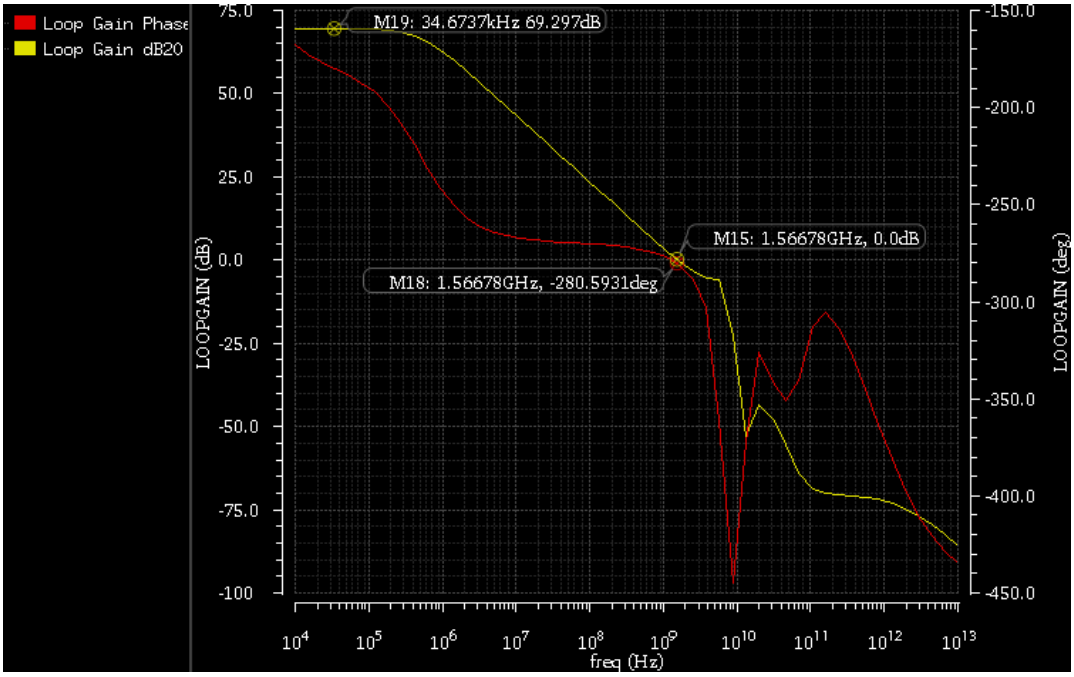

Fig. 8. Stability Analysis simulation of the differential loop for the first stage

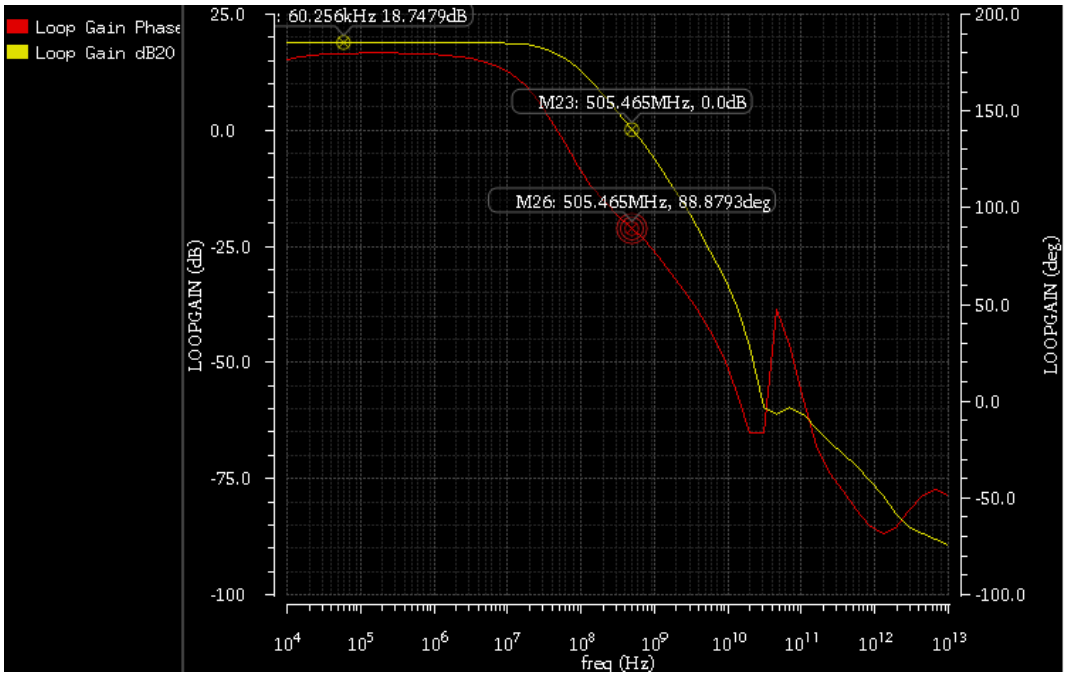

Fig. 9. Stability Analysis simulation of the common mode feedback loop for the first stage

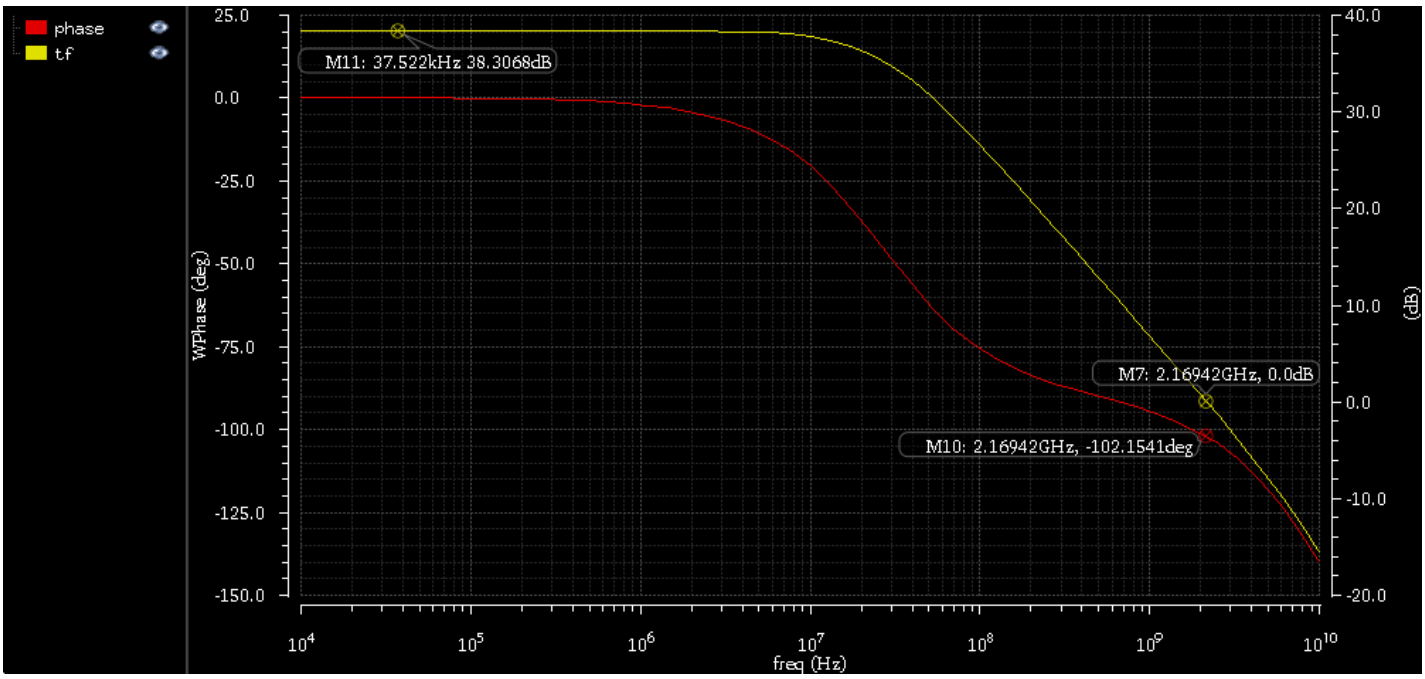

Fig. 10. AC response of PMOS gain boosters

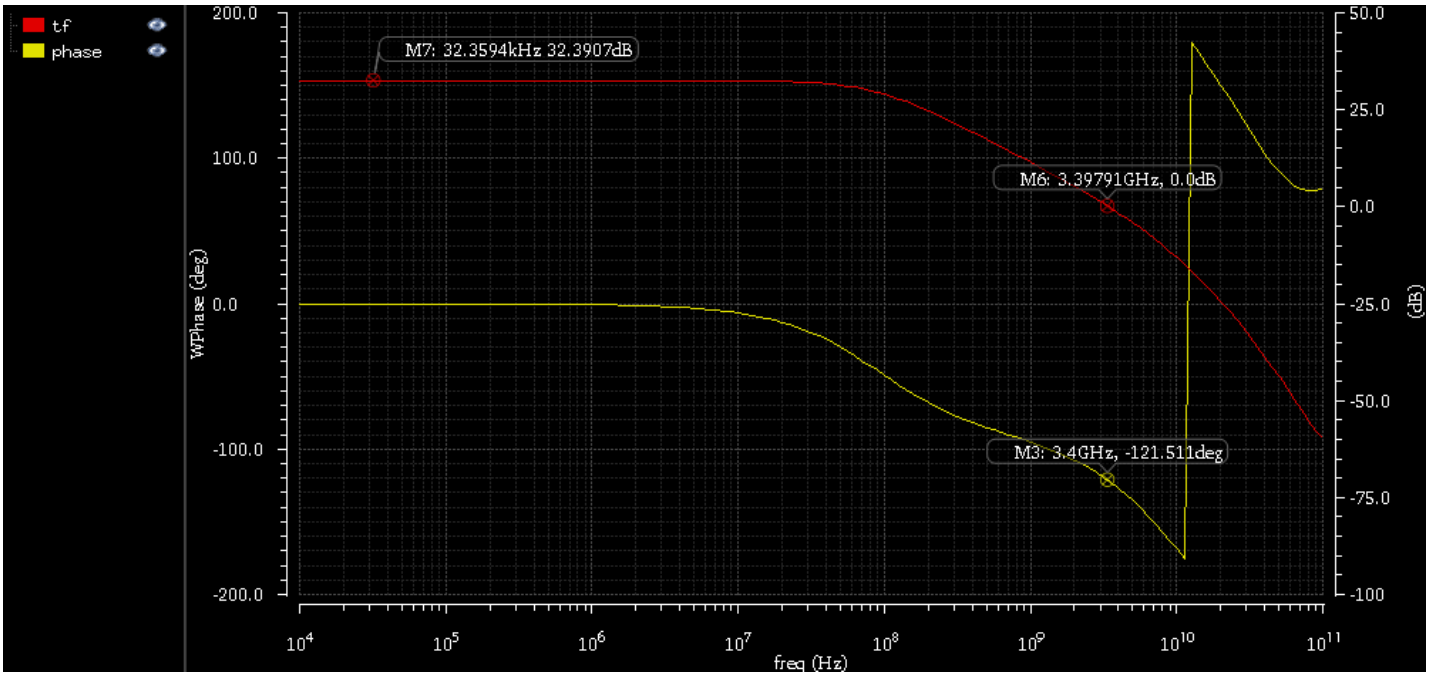

Fig. 11. AC response of PMOS gain boosters

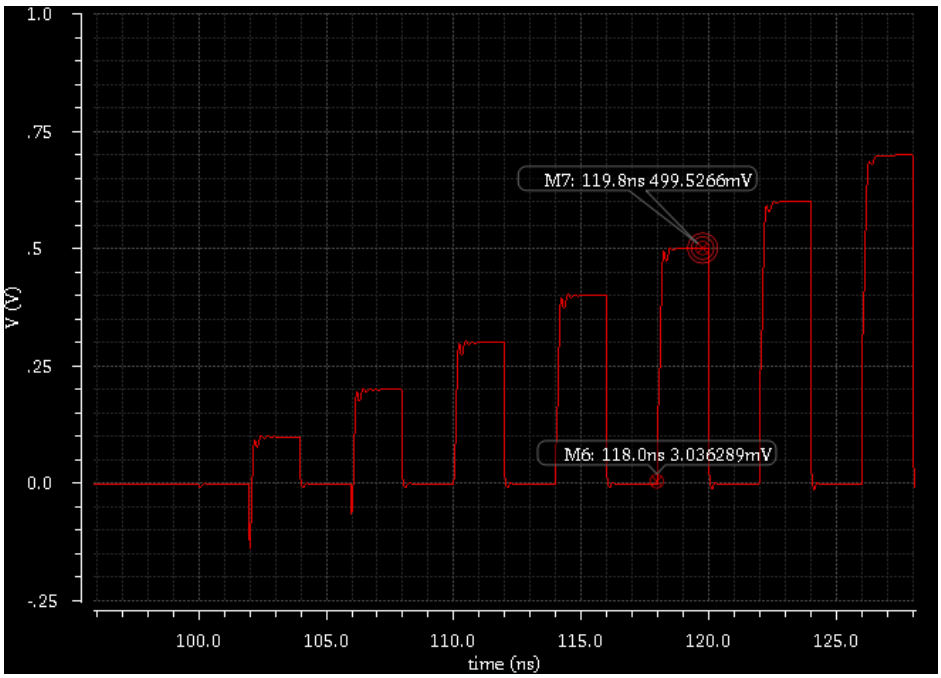

Fig. 12. Transient settling error of first integrator for a 100mV input

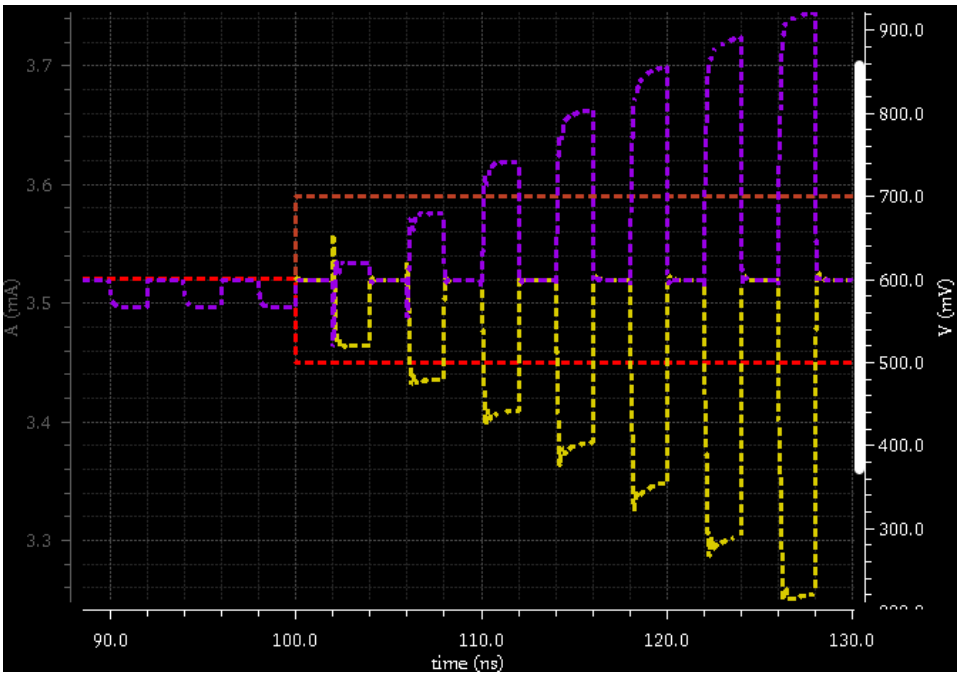

Fig. 13. Transient response of first integrator for a 100mV input

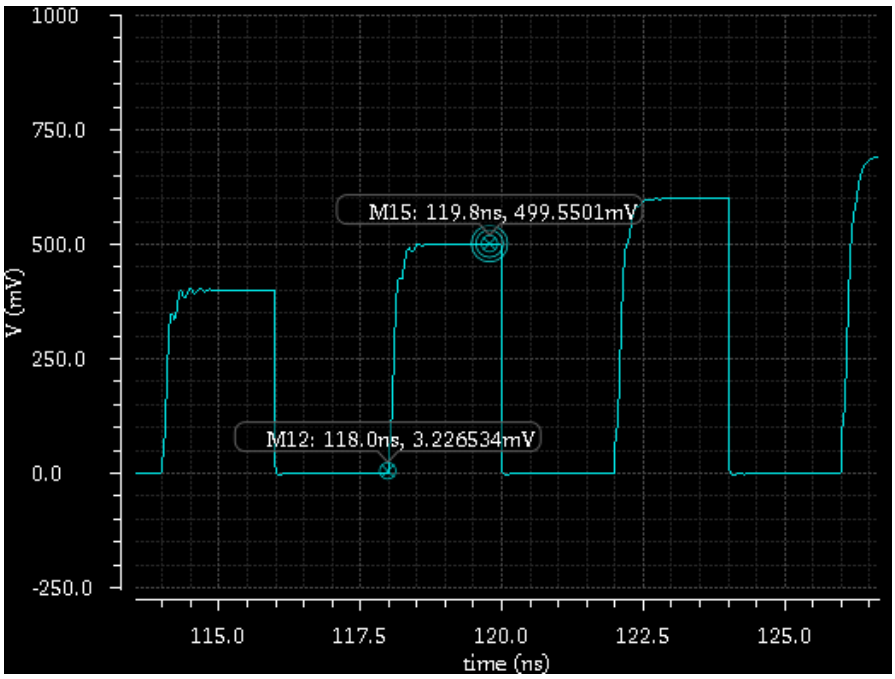

Fig. 14. Transient settling error of first integrator for a 100mV input

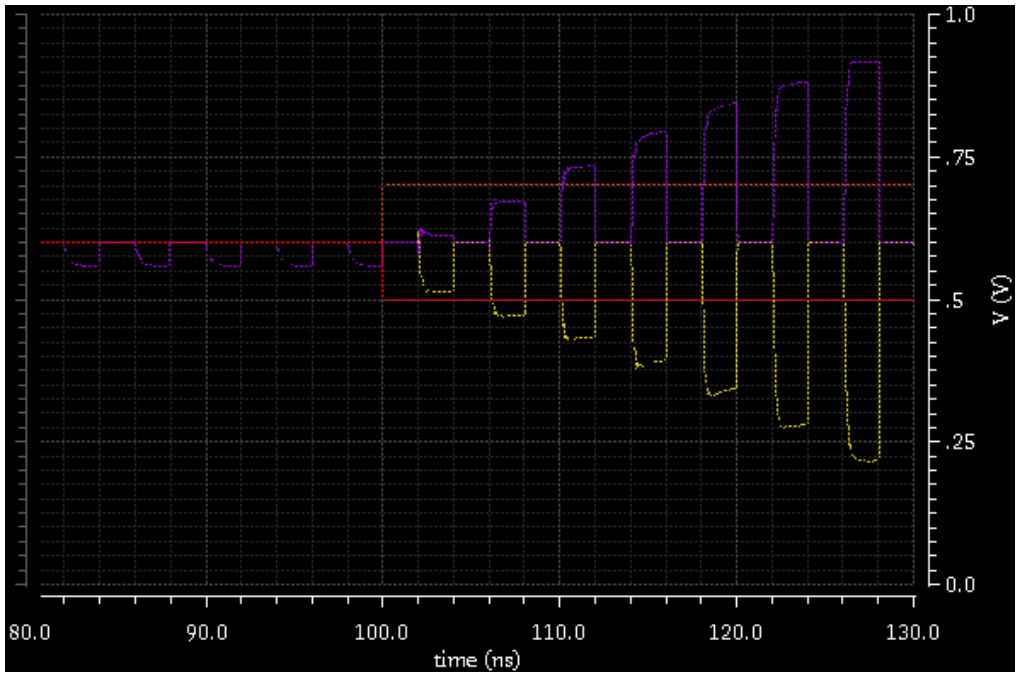

Fig. 15. Transient response of first integrator for a 100mV input

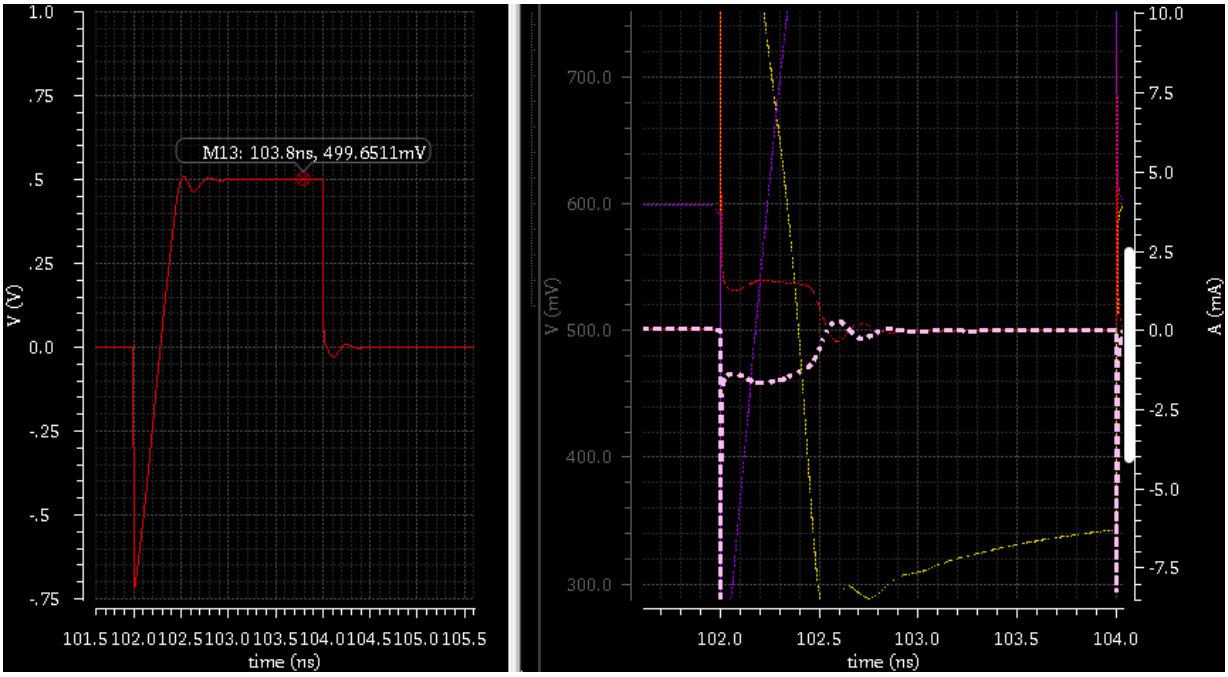

Fig. 16. Transient response of first integrator for a 1V input showing slewing