Design of Oversampled ADC Integrators

EE240B Project Report

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I. Introduction

We will propose a design for the integrator stages of an oversampled ADC. The design is driven by some specifications that include input-referred electronic noise, settling time as well as settling accuracy. We have chosen to use the same integrator architecture for both stages but tune the component values for each stage.

II. System-level Considerations

We started the design by modeling the ADC as transfer functions. We noticed that since the circuit implements an integration, the first stage should be a lot more carefully designed than the second stage. The input-referred noise transfer function from the output of the first stage is $N_1 = 2(z-1)$ while the second stage has a contribution that is affected by $N_2 = 0.25(z-1)^2$, assuming a second stage gain of 0.5. These transfer functions are also used later to verify the input-referred electronic noise of the circuit.

We estimated that the noise power contribution of the second stage is approximately 1000 times smaller than the first stage. We also noted that if we split the noise of a stage to each phases' noises (Φ_1 and Φ_2), the noise from Φ_1 is integrated along with the signal and is more important than the Φ_2 noise.

III. Integrator Implementation

Each integrator stage of the oversampled ADC has a gain of 0.5 and has to settle within 0.1% in 1.8ns wih a +/- 1V differential input. Fig. 1 shows the implementation of the integrator stages.

During Φ_1, C_S samples the input and during Φ_2 the input is amplified through charge transfer between C_S and C_F. The Φ_2 switch connecting the two sampling capacitors is a common mode rejection mechanism, transferring only the differential charge to C_F. C_F is connected in the feedback only during the amplification phase Φ_2 and is never reset, thus it integrates the input over time. C_L is the load capacitance; for the first stage this is the the sampling capacitor of the second stage, and for the second stage this is the input capacitance of the comparator.

Since the amplifiers form a second-order integrator, the first amplifier noise dominates the total noise. We begin by choosing C_S from the noise specification and the equation for noise at Φ_1.

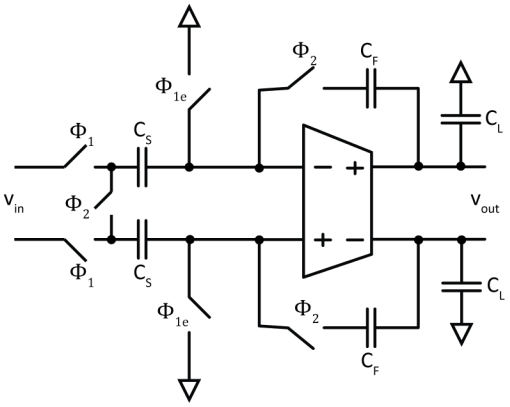

Fig. 1. Switched capacitor integrator

$$N_{\Phi 1} = \frac{kT}{C_S + C_L}$$

$$N_{\Phi 2} = \frac{\alpha}{\beta}\frac{kT}{C_{L,tot}}$$

The value of C_F is easily obtained from the required gain since the gain of the integrator is C_F/C_S. We want to budget $3.5\mu V_{RMS}$ to the noise at Φ_1 per differential input, but the signal bandwidth that we care about is only 100-500kHz and our equation for $N_{\phi 1}$ is over the entire spectrum. Therefore, we need to multiply the noise specification by the Oversampling Ratio, which is $\frac{f_S}{2BW}$. The noise that we want at the input therefore is $N_{\Phi 1} = 250 \cdot (3.5)^2 \cdot 10^{-12} V/\sqrt{Hz}$. We rounded the capacitor values up to get some headroom for error.

$$C_S = 1.5pF$$

$$C_F = 3pF$$

Our load capacitor is the sampling capacitor of stage 2. We first started at 100fF and iterated the design process to size the load capacitor C_L.

We next calculate the G_m of the OTA necessary to meet the settling time with those capacitors from the settling time requirement. The equation below expresses the dynamic settling error specification assuming an amplifier with a closed loop pole at τ and a zero.

$$t_s = -\tau ln\left(\epsilon_d\left(1 - \beta\frac{C_F}{C_F - C_L}\right)\right)$$

We budget half of the error to static error, so $\epsilon_d = 0.0005$. This results in a required transconductance of $G_m = 10.5mS$.

Next we calculated the required open loop gain of the amplifier. Since we are budgeting half of the settling error to static error, we require that

$$\frac{1}{T} = \frac{1}{\beta A} = \epsilon_s = 0.0005$$

With a β of 0.67, the required open loop gain is 3000, or 70 dB. This results in a required output resistance of $300k\Omega$.

With the design parameters, we started by building an ideal OTA using a VCCS. We created a testbench for AC, noise, and transient analysis and ran simulations to make sure the settling time, and noise requirements are met. The noise simulation was a performed with a noise current source from a resistor of value $\frac{\alpha}{G_m}$ inside of the OTA and 10Ω ON resistances in series with all of the switches. However, PSS and PNOISE are not really meant for integrators so we exported the noise density at the output of the integrator to Matlab, then multiplied by the input-refered transfer function from the noise source and then integrated over the signal bandwidth.

IV. Design Alternatives

We started with a telescopic OTA with an NMOS input but quickly realized that the V_{GS} of the input device is too large to get the V* we want since the input common mode of the OTA is $600mV$. To achieve high current efficiencies (low V*) the gate-source voltage of the device has to be close to the threshold voltage. We found that a V_{GS} of 0.4V is required to achieve a V* of $0.14V$. Such a low V* is ideal in our situation since larger current requires larger devices, which reduces the r_o of the devices.

Next we moved to a folded cascode OTA architecture. With a folded cascode, the V_{GS} of the input device can be almost arbitrarily set by the tail current. Setting the V_{GS} to $0.4V$ provides us with the V* we desired.

The transconductance g_m we needed is limited by the dynamic settling time. Using the dynamic settling equation with a pole and a zero, we found that the g_m required for the OTA is $\_21mS\_$. With a V* of $0.14V$, the drain current is $\_1.5mA\_$.

We set the current of the cascode branch to be greater than the current flowing through the input devices so the cascode devices never has zero current flowing through them even during slewing. This is important since the slew rate is now only dependent on the first stage current.

To avoid slewing for extended periods of time, the current in the input device has to be large enough to charge the load capacitance. Since when the closed loop amplifier is subjected to a step input there is a capacitive divider effect from the input to the output node, the output has to slew more than the maximum single-ended output swing of $0.25V$. Designing for a $0.5V$ slew in 0.4ns, with a total load capacitance of $C_{Ltot} = C_L + (1-\beta)C_F = \_1.1pF\_$, the current needed in the input devices is $1.5mA$. Since the required g_m of the OTA already enforces this drain current, we do not need to worry about slewing.

After attempting to build the OTA, we discovered that getting the output resistance to be high is very hard with the current architecture. The required open loop gain is 3000, and with a g_m of $\_21mS\_$ the required output resistance is $\_143k\Omega\_$. With the bias currents in the design, this output resistance is unachievable.

To realize the high output resistances, we added gain boosters to the folded cascode OTA. The gain booster requirements are derived from the current output resistance and the bandwidth of the OTA. Fig. 2 shows the gain-boosted folded cascode OTA circuit. based on the output resistance looking up from the output node $R_{out,up} = g_{m7}r_{o7}(r_{o5}||r_{o3}||r_{o1})$, the PMOS gain booster require an open loop gain of $36dB$. On top of that, the unity gain of the gain booster has to be larger than the 3dB bandwidth of the closed loop amplifier; we set the unity gain bandwidth to __.

The output resistance looking down from the output node is $R_{out,down} = g_{m9}r_{o9}r_{o11}$. This is relatively high compared to $R_{out,up}$, but is still not high enough to meet the total output resistance of $\_143k\Omega\_$. We also added a gain booster with an open loop gain of __ and a unity gain bandwidth of __.

To build these gain boosters, we attempted to use a common differential pair, but the input voltage bias and the output voltage bias are not ideal for such an architecture. For example, the PMOS gain boosters have an input voltage of $1V$ and an output voltage of $0.4V$. Using an NMOS input device would result in too much V_{GS}, hence too high V*. Just like the main OTA, we solved this problem by implementing a folded cascode.

gain booster design here

V. Circuit Implementation

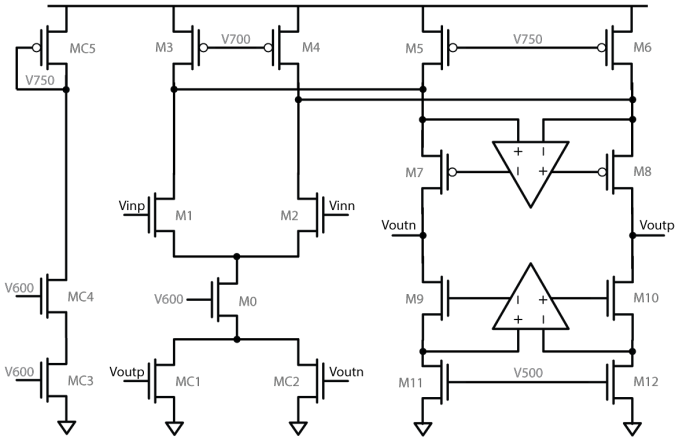

Fig. 2. Gain-boosted folded cascode OTA with CMFB

Device	W (μ)	L (n)	V*	I_D(m)	g_m(m)	f_T(G)
Differential pair						
M0	42.1	90	0.22	3.63	33	94.7
M1/2	15.9	60	0.20	1.81	18.4	224
M3/4	154.8	100	0.19	1.81	19	13.4
Output branch						
M5/6	172.98	80	0.15	1.8	23.5	20.2
M7/8	79.38	100	0.25	1.77	14.3	18.3
M9/10	71.35	300	0.19	1.77	18.8	97.2
M11/12	88.56	200	0.15	1.45Pm77	23.3	17.2
CMFB						
MC1/2	15.13	60	0.7	1.81	5.1	57.3
MC3	12.61	60	0.6	1.52	5.1	68.7
MC4	14.5	90	0.22	1.52	13.7	112
MC5	195.3	140	0.14	1.52	21.4	5.02

Device	W (μ)	L (n)	V*	I_D(m)	g_m(m)	f_T(G)
Differential pair						
M0	198.4	200	0.27	2.2	16	3.98
M1/2	77.5	60	0.13	1.1	16.3	43
Output branch						
M3/4	68.5	150	0.28	1.1	7.95	7.6
M5/6	49.7	100	0.13	1.1	17.3	58
M7/8	7.13	60	0.44	2.2	10.1	237

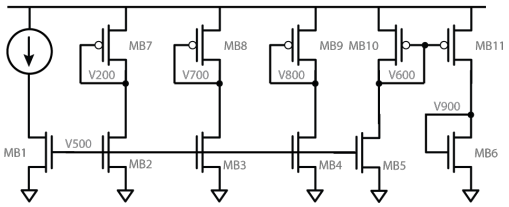

Fig. 5. Biasing Network

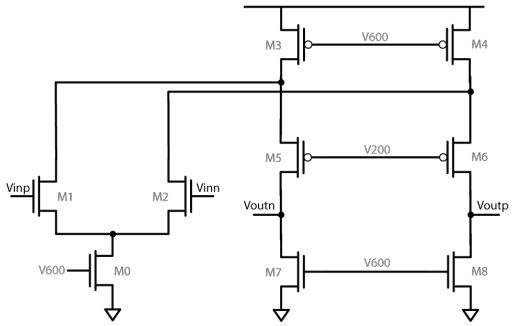

Fig. 3. PMOS Gain Booster

Device	W (μ)	L (n)	V*	I_D(m)	g_m(m)	f_T(G)
MB1	5.89	80	0.19	0.5	5.27	128
MB2	7.18	80	0.18	0.5	5.6	115
MB3	5.27	80	0.18	0.5	5.6	115
MB4	4.99	80	0.18	0.5	5.6	115
MB5	5.56	80	0.18	0.5	5.6	115
MB6	2.69	300	0.65	0.5	1.54	17.5
MB7	2.6	140	0.83	0.5	1.2	88.9
MB8	34	140	0.18	0.5	5.6	6.5
MB9	142.59	140	0.12	0.5	8.6	3.82
MB10	13.7	140	0.28	0.5	3.57	9.17
MB11	14.5	140	0.28	0.5	3.57	9.17

Device	W (μ)	L (n)	V*	I_D(m)	g_m(m)	f_T(G)
Differential pair						
M0	16.4	90	0.29	2	13.9	122.7
M1/2	14	90	0.14	1	14.2	78
Output branch						
M3/4	11.6	90	0.3	1.5	10.1	26.4
M5/6	2.6	90	0.4	0.5	2.53	108
M7/8	4	100	0.28	0.5	3.5	89

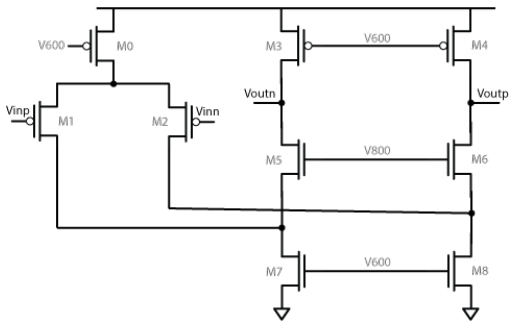

Fig. 4. NMOS Gain Booster

VI. Design Verification

VII. Final Specification

Gain	0.5
Input Referred Noise	9.18 μV_{RMS}
Settling	0.1% in 1.27 ns
Sampling Freq	250MHz
Total Power	43.056 mW

1st stage noise 8.86uV 2nd stage noise 0.31950uV 19.09 mA 1st stage 13.79 mA 2nd stage 3mA biasing 35.88 mA totall

VIII. Design Critique

flicker? - chopper stabilization

References

[1] B. Bernhard, *The Design of Sigma-Delta Modulation Analog-to-Digita1 Converters*, IEEE Journal of Solid-State Circuits, vol.23 ,no.6, 1988.