Design of Oversampled ADC Integrators

EE240B Project Milestone

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I. Introduction

We will propose a design for two integrator stages in an oversampled ADC. The design is driven by some specifications that include input-referred electronic noise, settling time as well as settling accuracy. We have chosen to use the same integrator architecture for both stages but tune the component values for each stage. Section II describes the motivation behind this tuning while Section III provides an early design for the integrator stages.

II. System Modeling

To see how our integrators take part in the overall Oversampled ADC architecture, we will first model our integrators with a simple gain and integrator in the z-domain. To model the circuit more accurately, we added two noise sources, one in the input and one at the output. We first assume that the noise in the circuit is white from thermal noise; if the 1/f noise dominates we can modify our circuit to mitigate the issue.

Fig. 1 shows the system model of our integrator stage. The input noise source N_{i1} for integrator i is caused by the sampling phase Φ_1 of the integrator. Since this sampled noise gets integrated over time, we model it as an addition to the signal at the input. On top of this, we model the noise associated by the amplifying phase Φ_2 by an addition with N_{i2} at the output of the integrator.

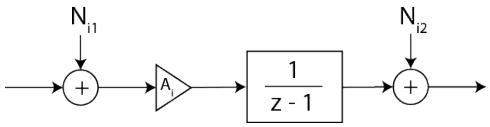

Fig. 1. Integrator model for stage i

Using this model, we can derive the input-referred noise contribution for each of the noise sources. The whole system can be modeled as Fig. 2. Here, the second integrator gain is A. We have also modeled the quantizer and DAC as quantization noise Q.

From the system model, we can derive how each input affects the output.

$$Y\left(1+\frac{A}{z-1}+\frac{A/2}{(z-1)^2}\right) = N_{22}+Q+\frac{A}{z-1}(N_{21}+N_{12})+\frac{A/2}{(z-1)^2}(N_{11}+X) \quad (1)$$

The contribution of each input as seen in the output Y can then be calculated.

$$\frac{Y_X}{X}=\frac{Y_{N11}}{N_{11}}=\frac{A/2}{(z-1)^2+A(z-1)+A/2}$$

$$\frac{Y_{N21}}{N_{21}}=\frac{Y_{N12}}{N_{12}}=\frac{A(z-1)}{(z-1)^2+A(z-1)+A/2}$$

$$\frac{Y_{N22}}{N_{22}}=\frac{Y_Q}{Q}=\frac{(z-1)^2}{(z-1)^2+A(z-1)+A/2}$$

If we divide each expression with the signal transfer function, we get the input-refered contribution of each noise source.

$$N_{11}:1$$

$$N_{12}=N_{21}:2(z-1)$$

$$N_{22}:\frac{(z-1)^2}{A/2}$$

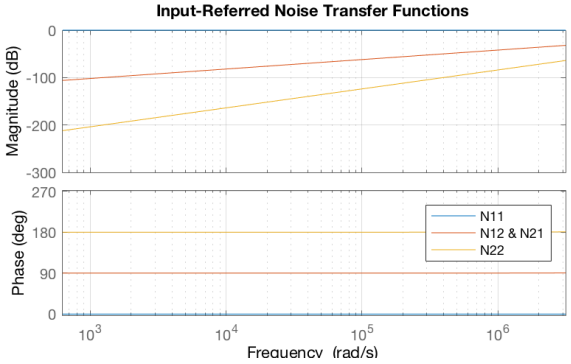

Fig. 3. Input-referred noise contributions

Fig. 3 shows the bode plot of these transfer functions in the signal frequencies. As expected, the second integrating stage noise is suppressed more than the first stage and the Φ_2 noise is suppressed more than the Φ_1 noise due to the integrating function of the circuit. When we budget the noise of the circuits, we should take these into account. The first integrator needs to be carefully designed to have a much lower noise compared to the second integrator.

To divide the noise budget, we use a first-order approximation. The N_{12} and N_{21} input-referred transfer function has a highest point at around -30dB, so the integrated noise power

of these noise sources compared to that of N_{11} is at the worst case $10^{30/10} = 1000$ times smaller. Similarly, the noise power contribution of N_{22} is 10^6 times smaller than that of N_{11}.

The second-stage gain A has negligible effects on the input-referred noise contribution, but the larger the gain the smaller the effect of N_{22} and Q. In practice this parameter is limited by the signal swing of the circuit.

III. Design

For this project the important specifications are:

Gain (Stage 1)	0.5
Input Referred Noise	$10\mu\ V_{RMS}$
Settling	0.1% in 1.8ns
Sampling Freq	250M Hz

We divided the settling error requirement evenly between static and dynamic error, so $\epsilon_d = 0.05\%$. Furthermore, we decided to budget noise based on the noise factor calculations from the previous section. We see that the noise ϕ_1 is the most important contribution to the noise. ϕ_2 will be divided by a factor of 1000, therefore budget nearly all of the noise requirements for noise from N_{11}. The spec is for differential noise, so calculating single ended, we need to hit $5\mu\ V_{RMS}$. We divide that further up, so that there is $3\mu\ V_{RMS}$ for one input of the first integrator, and $1\mu\ V_{RMS}$ for one input of the second stage and output of the second stage, taking advantage of the fact that the second integrator can be designed with much looser noise requirements.

From these specifications, we see that the small noise and rapid settling time will require careful design to meet both simultaneously. We began by considering a basic switch cap integrator to get an idea of the what values were needed to meet $3\mu\ V_{RMS}$ per input. We can use a design process similar to that of a sample and hold circuit, with only minor differences due to different switches.

PICTURE HERE OF BASIC SWITCH CAP

The necessary equations are below.

Gain:

$$\frac{V_{out}}{V_{in}} = \frac{C_S}{C_F}$$

Settling Time:

$$t_s = -\tau ln\left(\epsilon_d\left(1 - \beta\frac{C_F}{C_F - C_L}\right)\right)$$

Noise:

$$\phi_1 = \frac{kT}{C_S + C_L}$$

$$\phi_2 = \frac{\alpha}{\beta}\frac{kT}{C_{L,tot}}$$

Where in these equations, beta is the feedback factor.

$$\beta = \frac{C_F}{C_S + C_F + C_L}$$

In addition, $C_{L,tot}$ is the effective capacitive load.

$$C_{L,tot} = C_L + (1 - \beta)C_F$$

. And τ is the time constant of the system.

$$\tau = \frac{C_{L,tot}}{(\beta * G_m)}$$

A. First Stage

We begin by choosing C_S from the noise spec and the equation for phi_1. Then C_F is easily obtained from the required gain. We want to meet $3\mu\ V_{RMS}$ per input, but the BW that we care about noise is only 100-500kHz and our equation for ϕ_1 is over the entire spectrum. Therefore, we need to divide by the Oversampling Ratio, which is $\frac{f_S}{2BW}$. The noise that we want at the input therefore is $N_{11} = 9e-12V/\sqrt{Hz}$.

$$C_S = 2pF$$

$$C_F = 4pF$$

These are somewhat large capacitor values to drive. We next calculate the G_m of the OTA necessary to meet the settling time with those capacitors from τ. We get $G_M = 9mS$, which is a little large, but should be doable with large width MOSFETs. We began adding parasitics to the transconductor. Parasitic capacitors are from $C_{GS} = \frac{g_m}{\omega_T}$ and we made a first optimistic guess at a conservative $r_o = 10k$ and found that in simulation we needed significantly larger G_M. We decided that G_M was getting a little large and decided to check a cascaded setup. We used ideal transconductors for the diff pairs.

MOAR PICTURE

The relevant equations for this part change only a little: settling time stays same tau = cc/bgm1 noise = a/b/ kt/CC (1+b a2/a1 CC/cltot)

However, most of the equations for poles and zeros are very approximated, and they do not take into account that the cascaded pair are more stable when g_{m1} is larger than g_{m2}. We also had to use a Miller capacitance for pole splitting.

We had to iteratively find a stable value of g_ms that met timing, and eventually settled on $g_{m1} =$, $g_{m2} =$.

TWO STAGE TRANS?

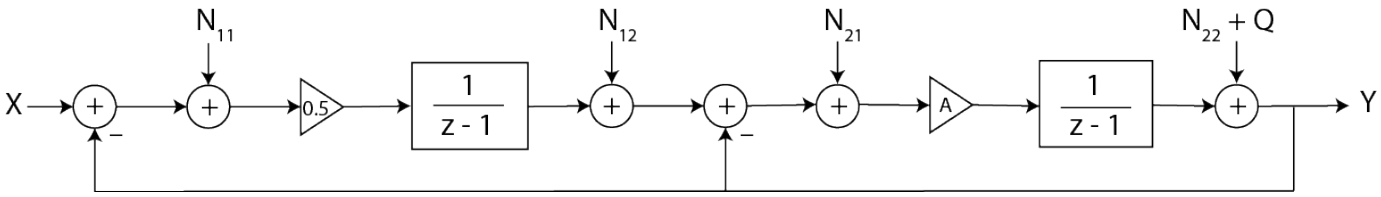

Fig. 2. Oversampled ADC system model

These value of g_m are not significantly better than the single stage transconductor and the noise of a single stage is better, so we decided that a very large diff pair would be better than cascading.

We re-examined the parasitic resistance and decided that increasing the r_o was the next best option, so that we needed the first stage OTA to be a single stage diff pair with cascoding, and approximated the new r_o as a conservative $100k\Omega$.

We ran a final transient sim to make sure that the settling time of the output of the first stage was 1.8ns to 1%.

FIGURES

The noise simulation was a performed with a noise current source of $\frac{1}{G_m}$ inside of the OTA and 10Ω ON resistances in series with all of the switches. However, PSS and PNOISE are not really meant for integrators so we got the $V/\sqrt{Hz}$ noise density at the output of the integrator which we exported to Matlab, then multiplied by the transfer function from the output to the input, which is N_{12} and then integrated over the BW.

We got a noise of $2.24\mu V_{rms}$ which gives us a lot of room to change the C_s if we need it.

C_S	2pF
C_F	4pF
G_M	19mS
$R_{o,min}$	100k

In this stage, the most important design factor is meeting the noise requirement. This means that if noise is a problem later in the problem we can increase C_S however, since we are very cleanly meeting the noise spec, we can trade some of it for lower G_M in the gain stage. The large capacitors in the feedback loop relative to the load capacitance of the net stage, however, mean that the loop gain is large and we don't need quite as good of output resistance to keep static error within spec.

B. Second Stage

For second stage, we are meeting a noise spec which is 1000 times more lenient. Thus, we can choose much smaller feedback capacitance and G_M of the OTA can be much more lenient. Using the same design procedure as before we obtain the values for the second integrator, also with a gain of $\frac{1}{2}$

C_S	30fF
C_F	15fF
G_M	5mS
$R_{o,min}$	1M

We did find, that because the feedback capacitors are not on the same order as the load cap, the static error is a much bigger concern, so we need to meet a larger output resistance of the OTA in order to keep the g_m build-able with one stage.

IV. Implementation

A. OTAs

The above simulations confirmed that we needed reasonably large g_m OTAs, and that output resistance is more important for the second stage than the first stage.

For the first stage we want a diff pair with reasonably large output resistance. We propose the following:

SCH OF DIFF PAIR WITH LAME RO

M_1 and M_2 completely determine the G_M of the OTA and will need to be sized accordingly. The large width of M_1 and M_2 necessitates using cascoding at least on the input caps, but careful sizing of M_5 and M_6 should meet the required output resistance of the first stage without having to use a full telescopic design which will limit the output swing a lot.

For the second stage, however, we need better output resistance, in which case we need a telescopic differential pair, but we shouldn't need gain boosting.

B. Switches

The resistance of the switches is something of a concern in the first stage. In particular,

C. Integrators

proposed schematic with all the bells and whistles

use common mode rejection switch on input

offset not a thing in simulation, but here is how we will add it to be through or something

bottom plate sampling with early switches

V. Non-Simulation Considerations

VI. Conclusion

TODO: The conclusion goes here.

References

[1] TODO: H. Kopka and P. W. Daly, *A Guide to LaTeX*, 3rd ed. Harlow, England: Addison-Wesley, 1999.