Design of Oversampled ADC Integrators

EE240B Project Milestone

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I. Introduction

We will propose a design for two integrator stages in an oversampled ADC. The design is driven by some specifications that include input-referred electronic noise, settling time as well as settling accuracy. We have chosen to use the same integrator architecture for both stages but tune the component values for each stage. Section II describes the motivation behind this tuning while Section III provides an early design for the integrator stages.

II. System Modeling

To see how our integrators take part in the overall Oversampled ADC architecture, we will first model our integrators with a simple gain and integrator in the z-domain. To model the circuit more accurately, we added two noise sources, one in the input and one at the output. We first assume that the noise in the circuit is white from thermal noise; if the 1/f noise dominates we can modify our circuit to mitigate the issue.

Fig. 1 shows the system model of our integrator stage. The input noise source N_{i1} for integrator i is caused by the sampling phase Φ_1 of the integrator. Since this sampled noise gets integrated over time, we model it as an addition to the signal at the input. On top of this, we model the noise associated by the amplifying phase Φ_2 by an addition with N_{i2} at the output of the integrator.

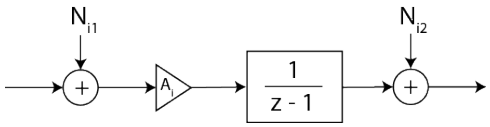

Fig. 1. Integrator model for stage i

Using this model, we can derive the input-referred noise contribution for each of the noise sources. The whole system can be modeled as Fig. 2. Here, the second integrator gain is A. We have also modeled the quantizer and DAC as quantization noise Q.

From the system model, we can derive how each input affects the output.

$$Y\left(1+\frac{A}{z-1}+\frac{A/2}{(z-1)^2}\right) = N_{22}+Q+\frac{A}{z-1}(N_{21}+N_{12})+\frac{A/2}{(z-1)^2}(N_{11}+X) \quad (1)$$

The contribution of each input as seen in the output Y can then be calculated.

$$\frac{Y_X}{X}=\frac{Y_{N11}}{N_{11}}=\frac{A/2}{(z-1)^2+A(z-1)+A/2}$$

$$\frac{Y_{N21}}{N_{21}}=\frac{Y_{N12}}{N_{12}}=\frac{A(z-1)}{(z-1)^2+A(z-1)+A/2}$$

$$\frac{Y_{N22}}{N_{22}}=\frac{Y_Q}{Q}=\frac{(z-1)^2}{(z-1)^2+A(z-1)+A/2}$$

If we divide each expression with the signal transfer function, we get the input-refered contribution of each noise source.

$$N_{11}:1$$

$$N_{12}=N_{21}:2(z-1)$$

$$N_{22}:\frac{(z-1)^2}{A/2}$$

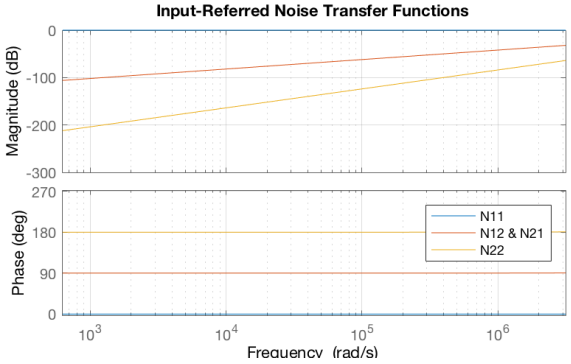

Fig. 3. Input-referred noise contributions

Fig. 3 shows the bode plot of these transfer functions in the signal frequencies. As expected, the second integrating stage noise is suppressed more than the first stage and the Φ_2 noise is suppressed more than the Φ_1 noise due to the integrating function of the circuit. When we budget the noise of the circuits, we should take these into account. The first integrator needs to be carefully designed to have a much lower noise compared to the second integrator.

To divide the noise budget, we use a first-order approximation. The N_{12} and N_{21} input-referred transfer function has a highest point at around -30dB, so the integrated noise power

of these noise sources compared to that of N_{11} is at the worst case $10^{30/10} = 1000$ times smaller. Similarly, the noise power contribution of N_{22} is 10^6 times smaller than that of N_{11}.

The second-stage gain A has negligible effects on the input-referred noise contribution, but the larger the gain the smaller the effect of N_{22} and Q. In practice this parameter is limited by the signal swing of the circuit.

III. Design

For this project the important specifications are:

Gain (Stage 1)	0.5
Input Referred Noise	$10\mu\ V_{RMS}$
Settling	0.1% in 1.8ns
Sampling Freq	250M Hz

We divided the settling error requirement evenly between static and dynamic error, so $\epsilon_d = 0.05\%$. Furthermore, we decided to budget noise based on the noise factor calculations from the previous section. We see that the noise ϕ_1 is the most important contribution to the noise. ϕ_2 will be divided by a factor of 1000, therefore budget nearly all of the noise requirements for noise from N_{11}. The spec is for differential noise, so calculating single ended, we need to hit $5\mu\ V_{RMS}$. We divide that further up, so that there is $4\mu\ V_{RMS}$ for one input of the first integrator, and $1\mu\ V_{RMS}$ for one input of the second stage, taking advantage of the fact that the second integrator can be designed with much looser noise requirements.

From these specifications, we see that the small noise and rapid settling time will require careful design to meet both simultaneously. We began by considering a basic switch cap integrator to get an idea of the what values were needed to meet $4\mu\ V_{RMS}$ per input. We can use a design process similar to that of a sample and hold circuit, with only minor differences due to different switches.

PICTURE HERE OF BASIC SWITCH CAP

The necessary equations are below.

Gain:

$$\frac{V_{out}}{V_{in}} = \frac{C_S}{C_F}$$

Settling Time:

$$t_s = -\tau ln\left(\epsilon_d\left(1 - \beta\frac{C_F}{C_F - C_L}\right)\right)$$

Noise:

$$\phi_1 = \frac{kT}{C_S + C_L}$$

$$\phi_2 = \frac{\alpha}{\beta}\frac{kT}{C_{L,tot}}$$

Where in these equations, beta is the feedback factor.

$$\beta = \frac{C_F}{C_S + C_F + C_L}$$

In addition, $C_{L,tot}$ is the effective capacitive load.

$$C_{L,tot} = C_L + (1 - \beta)C_F$$

. And τ is the time constant of the system.

$$\tau = \frac{C_{L,tot}}{(\beta * G_m)}$$

We begin by choosing C_S from the noise spec and the equation for phi_1. Then C_F is easily obtained from the required gain. We want to meet $4\mu\ V_{RMS}$ per input, but the BW that we care about noise is only 100-500kHz and our equation for ϕ_1 is over the entire spectrum

$$C_S = 100pF$$

$$C_F = 200pF$$

These are somewhat large capacitor values to drive. We next calculate the G_m from the OTA necessary to meet the settling time with those capacitors. cap choice from noise and gain (overdesigned for infinte spectrum, for buffer room) need larger gm leads to next schematic MOAR PICTURE More equations for first bout settling time stays same tau = cc/bgm1 noise = a/b/ kt/CC (1+b a2/a1 CC/cltot) gm1 gm2

use noise to get CC iterate for stable gm2 and gm1 for settling time

Sim to check specs Settling time meets AC stable Noise FUCKIT

IV. Implementation

gm gonna suck, also, low output impedance sucks too need cascode or even gain-boosting

RC time constant so suck need super good switch. gonna be enormous

proposed schematic with all the bells and whistles

use common mode rejection switch on input

offset not a thing in simulation, but here is how we will add it to be through or something

bottom plate sampling with early switches

V. Non-Simulation Considerations

VI. Conclusion

TODO: The conclusion goes here.

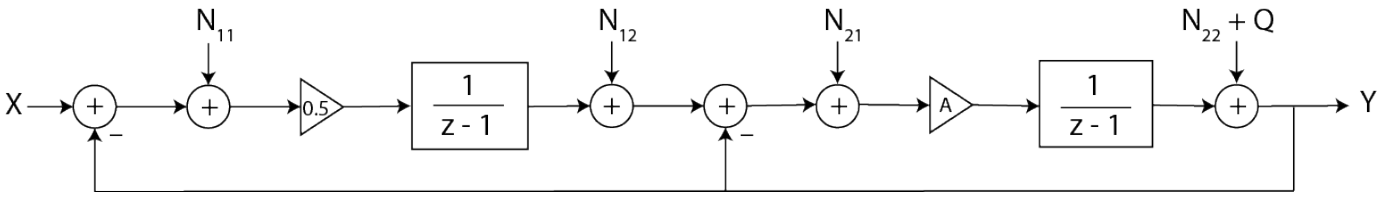

Fig. 2. Oversampled ADC system model

REFERENCES

[1] TODO: H. Kopka and P. W. Daly, *A Guide to LaTeX*, 3rd ed. Harlow, England: Addison-Wesley, 1999.