Design of Oversampled ADC Integrators

EE240B Project Milestone

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I. Introduction

We will propose a design for two integrator stages in an oversampled ADC. The design is driven by some specifications that include input-referred electronic noise, settling time as well as settling accuracy. We have chosen to use the same integrator architecture for both stages but tune the component values for each stage. Section II describes the motivation behind this tuning while Section III provides an early design for the integrator stages.

II. System Modeling

To see how our integrators take part in the overall Oversampled ADC architecture, we will first model our integrators with a simple gain and integrator in the z-domain. To model the circuit more accurately, we added two noise sources, one in the input and one at the output. We first assume that the noise in the circuit is white from thermal noise; if the 1/f noise dominates we can modify our circuit to mitigate the issue.

Fig. 1 shows the system model of our integrator stage. The input noise source N_{i1} for integrator i is caused by the sampling phase Φ_1 of the integrator. Since this sampled noise gets integrated over time, we model it as an addition to the signal at the input. On top of this, we model the noise associated by the amplifying phase Φ_2 by an addition with N_{i2} at the output of the integrator.

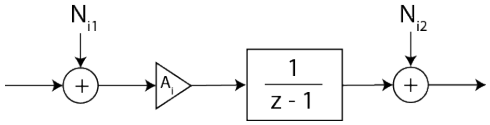

Fig. 1. Integrator model for stage i

Using this model, we can derive the input-referred noise contribution for each of the noise sources. The whole system can be modeled as Fig. 2. Here, the second integrator gain is A. We have also modeled the quantizer and DAC as quantization noise Q.

From the system model, we can derive how each input affects the output.

$$Y\left(1+\frac{A}{z-1}+\frac{A/2}{(z-1)^2}\right) = N_{22}+Q+\frac{A}{z-1}(N_{21}+N_{12})+\frac{A/2}{(z-1)^2}(N_{11}+X) \quad (1)$$

The contribution of each input as seen in the output Y can then be calculated.

$$\frac{Y_X}{X}=\frac{Y_{N11}}{N_{11}}=\frac{A/2}{(z-1)^2+A(z-1)+A/2}$$

$$\frac{Y_{N21}}{N_{21}}=\frac{Y_{N12}}{N_{12}}=\frac{A(z-1)}{(z-1)^2+A(z-1)+A/2}$$

$$\frac{Y_{N22}}{N_{22}}=\frac{Y_Q}{Q}=\frac{(z-1)^2}{(z-1)^2+A(z-1)+A/2}$$

If we divide each expression with the signal transfer function, we get the input-refered contribution of each noise source.

$$N_{11}:1$$

$$N_{12}=N_{21}:2(z-1)$$

$$N_{22}:\frac{(z-1)^2}{A/2}$$

Fig. 3 shows the bode plot of these transfer functions in the signal frequencies. As expected, the second stage noise is suppressed more than the first stage and the Φ_2 noise is suppressed more than the Φ_1 noise due to the integrating function of the circuit. When we budget the noise of the circuits, we should take these into account. The first integrator needs to be carefully designed to have a much lower noise compared to the second integrator.

The second-stage gain A has negligible effects on the input-referred noise contribution, but the larger the gain the smaller the effect of N_{22} and Q. In practice this parameter is limited by the signal swing of the circuit.

III. Integrator Implementation

IV. Conclusion

TODO: The conclusion goes here.

References

[1] TODO: H. Kopka and P. W. Daly, *A Guide to LaTeX*, 3rd ed. Harlow, England: Addison-Wesley, 1999.

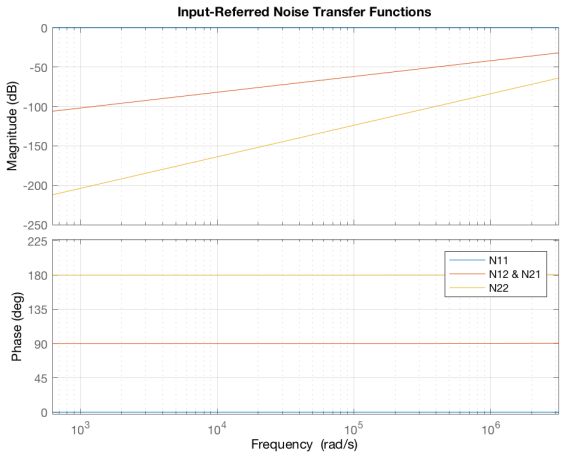

Fig. 3. Input-referred noise contributions

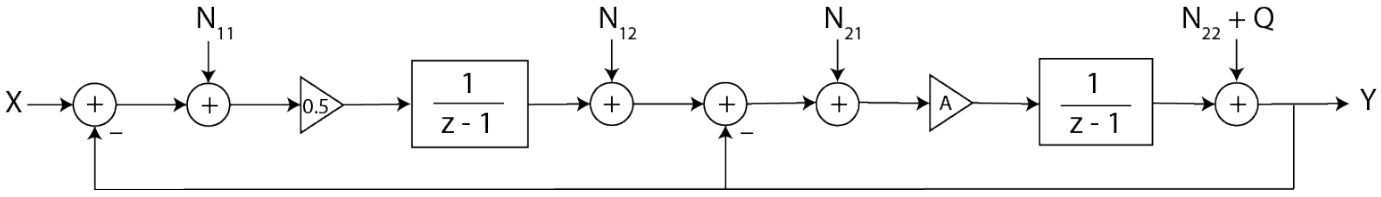

Fig. 2. Oversampled ADC system model