Design of Oversampled ADC Integrators

EE240B Project Report

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I. Introduction

We will propose a design for the integrator stages of an oversampled ADC. The design is driven by some specifications that include input-referred electronic noise, settling time as well as settling accuracy. We have chosen to use the same integrator architecture for both stages but tune the component values for each stage.

II. Integrator Implementation

III. Design Alternatives

IV. Circuit Implementation

V. Design Verification

VI. Final Specification

Gain	0.5
Input Referred Noise	?? μ V_{RMS}
Settling	0.1% in ?? ns
Sampling Freq	250M Hz
Total Power	?? mW

VII. Design Critique

flicker? - chopper stabilization

References

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