Reliability Aware Negative Bit-Line Voltage Write Assist Scheme for SRAM

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Abstract-- In nanoscale CMOS technologies, SRAMs employ aggressively small cells, which make them extremely vulnerable to process variations, degrading the write-ability of SRAM. The increased effect of process variations in nanoscale technologies requires additional techniques and treatments such as write assist techniques to ensure fast and reliable write operation. Many write assist techniques e.g. reduce V_{DD} at cell, raise V_{SS} at cell, WL(word-line) boost, strengthen pass gate NMOS, weaken pull-up PMOS, negative bit-line scheme have been presented earlier, out of which negative bit line voltage scheme and WL (word-line) boost scheme have been found two most promising solutions for assisting write operation of SRAM. Negative voltage required for negative bit-line voltage scheme is generated on chip. A major drawback of negative-bit line voltage scheme is that due to negative spike generated, reliability of circuit degrades. A new low power write assist scheme is presented in this paper in which negative bit-line voltage scheme is combined with WL(word line) boost technique to increase the reliability and performance of the write assist circuit.

Keywords--NBLV (Negative bit-line voltage), WL_{CRIT}, Write-ability, WL (Word-Line) boost , WA (Write Assist)

I.　　　INTRODUCTION

The 6-T SRAM cell design has been successfully scaled in both bulk and SOI, and has remained for more than a decade the dominant technology development vehicle for advanced CMOS technologies. SRAMs are occupying more than 70% of the final SoC area and hence SRAM's area, power, performance and leakage became significant deciding factors in over all budgeting of SoC. Reduced device dimensions and operating voltages that accompany technology scaling have led to increased design challenges with each successive technology node. This is especially true for the 6-T SRAM cell that often uses minimum device dimensions and requires many waived design rules to achieve its aggressive density targets. Despite these challenges, the 6-T SRAM is expected to continue to play a dominant role in future technology generations because of its combination of density, performance, and compatibility with the CMOS logic process. Circuit operations over a wide range of supply voltages enables maximum energy efficiency for a given performance requirement, yet increased variability in deeply scaled technologies prevents static random-access memory (SRAM) from achieving as low an operational voltage (V_{MIN}) as logic. Assist techniques that dynamically change the operating characteristics of bit-cells, such as boosting the word-line voltage above the cell voltage, can lower V_{MIN} for SRAM. A unique feature of the 6-T SRAM is an inherent trade-off between stability when holding data during a read or non-column selected write access and the ability of the cell to be written. This fact means that the device dimensions and threshold voltage targets established for the SRAM devices are a compromise by design. The ability to read and write is characterized in terms of margins to assess the functional implications. These margins, which are referred to as write margin (WM), and read static noise margin or static noise margin, tend to decrease with scaling. Reduced functional margins combined with the growth in bit count and increased variation with each successive generation, lead to a mounting concern for the viability of the 6-T SRAM in future generations. Local random variations in device threshold voltage (V_{TH}) and other parameters can result in read disturb (cell flipping during read), write failures (unsuccessful write operation) as scaling continues. Owing to the requirement of different drive strength of the pass gate, it is difficult to design SRAM cells which are stable for both read and write without a large area overhead in SRAM cell size. So, a better method is to make the cell stable for read by making pass-gate strength small and use a write-assist technique for write robustness. One another stringent requirement on write ability of SRAM cell is to write proper data in SRAM cell within the specified time (limited word-line pulse width time). So a promising, highly reliable and performance efficient technique is proposed in this paper. The effectiveness of an SRAM write operation is typically quantified by the minimum (or critical) width of word-line pulse (defined as WL_{CRIT}) during which the bit cell changes state. The definition is important because it captures the dynamic write margin which is more accurate.
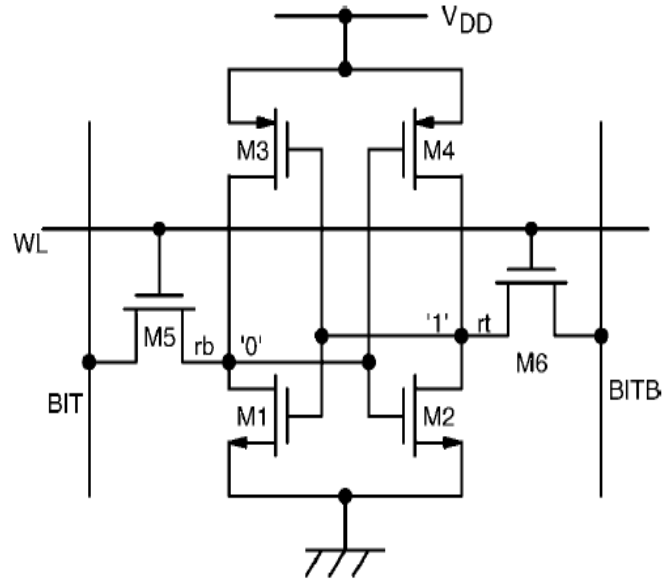
Fig 1: 1-bit 6-T SRAM Cell

For the SRAM Cell shown in Fig.1, when BITB goes to logic '0' during a write operation, 'rt' node should go to '0' and 'rb' node should go to '1' for a correct write operation. If the internal nodes do not flip, it is a write failure as shown in Fig. 2a. An example of a correct write operation is shown in Fig. 2b.
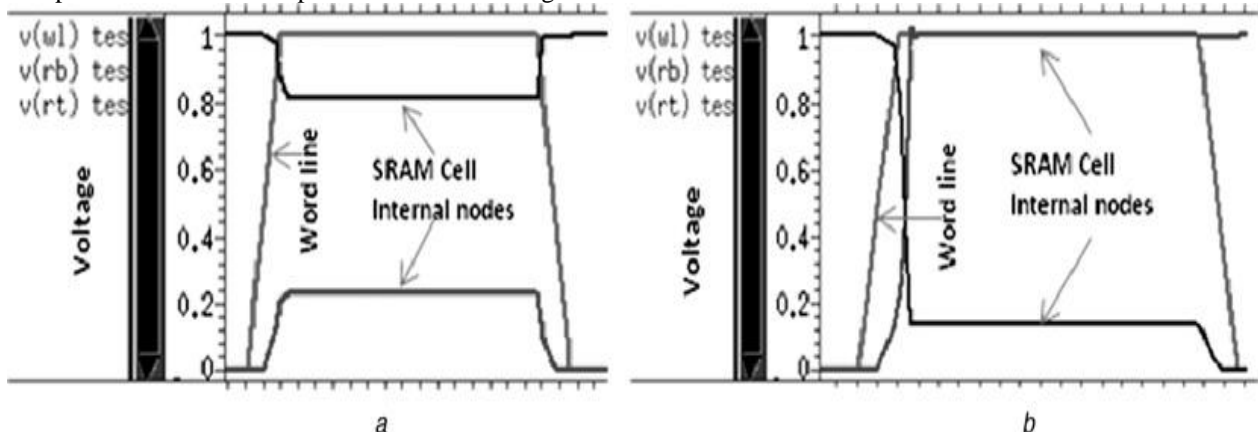

Fig 2: SRAM cell write waveforms (a) Write failure case (b) Correct write operation

Fig 3 shows how the internal nodes (n1 and n2) of a bit cell change when word-line of different pulse widths are applied during the write operation. In Fig 3(a), the pulse width of WL is smaller than the WL_{CRIT} whereas in Figure 3(b), the pulse width of WL is equal to or greater than WL_{CRIT}. In the case of Fig 3(a), the nodes n1 and n2 tend to move towards the other state but they return back to the original state. In Fig 3(b), however, the nodes n1 and n2 are able to move to other stable state. In other words, to have a successful write, $WL \geq WL_{CRIT}$.
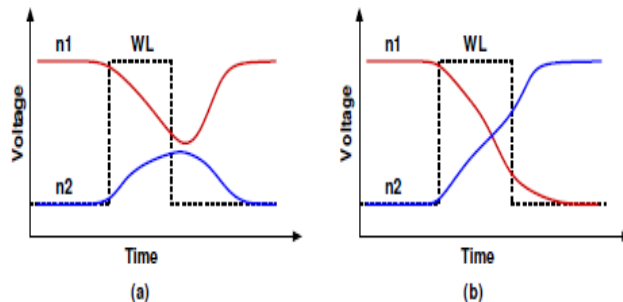

Fig. 3: Internal nodes of a bit cell during write operation (a) WL <WLcrit (b) WL ≥ WLcrit

Write operation in a bi-stable cell (like a bit cell) can be defined as a transition from one equilibrium state to the other. To deal with the write problem in SRAM, many write assist schemes e.g. reduce V_{DD} at cell, raise V_{SS} at cell, WL(word-line) boost, strengthen pass gate NMOS, weaken pull-up PMOS, negative bit-line scheme have been presented earlier out of which WL boost (in which some form of boost to the word line gate voltage is applied) and negative bit- line voltage scheme(in which negative bit-line voltage is applied to increase the gate to source voltage (V_{GS}) of the pass gate device) are two most promising solutions. Fig. 4 shows the WL boost scheme in which voltage higher than the supply voltage is given to the word line which assists the bit cell to flip during a write event.
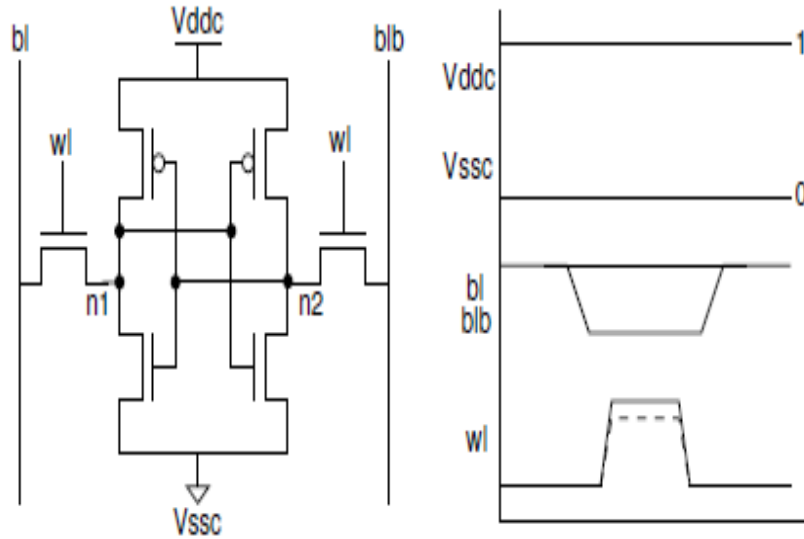

Fig. 4: Write assist using WL boost

The boosting increases the V_{GS} of the access transistor and hence increases its drive strength. The increased drive strength of the access transistor aids significantly in flipping the bit cell. The boost voltage can be routed as a separate power supply or it can be generated internally by a charge pump or by capacitive coupling. WL boost improves write ability by strengthening the pass gate, but hurts stability. The WL_{CRIT} in this case is substantially better than the nominal case with no write assist as shown in fig. 5. The benefits of this write assist scheme increases significantly as the supply voltage is scaled down.
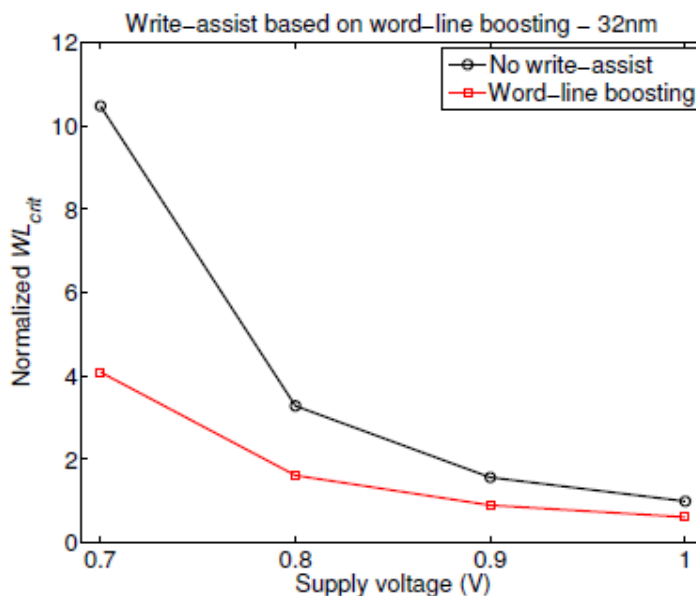

Fig. 5: Normalized WL_{CRIT} for write-assist based on word-line boosting

Fig. 6 shows the waveforms of write operations using negative bit-line scheme in which to create a larger V_{GS} for the NMOS pass transistor, either the gate voltage needs to be increased or the source voltage needs to be decreased. The approach of negative bit-line based write assist swings the bit-line voltage below zero during the write operation. The increase in V_{GS} causes the access transistor to become stronger and hence can flip the bit cell easily. Negative bit-line improves writeability by increasing the V_{GS} on the PG .
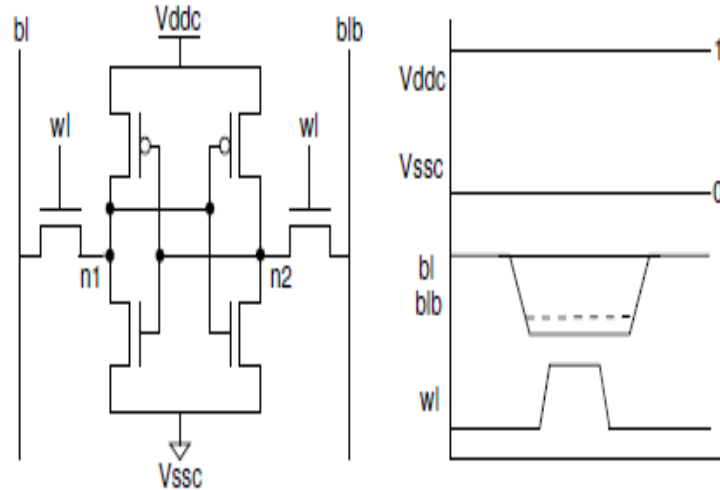
Fig. 6: Write assist using negative bit-line voltage

Simulation results show this as the most effective write assist, because it strengthens both the PG and helps pull the high-node low while also strengthening the low-node PU to complete the write operation. However, by decreasing one of the bit-lines below GND, a non-zero V_{GS} will appear across the PG of unaccessed rows. If the internal node of an unaccessed bit-cell on this side is high, then the value of the cell could flip, causing a write stability error. Similar to the word-line boosting, the negative bit-line voltage can be generated internally using a charge pump technique or using a capacitive coupling technique. Improved Normalized WL_{CRIT} for write-assist based on negative bit line voltage is shown in fig. 7.
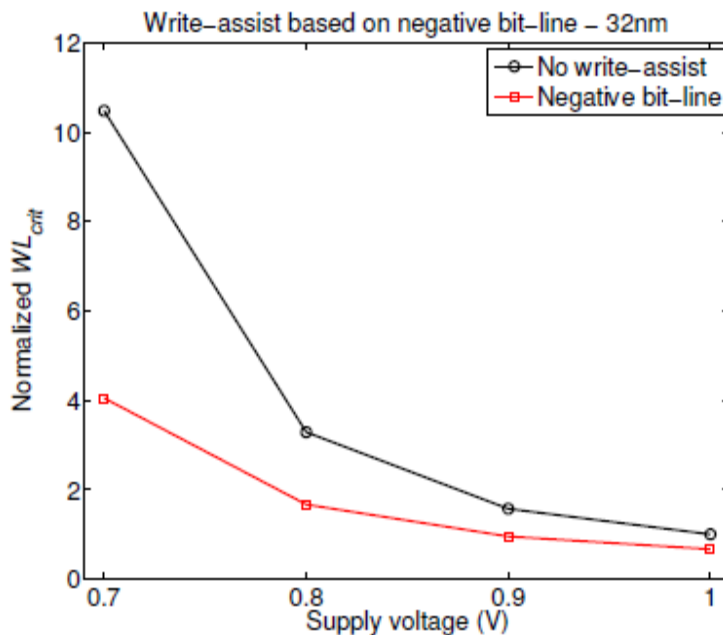
Fig.7: Normalized WL_{CRIT} for write-assist based on negative bit line voltage

Conventional negative bit-line voltage scheme is shown in fig. 8.It consists of a negative voltage generator and control circuit. The source terminals of the write-drivers are connected to this negative voltage line, NBLV.
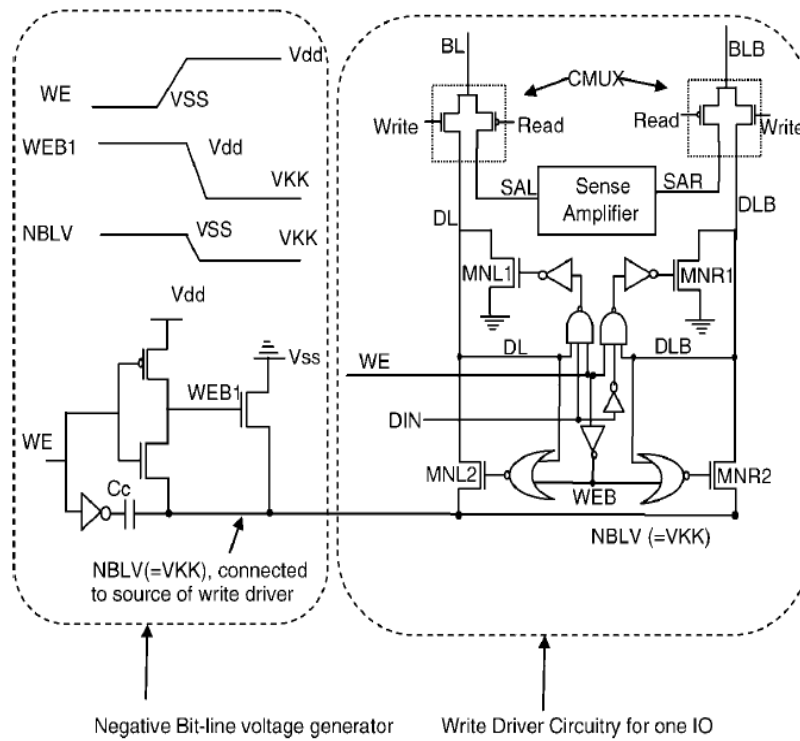
Fig.8: Negative bit-line scheme for write assist in SRAMs

As shown in Fig. 8, the write control circuitry consists of two sets of write drivers (MNL1, MNR1) and (MNL2, MNR2). Both the bit-lines (BL and BLB) are precharged to V_{DD}. Whenever write operation starts, write enable (WE) signal goes high. Depending on the status of write data (DIN), one of the first set of write drivers, MNL1or MNR1, becomes on and pulls the corresponding bit-line to low. During this time the write drivers of second set (MNR2, MNR2) are off as both the bit-lines are precharged. When one of the bit-lines goes low, it disables the first set of write drivers and enables the second set of write drivers (MNL2, MNR2) which finally takes the bit-line to negative voltage VKK (2150 mV). So, the bit-lines go to negative in two steps, first goes to '0' and then negative.

As shown in Fig. 8, there is no loading effect on bit-lines (BL and BLB) or sense amplifier internal nodes (SAL and SAR), because of the additional circuitry. So, there is no loss in read performance. When the bit-line goes to a lower voltage during read operation (V_{DD}-100 mV typically), there cannot be any glitch on the input of second set of write driver as this is gated by write signal. Also the negative voltage on line NBLV is generated when WE signal goes high, so write operation is fast. The negative voltage generator along with waveforms is shown in Fig.8. When WE signal is low, WEB1 signal is high, so NBLV line is pre-discharged to V_{SS}. When WE signal goes high, the coupling capacitor couples the NBLV line to negative voltage, VKK and WEB1 signal also goes to VKK. The circuit switching is lesser in the proposed scheme, so, the dynamic power consumption is also reduced.
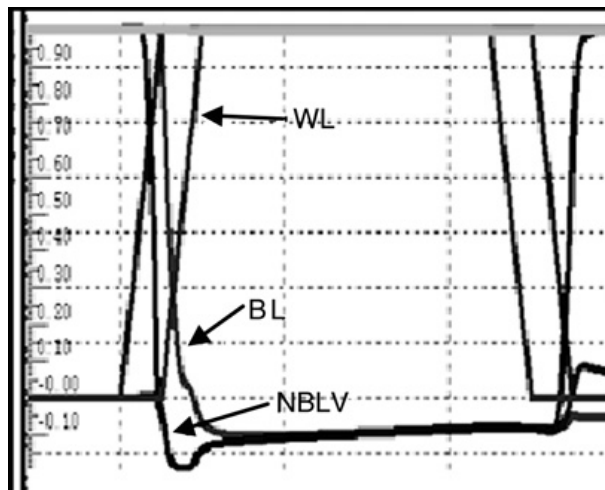

Fig. 9: Write waveforms with conventional NBLV scheme

Negative bit line generator generates a negative voltage spike initially which smoothes down with time as can be shown from fig.9 above. Due to this negative voltage spike, V_{GS} of MLN2 and MNR2 increases which causes the electric field to increase which increases the peak stress and breakdown the dielectric in these transistors. When dielectric of MOS transistors breakdowns, MOSFET get damaged. More the negative voltage peak, more chances of the transistors to get damaged and less will be the reliability of the circuit.

II. PROPOSED HIGH RELIABILITY ASSIST CIRCUITRY FOR SRAM

Proposed high reliability assist scheme is shown in fig.10 below. As we know if more negative voltage peak is generated by negative bit line voltage, less will be reliability of the circuit. To overcome this problem, a capacitor is connected (whose other end is connected to ground) to the output of the NBLV generator which increases the absolute capacitance of the NBLV. This capacitor works as a low pass filter which smoothes out the negative voltage spike. When level of negative voltage spike decreases, V_{GS} of MOSFET reduces which reduces the strength of electric field. Due to low strength of electric field, these will be very low chances of dielectric breakdown and hence less chances of transistors' to get damaged, hence reliability of the circuit is increased.
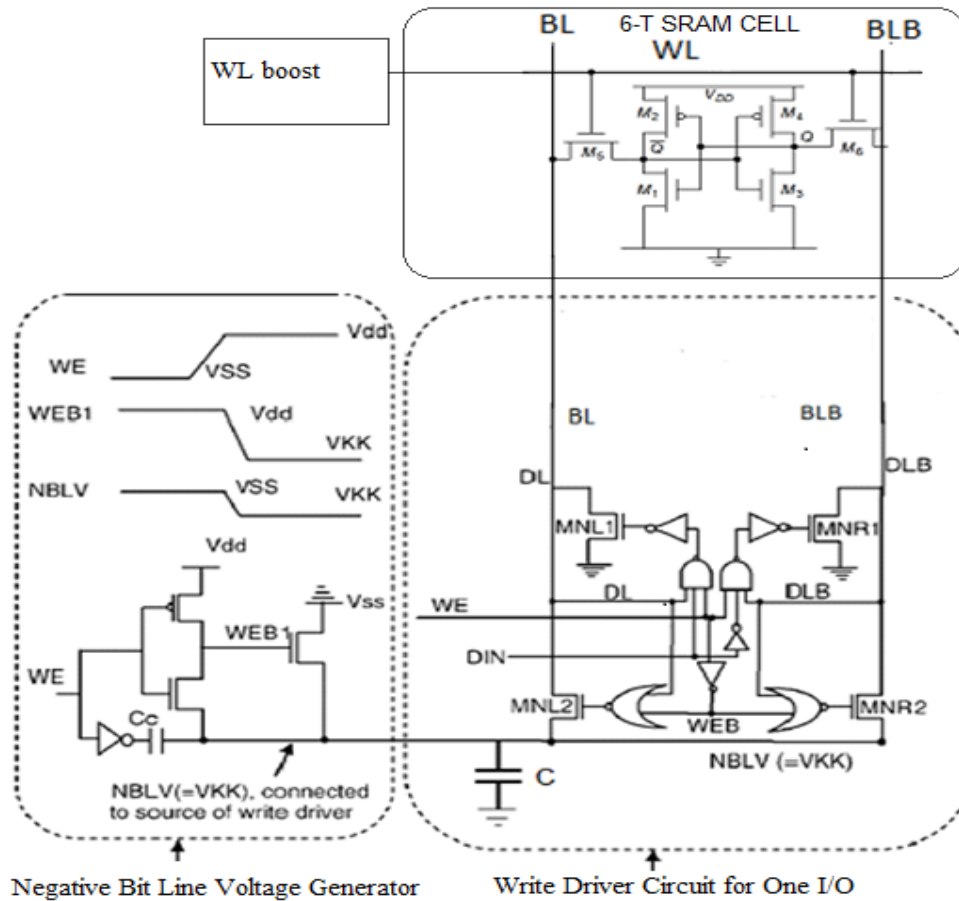

Fig 10: Reliability enhanced write assist circuit

As we have seen that, to increase the reliability of the circuit, level of negative voltage generated by NBLV generator is reduced. But due to this reduced level of negative bit line voltage, the assisting effect of NBLV write assist scheme reduces which may cause the memory to fail. So, this reduced influence of assist circuit needs to be compensated to achieve high write ability and hence high efficiency of the SRAM. This compensation can be achieved by combining another write assist scheme with NBLV write assist scheme. So, we combine the word-line (WL) boost write assist scheme with NBLV write assist scheme. By combining these two schemes together we can achieve high reliability as well as write abilty.

III. SIMULATION RESULTS

Schematic & simulation waveforms of high reliability negative bit-line write assist scheme is shown below in fig.11(a) & 11(b). The proposed scheme is applied to SRAM and the waveforms are shown in fig.11 below. As we can see that nodes 'rb' and 'rt' are flipping successfully with a low level of negative bit line voltage as compared to voltage in conventional negative bit line voltage scheme. Because of this reduced level of negative bit line voltage, peak stress on transistors decreases and reliability of the circuit increases.
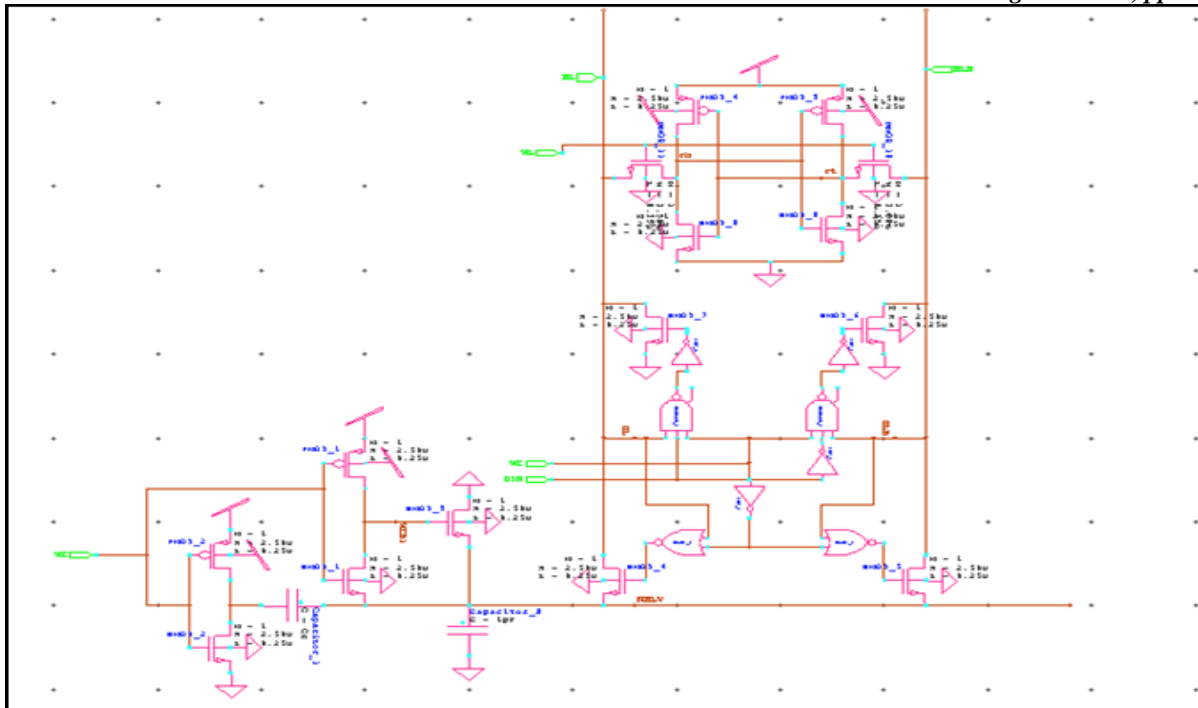
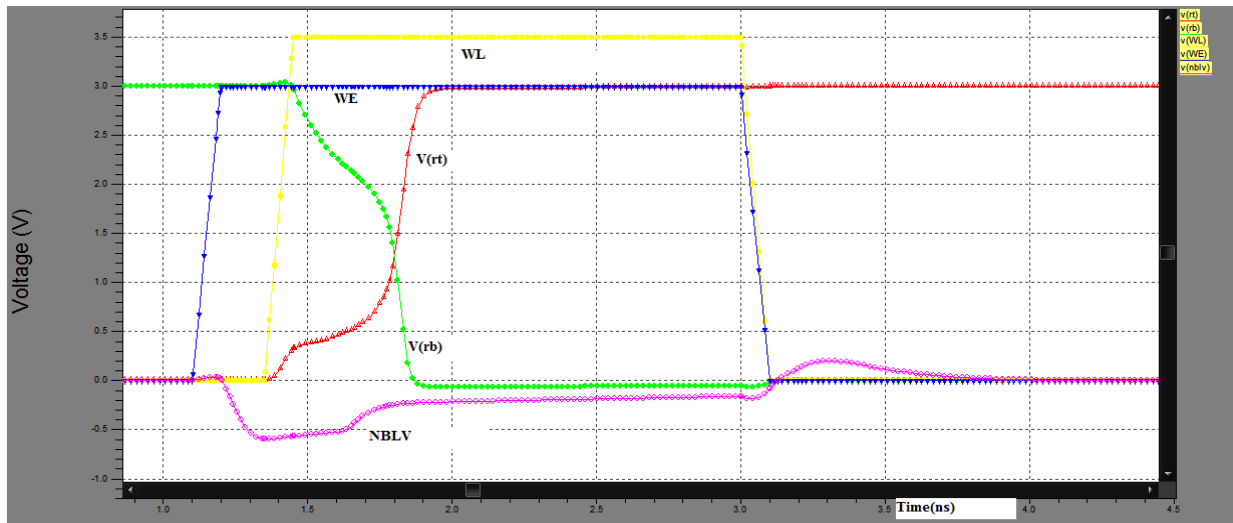Fig.11(a):Schematic of high reliability negative bit-line write assist scheme

Fig.11(b): Waveforms with proposed write assist scheme

IV. Conclusion

Write assist is very important to achieve good yield in SRAM memories. In this project work, the conventional assist techniques have been studied and a new write assist is presented which offers high reliability in SRAMs. To minimize the peak negative voltage at bit-line, the negative bit-line voltage scheme is combined with WL boost technique which increases the write-ability of the memory without overstressing the transistors. The merits of the proposed technique were illustrated using simulation results.

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