Interleaved SRAM Read Stability Assist Techniques

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I. Project Proposal

The 6T SRAM cell is the most commonly used architecture due to its simplicity and area efficiency. With technology scaling, the ultimate goal is to reduce the supply voltage of the SRAM along with that of logic circuits. To achieve lower supply voltages, however, bit cell assist techniques are required to solve 3 problems: readability, writability and stability. However, some readability and writability assist techniques like word line (WL) boost and negative bit line actually hurt cell stability. To alleviate this problem we will explore some novel SRAM bit cell and array architectures that enable readability and writability assist techniques to be implemented without harming cell stability.

In an interleaved SRAM, half-selected bit cells are prone to stability issues since the WL is on, leaving an open pass gate (PG). One of the solutions to this problem is to control the WL signals for each column. If we have 4-interleaved cells, we can use 4 WLs in each row and drive only the cells of interest (Fig. 1). Each WL will then drive only a quarter of the cells in the row, driving less capacitance; however, the area opportunity cost might be significant and has to be evaluated. Another solution is to add a WL pass gate controlled by a column enable signal; this will only provide a high WL signal to PGs of the relevant cells (Fig. 2). A similar effect can be done by controlling a column PG by the WL (Fig. 3). These last two approaches only add a vertical line to each column but they require better control over the timing of the arriving signals CE and WL, so it might incur area penalties in the peripheral circuit. We will explore a combination of these techniques and how well they interact with common bit cell assist techniques such as WL boost.

To evaluate these read stability assist techniques, we will examine the static noise margin (SNM), write margin, minimum supply voltage, leakage, and power consumption. We will also examine the overhead of these assist techniques in terms of area and extra peripheral logic.

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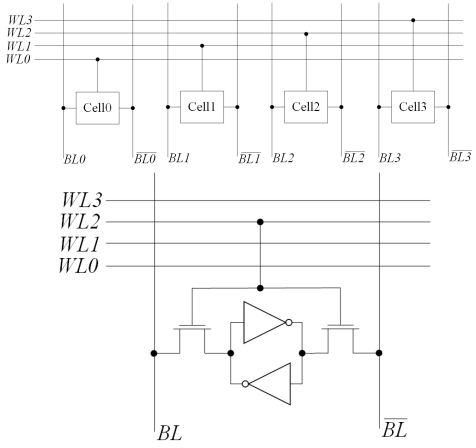

Fig. 1. Multiple word line per row

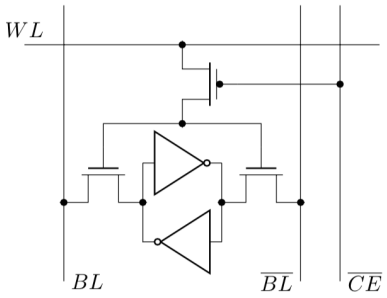

Fig. 2. Column-controlled word line

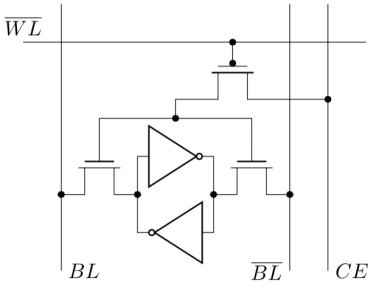

Fig. 3. Word-line-controlled PG

References

[1] B. Zimmer, S. O. Toh, H. Vo, Y. Lee, O. Thomas, K. Asanović, and B. Nikolić, "SRAM Assist Techniques for Operation in a Wide Voltage Range in 28-nm CMOS," *IEEE Transactions on Circuits and Systems*, vol. 59, no. 12, pp.853-857, Dec. 2012.