Chapter 2
SRAM Bit Cell Optimization

This chapter discusses different SRAM bit cell topologies. This chapter first provides an overview of the conventional SRAM 6T cell and its limitations. Then different SRAM cell topologies are discussed which offers better stability margins compared to 6T SRAM cell. Different cell topologies discussed are broadly categorized as 7T, 8T, and 10T. It also classifies SRAM cells based on single ended and differential sensing. Finally, the chapter concludes with a summary of different SRAM cells topologies.

2.1 Introduction

The usage of SRAM is continuously increasing in system-on-chip (SOC) designs. Process technology scaling has contributed remarkably in improving the performance of and area density of SOC. The SRAM cell typically utilizes the minimum sized transistor in order to realize a high density. With the result impact of increased intra die variations with the technology scaling is more pronounced on the SRAM cells. With the result SRAM scaling has become extremely difficult in the advanced technology nodes (e.g., 65, 40, or 32 nm LP CMOS technology).

The lowest operational VDD (VDDmin) for embedded memories (SRAM) is limited by either SNMread (cell stability) or write ability [write margin (WM)]. SRAM bit cell functional parameter degradation due to increasing variability and decreasing power supply is of utmost concern. The random threshold variations in subnanometer technologies have resulted in serious yield issues for realizing low VDD READ/WRITE operations with a 6T SRAM cell. Figure 2.1 shows 6T SRAM cell diagram. It relies on rationed operation to achieve the required functionality. The area of an SRAM cell is very important because the cell area contributes significantly to the silicon area. For instance, SRAM L1 caches occupy a significant portion of many designs. The minimum sized 6T cell in 65 nm

V. Sharma et al., *SRAM Design for Wireless Sensor Networks*,
Analog Circuits and Signal Processing, DOI: 10.1007/978-1-4614-4039-0_2,

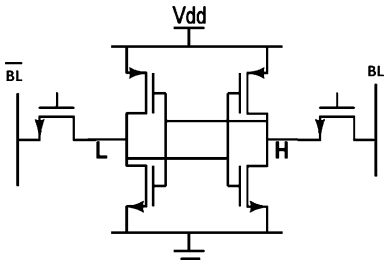

Fig. 2.1 6T SRAM cell

occupies 0.4 μm^2 (Utsumi et al. 2005), in the 40 nm 0.33 μm^2 (Yabuuchi et al. 2007), and in the 32 nm 0.124 μm^2 (Chang et al. 2005).

Impact of Process Variations

As the SRAM cell is scaled, it is difficult to ensure cell stability. For low VDD values, the read SNM becomes negative (loss of bistability). This is because of the reduced signal levels at the low VDD levels and also because of the impact of Vt variations. SRAM cell design can be optimized to minimize the impact of Vt variation on SNMread. The SRAM cell beta ratio is defined as the (W/L) of NMOS pull down transistors of inverter to the (W/L) of nMOS pass transistors. The cell beta ratio balances performance and stability. For stability, increasing the beta reduces the risk of data flip during the READ operation. However, for performance stronger pass transistor is desired. The conventional 6T SRAM cell topology has an inherent disadvantage that it requires a very complex tradeoff between stability (SNMread) and performance (Iread). The higher value of beta favors cell stability but has a negative impact on Iread. Similarly, lower value of beta increases Iread but also increases the risk of data flips (less stable).

There is another problem of write ability, causing write failures in the SRAM cell. A failure to write occurs when the pass transistor is not strong enough to overpower the pull-up PMOS and pull the internal node to ground (writing "0"). The increased strength of pull up PMOS transistors or the decreased strength of NMOS pass transistors due to the process variations impedes the discharge process through the pass transistor. Furthermore, process variations also reduce the trip point of inverter holding the state "H", resulting in the write failure. The current ratio between the pull up PMOS transistors and the pass access NMOS transistors determines the WM. The successful WRITE operation is achieved by increasing the strength of the write access NMOS pass transistors or by decreasing the strength of the pull up PMOS transistors.

Figure 2.2 shows SNMread versus WM for a 6T cell under different PVT conditions. Utilizing high Vt transistors for SRAM cells increase the cell stability but has an adverse impact on the WM. Similarly, low Vt transistors for SRAM cells improve the WM but results in lower stability. Utilizing a high Vt cell decreases the WM by 14 % and low Vt transistors result in the 36 % degradation of cell

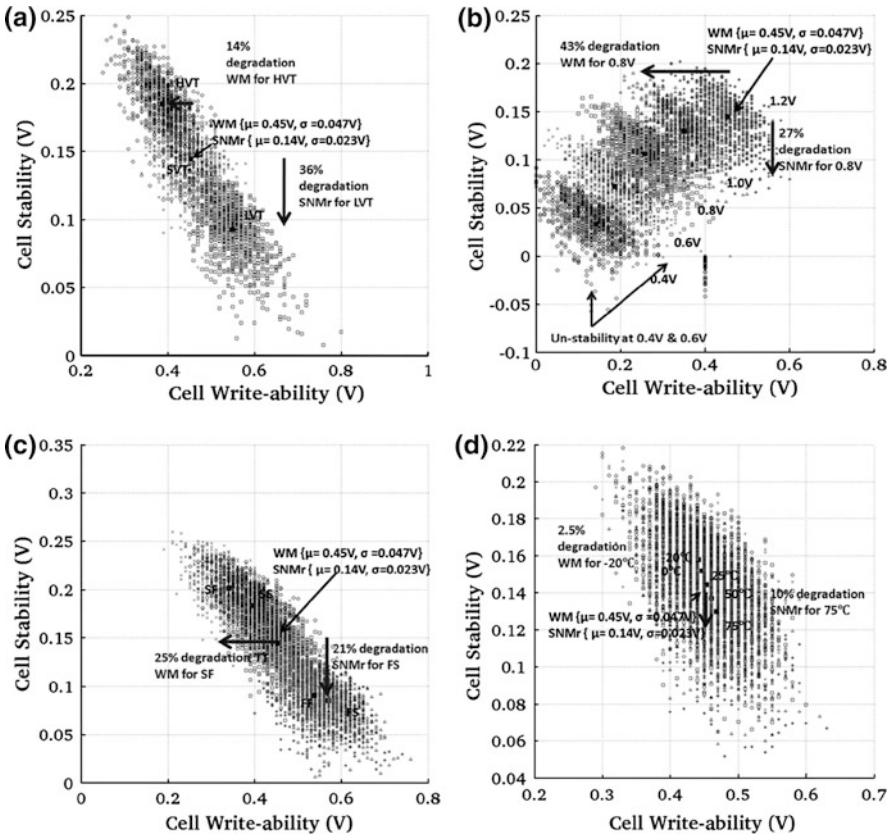

Fig. 2.2 6T cell, 65 nm LP technology, minimum sized SRAM cell. **a** Vt variation. **b** VDD variation for standard Vt 6T cell. **c** Process variation for standard Vt 6T cell. **d** Temp variation for standard Vt 6T cell

stability. Scaling VDD has an adverse impact on both cell stability and WM as explained above because of the increased impact of Vt variations. Regarding inter die variations (considering process corners), slow NMOS (weak pass transistor) and fast PMOS (strong pull up transistor) is the most difficult situation for write ability. This result in 25 % degradation in the WM compared to the nominal process corner. Similarly, from SNMread perspective fast NMOS and slow PMOS results in 21 % degradation in the cell stability. Increasing temperature reduces the Vt of NMOS transistors thereby resulting in reduced cell stability (NMOS pass transistor and NMOS pull down low Vt scenario) by 10 % compared to the nominal temperature.

Similarly, reducing the temperature increases the Vt for NMOS transistors (weak NMOS access transistor) and it results in 2.5 % degradation in WM.

Figure 2.3 shows Iread versus leakage for 6T cell under different PVT conditions. Reducing VDD results in 2.67 orders of magnitude reduction in Iread

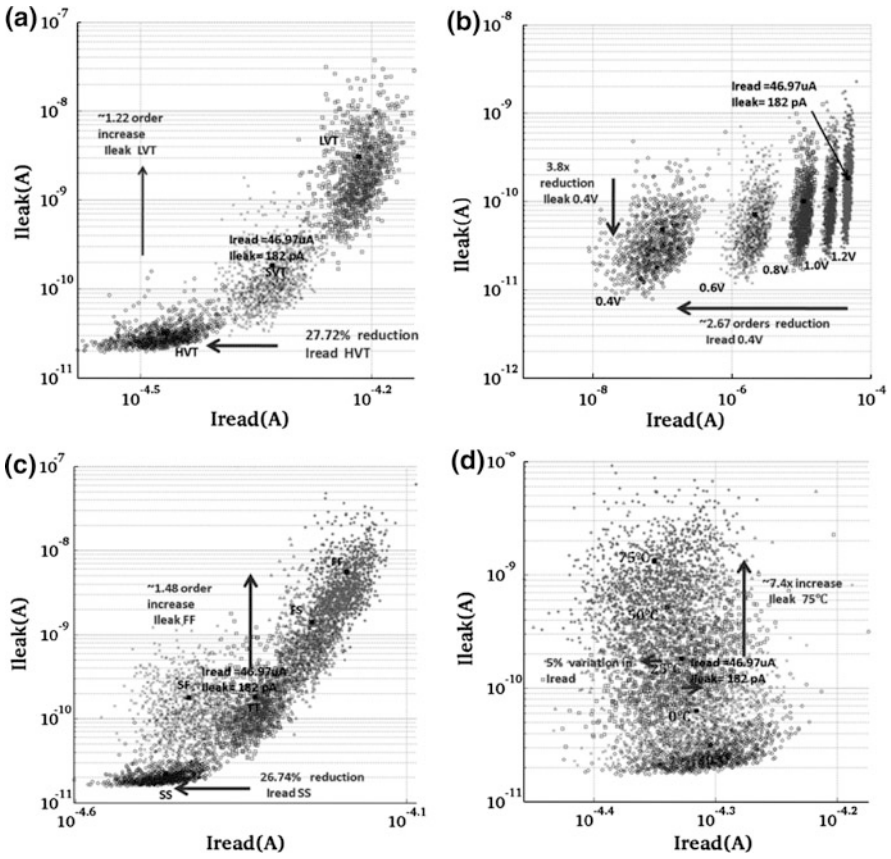

Fig. 2.3 6T cell, 65 nm LP technology, minimum sized SRAM cell. **a** Vt variation. **b** VDD variation for standard Vt 6T cell. **c** Process variation for standard Vt 6T cell. **d** Temp variation for standard Vt 6T cell

at 0.4 V compared to 1.2 V for SRAM 6T cell at 65 nm LP technology node. This serious degradation of Iread at low VDD levels makes SRAM 6T cell less attractive for low VDD applications. The combination of variation on top of dramatically reduced mean Iread means that the read access time is very high, thereby making it less suitable for low VDD applications.

2.2 Different Cell Topologies

This section describes different SRAM cell topologies which solves the issues like degraded SNMread, Iread, WM with 6T SRAM cell for realizing low VDD SRAM.

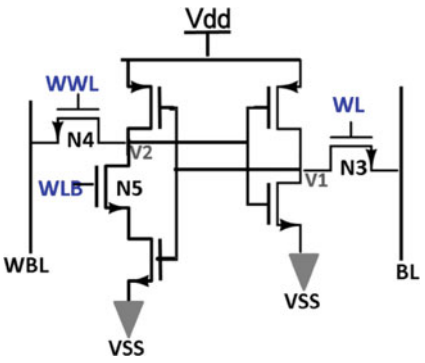

Fig. 2.4 SNMr free 7T cell

2.2.1 Read SNM Free (RSNF) 7T Cell

A transistor N5 is inserted into the 6T cell structure for loop cutting (Fig. 2.4) (Takeda et al. 2006). It enables differential WRITE operation and single ended READ operation. During an idle state when the cell is not accessed WLB is high and the data retention process is exactly same as that of 6T cell. During READ operation WLB is deactivated, the logical threshold voltage of the CMOS inverter driving Node V2 becomes very high (Takeda et al. 2006). Therefore, the SNMread value at V1 = "0" becomes large no matter with the N3 pass transistor activate and increased voltage at node V1. It is difficult to quantify the SNMread with static analysis methods. There is no information provided on how the authors obtained butterfly curves for the read operation. The test chip (Takeda et al. 2006) of 64 Kb RSNF 7T cell macro in 90 nm obtains VDDmin of 0.44 V and 20 ns access time at 0.5 V.

2.2.2 Differential Data Aware Power-Supplied (D^2AP) 8T SRAM Cell: Improved Write Margin and Half-Select Accesses

Figure 2.5 shows the D^2AP-8T SRAM cell (Chang et al. 2009a). The basic structure is similar to the 6T SRAM cell, except it is powered by its bit-line pair (PSWL and PSWR). During the hold mode the bitlines are kept VDD precharged. The PMOS switches (PSWL and PSWR) are kept ON (ZWL = 0) to power the PUL and PUR of the cross-coupled inverters (invL and invR) from the bit-line pair. The application of differential data-aware (powered by bitlines) voltages to the cross-coupled inverters improve the WM and enlarge the stability margins for half select accesses.

During WRITE operation, the BL is pulled to VSS (writing "0") and BL bar is kept at VDD. The header PMOS switches PSWL and PSWR are ON, the source of invL is reduced (BL pulled to VSS). The trip point of invL becomes lower because of the reduced strength of PMOS transistor of invL. The source voltage of PMOS transistor of invR is at VDD enabling a faster pull up for the complementary node.

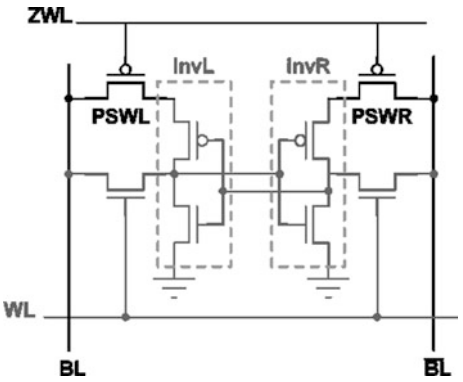

Fig. 2.5 D^2AP-8T cell

The negative feedback mechanism increases the stability margin for half select accesses. Regarding half select condition immunity of the inactivated cells on the asserted word line. If the storage node Q rises being connected with BL and QB is dropped. Then automatically due to the lowering of the BL, it becomes difficult for invL to flip. The READ operation of this cell is similar to the 6T SRAM cell. This cell relies on the boosted bit-line voltage (discussed in Chap. 3) for increasing read cell current and the read static noise margin, especially at lower voltages.

The test chip (Chang et al. 2009a) of 39 Kb SRAM macro featuring D^2AP-8T SRAM cell is fabricated in 40 nm LP CMOS technology. The measured VDDmin of the D^2AP-8T macro is 540 mV. Figure 2.6 shows WM versus VDD for D^2AP-8T and 6T cell at nominal process corner. There are number of issues with D^2AP-8T SRAM cell. The PMOS switches (PSWL and PSWR) of the unselected D^2AP-8T cells on the accessed column are temporarily turned off to isolate the storage nodes from BL during the short BL switching period which increases the risk of data retention. Secondly, the bitlines are kept precharged to VDD (required for powering the inverters of the SRAM cell), increases the stand by leakage power consumption.

2.2.3 Half Select Condition Free Cross Point 8T (CR8T) SRAM Cell

The cross point 8T-SRAM provides two additional access transistor compared to the conventional 6T SRAM cell. It has four access transistors for the Y-address controls as well as the X-address (Fig. 2.7). These access transistors are controlled by the horizontal word line (WLH) and the vertical word line (WLV) signals. For the accessed SRAM cells, both WLH and WLV signals are activated and the internal storage nodes are exposed to the bitlines. For the un-accessed SRAM cells either on the activated column or on the activated row only the WLV is activated or the WLH is activated with the result that internal storage nodes are never exposed to the bit-line information. This is how the half select condition is

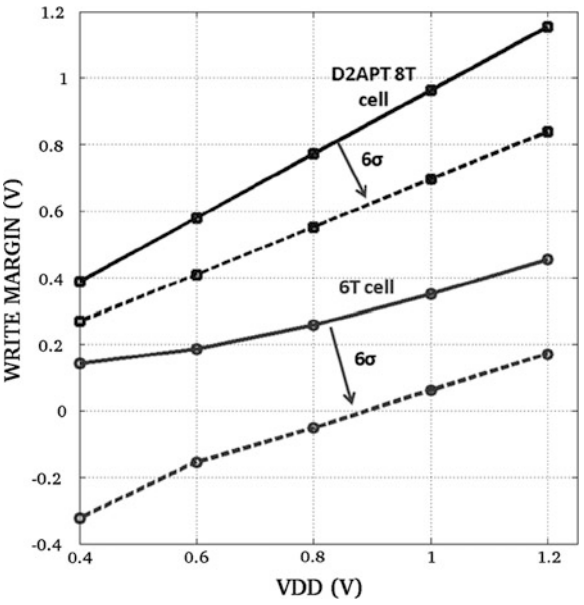

Fig. 2.6 WM versus VDD for 6T SRAM cell and D^2APT 8T SRAM cell in 65 nm LP technology node, nominal process corner, and 25 °C. WM is negative below VDD of 0.9 V for SRAM 6T cell, whereas D^2APT results in positive WM even for 0.4 V

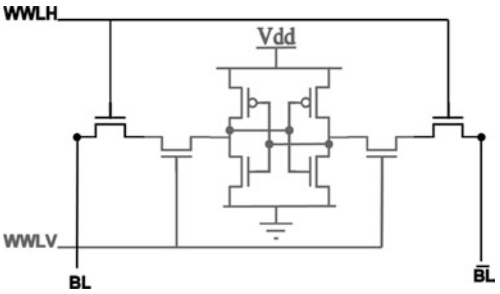

Fig. 2.7 CR8T cell

eliminated. The presence of two NMOS series access transistor also improves the SNMread; it results in 64.3 % improvement in SNMread compared to the same sized 6T SRAM cell. However, two series access transistor results in 44.44 % degradation in the WM and 29.87 % degradation in the cell read current compared to the 6T SRAM cell (Yabuuchi et al. 2009).

The degradation in the cell read current and the WM is addressed by using voltage optimization techniques discussed in Chap. 3. The test chip featuring 1 Mb CR8T SRAM cell along with the negative VSS and the negative bit-line technique achieves VDDmin of 0.6 V in 45 nm LP technology. The negative VSS technique used for the read operation improves read access time by 8.61 ns at 0.6 V and the negative BL technique proposed improves writeability. Figure 2.8 shows SNM-read versus WM for different PVT conditions.

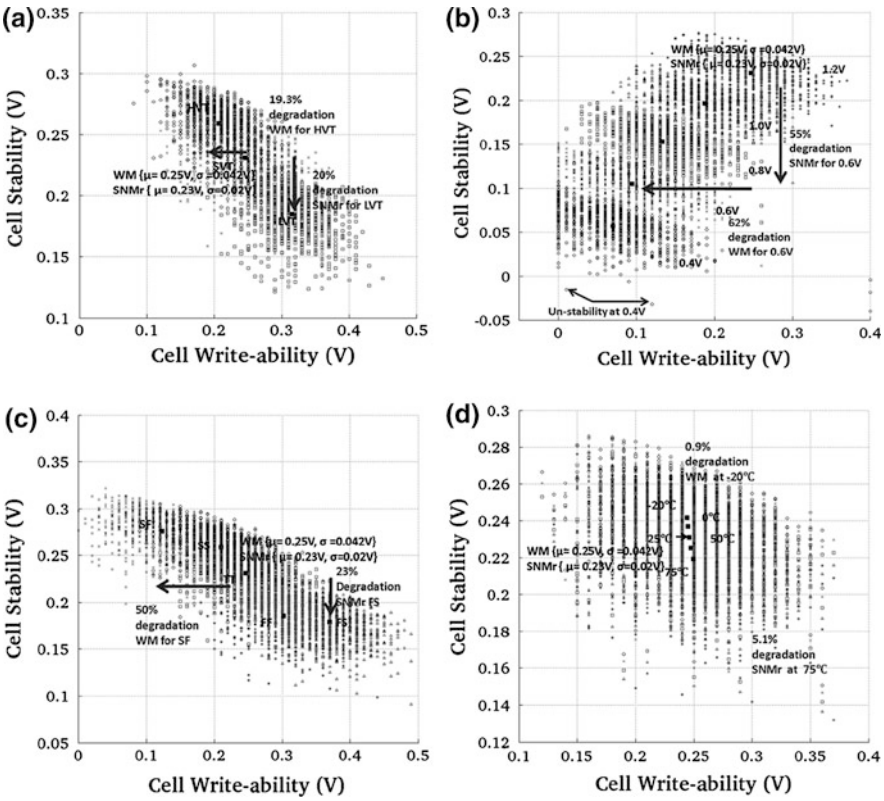

Fig. 2.8 CR8T cell, 65 nm LP technology, minimum sized SRAM cell. **a** Vt variation. **b** VDD variation for standard Vt CR8T cell. **c** Process variation for standard Vt CR8T cell. **d** Temp variation for standard Vt CR8T cell

2.2.4 Read Decoupled 8T and 10T Cell (Isolation of the Internal Storage Nodes from the Read Bit-Lines)

The worst case SNMread in the conventional 6T SRAM cell becomes extremely small with the reduction of the supply voltage refers to Fig. 2.2. With the result 6T SRAM cell cannot be used for the low voltage operations as discussed earlier. This section will discuss different SRAM cells which decouples the cell node from the read bit line by using additional read port transistors. This isolation results in a SNMread equal to the SNMhold (Fig. 2.9).

1. Read decoupled (RD) 8T SRAM cell (Chang et al. 2008)

Figure 2.10 shows RD 8T cell. The structure is similar to the 6T cell except that the two transistors (read stack) are added to a conventional 6T cell. There are separate write and read ports. The word line of the 6T structure is used only during the WRITE operation. Similarly, the word line of the read stack transistors is used

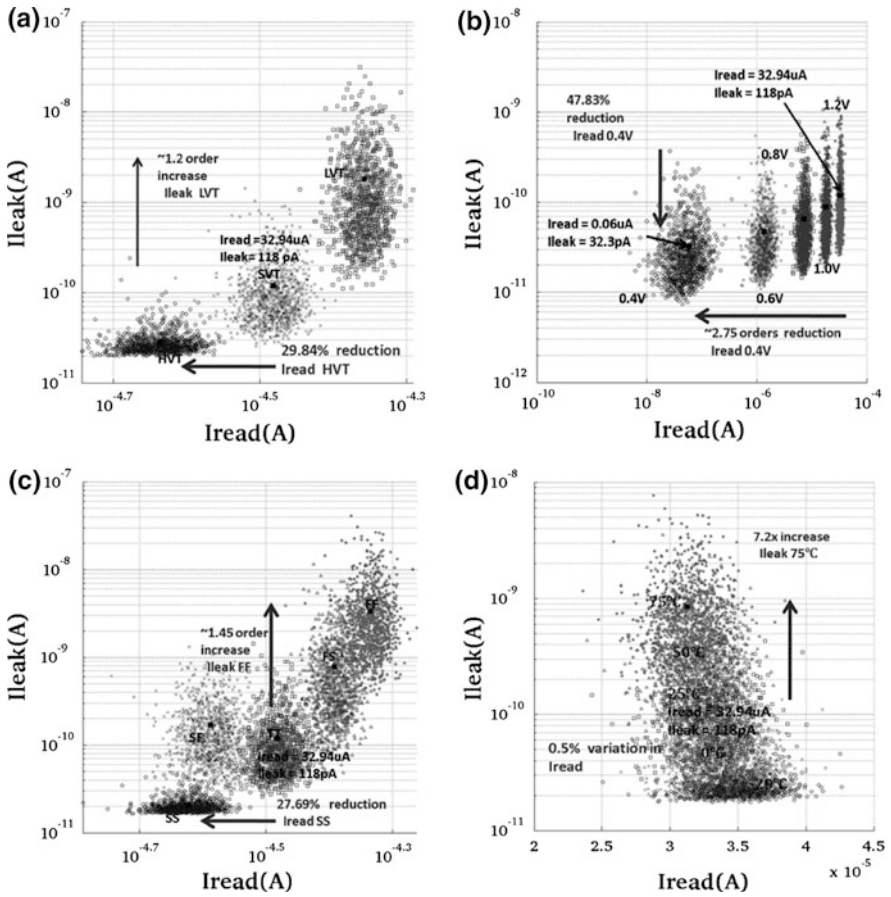

Fig. 2.9 CR8T cell, 65 nm LP technology, minimum sized SRAM cell. **a** Vt variation. **b** VDD variation for standard Vt CR8T cell. **c** Process variation for standard Vt CR8T cell. **d** Temp variation for standard Vt CR8T cell

only for the READ operation. The read word line (RWL) runs parallel to the write word line (WWL). The decoupled read ports eliminate bit-line charge sharing with SRAM internal storage nodes. It avoids read disturb issue for the activated word line. In other words, hold SNM of cell is same as the SNM read. The area overhead of RD-8T SRAM cell is 30 % compared to the 6T SRAM cell (Chang et al. 2008).

The worst case SNMread of RD 8T cell is $\sim 2.1\times$ compared to the SRAM 6T cell SNMread at VDD = 1.2 V. Further, the WM can be improved by increasing the strength of the pass transistors of the write port. The read performance Iread, cell is determined by the strength of the read stack transistors. In this analysis the transistor sizes are kept same (minimum sized); therefore, the WM values are in the same order as that of the SRAM 6T cell. Figure 2.11 shows SNMread versus WM for different PVT conditions. The RD 8T SRAM cell is more suitable for low

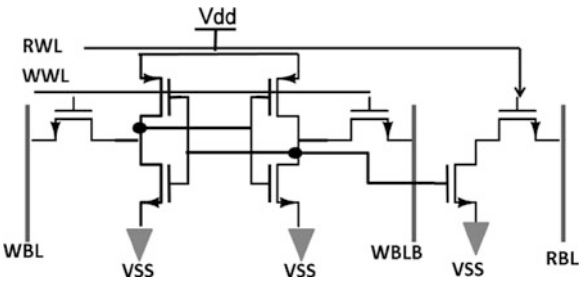

Fig. 2.10 RD 8T cell

VDD applications. The degradation in Iread cell with reducing voltage level is much less compared to that of the 6T cell. The Iread, cell of RD 8T cell is 10.98 and 18.19 uA at 0.4 and 0.6 V compared to the 0.1 and 2.18 uA for the SRAM 6T cell. Figure 2.12 and Iread, cell versus leakage for different PVT conditions. The test chip (Chang et al. 2008) macro of 32 Kb RD 8T SRAM macro in 65 nm operates at 295 MHz at VDDmin of 0.41 V. This high performance is also because of the divided bit-line architecture used in the test chip (discussed in Chap. 4).

2. Data independent bit-line leakage (DIL) 10T cell (Calhoun et al. 2006; Kim et al. 2007)

The single ended READ operation with RD 8T SRAM cell results in a data dependent bit-line leakage. For the worst case scenario (stored value Q = "L", voltage drop across pass device of the read port) the increase in leakage can be as high as 30 %. This problem is remedied by eliminating voltage drop across the pass transistor of the read port irrespective of the value of the data stored for the un-accessed SRAM cells.

The node QBB is actively driven high when QB is low and when QB is high, the value at the node QBB is set by the relative leakage currents of M9 and M10 (Fig. 2.13). The threshold voltage of M9 is taken to be lower compared to the NMOS devices M10 and M7. With the result leakage current of M9 is higher compared to the NMOS M10 device and the node QBB approach to VDD. This is how the voltage drop across M8 pass transistor of the read port for the un-accessed SRAM cells remains zero irrespective of the stored value QB. However, this structure is less robust for the skewed process corners where the PMOS strength is less compared to the NMOS strength.

The DIL 10T cell (Kim et al. 2007) (Fig. 2.14) provides a more variability resilient solution. The node A (QBB) is actively driven high independent of the stored data value by turning ON PMOS transistor M10 for un-accessed SRAM cells. The DIL 10T cell results in 55.5× reduction in the bit-line leakage for the same value of the cell read current. The test chip of 480 kb DIL 10T cells in 130 nm technology achieves VDDmin of 0.2 V operating at 120 kHz. The test chip (Calhoun et al. 2006) of 256 kb 10T cells in 65 nm technology achieves VDDmin of 0.4 V operating at 475 kHz. However, the area overhead with read decoupled 10T cells is extremely high (Fig. 2.15).

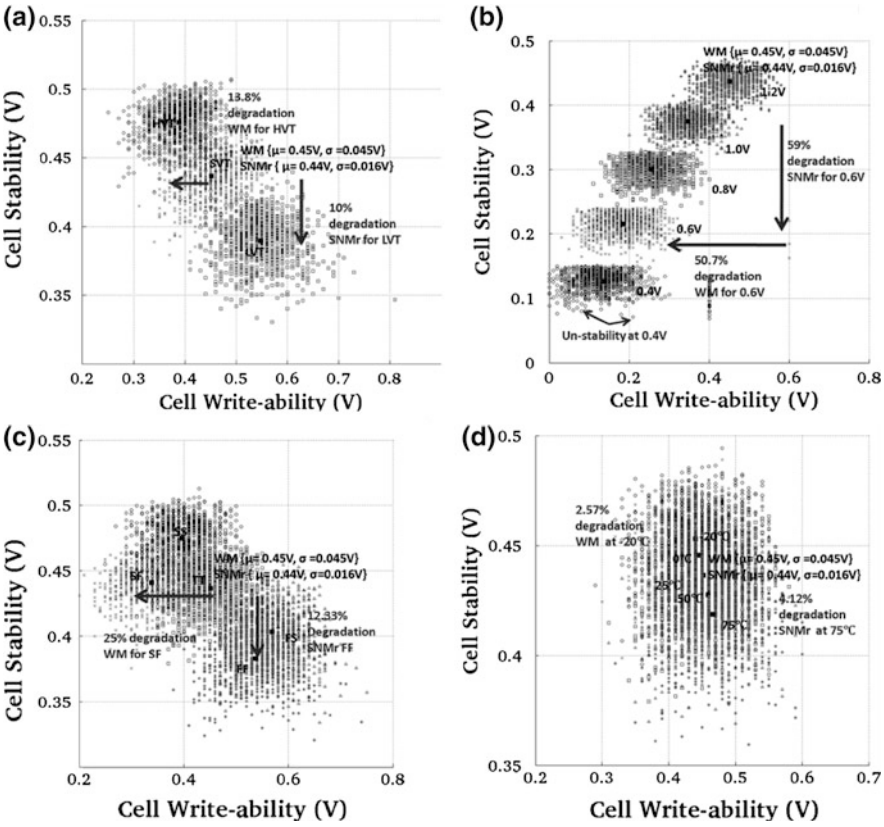

Fig. 2.11 RD8T cell, 65 nm LP technology, minimum sized SRAM cell. **a** Vt variation. **b** VDD variation for standard Vt RD8T cell. **c** Process variation for standard Vt RD8T cell. **d** Temp variation for standard Vt RD8T cell

3. Reduced Swing Dual Vt (RSDVt) 8T SRAM Cell (Sharma et al. 2011b)

Traditional 8T SRAM cells decouple the read port from the internal nodes, thereby eliminating the risk of instability during the read operation. The cell has separate read and WWLs, as well as separate read and write bitlines. The read port consists of two stacked NMOS transistors which deliver the cell read current (I_{READ}) when the RWL is asserted. The two stacked NMOS transistors introduce an additional data dependent leakage path. For the worst-case data pattern, cell leakage increases by 30 % compared to the 6T cell. The cell leakage can be reduced drastically by using HVT devices in the cell. However, using HVT transistors in the read path of the cell reduces the I_{READ}. The degradation in I_{READ} is further aggravated by the ever increasing V_T mismatch, as well as to process and temperature variations. The time required for the development of the bit-line voltage difference increases with decreasing I_{READ}, which directly increases the read access time.

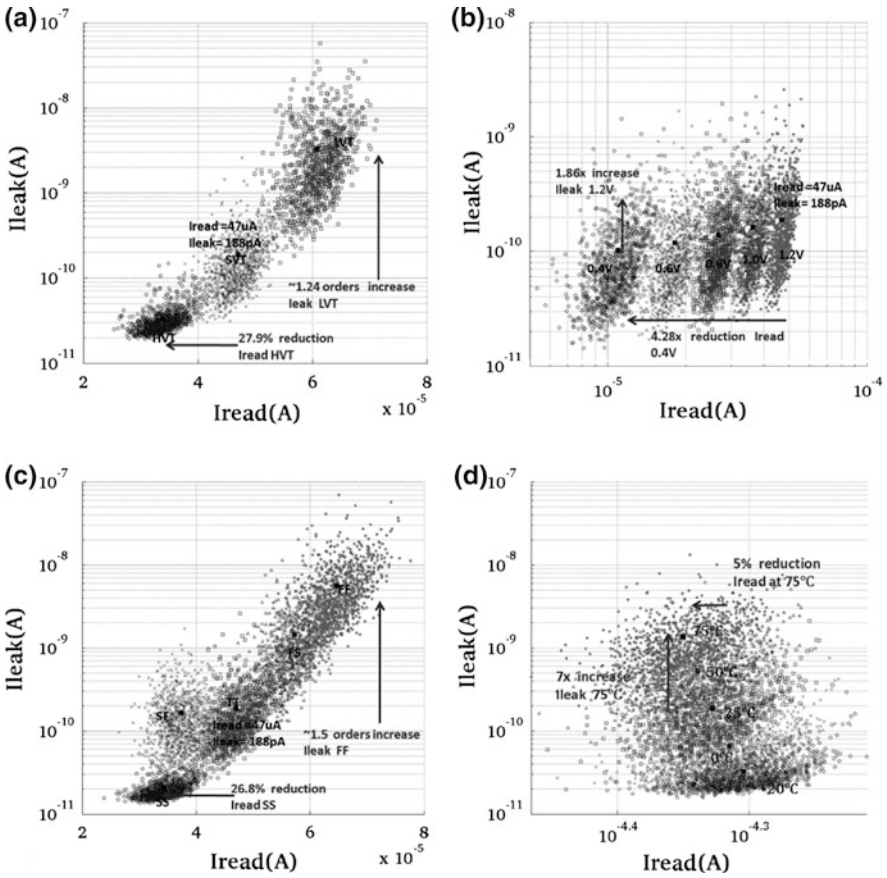

Fig. 2.12 RD8T cell, 65 nm LP technology, minimum sized SRAM cell. **a** Vt variation. **b** VDD variation for standard Vt RD8T cell. **c** Process variation for standard Vt RD8T cell. **d** Temp variation for standard Vt RD8T cell

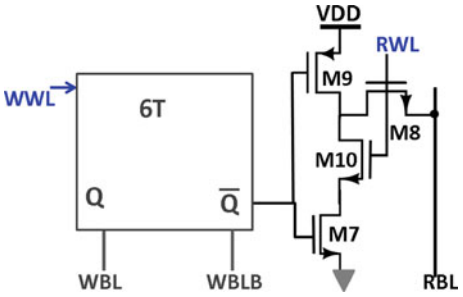

Fig. 2.13 10T cell (Calhoun et al. 2006)

Dual Vt 8T SRAM cell. HVT transistors are used for the 6T part of the cell (the cross-coupled invertors and the write access transistors). This results in a large reduction in the leakage current, as the cross-coupled inverters and the write access

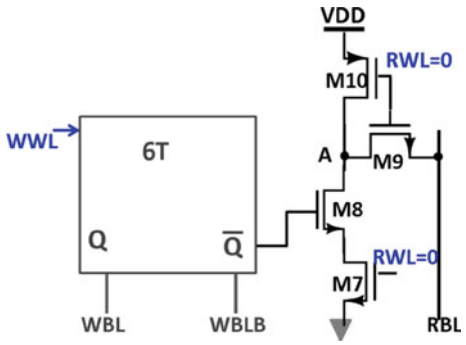

Fig. 2.14 DIL 10T cell (Kim et al. 2007)

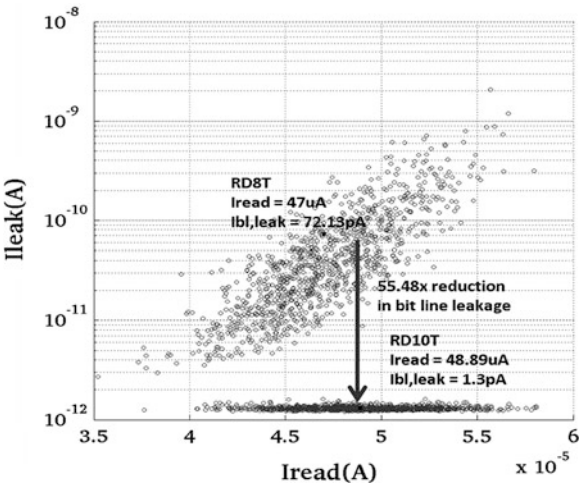

Fig. 2.15 Bit-line leakage reduction with DIL 10T cell (Kim et al. 2007) in 65 nm at VDD = 1.2 V

transistors contribute 70 % of the leakage. The two stacked NMOS transistors (read buffer) determine the read access time. To meet the target performance requirements, SVT transistors are used for the read port.

Reduced Swing Dual Vt 8T SRAM cell (Fig. 2.16). Leakage is further reduced by reducing the read bit-line precharge voltage. In a traditional 6T cell, the bit-line precharge voltage cannot be reduced below VDD-Vt as this increases the risk of read instability. Due to the isolation of the internal storage node from the read bitline, 8T cells do not suffer from this issue, hence a lower read bit-line voltage of 0.2 V is used in this design. The lower drain-to-source voltage reduces the bit-line leakage current because of the reduced drain-induced barrier lowering (DIBL).

The reduced read bit-line precharge voltage (0.2 V) further reduces the leakage current on the read bitline with 3.5× in case of the worst data pattern (Q = "H" for all nonselected cells). Using a low precharge voltage on the read bitline also reduces the dynamic energy consumption discussed in Chap. 5. The dual Vt 8T SRAM cell with 0.2 V read bit-line precharge voltage consumes only 20 % more leakage current compared with the VDD precharged read bit-line single Vt HVT

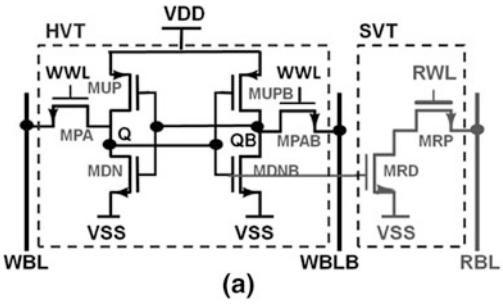

TABLE I
Normalized dual Vt 8T sizing

Pull-up	(W_{MUP} / L_{MUP})	1.25/1
Pull-down	(W_{MDN} / L_{MDN})	1.25/1
Pass-gate	(W_{MPA} / L_{MPA})	1.25/1
Read Pull-down	(W_{MRD} / L_{MRD})	2/1
Read Pass-gate	(W_{MRP} / L_{MRP})	1.25/1

(b)

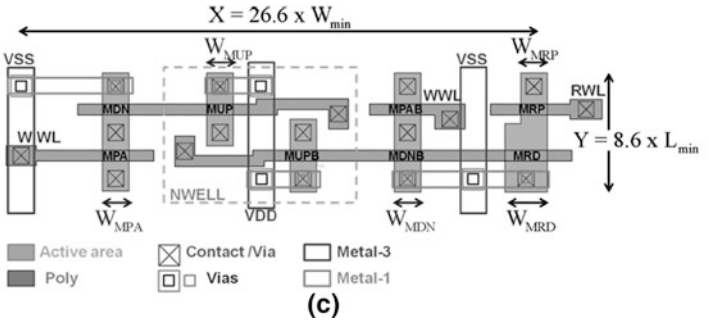

Fig. 2.16 Reduced swing dual Vt 8T SRAM cell. **a** Schematic (HVT write structure and SVT read buffer RB). **b** Table for normalized sizing of dual Vt 8T cell transistors. **c** Layout with power routing of low swing dual Vt 8T cell

8T SRAM cell and delivers 45 % more read current. For a given bit-line swing, a lower read bit-line precharge voltage also increases the resilience to functionality errors that might arise from bit-line leakage. The read bit-line leakage reduction not only reduces the static power consumption, it also improves the read signal. A read failure can occur when the ratio of the read current of the asserted cell to the total leakage current of all the "off" cells on the read bit-line degrades too much due to high leakage currents. It becomes difficult to differentiate between the bit-line discharge caused by the stored data and the bit-line droop because of the leakage current. Figure 2.17 shows Ion/Ioff as function of the supply voltage for different column heights. The dual Vt-8T cell with read bit-line precharged to 0.2 V improves the current ratio with 2.7× compared to a dual Vt-8T cell with read bit-line precharged to VDD. For column height of 256 cells, even for the worst case (FF) process corner and 70 °C the improvement is 1.25× at 0.8 V VDD (Fig. 2.17b). This is because of the leakage mitigation achieved from the reduced DIBL.

4. Dual-Ended Transmission Gate (DETG) Write Cell: WRITE Margin improved (Agarwal et al. 2010)

In the DETG SRAM cell the NMOS access transistors are replaced by full transmission gates (Fig. 2.18). It improves writeability and reduces the WRITE

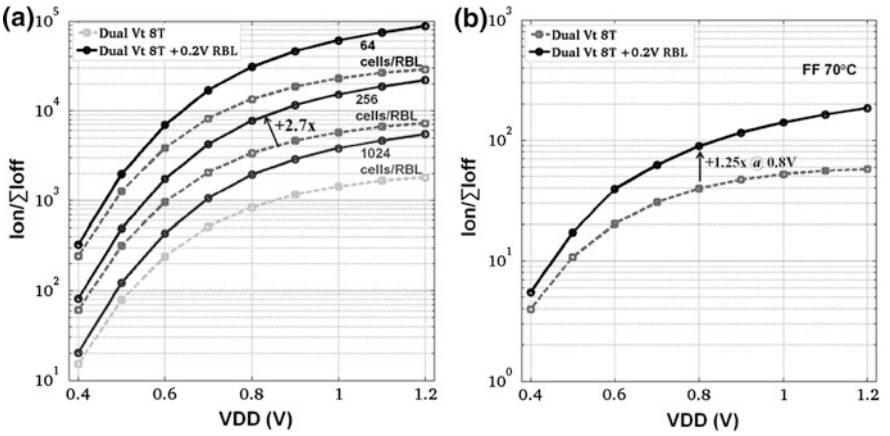

Fig. 2.17 **a** Ion/∑Ioff ratio versus VDD for the different value of column heights. **b** Ion/∑Ioff for the column height of 256 cells (this design) for the worst case FF process corner and 70 °C. Reduced value of RBL reduces the bit-line leakage with the result Ion/∑Ioff is higher with reduced swing dual Vt-8T cell

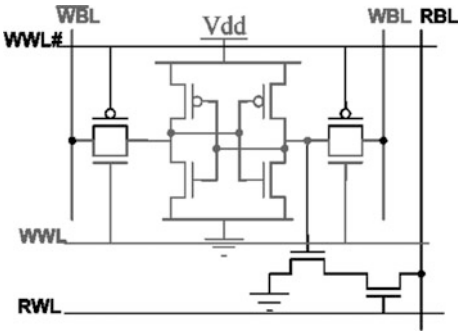

Fig. 2.18 Dual-ended transmission gate (DETG) write memory cell (Agarwal et al. 2010)

access transistor. The WM is 56.3 % more compared to the RD 8T SRAM cell. Figure 2.18 shows WM versus SNMread for different PVT conditions. The READ and WRITE operation is exactly the same as that of RD 8T SRAM cell. The cell symmetry with respect to NMOS and PMOS reduces the effect of the systematic variations and also the redundancy results in averaging out the random variations across the two transistors. Figure 2.19 shows Iread, cell versus leakage for different PVT conditions. The test chip (Agarwal et al. 2010) (register file) based on the DETG cell in 32 nm achieves VDDmin of 0.34 V (Fig. 2.20).

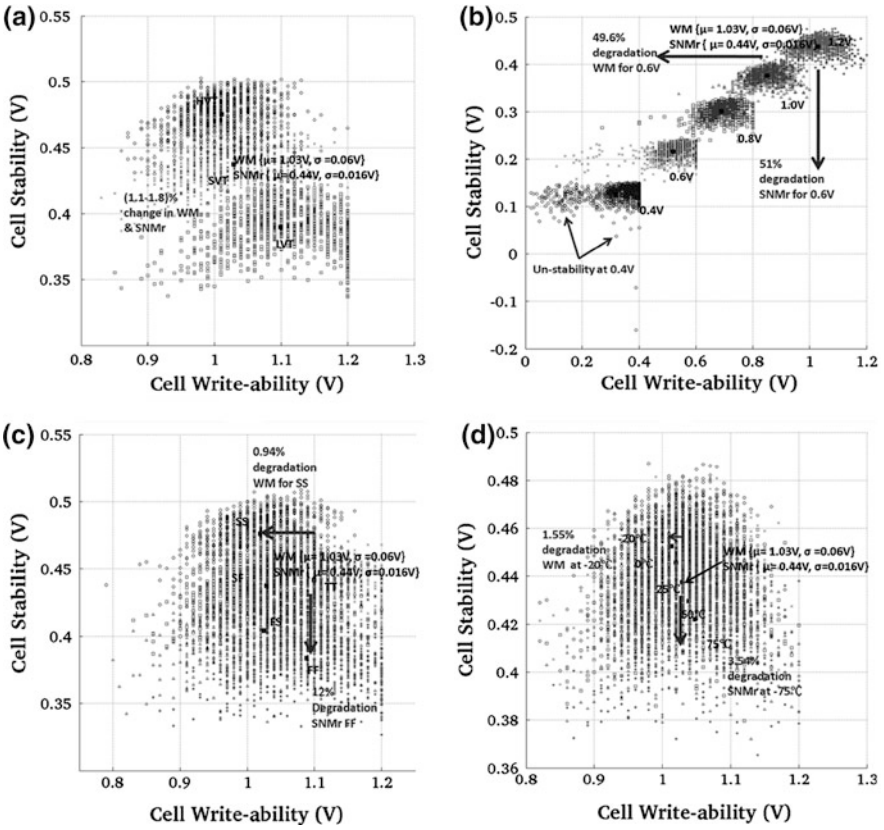

Fig. 2.19 DETG cell, 65 nm LP technology, minimum sized SRAM cell. **a** Vt variation. **b** VDD variation for standard Vt DETG cell. **c** Process variation for standard Vt DETG cell. **d** Temp variation for standard Vt DETG cell

2.2.5 Differential Read Decoupled 8T and 10T SRAM Cells

The read decoupled SRAM cell topologies discussed earlier are single-ended bit cells. There is an inherent loss of common mode noise rejection capability on the bitlines with the single-ended sensing. It is very crucial to ensure a desired level of the noise margin in order to distinguish between genuine bit-line discharge and the read-data droop because of leakage current. In this section read decoupled differential SRAM cells will be discussed.

1. Complementary 10T (CP10T) SRAM Cell (Chang et al. 2009b)

Figure 2.21 shows a read decoupled CP10T SRAM cell. During READ operation WL is activated and VGND is pulled to VSS. W_WL is kept disabled and the internal storage nodes (Q, Qbar) remain isolated from the bit-line. Depending on the storage node information one of the bit-lines starts discharging on the assertion

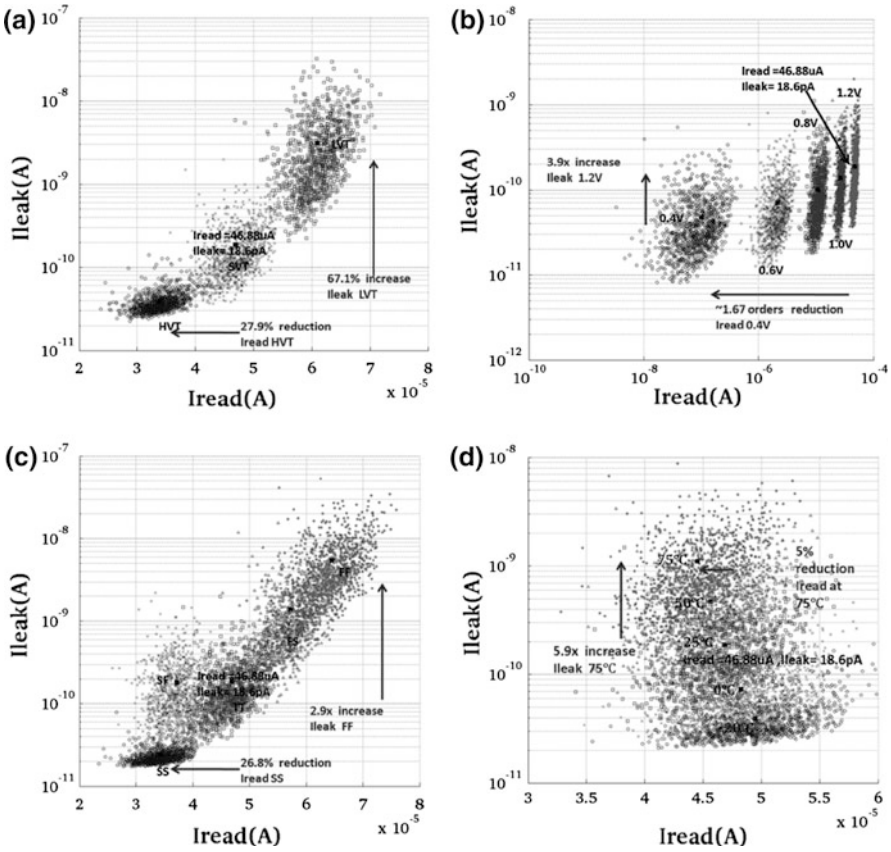

Fig. 2.20 DETG cell, 65 nm LP technology, minimum sized SRAM cell. **a** Vt variation. **b** VDD variation for standard Vt DETG cell. **c** Process variation for standard Vt DETG cell. **d** Temp variation for standard Vt DETG cell

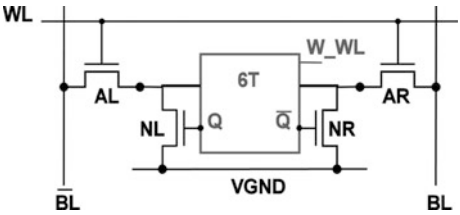

Fig. 2.21 Complementary 10T (CP10T) SRAM cell

of the WL signal and VGND pulled to VSS. Due to the inverted nature of the sensing the bit-line positions are swapped.

During WRITE operation both WL and W_WL are activated to transfer the write data to cell node from bitlines. Two series access transistors degrade the writeability of the CP10T cell. This results in 44.44 % degradation in the WM.

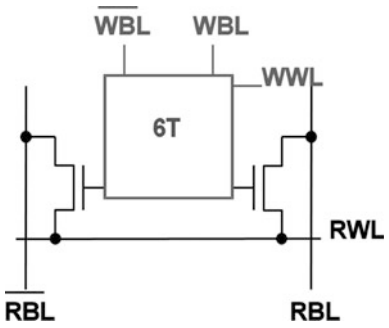

Fig. 2.22 Z8T SRAM cell

The test chip (Chang et al. 2009b) of 32 Kb CP10T cell SRAM macro (Chang et al. 2009b) in 90 nm CMOS achieves VDDmin of 0.18 V operating at 31.25 kHz.

2. Zigzag (Z) 8T SRAM Cell (Wu et al. 2010) (Suzuki et al. 2010)

Figure 2.22 shows a decoupled differential Z8T SRAM cell. It reduces the area overhead associated with CP10T cell and also achieves a better WM. The Z8T cell consists of a 6T cell and a 2T decoupled differential read port. For the un-accessed cells, bitlines are kept precharged at VDD, the write word line (WWL) are inactive and the read word line (RWL) is held at VDD (gate-to-source voltage of NMOS transistors is zero). The 2T decoupled differential read port is inactive.

During READ operation, the selected RWL is discharged to low and develops a voltage swing on the RBL (Q = "H"). The RWLs of the unselected cells remain at VDD. The voltage swing on the RBL is kept at less than 10 % of VDD. The 2T decoupled differential read port of un-accessed cells on the activated column remains in the cut-off region. The potential risk of the bit-line leakage is avoided. The differential read and suppressed BL leakage achieves faster read access. For enhancing the write ability WRITE access transistors are upsized in order to achieve better writeability. The WRITE operation of Z8T cell is similar to the SRAM 6T WRITE operation. Figure 2.23 shows SNMread versus WM for different PVT conditions. Figure 2.24 shows Iread versus leakage under different PVT conditions. The test chip (14 Kb Z8T SRAM macro) (Suzuki et al. 2010) in 65 nm LP CMOS technology achieves VDDmin of 0.5 V operating at 154 MHz. The 32 Kb (Wu et al. 2010) SRAM macro achieves VDDmin of 0.44 V in 90 nm CMOS technology.

The RWL line of Z8T cell has to sink all the discharge current of differential 2T and can result in serious voltage drop thereby impacting the gate-to-source voltage of differential transistors and the Iread, cell. The IR drop on RWL line for the wider word lengths can result in a severe degradation of Iread, cell. With the result Z8T SRAM cell and CP10T structure inhibits its usage for large test arrays. Alternatively, pseudo 8T gated read buffer local architecture (Sharma et al. 2011a) discussed in Chap. 4 enables a differential 8T sensing which can be applied to much larger SRAM arrays and also have a less area overhead.

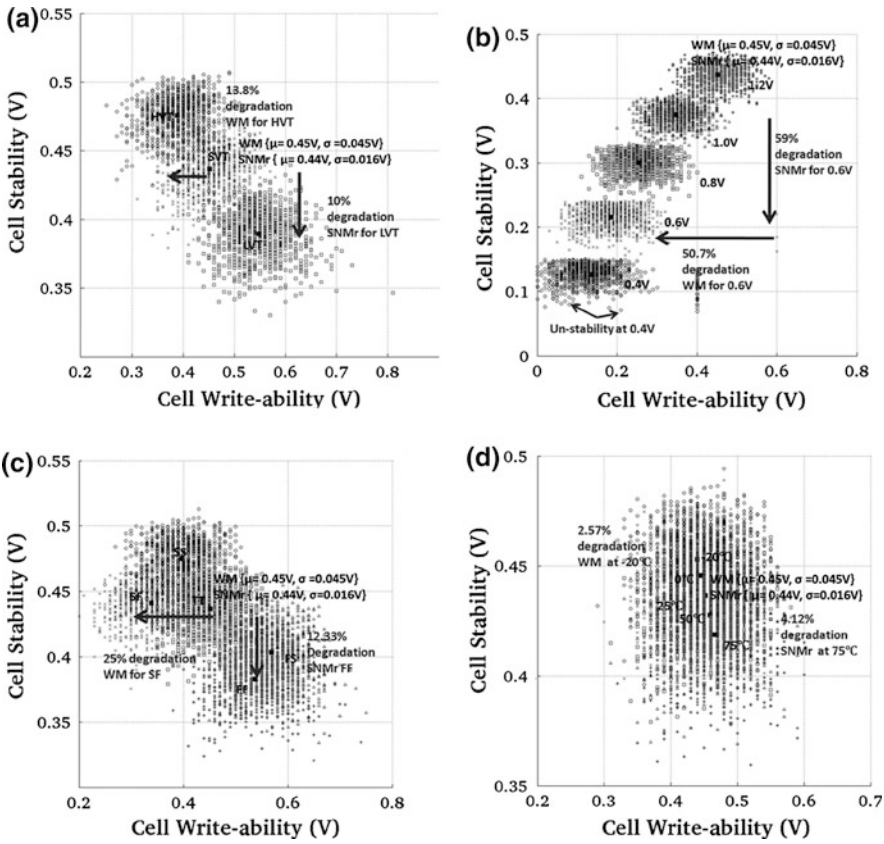

Fig. 2.23 Z8T cell, 65 nm LP technology. **a** Vt variation. **b** VDD variation for standard Vt Z8T cell. **c** Process Variation for standard Vt Z8T cell. **d** Temp variation for standard Vt Z8T cell

2.3 Summary

Table 2.1 shows the comparison of different SRAM cell topologies with reference to the conventional 6T SRAM cell. As it can be observed there is not a single cell topology which can address all the issues like SNMread, WM, half select condition free and also occupies minimum cell area. But the reduced swing dual Vt 8T cell solves most of the issues and is a logical choice for designs in advanced technologies as it avoids read disturbs and allows optimizing the 6T core for write ability. As the 6T core has no impact on memory speed, it can be implemented with slow, low leakage transistors, significantly reducing the standby power consumption. The read buffer current has a large impact on the memory speed, hence the use of fast, low-Vt transistors. This not only improves the nominal read current, but also the variations on the read current thanks to the increased gate-source overdrive voltage. This improvement is most welcome in scaled

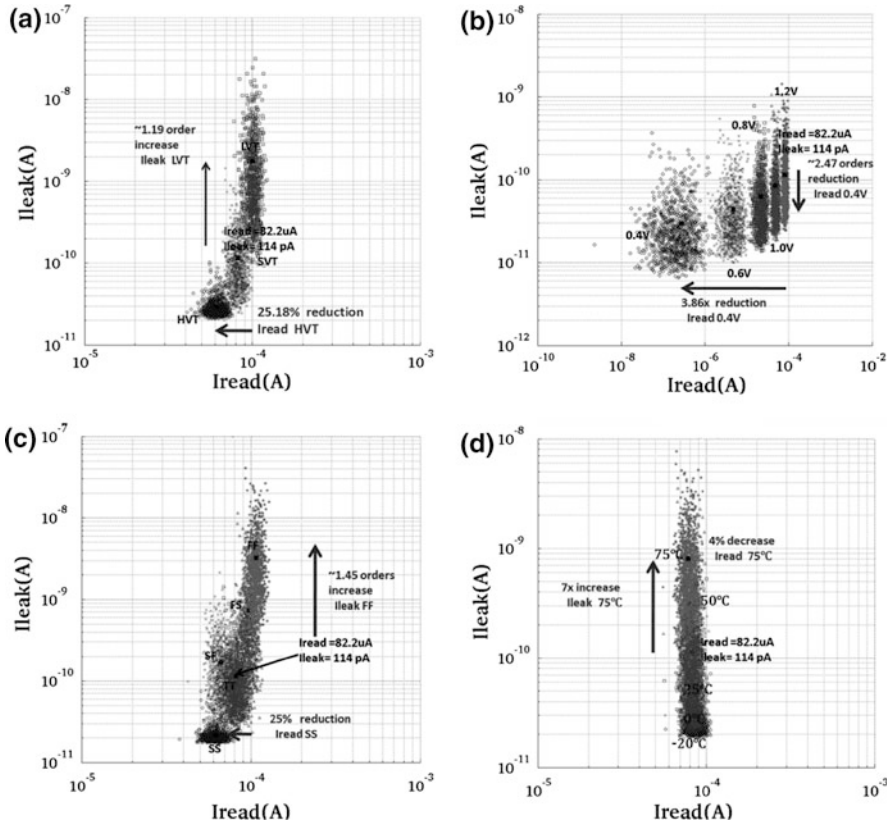

Fig. 2.24 Z8T cell, 65 nm LP technology. **a** Vt variation. **b** VDD variation for standard Vt Z8T cell. **c** Process Variation for standard Vt Z8T cell. **d** Temp variation for standard Vt Z8T cell

designs with lower VDD and higher transistor variations. Additionally, the low precharge voltage reduces the average bit-line discharge energy and improves the Ion/Ioff ratio on the read bit-line.

The D2APT 8T cell does not rely on voltage modulation for higher WMs but it does not offer improved cell stability. The DETG cell offers very high write and cell stability margins but it consists of 10 transistors and also the read sensing is single ended. The Z8T SRAM cell offers better read stability and differential sensing, but there is an inherent problem in its topology as discussed which limits it applicability. The best solution for the variability resilience and low energy lies in combining the cell topology based solution as discussed with the voltage modulation and local architecture modifications of SRAM array are discussed in next chapters.

Table 2.1 Summary of different SRAM cell topologies with reference to SRAM 6T cell

	RSNF7T	D2AP8T	CR8T	RD8T	RSDVt8T	DIL10T	DETG	CP10T	Z8T
Min cell area	1.13×	1.5×	1.3×	1.3×	1.3×	1.8×	…	2.02×	1.34×
#Control signals	3	2	2	2	2	2	3	3	2
Sensing	Single	Differential	Differential	Single	Single	Single	Single	Differential	Differential
VDD min	0.44 V (90 nm)	0.54 V (45 nm)	0.6 V (45 nm)	0.41 V (65 nm)	0.7 V (65 nm)	0.4 V (45 nm)	0.34 V (32 nm)	0.2 V (90 nm)	0.5 V (65 nm)
Read disturb free	Yes	No	No	Yes	Yes	Yes	Yes	Yes	Yes
Write ability	…	High	Low	Same	Same	Same	High	Low	Same
Half-select condition immunity	High	High	Very high	Same	Same	Same	Same	Same	
Leakage	High	Low	High	Low	Low	Low	High	Same	Low

References

A. Agarwal et al., A 32 nm 8.3 GHz 64-entry × 32b Variation Tolerant Near-Threshold Voltage Register File. *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 105–157 (2010)

B.H. Calhoun et al., A 256 k Sub threshold SRAM Using 65 nm CMOS. *Proceedings of IEEE International Solid-State Circuits Conference* (*ISSCC*), pp. 628–629, Feb 2006

L. Chang et al., Stable SRAM Cell Design for the 32 nm Node and Beyond. *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 128–129 (2005)

L. Chang et al., An 8T-SRAM for variability tolerance and low-voltage operation in high-performances caches. IEEE J. Solid-State Circuits, **43**, 4, April (2008)

M.F. Chang et al., A Differential Data Aware Power-supplied (D^2AP) 8T SRAM Cell with Expanded Write/Read Stabilities for Lower VDDmin Applications. *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 156–157 (2009a)

I.J. Chang et al., A 32 kb 10T sub-threshold SRAM array with bit-interleaving and differential read scheme in 90 nm CMOS. IEEE J. Solid-State Circuits **44**(2), 650–658 (2009b)

T.H. Kim et al., A High-Density Sub threshold SRAM with Data–Independent Bitline Leakage and Virtual Ground Replica Scheme. *Proceedings of IEEE International Solid-State Circuits Conference* (*ISSCC*), pp. 330–331, Feb 2007

V. Sharma et al., A 4.4 pJ/Access 80 MHz, 128 kbit variability resilient SRAM with multi-sized sense amplifier redundancy. IEEE J. Solid-State Circuits, **46**, 10 (2011a)

V. Sharma et al., 8T SRAM with Mimicked Negative Bit-lines and Charge limited Sequential Sense Amplifier for Wireless Sensor Nodes. *Proceedings of IEEE European Solid-State Circuits Conference* (*ESSCIRC*), pp. 531–534, Sept 2011b

T. Suzuki et al., 0.5 V, 150 MHz, Bulk-CMOS SRAM with Suspended Bit-Line Read Scheme, *Proceedings of IEEE European Solid-State Circuits Conference* (*ESSCIRC*), pp. 354–357, Sept 2010

K. Takeda et al., A read-static-noise-margin-free SRAM cell for low-VDD and high-speed applications. IEEE J. Solid-State Circuits **41**(1), 113–121 (2006)

K. Utsumi et al., A 65 nm low power CMOS platform with 0.495 μm^2 SRAM for digital processing and mobile applications. *Proceedings of IEEE Symposium VLSI Technology*, pp. 216–217 June 2005

J. Wu et al., A Large σV_{TH}/VDD Tolerant Zigzag 8T SRAM with Area-Efficient Decoupled Differential Sensing and Fast Write-Back Scheme. *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 101–102 (2010)

M. Yabuuchi et al., A 45 nm low-standby-power embedded SRAM with improved immunity against process and temperature variations. *Proceedings of IEEE International Solid-State Circuits Conference*, pp. 326–327, Feb 2007

M. Yabuuchi et al., A 45 nm 0.6 V Cross-Point 8T SRAM with Negative Biased Read/Write Assist, *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 158–159 (2009)

http://www.springer.com/978-1-4614-4038-3

SRAM Design for Wireless Sensor Networks
Energy Efficient and Variability Resilient Techniques
Sharma, V.; Catthoor, F.; Dehaene, W.
2013, XII, 172 p., Hardcover
ISBN: 978-1-4614-4038-3