The Report Committee for QuocDat Tai Nguyen
Certifies that this is the approved version of the following report:

Read/Write Assist Circuits and SRAM Design

APPROVED BY
SUPERVISING COMMITTEE:

Supervisor:

Abraham A. Jacob

Mark McDermott

Read/Write Assist Circuits and SRAM Design

by

QuocDat Tai Nguyen, B.S.E.E.

Report

Presented to the Faculty of the Graduate School of

The University of Texas at Austin

in Partial Fulfillment

of the Requirements

for the Degree of

Master of Science in Engineering

The University of Texas at Austin

December 2009

Dedication

Dedicated to my family and friends for their love and support.

Acknowledgements

Special thanks to Professor Jacob Abraham and Research Fellow Mark McDermott for their guidance and support. Thanks to Huy Nguyen for providing idea and his advising support on this project. I’m also grateful for the support from my Mom & Dad.

December 2009

Abstract

Read/Write Assist Circuits and SRAM Design

QuocDat Tai Nguyen, M.S.E.

The University of Texas at Austin, 2009

Supervisor: Abraham A. Jacob

This report discusses the design of read/write assist circuits which are used in a SRAM cell's design to overcome the cell's variations. It also explains the variability problems in a SRAM bit-cell and many approaches to address them. The basic operations, SNM concept, and write margin of an SRAM are described theoretically as well as measured in simulation. The write assisted circuit, the Negative Bit-line Voltage Bias scheme, is discussed and implemented at transistor level using a six-transistor (6T) SRAM cell. With the write assisted circuit, the implemented memory array successfully performs a write operation at 0.6V and $-25^{o}C$, the condition in which the same operation would fail without the write assisted circuit. During the simulation, this write assisted circuit helps to achieve the negative bias voltage of -70mV on the SRAM's bit-lines. The cost overhead includes chip area, power consumption, and current leakage when this Negative Bit-line Voltage scheme is implemented.

Table of Contents

List of Tables ix

List of Figures x

I. INTRODUCTION 1

II. SRAM CIRCUIT ARCHITECTURE 3

2.1SRAM Cell Architecture ……..... 3

2.1.1 SRAM ARRAY ARCHITECTURE AND BLOCK STRUCTURE ……..... 3

2.1.2 SIX-TRANSISTOR (6T) CMOS SRAM CELL ……4

2.2 SRAM Cell Operation ……. 5

2.2.1 READ OPERATION ……...5

2.2.2 WRITE OPERATION …… 8

III. SRAM CELL STABILITY THEORY AND DESIGN CHALLENGES 11

3.1 SRAM Cell Stability Theory …….. 11

3.1.1 SNM DEFINITION ……... 11

3.1.2 ANALYTICAL SNM EXPRESSION FOR A 6T SRAM CELL …… 13

3.2 SRAM Design Challenges ……. 15

3.2.1 VARIABILITY IN THE SRAM BIT-CELL ……... 16

3.2.2 READ ASSIST CIRCUITS ……... 17

3.2.3 WRITE ASSIST CIRCUITS ……. 22

IV. SRAM CELL DESIGN AND SIMULATION 26

4.1 SRAM Cell Basic Operation and SNM Simulation …….. 26

4.1.1 MEMORY BIT-CELL SIMULATION ……. ……... 26

4.1.2 MEMORY IMPLEMENTATION……... 30

4.1.3 SIMULATION RESULTS ……..……... 35

4.1.3.1 READ OPERATION ……..…….. 35

4.1.3.2 WRITE OPERATION ……..…… 36

4.2 Write-Assist Circuit: Negative Bit-line Voltage Scheme ……. 39

V. CONCLUSION 42

Appendix A: Derivation of SNM for 6-T SRAM Cell 43

Bibliography 46

Vita 48

List of Tables

Table 4.1: Worst Case Array Access Timing.....35

Table 4.2: Power Consumption for the Memory Array Operates at 1.5GHz 37

Table 4.3: Complete Write Margins.....38

Table 4.4: Power Consumption for Integrated Charge-pump Memory Array...41

List of Figures

Figure 2.1: Architecture of 64Kb SRAM ..……..…….....4

Figure 2.2: Six-transistor SRAM cell.....5

Figure 2.3: 6T SRAM cell's initial condition before a Read/Write operation 6

Figure 3.1: a 6T SRAM Cell during a read access.....11

Figure 3.2: Flip-flop with two noise sources with adverse polarities.....12

Figure 3.3: SNM estimation based on "maximum squares" in a 45^o rotated coordinate system.....13

Figure 3.4: A 6T full CMOS SRAM cell in read-accessed mode.....13

Figure 3.5: Read-assist circuit schematic.....18

Figure 3.6: Circuit diagram of a read-assist circuit.....19

Figure 3.7: Vdd dependence of SNM of 0.614 μm^2 and 0.494 μm^2SRAM with and without read-assist circuit.....19

Figure 3.8: MUXing power supplies based on Read or Write 21

Figure 3.9: Diagram of read-assist and write-assist circuits.....23

Figure 3.10: The wave form of read and write cycles.....23

Figure 3.11: The proposed Tran-NBL scheme.....24

Figure 4.1: Schematic Diagram of a 6-T SRAM Bit-cell.....27

Figure 4.2: Optimal SNM of SRAM Bit-cell.....28

Figure 4.3: SRAM Bit-cell Write Margin 29

Figure 4.4: SRAM Memory Cell Current.....30

Figure 4.5: Folded Bit Slice Structure of a 4-to-1 Column Mux with Shared Column Write Logic 31

Figure 4.6: Physical Implementation of the Top Level Memory Array 32

Figure 4.7: Memory Array Read Control Timing Waveform 33

Figure 4.8: Write Control Timing 34

Figure 4.9: Memory Array Read Operation 36

Figure 4.10: Waveform of a Successful Write 37

Figure 4.11: Memory Cell Unable to Switch in Write 39

Figure 4.12: Negative Charge-Pump Circuit Diagram 40

Figure 4.13: A Successful Write on Memory Cell with Negative Charge-Pump Implemented 41

I. INTRODUCTION:

Moore's law predicts that the number of transistors that can be placed on an integrated circuit is doubled approximately every two years. In parallel, the need for bit counts in an embedded Static Random Access Memory (SRAM) has been growing exponentially. Thus, the probability of a defect in an embedded SRAM cell is constantly increasing. In addition, as the process technology continues to scale, the stability of an embedded SRAM cell is not only a major design consideration, but also a concern for testing as well. [1-3].

SRAM cell's designers encounter many challenges as technology scales. First of all, it has become increasingly complicated to maintain an acceptable Static Noise Margin (SNM) in a SRAM cell while scaling the minimum size and supply voltage. As a result, the control of the process parameters becomes exceedingly difficult, because the increased process variations are translated into a wider distribution of transistor and circuit characteristics. Secondly, it has been observed that there are many variability problems at a transistor level in the SRAM bit-cell. For example, as the Operating Voltage (VDD_{MIN}) is reduced, it causes Read/Write/Access fails, or Data Retention fails. In addition there are other failures relating to variability in the SRAM cell's Sense Amplifier circuitry. Thirdly, tightly packaged chip areas can be especially susceptible and sensitive to manufacturing defects and process variations. For example, as large SRAM arrays are condensed to minimize their footprints in an integrated chip, they are more susceptible to defects. According to International Technology Roadmap for Semiconductors, it is predicted that "greater parametric yield loss with respect to noise margin" for high density circuits such as SRAM arrays, which are projected to occupy more than 90% of the SoC area in the next 10 years [4, 5].

To this end, this paper will discuss a design of a SRAM cell and implementation of SRAM's related circuitry such as Read/Write assist circuits in order to address the discussed challenges in the current design of a SRAM cell. As shown in this paper, SRAM cell design in theory including SRAM cell architecture and basic operations of an

SRAM are briefly overviewed in section II. Section III presents a theory of SRAM stability (SNM) and challenges in an SRAM cell's design. Finally, the proposed SRAM cell designs with a write assist circuit are discussed in Section IV. The paper also analyzes and compares the results of the simulated circuits and what the proposed circuits have achieved.

II. SRAM CIRCUIT ARCHITECTURE AND OPERATION:

SRAM arrays are widely integrated in modern System on the Chips (SoCs). In an Intel micro-processor Montecito as an example, SRAM-based caches occupy more than 90% of the total 1.72 billion transistors of the processor [6]. For that reason, understanding the architecture and operation of a SRAM cell is crucial for its future design enhancement.

SRAM cell design considerations are essential for a number of reasons [6]. First, the design of a SRAM cell is a key to ensure the stability and robustness of SRAM operations. Second, while more components are tightly packaged in a high density area to enhance on-chip storage capacity, other constraints have to be met such as stability, speed, and power. Thus this makes the cell transistors more susceptible and sensitive with respect to process variations. Third, the cell layout also plays an important role on a SRAM area as well as the overall chip one. A thorough understanding of the involved trade-offs can help a SRAM designer to meet all constraints.

2.1 SRAM Cell Architecture:

2.1.1 SRAM ARRAY ARCHITECTURE AND BLOCK STRUCTURE:

Figure 2.1 shows a typical small SRAM memory array architecture which consists of 2^n words of storage of 2^m bits each. In particular it is a block diagram of 64Kb SRAM memory array including 256 words (2^8 rows with n=8) and 256 bits (2^8 columns with m=8). In a simplest memory design, an array is organized with one row per word and one column per bit. There are far more words in the memory than bits in each word. This would lead to a very long and skinny memory architecture which is hard to fit in a floor plan or very slow because of a long bit line wire. Folding the rows to make more columns is the approach. Each row of memory contains 2^k words, so the array is physically organized as 2^{n-k} row of 2^{m+k} columns or bits.

There are a few major components in SRAM architecture as shown in Figure 2.1. They are row/column decoders, bit line conditioning, and column circuitry. The row decoder activates one particular row by inserting one of the word lines. Column decoder controls a multiplexer in the column circuitry to select 2^m bits from the row as the data to access. Bit-line conditioning circuitry helps to pre-charge bit lines before any SRAM operation. Finally, the column circuitry contains write drivers and read sensing circuits which are also called sense amplifiers.

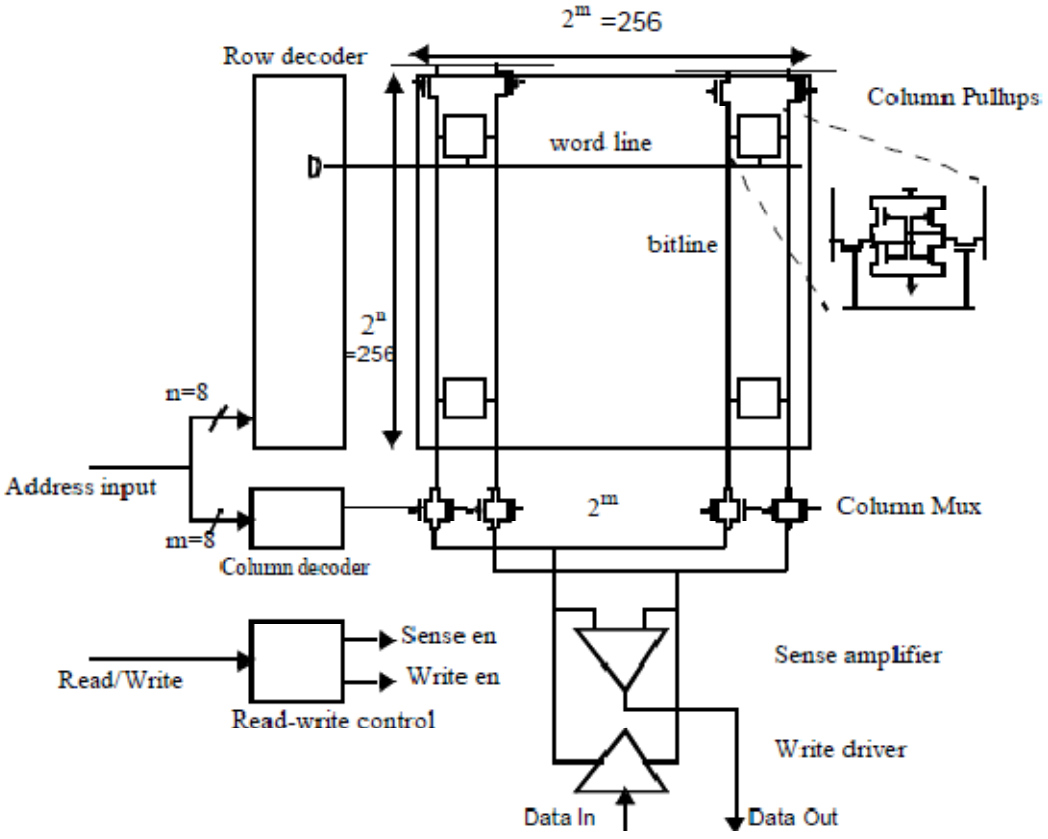

Figure 2.1: Architecture of 64Kb SRAM.

2.1.2 SIX-TRANSISTOR (6T) CMOS SRAM CELL:

The core storage element used for most register file and cache designs on high-performance microprocessors is a six-transistor CMOS cell with a single word-line

and both true and complementary bit-lines. Figure 2.2 shows the circuit diagram of a 6T SRAM. The cell contains a pair of cross-coupled inverters and an access-transistor for each bit-line as combination read/write port. True and complementary versions of the data are stored on the cross-coupled inverters. If the data is disturbed slightly, positive feedback around the loop will restore it to V_{DD} or GND. The word-line in inserted to read or to write the cell.

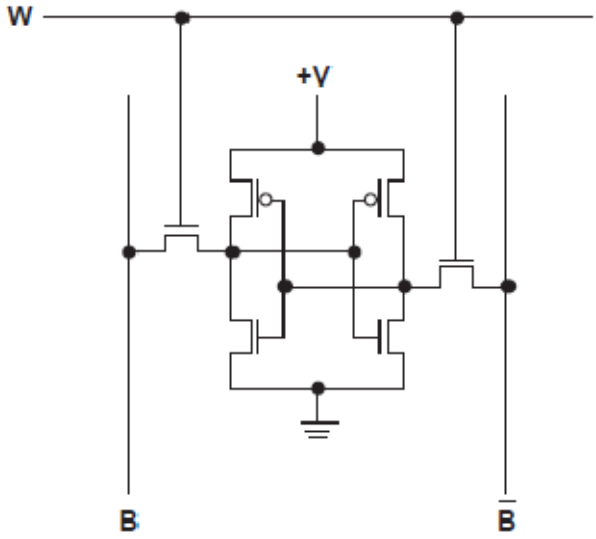

Figure 2.2: Six-transistor SRAM cell.

2.2 SRAM Cell Operation:

SRAM operation can be divided into two phases, phase 1 - Φ1 and phase 2 - Φ2, which can be generated from clk and its complement clkb signals. Assume that the SRAM is pre-charged in phase 2. In phase 1, the SRAM is written, or read by raising the appropriate word line and either driving the bit lines to the value that should be written or leaving the bit lines floating and observing which one is pull down. The row and column are selected by row or column decoders.

Reading a large SRAM array can be slow due the capacitance of the SRAM cells which are sharing the same bit line. The sense amplifier circuit (sense amp) can

accelerate the read by detecting the differential voltage between the two complementary bit lines.

2.2.1 READ OPERATION:

Prior to initiating a read operation the two bit lines are pre-charged to VDD. The read operation begins by enabling the word line (word) and connecting the pre-charged bit lines, bit and bit_b, to the internal nodes of the cell. Figure 2.3 shows the data value of a 6T SRAM cell before a read operation.

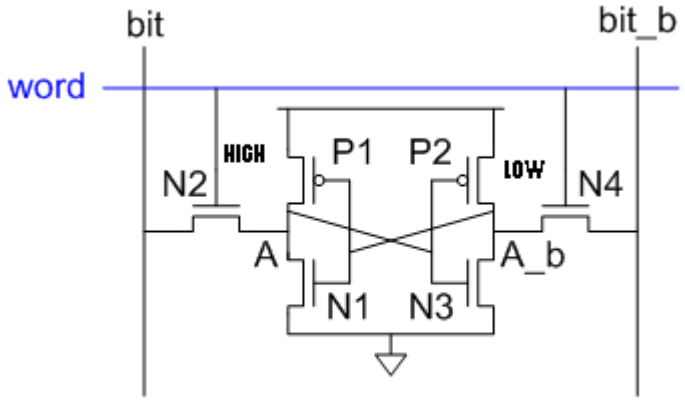

Figure 2.3: 6T SRAM cell's initial condition before a Read/Write operation.

Assume that the cell is currently storing logic "1"; node A (HIGH) is being held at VDD by device P1 while node A_b (LOW) is being held at VSS by device N3. The series connection between turned ON device N3 and N4 allows the current to sink from the bit line node bit_b, therefore discharging it toward ground. Node HIGH stays the same at VDD because device P1 is ON and there is very little current flowing through. After a sufficient time a differential voltage developed on nodes bit and bit_b is detected by the sense amp circuit. This sense amp circuit is activated and helps to further pull up and pull down the voltage the two bit lines bit and bit_b respectively. Finally the value that placed onto the bit lines is read.

There is a timing design issue involved in order to make the sense amp circuit worked timely in a SRAM cell. First, notice that the bit line bit_b is discharged through the two devices N3 and N4 in series, both of which are typically designed minimum in size to minimize cell area. The charge is pulled from bit line bit_b, therefore the differential voltage between bit and bit_b will be limited by the small size of these devices. This affects the read speed of the array because it depends on the time required to build sufficient differential voltage on bit lines for the sense amplifier to read correct value. Second, device N3 and N4 form a resistive divider between the node bit_b and node LOW. At the same time bit_b is being pull down, node LOW tends to rise. Node LOW is held low by device N3, but raised by current flowing in from device N4. This can be problematic since it can potentially cause N1 to turn on, discharging the HIGH node. This disastrous condition can flip the cell from storing a logic "1" to a logic "0". This condition is known as a read-disturb or read-upset. Consequently N3 must be stronger than N4. Specially, the transistors must be ratioed such that node LOW remains below switching threshold of the P1/N1 inverter. This constraint is called read stability. The principle is that designer must careful limit the raised voltage at node LOW to prevent the read-upset condition while maintaining an acceptable circuit speed and area constraints.

The voltage which rises on the node LOW can be estimated be examining simplified Ids equations for devices N3 and N4 [7]. According the initialization conditions of a SRAM cell for a read operation we can assume that device N4 is in saturation mode and device N3 is in linear mode. To the first order, we can also assume that the current through device N3 and N4 is equal (Note: in the following analysis, first-order, long-channel device equations are employed to simplify the analysis and demonstrate the basic concepts.) [7]

$$\frac{1}{2}\left(\frac{\mu\varepsilon}{T_{ox}}\right)\left(\frac{W_{N4}}{L_{N4}}\right)(V_{word}-V_{LOW}-V_T)^2 = \left(\frac{\mu\varepsilon}{T_{ox}}\right)\left(\frac{W_{N3}}{L_{N3}}\right)(V_{HIGH}-V_T-\frac{1}{2}V_{LOW})V_{LOW}$$

This equation shows that the voltage on node LOW is affected by the sizes of both N3 and N4. As node LOW voltage rises, less charge is removed from the BIT# line,

and thus slowing down the read. However the LOW voltage rise also increases the current flow through device N3 helping to keep node LOW from rising too far. In order to stable the cell and to meet array read speed, proper size ratio must be chosen for devices N3 and N4. Let define CR as the ratio of the pull down to the pass gate as the cell ratio.

$$CR = \frac{\frac{W_{N3}}{L_{N3}}}{\frac{W_{N4}}{L_{N4}}}$$

Equation can be arranged and simplified as the following:

$$\frac{1}{2}(V_{DD} - V_{LOW} - V_T)^2 = CR(V_{DD} - V_T - \frac{1}{2}V_{LOW})V_{LOW}$$

The resulted equation describes the quadratic relationship for the voltage rise on node LOW with cell ratio, V_{DD}, and V_T.

$$V_{LOW} = \frac{(V_{DD} - V_T)(1 + CR \pm \sqrt{CR(1 + CR)})}{1 + CR}$$

An analysis showed that if holding node LOW to less than V_T is assumed acceptable, the cell ratio should be kept greater than about 1.28. This limit is typical of most recent microprocessor fabrication technologies where a minimum cell ratio of 1.25 to 2.0 is required under normal operating conditions [7].

SPICE simulation should be also performed in practice to establish cell stability in addition to the approximate analytical presented above.

2.2.2 WRITE OPERATION:

The same as SRAM cell reading operation, the two bit lines are pre-charged to VDD in a write operation. The address decoder enables the word line (word) to open the two pass gates. Figure 2.3 shows a 6T SRAM cell's initial condition before a write operation, where the cell initially stored a logic "1"at node HIGH and is written with a logic "0" (Node HIGH is pulled down to Vss).

As discussion in a read operation, a minimum cell ratio is required to prevent undesired cell writing. Smaller cell ratios while preventing accidental updates also make it

somewhat harder to accomplish a desired write operation. The read disturb condition which holds the internal node to a very low value. As a result, the inverter pair formed by device P2/N3 does not amplify the new write data and the high going side of the cell, does not contribute to the write operation of the cell.

The LOW going bit line (bit), also forms a voltage divider between the PMOS inverter P1 and pass gate N2. The pass gate must be much more conductive than the PMOS device for a write to the cell.

The cell must be written by forcing A low through N2. P1 opposes this operation; thus P1 must be weaker than N2 so that A can be pulled low enough. This constraint called write-ability. Once A falls low, N3 turns OFF and P2 turns ON, pulling A_b high as desired.

Below is a rough analysis establishing the maximum ratio of the pull-up size to that of the pass gate required for a cell to be write-able. Based on the condition of the SRAM cell during a write, we can assume that the pass gate is in the linear region and the PMOS device is in saturation mode at the end of the write operation. The below equation illustrates this condition. (once again long-channel device equations are used for simplicity.)

$$\left(\frac{\mu_n \varepsilon}{T_{ox}}\right)\left(\frac{W_{N2}}{L_{N2}}\right)\left[V_{word} - V_{bit} - V_{Tn} - \left(\frac{1}{2}\right)(V_{HIGH} - V_{bit})\right](V_{HIGH} - V_{bit})$$

$$= 1/2(\frac{\mu_P \varepsilon}{T_{ox}})\left(\frac{W_{P1}}{L_{P1}}\right)(V_{DD} - V_{LOW} - V_{Tp})^2$$

To start the simplification of this equation, $V_{DD}$is substituted for V_{word} , 0 is substituted for V_{bit}, and finally V_{Tn} is substituted for V_{LOW}

$$\mu_N\left(\frac{W_{N2}}{L_{N2}}\right)(V_{DD} - V_{Tn} - \left(\frac{1}{2)V_{HIGH}}\right)V_{HIGH} = 1/2\mu_P\left(\frac{W_{P1}}{L_{P1}}\right)(V_{DD} - V_{LOW} - V_{Tp})^2$$

Define the size ratio of the pull-up device P2 to the pass gate N2 as the pull-up ratio:

$$PR = \frac{\frac{W_{P1}}{L_{P1}}}{\frac{W_{N2}}{L_{N2}}}$$

Voltage on the HIGH node is solved as the following.

$$V_{HIGH} = (V_{DD} - V_{Tn}) \pm \sqrt{(V_{DD} - V_{Tn})^2 - \frac{\mu_P}{\mu_N}(PR)(V_{DD} - V_{Tn} - V_{Tp})^2}$$

Analysis has shown that in normal case, it appears that the sizing for write operation would not be an issue. When all effects and worst-case conditions are taken into account, the pull-up ratios limit may become significant. The equation for V_{HIGH} shows that a successful writing of a cell is a function of the transistor sizing, V_{DD}, the mobility ratio of the P and N devices, and the threshold voltages. The limiting case on a write operation occurs at high $V_{DD}$when P device is strong (μ_P high, V_{TP}low) and the N device is weak (μ_N low, V_{Tn}high)

III. SRAM CELL STABILITY THEORY AND DESIGN CHALLENGES:

Cell stability and cell area are the two most important aspects of SRAM cell design. They are interdependent to each other because a stable SRAM cell requires a larger cell area. This task is even more complicated when a higher bit count, lower power consumption, and high performance are also taken into account. The challenges include the scaling of CMOS transistors which involves the scaling down of voltage supply while maintaining the device reliability. In addition, there are other factors that affect the repeatability of the threshold voltage. It has been projected that SRAM stability margin or Static Noise Margin (SNM) reduces by 4X as scaling progresses from 250 nm CMOS technology down to 50 nm technology [8,9].

The following section discusses the definition of a SRAM cell SNM and analytical expression on how to calculate a SNM of a 6T SRAM.

3.1 SRAM Cell Stability Theory

3.1.1 SNM DEFINITION:

There are several existing definitions of the static noise margin in literature. However a widely accepted SNM definition is a SNM as a side of the maximum square drawn between the inverter characteristics.

Figure 3.1 shows the circuit diagrams of the 6T full-CMOS cell during a read access with the bit lines pre-charged to the power supply. This is the most critical situation because the PMOS devices are now shunted by the NMOS access transistors, which reduces the gain of the cell inverters.

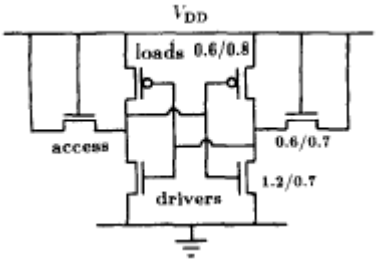

Figure 3.1: a 6T SRAM Cell during a Read Access.

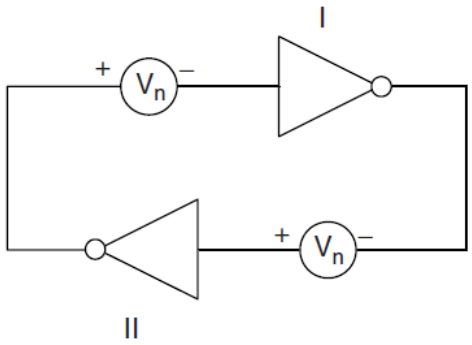

Figure 3.2: Flip-flop with Two Noise Sources with Adverse Polarities.

The SRAM cell is presented as two equivalent inverters like a flip-flop with a noise sources (V_n) inserted between the corresponding inputs and outputs (figure 3.2). Static-noise is a dc disturbance such as offsets and mismatch due to processing and variations in an SRAM's operating conditions. The SNM of the flip-flop is defined as the maximum value of V_n that can be tolerated by the flip-flop before changing the states [10]. A SRAM should be designed such that it can cope with any disturbance caused by voltage variations, crosstalk, and thermal noise. The SRAM tolerance is defined by SNM.

Figure 3.3 shows the superimposed normal inverter transfer curve of a read-accessed 6T SRAM cell and its mirrored with respect to x = y line counterpart in a x – y coordinate system. The u – v system of coordinates is rotated counter clockwise by 45^o around the same origin with respect to x – y system. This is a convenient arrangement since by knowing the diagonals of the maximum embedded squares we can calculate the sides.

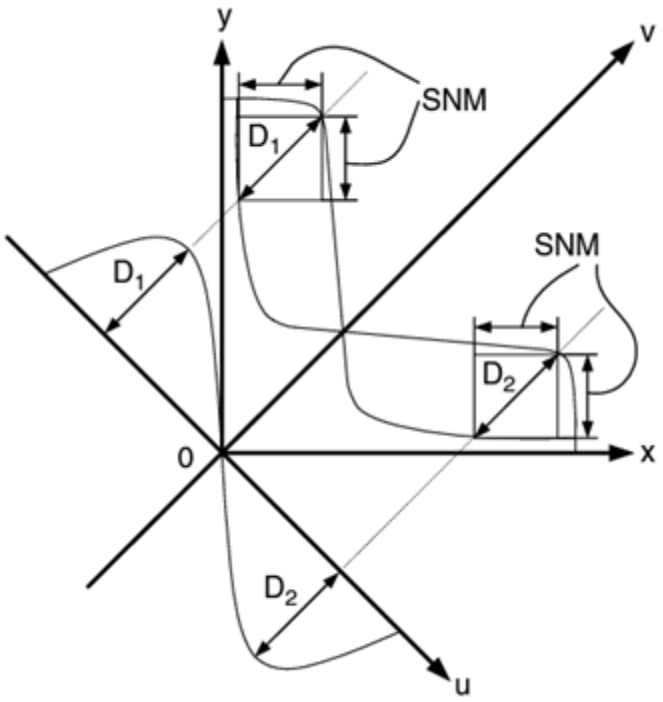

Figure 3.3: SNM estimation based on "maximum squares" in a 45^o rotated coordinate system [6].

3.1.2 ANALYTICAL SNM EXPRESSION FOR A 6T SRAM CELL

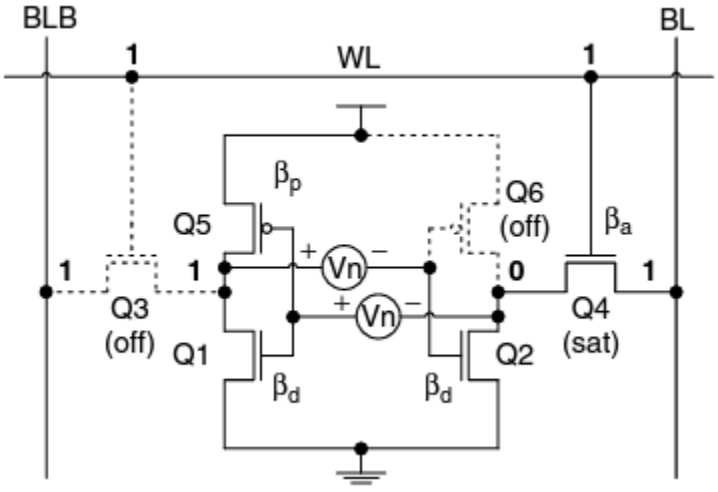

Figure 3.4: A 6T full CMOS SRAM cell in read-accessed mode [6].

Analytical expressions for SNM calculation is not only a very helpful tool to estimate value of SNM to learn about the impact of various process parameters, but also an optimizing mean to alleviate a SRAM design for specific requirement such as high performance, low power or low voltage.

An SNM analytical expression for a six-transistor 6T full CMOS cell can be derived by applying Kirchhoff equations and one of the mathematically equivalent noise margin criteria [11]. Figure 3.4 shows the equivalent circuit diagram of a 6-T SRAM cell when we assume that the right sides of an SRAM cell to be at level ZERO and the left sides at level ONE. This SNM_{6T} equation was obtained by using the basic MOS model equation with constant V_{TH} and neglecting second-order effects such as mobility reduction and velocity saturation. The detailed derivation is presented in Appendix section.

$$SNM_{6T} = V_{TH} - \left(\frac{1}{k+1}\right) \times \left(\frac{V_{DD} - \frac{2r+1}{r+1} V_{TH}}{1 + \frac{r}{k(r+1)}} - \frac{V_{DD} - 2V_{TH}}{1 + k\frac{r}{q} + \sqrt{\frac{r}{q}(1 + 2k + \frac{r}{q}k^2)}} \right) \tag{3.17}$$

where

V_{TH} of NMOS transistors in the cell is assumed V_{TH} of PMOS transistor

$q = \beta_p/\beta_a$

$r = ratio = \beta_d/\beta_a.$

$k = \left(\frac{r}{r+1}\right)\left(\sqrt{\frac{r+1}{r+1-\frac{V_S^2}{V_T^2}}} - 1\right)$

Analysis of the Equation 3.17 helps to draw some conclusions. First, SNM depends only on V_{TH}, V_{DD}, and β cell rations and not on the absolute values of β. SNM_{6T} increases with r and $SNM_{6T} > 0$ for all $r > 0$.

Second, SNM can be maximized by selecting the cell transistor ratios β such that $^{q}/_{r} = {}^{\beta_p}/_{d} = max$. Note that the cell ratios are constrained by the minimum area and reliable write operation requirements.

Third, the SNM_{6T} is independent of V_{DD}variations for particular values of q and r. This is due to the coefficients of V_{DD} in Equation 3.17 having opposite signs [6]. Variation of q and r will then result in either a positive or a negative dependence of SNM_{6T} on V_{DD}. This means that a particular cell stability behavior as a function of V_{DD}can be obtained by selecting specific values of q and r [6].

Lastly, larger V_{TH} of the cell transistor will produce larger SNM_{6T}. Since V_{TH}decreases with temperature, the SNM will also decrease with temperature.

3.2 SRAM Design Challenges:

SRAM cell design challenges also consist of the sources of "Within Die Variation" [15]. They are Random Dopant Fluctuation (RDF), Line Edge Roughness (LER), Lithography, Hot Carriers, and many others. These cause mismatch in both global and local voltage threshold. The complexity of the increase of threshold voltage (V_{TH}) variation within a die in a sub-micron is caused by RDF and LER [16]. As a result the large V_{TH} variation induces a mismatch in the DC characteristic, which deteriorates both the SNM and the write ability of an SRAM. In addition this problem in a 6T SRAM manifests itself as the increase of memory capacity on a chip.

Random Dopant Fluctuation (RDF) describes the statistical variation in the number and placement of dopants in a transistor channel. With the scaling of CMOS dimension, RDF in the channel of the device causes the limitation of electrical deviations in device characteristics [17]. Consequently, the threshold voltage mismatch due to this intrinsic fluctuation contributes largely to the reduction of an SRAM static noise margin.

Line Edge Roughness (LER) is caused by imperfections of patterning process which makes a certain roughness in a printed gate. This LER also causes fluctuation in transistor parameters which can seriously degrade the analog performance and yield of a

device. It is experimentally shown that LER has a significant impact on device with the gate length of 32 nm.

At this point, the paper has discussed thus far many important theoretically aspects of an SRAM cell design including factors affecting an SRAM basic read/write operations, SNM theory behind the stability of an SRAM, and the effects of operating condition and fabrication variations on an SRAM's SNM. The following section explains in more details the challenges and problems of variations in the SRAM bit-cell.

3.2.1 VARIABILITY IN THE SRAM BIT-CELL:

As the process technology continues to scale, especially for SRAM arrays beyond the 65nm and 45nm technologies, it becomes increasingly difficult to reduce the operating voltage (VDD_{MIN}) while maintaining the device reliability. Besides the problem of the increase of leakage current causes the IDDQ failures.

There are many consequences from the above challenges. The technology scaling trends for the SRAM arrays show that traditional voltage scaling can no longer be supported. The operating voltage scaling might cause failures in SRAM are fundamentally due to **access** (reduction in the bit-differential produced while accessing the cell, I_{READ} or I_{CELL}), **read** (data flipping while reading, SNM), **write** (unsuccessful write, VTRIP), and **hold** (data flipping at a lower voltage in standby mode, V_{HOLD}).

The problems mentioned above can produce other side-effects on the SRAM performance and leakage. Those side-effects include the difficulty in performance scaling, and the increasing of leakage in SRAM cell.

Lastly, as the process technology scale, bit-cell and SRAM area is scaling less than 50% [15]. For instances, the bit cell area is greater than 0.5 μm^2 for the 65 nm technology and 0.25 μm^2 for the 45 nm technology.

There have been many solutions discovered and achieved to addresses these problems. The below sections discuss a few read and write assist circuits. They also explain the advantages and disadvantages for each approach.

3.2.2 READ ASSIST CIRCUITS:

Read & Write-back method is an approach to provide data recovery by writing back the original data prior to the disturb [12]. Figure 3.5 shows the read-assist schematic, which features a sense-amplifier (SA) integrated in each sub-array column.

This read-assist circuit provides full Bit-Line (BL) amplification to the half-selected columns, which are idle columns during write or read operations. These half selected columns also contain unstable cells which are vulnerable during the half-selected operations. Full BL amplification improves the discharge rate of the low-node of the cell and provides the data recovery write back mechanism. As a result this discharge rate of the BL helps to reduce the failure of losing data on unstable cells when disturbed.

If BLs, BLC0/BLT0, are written to during a write operation, BLs, BLC1/BLT1, are concurrently sensed and fully amplified. A masking function can be enabled to mitigate the increase in power resulting from generating a full signal swing in all sub-array columns. Signal amplification on half-selected BLs can be inhibited by disabling the MASK signal at the sub-array level. During the masking operation, bit-switch signals BSO and BS1 enable the sense-amplifier activation only on the selected column.

This read & write-back approach requires more power and area overhead for the additional circuits. It is approximately 4% additional circuits in a 128-Word-Line implementation [12].

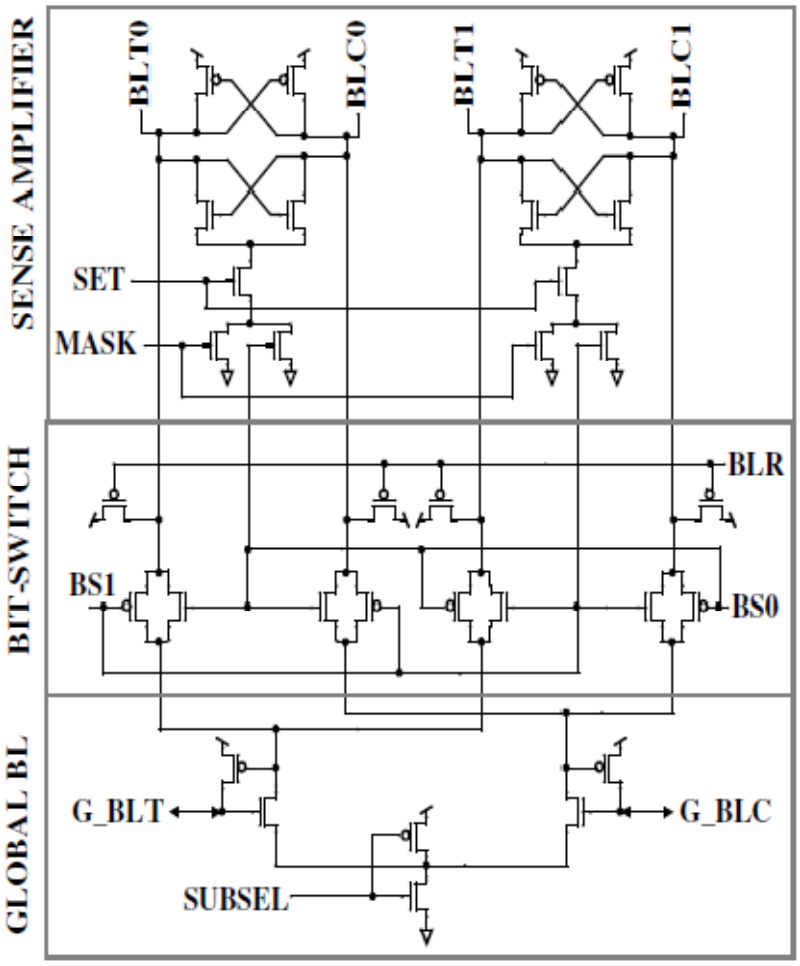

Figure 3.5: Read-assist circuit schematic [12].

Another approach in a read-assist circuit (R-AC) is to lower the Word-Line in an SRAM cell. As discussed in an SRAM read operation section, the node LOW must remains below a switching threshold to avoid a read-disturb condition. Lowering the WL voltage level reduces the read current and then limits the voltage level of node LOW. Figure 3.6 shows the circuit diagram of a Lower Word-Line level approach [13]. Figure 3.7 illustrates the implementation of an R-AC and write-assist (W-AC) circuits in multiple SRAM cell array [13]. In this proposed R-AC, each WL is connected to several

normally-on replica access transistors (RATs), which lower the WL level compared to Vdd.

The decreased SNM in the high Vdd region (>1.2V) is improved by the implementation of R-AC (see Figure 3.7).

A draw-back of this WL lower level R-AC approach is that it makes the write is more difficult due to the reduction of read current. A write-assist circuit by lowering Vdd (by column) was also proposed to address the write operation problem (see Fig. 3.8) which is discussed in the next write-assist circuit section.

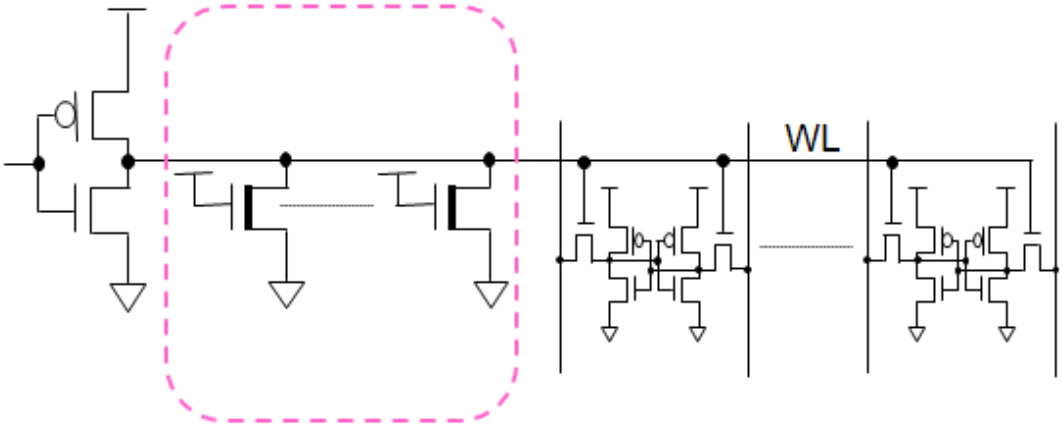

Figure 3.6: Circuit diagram of a read-assist circuit [13].

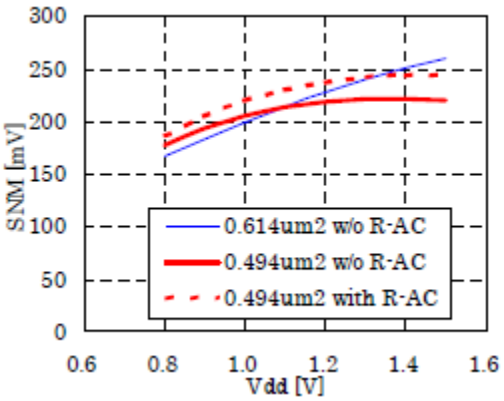

Figure 3.7: Vdd dependence of SNM of 0.614 μm^2 and 0.494 μm^2SRAM with and without read-assist circuit [13].

A read operation on an SRAM cell can be improved by raising the bit-cell voltage VDD level as discussed in a column based dynamic power supply (VCC) scheme below. Figure 3.8 illustrates the distributing of supply voltage to a bit cell in the scheme using Multiplexers [14]. When it is compared to prior work that power supplies are implemented along the word-line direction where Read and Write may happen simultaneously, this makes it very difficult to gain significant improvement on read/write margins. They are because of conflicting requirements on the bit-cell design on a Read and a Write. This scheme allows SRAM voltages to be switched dynamically whether it is a read, a write, a stand-by mode. As a result it helps to improve bit-cell margins in both Read and Write while minimizing the leakage power.

During a read, a higher voltage VDD is connected to the memory cells. It creates a positive voltage different between the cell and WL and consequently increases the bit cell SNM. During a write, it is switched to a lower voltage which creates a negative voltage different between the memory cell and the WL, making the cell easier to flip.

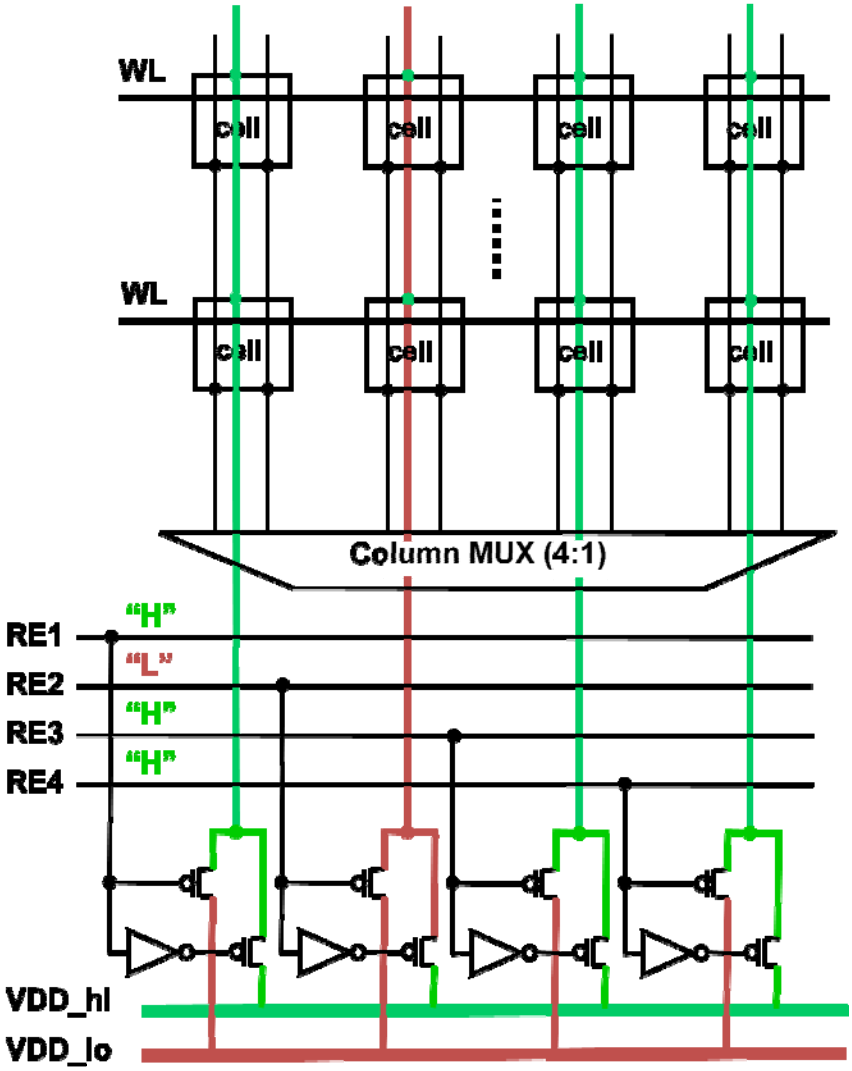

Figure 3.8: Multiplexing power supplies based on Read or Write [14]

Figure 3.8 shows a memory bank containing 4 columns during a write operation. During a read, a entire memory bank is switched to VDD_hi to achieve a better read stability, regardless which column (out of 4 columns) is actually selected for a read. During a write, three out of the four columns are connected to a "dummy read" stress which is switched VDD_hi while the column is actually written is connected to Vdd_lo. When the bank is not selected, it is always switched to VDD_lo to minimize the leakage power.

3.2.3 WRITE ASSIST CIRCUITS:

One of several write-assist circuits in an SRAM cell is a Lower VDD by column W-AC approach. Lowering an SRAM cell voltage Vdd level reduces the current to the pull-up pMOS device. As a result, this assists an SRAM's write operation. Figure 3.9 shows the schematic diagram of capacitive W-AC [13]. Typically, the arvdd wire is not shared between adjacent columns. In this approach the bit-cell VDD is lowered below the WL voltage level through a capacitive charge sharing scheme.

Figure 3.10 explains the wave forms of read and writes cycles [13]. During the read cycle, arvdd = Vdd, and downvdd = GND. During the write cycle, both the arvdd of the selected column and downvdd are put into a floating state and then the arvdd is shorted to the downvdd by the nMOS. So, the voltage level of arvdd falls proportion to the capacity ratio between the arvdd node and the downvdd node.

The proposed W-AC has the advantages compared to other W-AC implementations in that first there is no need to use an additional power supply, and secondly the voltage falling arvdd is rapid and large.

In addition, reducing an SRAM cell voltage Vdd level to have a better SNM for a write operation in a write-assist circuit can be done using a column based dynamic power supply (VCC) scheme as mentioned above in the read-assist circuit (see fig. 3.8). In that read-assist circuit approach an SRAM cell voltage was raised instead.

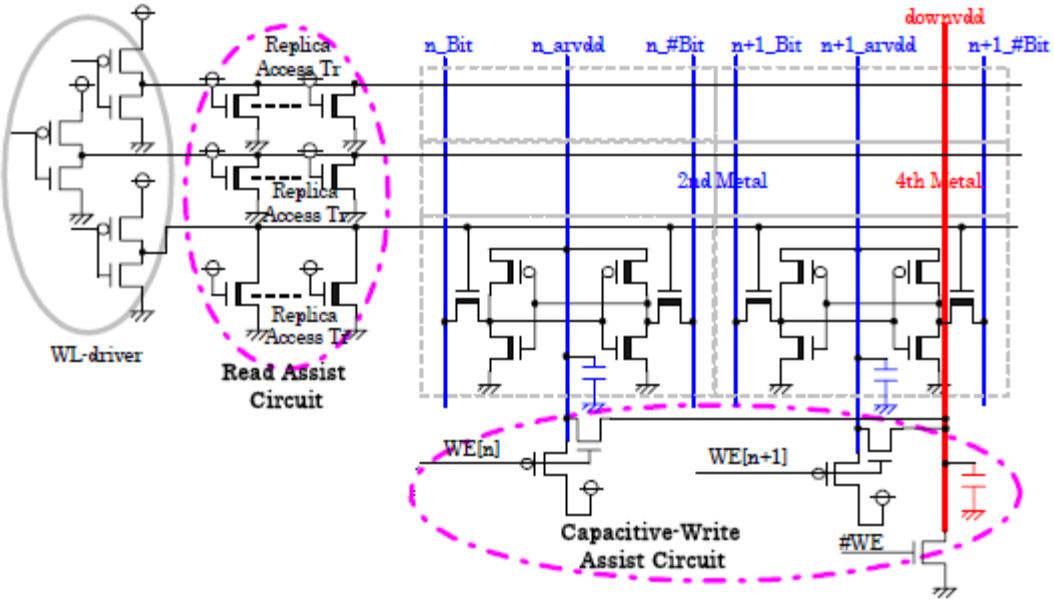

Figure 3.9: Diagram of read-assist and write-assist circuits [13].

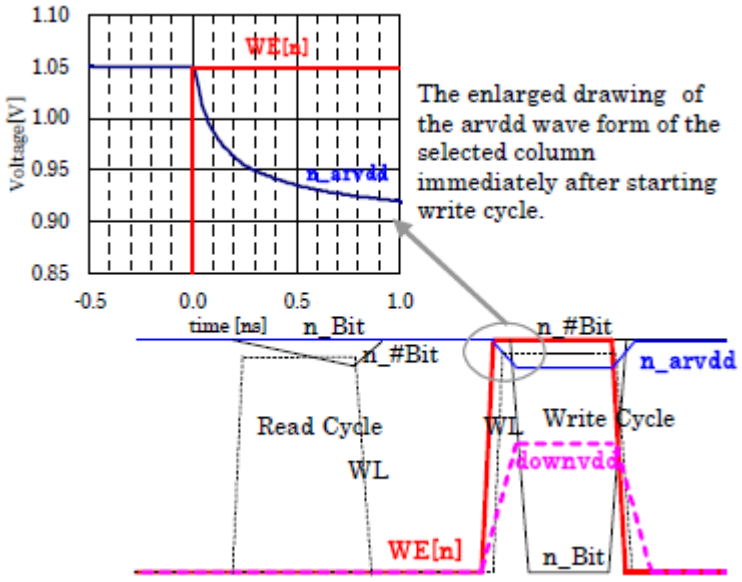

Figure 3.10: The wave form of read and write cycles [13].

Another approach to improve an SRAM cell write-ability is to use a Negative Bit-line Scheme. The principle behind this approach is that a negative voltage at the low bit-line

increases the strength of the access transistor without impacting the strength of the pull-up devices. The write-ability is improved due to the increase of the discharge rate (of an SRAM cell node).

Figure 3.11 shows the technique of the Capacitive Coupling Based Transient Negative Bit-line Voltage (Tran-NBL) scheme [18].

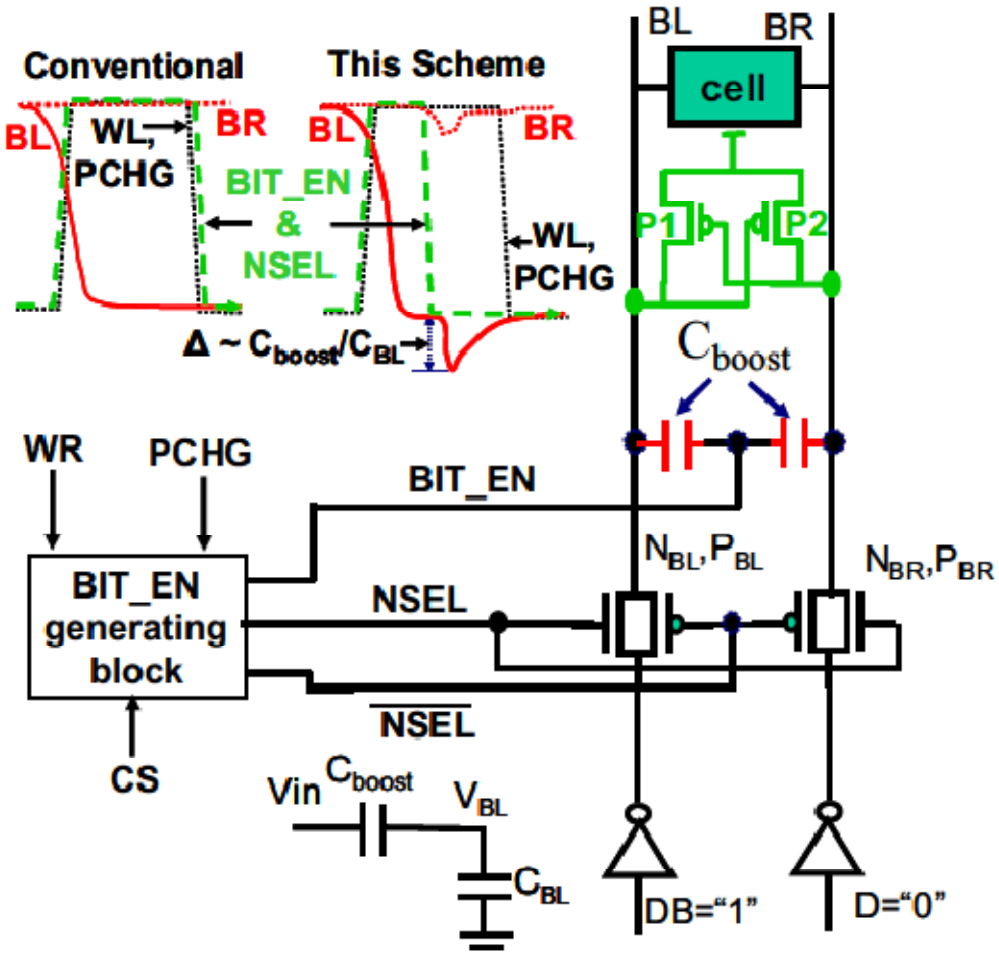

Figure 3.11: The proposed Tran-NBL scheme [18].

In the proposed scheme, as shown in Figure 3.11, the two bit-lines BR and BL are connected to two boosting capacitors, C_{boost_BR} & C_{boost_BL} respectively. The other ends of capacitors are connected to BIT_EN. This BIT_EN is controlled based on pre-charge

signal which is synchronized with other signals such as word-line (WL), read/write (WR), and column select (CS) signals.

In conventional memory operation, pass gates (N_{BL}, P_{BL} & N_{BR}, P_{BR}) are on and the bit-lines are strongly held at ground ("0") and V_{DD} ("1") for entire duration of WL. In this proposed approach, the BIT_EN and NSEL signal are asserted "high" at initial part of WL pulse and de-asserted (to low) at the midway of the WL pulse. This makes both BL & BR bit-lines floating at "0" and "1" respectively. The floating bit-lines go undershot as a result during the high-to-low transition of the signal BIT_EN due to the capacitive coupling through the boosting capacitors. Because the bit-line BL is floating at "0", this results in the negative voltage at the bit-line BL. This transient negative pulse enhances the strength of the access transistor and improves the write-ability.

IV. SRAM CELL DESIGN AND SIMULATION:

As discussed above, a deep sub-micron memory design faces many challenges: one of the biggest challenges is the on-die process variation which is the same challenge that the whole Semiconductor industry faces today. It is widely discussed that the current Semiconductor road-map is getting near the end. The percentage of variability increases and diversifies into many sources such as process induced, environmental, and Physical limit induced variation, etc. These sources of variation can greatly shift the balance of the circuit. Especially in SRAM design where circuit operates in meta-stability state, any shift in Vt, physical dimension can cause SRAM cell to fail. Fortunately, there are many researchers in the Semiconductor industry today who have made progress to compensate for this variability problem and provide solutions such as the Read and Write assist circuits. This report will employ a Write assist into a 256x7 bit memory array to evaluate the total overhead cost including chip area, power consumption and speed.

4.1 SRAM Cell Basic Operation and SNM Simulation

4.1.1 MEMORY BIT-CELL SIMULATION:

The conventional 6-T single port memory bit cell is shown in Figure 4.1. The bit cell is sized and optimized to achieve the best balanced of SNM and Write Margin (WMG).

The simulation of the memory cell was constructed as described in Section SNM above, the transistor sizes were parameterized at Typical Voltage and Temperature to find the optimal SNM. Once the SNM is achieved, the memory cell WMG is then simulated. However, because of the way the memory cell functions, getting the best SNM compromises WMG and therefore the process of optimizing the SNM and WMG need to be repeated in order to achieve performance targets. Figure 4.2 & 4.3 below show the optimal SNM and WMG at the desired 45µA memory cell currents. The SRAM memory cell current is also presented in the Figure 4.4 below.

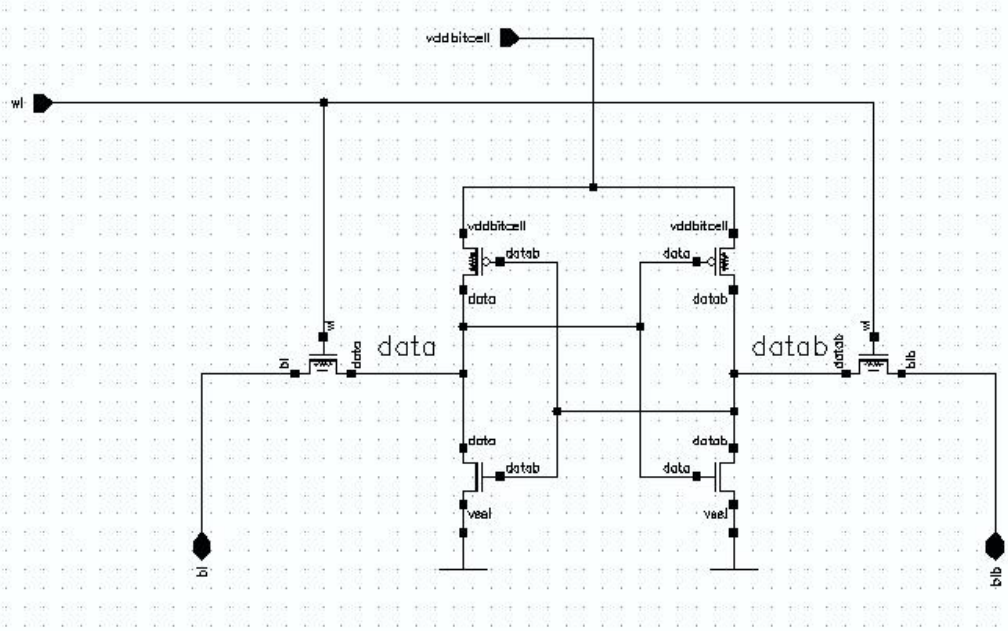

Figure 4.1: Schematic Diagram of a 6-T SRAM Bit-cell.

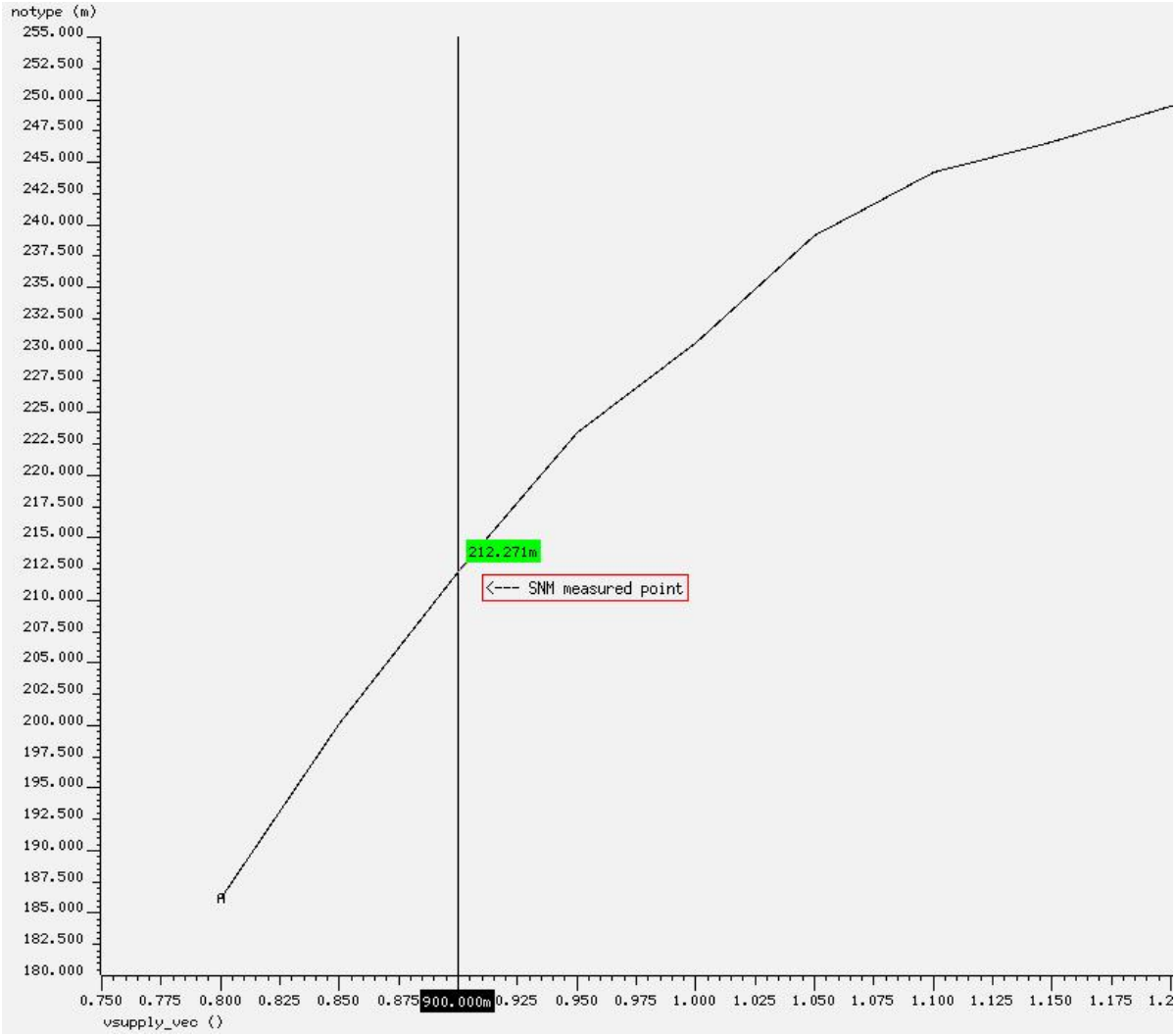

Figure 4.2: Optimal SNM of SRAM Bit-cell.

Figure 4.3: SRAM Bit-cell Write Margin.

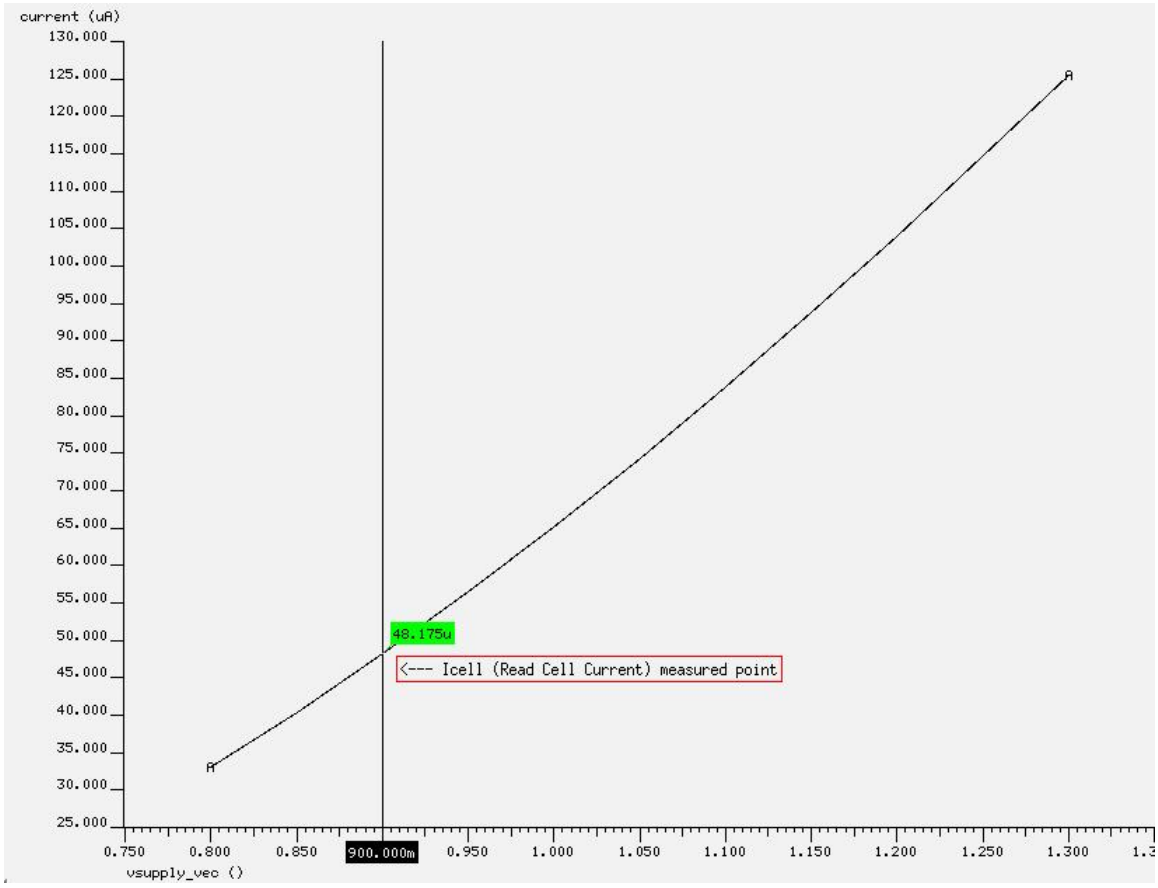

Figure 4.4: SRAM Memory Cell Current.

4.1.2 MEMORY IMPLEMENTATION:

The memory array implemented is arrayed by 256 sets and 7 data bits. The 256 sets are folded into 4-to-1 column with each bit line consists of 64 bits as show in Figure 4.5 below. The folded architecture formed a physical array of 64 sets by 28 columns and consists of three sub-functional units: Array Control Unit, Address Decoding Unit, and Memory Cell Unit as shown in Figure 4.6.

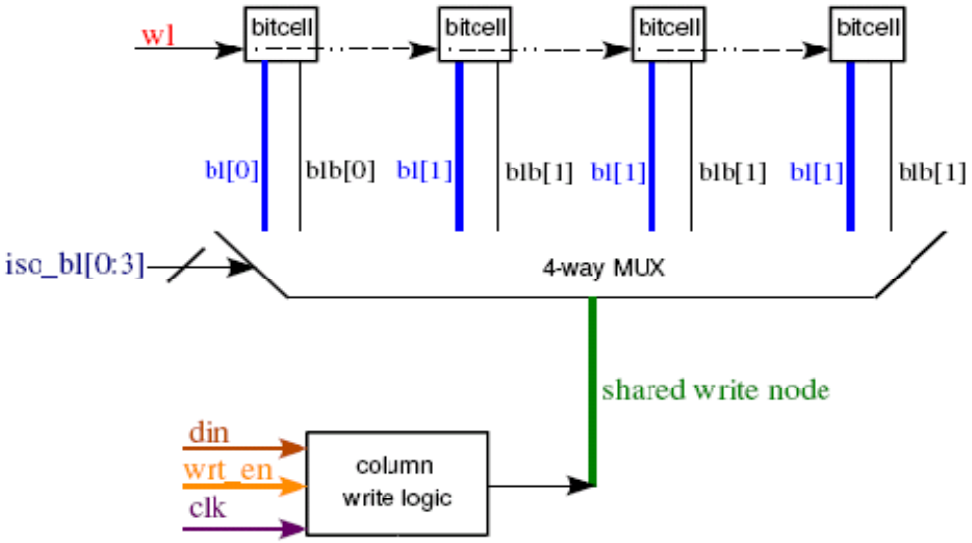

Figure 4.5: Folded Bit Slice Structure of a 4-to-1 Column Mux with Shared Column Write Logic.

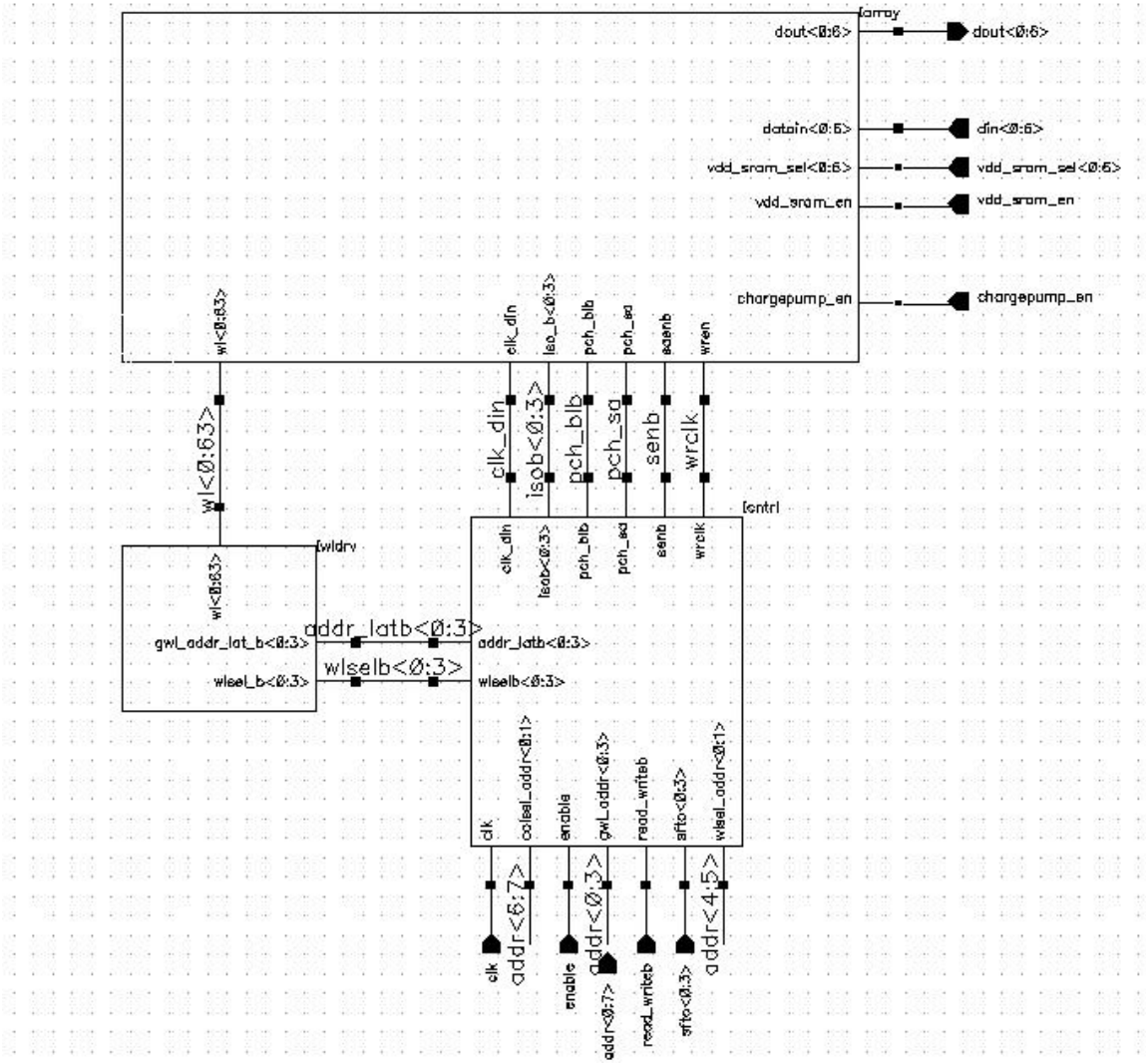

Figure 4.6: Physical Implementation of the Top Level Memory Array.

The Memory Array Control Unit interfaces with the array address, clock, and other array enable signals from external units. The Array Control Unit regenerates the primary input clock to form two internal clocks for memory read and write. The memory read clock, rdclk, is formed from the positive phase and the memory write clock, wrclk, is formed from the negative phase. The read operation is a sense-amplifier based design with a static configurable controller to control the bit line and bit line bar separation which is needed for proper sense-amplification. Figure 4.7 shows timing control of the

memory array which has all the internal control signals manifested from the rising and falling edge of the rdclk. Rising edge of the rdclk enables word-line, sense-amp pre-charge, isolation, bit-line pre-charge, and fires sense-amp. The falling edge of the rdclk de-asserts sense-amp pre-charge, sense-amp signals, while the delay version of the rdclk de-asserts word-line, bit line pre-charge and isolation signals.

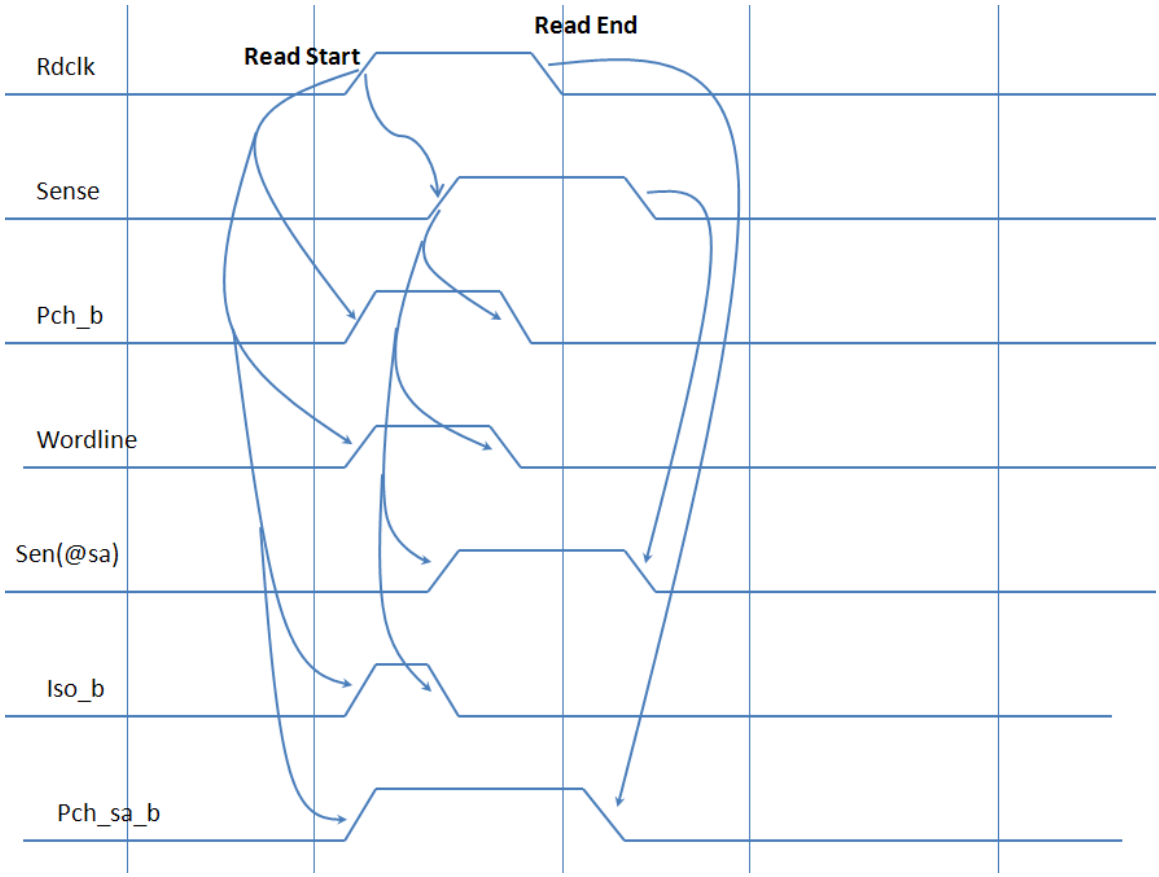

Figure 4.7: Memory Array Read Control Timing Waveform.

The write operation is controlled by an internally generated write clock, wrclk. The wrclk clock is then converted into a pulse which sets the duration for the memory write time. The pulse width is programmable which can be widened to help improve memory cell write-ability. Write Control Timing in Figure 4.8 shows the wrclk clock, which enables word-line, write_pulse, and pre-charge signals, and to setup for a memory write operation.

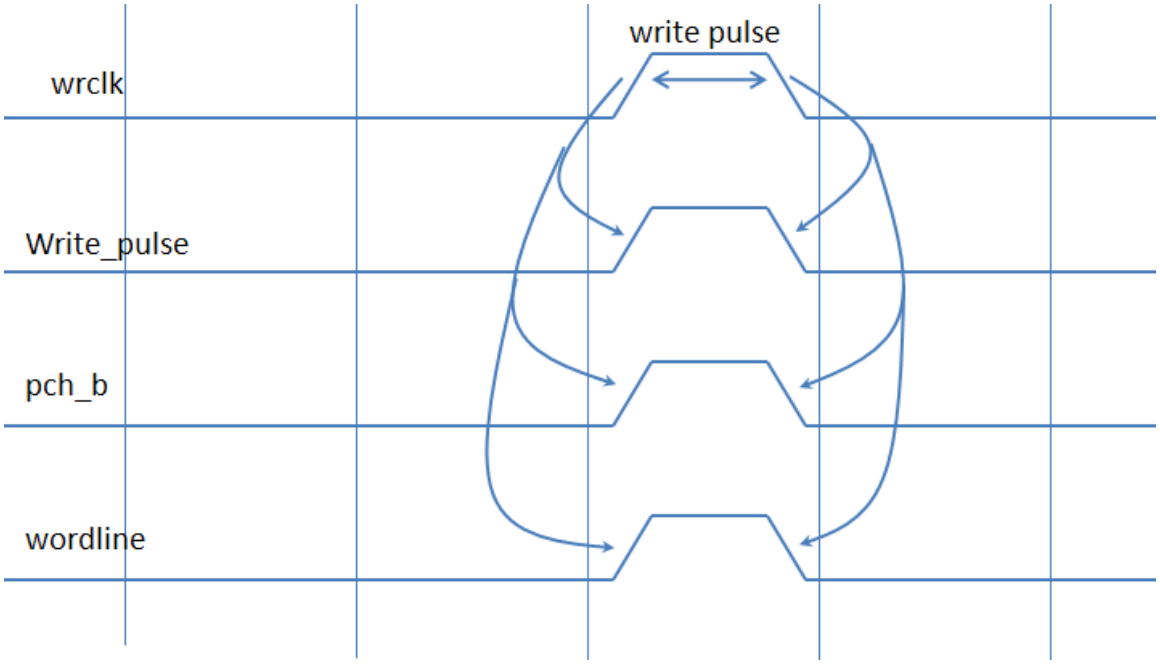

Figure 4.8: Write Control Timing.

The Memory Address Decoding Unit is designed using two stages of AND2 logic scheme. The first stage has two address bits gated with a write clock, wrclk, and decoded into 4-bits. The other four address bits are decoded straight into 16-bits without clock-gating. The 4-bits and 16-bits from the first stage are then decoded into 64-bits word-lines. Each bit in 64-bits is connected uniquely to one set of the memory array which ensures only one set of memory array turns on for every input combination.

Finally, the Memory Array Unit consists of 7 memory array write drivers, a 64x28 memory array bit cells, and 7 columns multiplexer, column logics, sense-amplifiers, and a hold latch for which to capture and hold the data until the next read. The Memory Array Unit also performs column address decoding: the 2 remaining address bits are gated with the rdclk and wrclk through an AOI logic and decoded into 4-bits for 4-to-1 column multiplexer selection. Gating with both clocks enables the array to share both read and write through 4-to-1 column multiplexer and thus power and area are minimized.

4.1.3 SIMULATION RESULTS:

4.1.3.1 Read Operation:

The waveform in Figure 4.9 below is the actual simulation result which shows a successful read. Similar to the concept description in Figure 4.7, when rdclk rises, the bit-line pre-charge signal de-asserts and word-line signal is asserted to allow the bit-line and bitline_b signals to develop a differential. When there is enough separation between bit-line and bitline_b, the sense-amplifier signal is fired and the read data is captured in the hold latch and will remain there until next read. The array access time shows in Table 4.1 below is a worst case delay which is accessed from set (row) 64 and bit 28 of the memory array.

Delay Path	Delay in Picosecond (ps)
Clk → wordline	122ps
Word-line → sense-amp	110ps
Sense-amp	34ps
Hold Latch	36ps
Rdclk → data_out7	302ps

Table 4.1: Worst Case Array Access Timing.

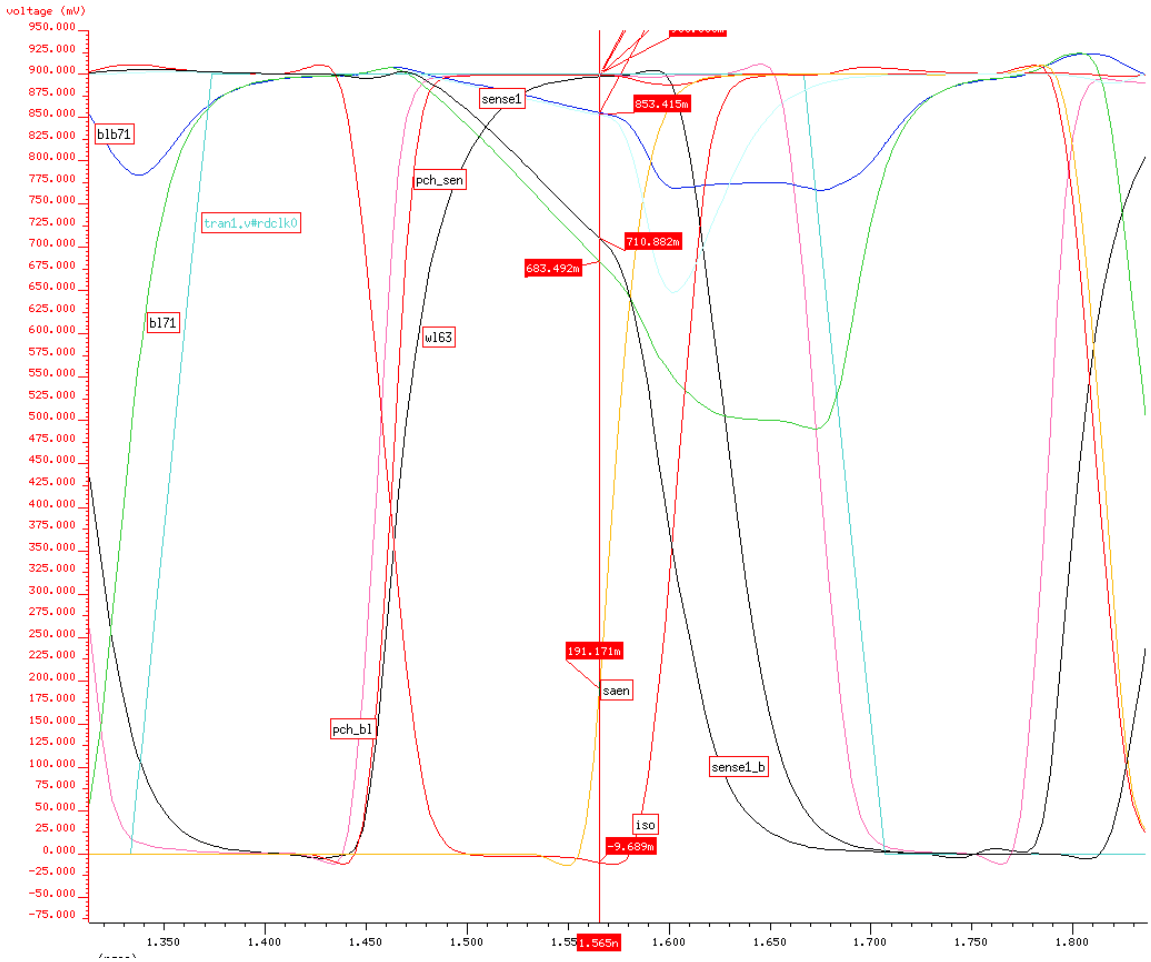

Figure 4.9: Memory Array Read Operation.

4.1.3.2 Write Operation:

The waveform in Figure 4.10 below is the actual simulation result of a successful memory write. Again, similar to concept described in Figure 4.8, when the wrclk rises, the bit-line pre-charge signal de-asserts leaving bit-line and bitline_b in un-driven state. Since the bit-line and bitline_b have been pre-charged to the VDD level, both will stay in pre-charged state until the write occurs. The word-line is then asserted to allow the write_pulse signal to pull the bit-line (or bitline_b) to the ground, forcing a logic value into the memory array. Once the data/datab (content of the memory cell) node is fully

stored in the memory cell, the write is succeeded and the word-line and the write_pulse are de-asserted, the pre-charge (pch_b) is asserted.

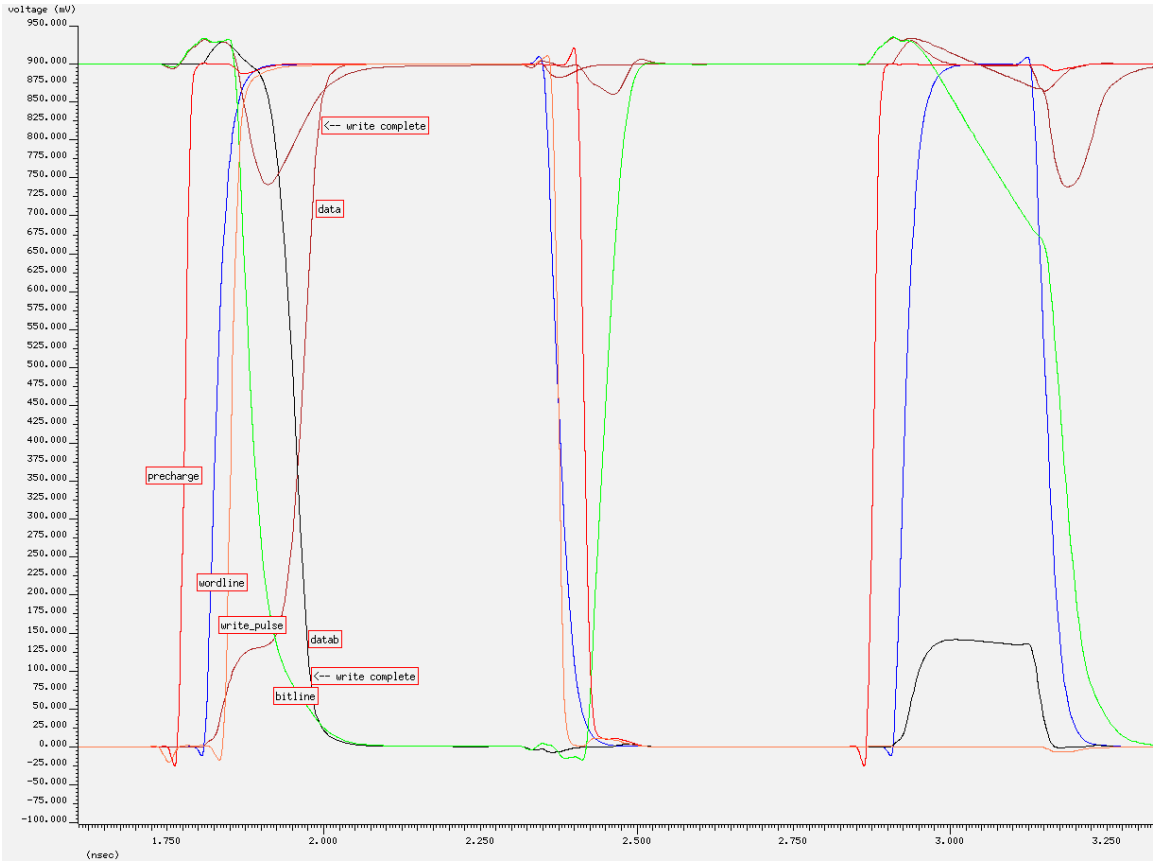

Figure 4.10: Waveform of a Successful Write.

Table 4.2 shows power consumption for the memory array operates at 1.5GHz.

Corner & Freq.	Read(Avg current)	Write (Avg current)	Leakage
Typ @1.5Ghz	9.3mA	5.3mA	1.038mA

Table 4.2: Power Consumption for the Memory Array Operates at 1.5GHz

Table 4.3 shows complete write margins that are required for a successful write and also keeping the memory cell stable.

Margins	Write margin in (ps)
Precharge Deassert → Word-line Assert	-12ps
Precharge Deassert → write_pulse Assert	10ps
Write_Pulse Assert → word-line Assert	16ps
Write_Pulse Width	266ps
Write Time(20% write pulse → 95%VDD data)	178ps
Write Complete (95%VDD data → 20%Wordline)	91ps
Write_Pulse Deassert → Precharge Assert	-5ps
Word-line deassrt → Precharge Assert	-16ps

Table 4.3: Complete Write Margins.

For memory robustness, the lower voltage and colder temperature of the memory write is also simulated. The memory appears to work well in simulation even at 0.7V and 0^0C temperature. However, when the voltage and lower temperature were further pushed down, the memory array failed to write at 0.6V and -25^0C temperature. Figure 4.11 shows unsuccessful memory write.

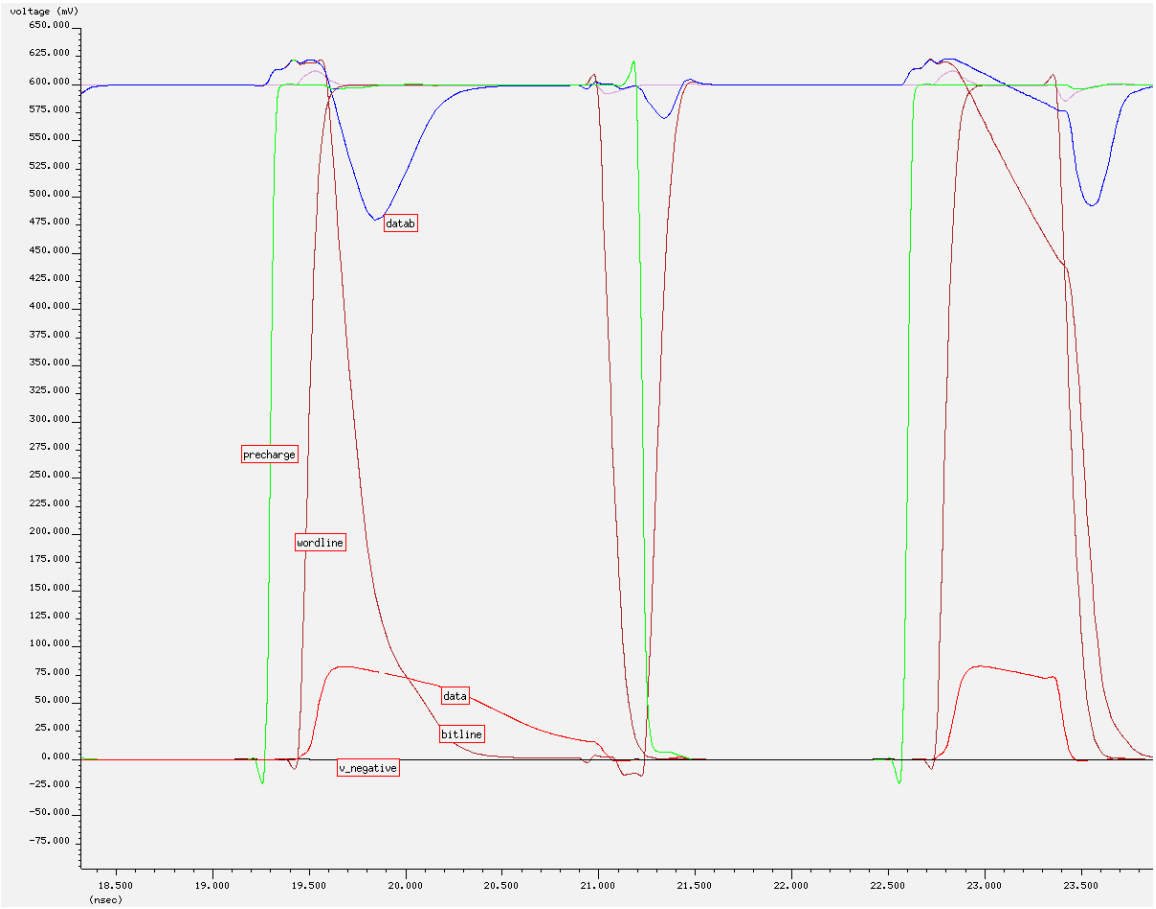

Figure 4.11: Memory Cell Unable to Switch in Write.

4.2 Write-Assist Circuit: Negative Bit-line Voltage Scheme

As technology shrinks, the process variability become greater and poses greater impact to memory array and thus makes it more difficult and even fail to write. There are several design techniques including Negative Bit-line Voltage Bias that can be used to improve write robustness. The below implementation integrates the Negative Voltage Bias mechanism to the basic memory designed above to evaluate the necessity of the memory write assist.

The design employs a Negative Charge-Pump as shown in Figure 4.12. When in used, the negative charge-pump pumps negative charge through a series of PMOS

devices and stored them in a capacitor to create a negative potential. The capacitor is ensures to be capable enough to hold the total charge that pulled down from 7 bit-lines during a full memory write. The Negative Voltage Bias Unit is then gated off with a write enable signal to deactivate the charge-pump when the memory is not in write. The number of stages chosen for the charge-pump is based on a constraint of -250mV in 1 clock cycle.

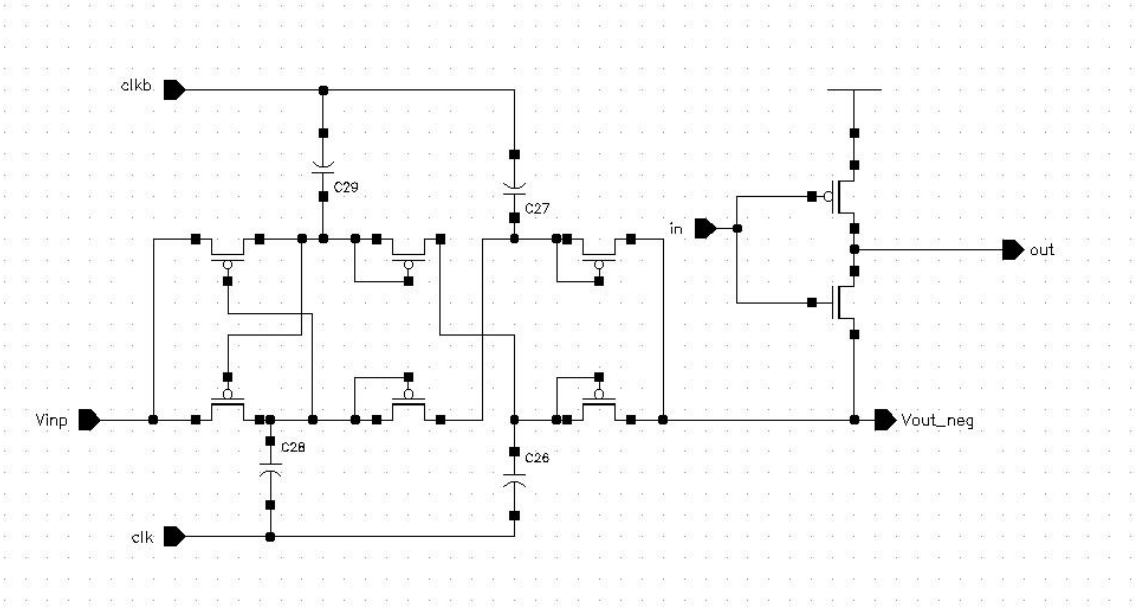

Figure 4.12: Negative Charge-Pump Circuit Diagram.

Figure 4.13 shows simulation result of the integrated charge-pump. Before the write, the charge-pump enable signal is asserted to generate a -250mV. When the write occurs, the bit-lines are pulled to the negative voltage which results in a significant positive charge added to the capacitor that holding the negative charge. The positive charge, therefore, cancelled out the negative charge and pulled the negative voltage closer to the neutral ground (0V). However, even at the -70mV on the bit-line, the memory shows a successful write at 0.6V and -25^0C which previously failed to write without write assist. The power consumption is also recorded and reported in Table 4.4 which shows slightly increase during write, but quite significant increased in leakage.

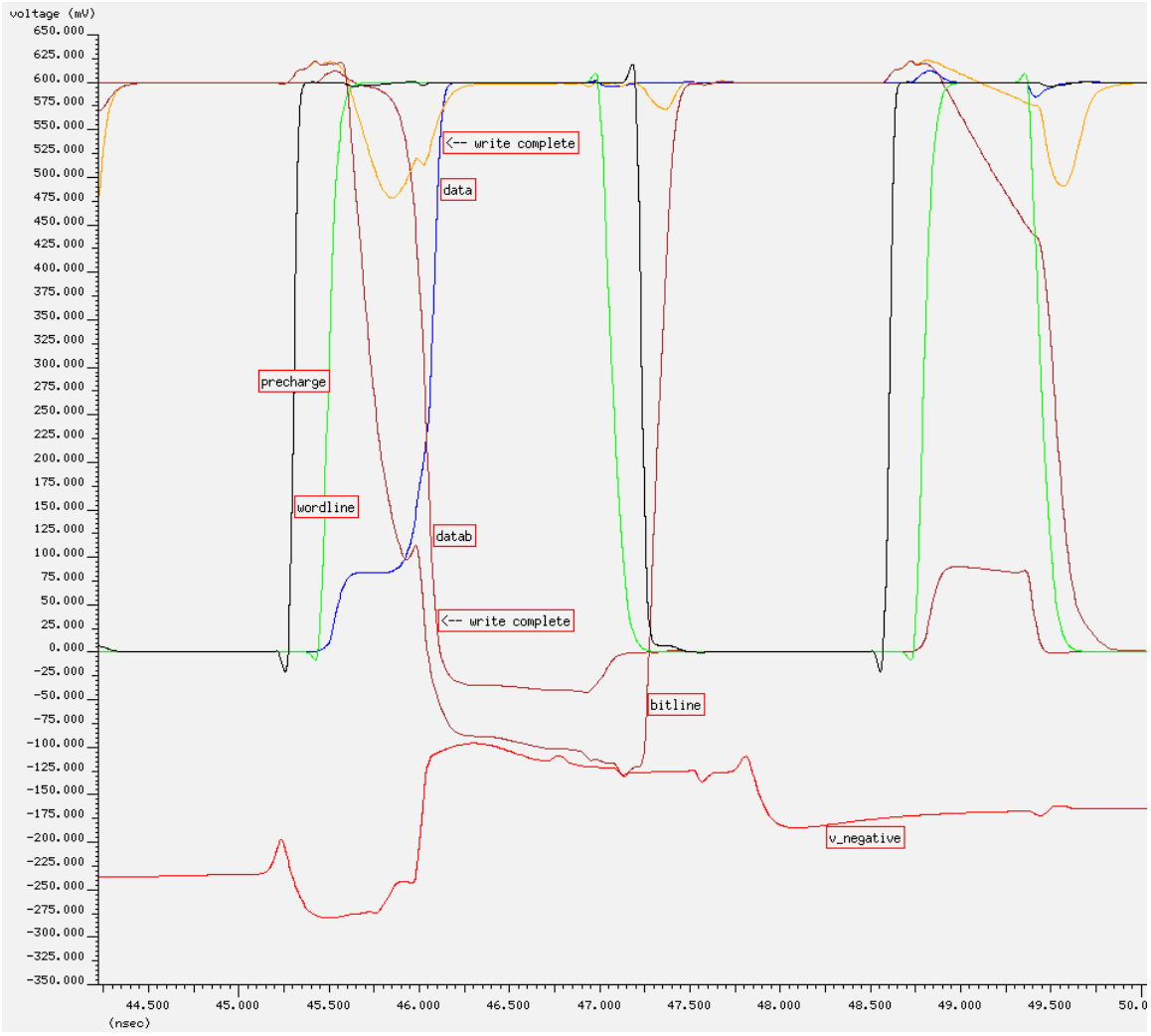

Figure 4.13: A Successful Write on Memory Cell with Negative Charge-Pump Implemented.

Corner & Freq.	Read(Avg current)	Write (Avg current)	Leakage
Typ @1.5Ghz	9.3mA	6.334mA	2.58mA

Table 4.4: Power Consumption for Integrated Charge-pump Memory Array

V. CONCLUSION:

Memory array design is facing many challenges as technology node shrinks. Many issues such as process variation, voltage scaling, soft-error rates can make memory array to fail more easily than ever before. Designing a robust system with a large memory capacity requires memory designers to create more sophisticated and complex solutions to ensure system reliability and robustness. One of the design techniques that help improving memory write-ability is the Negative Bit-line Voltage Bias write assist. Based on the results shown in this report, the design memory array achieved a successful write operation at (0.6V and -25^0C) which otherwise would fail without the write assist. The read access time is unchanged compares as expected because the charge-pump is deactivated during read. Although, the result seems promising, there are other design factors such as size, power consumption, need to be put into consideration. The overhead cost in area of the charge-pumps circuits and holding capacitors, along with their additional power consumption can be significant for cost sensitive products.

Appendix A

DERIVATION OF SNM FOR 6-T SRAM CELL

The long-channel MOS equations are:

$$I_{D(sat)} = \frac{1}{2}\beta(V_{GS} - V_{TH})^2 \qquad (3.1)$$

and

$$I_{D(lin)} = \beta(V_{GS} - V_{TH} - \frac{1}{2}V_{DS}) \qquad (3.2)$$

Employing the two long-channel MOS equations (3.1 & 3.2) for the circuit in Figure 3.4 (as above and assuming that transistors Q1 and Q4 are saturated and transistors Q2 and Q5 are in the linear mode.

$$(V_{GS1} - V_{TH})^2 = \frac{2q}{r}V_{DS5}(V_{GS5} - V_{TH} - \frac{1}{2}V_{DS5}) \qquad (3.3)$$

$$(V_{GS4} - V_{TH})^2 = 2rV_{DS2}(V_{GS2} - V_{TH} - \frac{1}{2}V_{DS2}) \qquad (3.4)$$

where V_{TH} of NMOS transistors in the cell is assumed V_{TH} of PMOS transistor and $q = \beta_p/\beta_a, r = \beta_d/\beta_a$.

The Kirchhoff equations for the 6T SRAM cell are:

$$V_{GS1} = V_n + V_{DS2} \qquad (3.5)$$

$$V_{DS5} = V_{DD} - V_n - V_{GS2} \qquad (3.6)$$

$$V_{GS5} = V_{DD} - V_n - V_{DS2} \qquad (3.7)$$

and

$$V_{GS4} = V_{DD} + V_{DS2} \qquad (3.8)$$

Substituting Equations 3.5-3.8 into Equations 3.3 and 3.4 yields:

$$(V_{DS2} + V_n - V_T)^2 = \frac{q}{r}(V_{DD} - V_n - V_{GS2}) \times (V_s - V_{TH} - V_n - 2V_{DS} + V_{GS2}) \quad (3.9)$$

$$(V_s - V_{DS2})^2 = 2rV_{DS2}(V_{GS2} - V_{TH} - \frac{1}{2}V_{DS2}) \qquad (3.10)$$

where $V_s = V_{DD} - V_{TH}$

Eliminating $V_{GS2} and\ V_{DS2}$ from equations 3.9 and 3.10 yields a fourth-degree equation. Assuming local linearity of the transfer characteristic on inverter Q2-Q4 around its operating point where Q2 in linear region, it can be simplified as [11]:

$$V_{DS2} = V_0 - kV_{GS2} \qquad (3.11)$$

where $V_r = V_s - (\frac{r}{r+1})V_{TH}$ (3.12)

$$k = \left(\frac{r}{r+1}\right)\left(\sqrt{\frac{r+1}{r+1-\frac{V_s^2}{V_r^2}}} - 1\right) \qquad (3.13)$$

$$V_0 = kV_s + (\frac{1+r}{1+r+{}^{r}/_{k}})V_r \qquad (3.14)$$

Eliminating V_{0ds2} from Equations 3.9 and 3.10 and simplification, we obtains:

$$X^2\left(1 + 2k + \frac{r}{q}k^2\right) + 2X\left(\frac{r}{q}kA + A + V_{TH} - V_s\right) + \frac{r}{q}A^2 = 0 \quad (3.15)$$

where $X = V_{DD} - V_n - V_{GS2}$ (3.16)

$$A = V_0 + (k+1)V_n - kV_{DD} - V_{TH}$$

The double-root stability criterion was applied to Equation 3.15. Next, when Equation 3.16 is substituted, Equation 3.15 can be solved for the dc disturbance represented by V_n to obtain the SNM:

$$SNM_{6T} = V_{TH} - \left(\frac{1}{k+1}\right) \times \left(\frac{V_{DD} - \frac{2r+1}{r+1} V_{TH}}{1 + \frac{r}{k(r+1)}} - \frac{V_{DD} - 2V_{TH}}{1 + k\frac{r}{q} + \sqrt{\frac{r}{q}(1 + 2k + \frac{r}{q}k^2)}} \right) \tag{3.17}$$

Bibliography

1. Meixner and J. Banik. Weak write test model: An SRAM cell stability design for test technique. In Proc. IEEE International Test Conferrence (ITC), pages 1043-1052, November 1997.
2. D.-W. Kwai, H.-W. Chang, H.-J. Liao, C.-H. Chiao, and Y.-F. Chou. Detection of SRAM cell stability by lowering array supply voltage. In Proc of the Ninth Asian Test Symposium (ATS 2000), pages 268-273, December 2000.
3. C. Kou, T. Toms, B.T. Neel, J. Jelemensky, E.A. Carter, and P. Smith. Soft-defect detection (SDD) technique for a high-reliability CMOS SRAM. IEEE Journal of Solid-State Circuits (JSSC), 25:61-67, February 1990.
4. ITRS. International Technology Roadmap for Semiconductors - 2003 (ITRS-2003); http://public.itrs.net/
5. ITRS. International Technology Roadmap for Semiconductors (ITRS-2004) update; http://public.itrs.net/common/2004update/2004update.htm
6. Vishwani D. Agrawal. CMOS SRAM Circuitry Design and Parametric Test in Nano-Scaled Technologies, edited by Pavlov, Andrei and Sachdev, Manoj. Location: Springer, January 01, 2008.
7. Anantha Chandrakasan, William J. Bowhill, and Frank Fox. Design of High-Performance Microprocessor Circuits. New York: IEEE Press, 2001.
8. A. Bhavnagarwala, X. Tang, and J. Meindl. "The impact of intrinsic device fluctuation on CMOS SRAM cell stability." IEEE Journal of Solid-State Circuits (JSSC), 36:658-665, April 2001.
9. F. Lai and C. Lee. "On-chip voltage down converter to improve SRAM read-write margin and static power for sub-nano CMOS technology." IEEE Journal of Solid-State Circuits(JSSC), 42:2061–2070, September 2007
10. J. Lohstroh, E. Seevinck, and J. de Groot. "Worst-case static noise margin criteria for logic circuits and their mathematical equivalence." IEEE Journal of Solid-State Circuits (JSSC), SC-18:803–807, December 1983.
11. E. Seevinck ,F. List, and J. Lohstroh. "Static-noise margin analysis of MOS SRAM cells." IEEE Journal of Solid-State Circuits (JSSC), SC-22:748–754, October 1987.
12. Harold Pilo, John Barwin, Geordie Braceras, Chistopher Browning, Steve Burns, John Gabric, Steve Lamphier, Mark Miller, Al Roberts, Fred Towler, "An SRAM

Design in 65nm and 45nm Technology Nodes Featuring Read and Write-Assist Circuits to Expand Operating Voltage," 2006 Symposium on VLSI Circuits, IBM.

13. Azeez Bhavnagarwala, Stephen Kosonocky, Stephen Kowalczyk, Rajiv Joshi, Yuen Chan, Uma Srinivasan, Jatinder Wadhwa, "A Transregional CMOS SRAM with Single, Logic VDD and Dynamic Power Rails", 2004 Symposium on VLSI Circuits, IBM.
14. Kevin Zhang, Uddalak Bhattacharya, Zhanping Chen, Fatih Hamzaoglu, Daniel Murray, Narendra Vallepalli, Yih Wang, Bo Zheng, Mark Bohr, "A 3GHz 70Mb SRAM in 65nm CMOS Technology with Integrated column-Based Dynamic Power Supply" IEEE Journal of Solid-State Circuits, vol 41, no. 1, Jan 2006, Intel.
15. Michael Clinton, "Variability and SRAM Design", [Presentation], Feb 2008.
16. Makato Yabuuchi1, Koji Nii1, Yasumasa Tsukamoto1, Shigeki Ohbayashi1, Susumu Imaoka2, Horoshi Makina1, Yshonobu Yamagami3, Satoshi Ishikura3, Toshio Terano3, Toshiyuki Oashi1, Keiji Hashimoto1, Akio Sebe3, Gen Okazaki3, Katsuji Satomi3, Hironori Akamatsu3, Hirofumi Shinohara1, "A 45nm Low-Standby-Power Embedded SRAM with Improved Immunity Against Process and Temperature Variations", IEEE International Solid-State Circuits Conference 2007, 1-Renesas Technology, 2-Renesas Design, 3-Matsushita.
17. J. Bhavnagarwala, X. Tang, and J. D. Meindl, "The impact of intrinsic device fluctuations on CMOS SRAM cell stability," IEEE J. Solid-State Circuits, vol. 36, no. 4, pp. 658–665, Apr. 2001.
18. S. Mukhopadhyay, R. Rao, J. J. Kim, C. T. Chuang, " Capacitive Coupling Based Transient Negative Bit-line Voltage (Tran-NBL) Scheme for Improving Write-ability of SRAM Design in Nanometer Technologies", IEEE International Symposium on Circuits and System, 2008.

Vita

QuocDat Tai Nguyen was born in Saigon, Viet Nam. During the third year of his studying at HoChiMinh City University of Technology in 1994, he and his family immigrated to the United States. QuocDat received his Bachelor's degree in Electrical and Computer Engineering at the University of Houston in summer 2001. QuocDat had an internship position and have joined Dell inc. for a full-time position since 2001. QuocDat have worked in an Enterprise Solution Engineering group in which the main job functionalities are to evaluate and engineering develop Fibre Channel/iSCSI and SAN based storage system products/solutions and applications for enterprise customers. During his full-time position at Dell, he attended the graduate school of engineering at the University of Texas at Austin in spring 2006.

Permanent address (or email): 1811 Montana Sky Dr. Austin, TX 78727

This report was typed by QuocDat Tai Nguyen.