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A new asymmetric 6T SRAM cell with a write assist technique in 65 nm CMOS technology

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ABSTRACT

A new asymmetric 6T-SRAM cell design is presented for low-voltage low-power operation under process variations. The write margin of the proposed cell is improved by the use of a new write-assist technique. Simulation results in 65 nm technology show that the proposed cell achieves the same RSNM as the asymmetric 5T-SRAM cell and 77% higher RSNM than the standard 6T-SRAM cell while it is able to perform write operation without any write assist at $V_{DD}=1$ V. Monte Carlo simulations for an 8 Kb SRAM (256×32) array indicate that the scalability of operating supply voltage of the proposed cell can be improved by 10% and 21% compared to asymmetric 5T- and standard 6T-SRAM cells; 21% and 53% lower leakage power consumption, respectively. The proposed 6T-SRAM cell design achieves 9% and 19% lower cell area overhead compared with asymmetric 5T- and standard 6T-SRAM cells, respectively. Considering the area overhead for the write assist, replica column and the replica column driver of 2.6%, the overall area reduction in die area is 6.3% and 16.3% as compared with array designs with asymmetric 5T- and standard 6T-SRAM cells.

1. Introduction

CMOS technology has been the cornerstone of semiconductor devices for years. Moore's law predicts technology down scaling that leads to improvements in performance features such as speed, power consumption and area. Although circuits and systems benefit from technology down scaling in some aspects, the undesired features such as short channel effects (SCEs) and sensitivity to process variations are also consequential. The effect of process variations on performance is a key issue in scaled CMOS technology. This effect gets more pronounced as the size of transistors is reduced. One of the highly sensitive circuits to process variations is SRAM that is due to the use of small devices in order to achieve a higher density. Process variations can be due to global or local mismatches between devices. Global variation refers to die-to-die variations in devices and local mismatch refers to mismatch between transistors on the same die [1]. Local mismatch in SRAM devices can easily lead to read stability degradation (stored data is flipped during read), read failure (data is not read during read period), writeability decrease or write time increase. Besides, improving the write features of the SRAM leads to degradation in its read performance and vice versa.

Fig. 1 shows the standard 6T-SRAM cell structure. It consists of two back to back inverters (PUL–PDL and PUR–PDR) which keep the data and its inverse on nodes Q and QB, respectively. The access transistors (ACL–ACR) are used to perform read and write operations. Due to using a common path (ACL–ACR) for read and write, improving read stability will lead to degradation of writeability of the cell and vice versa. To improve the Read Static Noise Margin (RSNM) of an SRAM cell, beta ratio ($\beta=W_{PD}/W_{AC}$) can be increased, while a lower alpha ratio ($\alpha=W_{PU}/W_{AC}$) is desirable to improve the cell writeability. Finally, during hold mode, equal strength for pull up and pull down transistors sets the trip point of the two back-to-back inverters at $V_{SUPPLY}/2$ and ensures maximum noise margin.

Several solutions have been proposed in the literature from device to architecture levels to improve SRAM cell functionality. For instance, at device level, using new devices such as FinFETs leads to significant SRAM performance improvement [1–4]. At cell level, new cells such as 7T, 8T, 9T, 10T, and 11T [5–11] have been proposed that come with a penalty in area overhead while other proposed cells such as asymmetric 6T and 5T topologies [12,13] occupy the same area compared to the standard symmetric 6T SRAM cell. At architecture level, read and write assist techniques improve SRAM robustness and performance while they occupy

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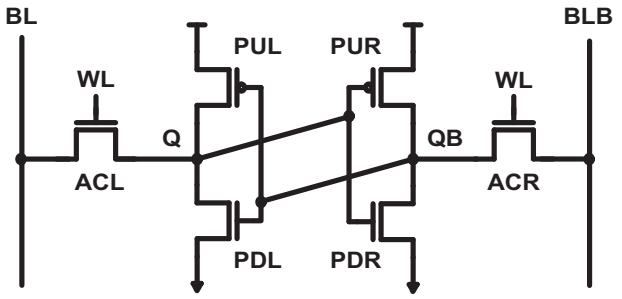

Fig. 1. The standard 6T-SRAM cell.

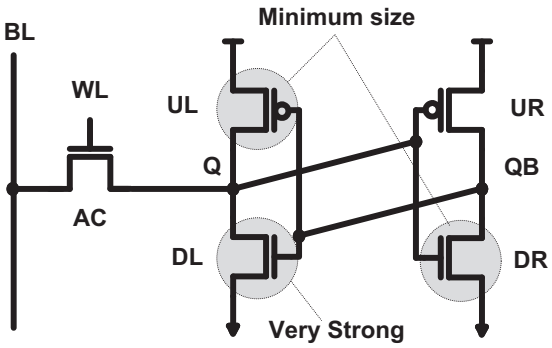

Fig. 2. The asymmetric 5T-SRAM cell [12].

less area in comparison with the cell techniques (e.g. 8T and 10T) and can be utilized with any SRAM cell [14–23].

Memories take up 80% of the die area in high performance processors [24]. Hence, there is a crucial need for a low-leakage, high density, and highly robust SRAM design. Amongst different cell topologies, the asymmetric 5T-SRAM cell is one of the best candidates in order to achieve high density. However, the write margin of the 5T-SRAM cell degrades drastically and this limits the lowering of the supply voltage. This in turn restricts the improvement of the cell leakage power.

In this paper, a new asymmetric 6T-SRAM cell is proposed which can significantly improve read and write performance with less area. The asymmetric 6T-SRAM cell has the advantage of using transmission gate as access device which improves the writeability of the cell. In addition, applying a write assist technique improves the robustness of the cell. It allows SRAM to work at lower supply voltages and this leads to lower leakage power consumption.

Moreover, a new write assist technique that improves the write margin of the proposed 6T-SRAM cell is proposed. The proposed write assist technique applies a boosted voltage ($V_{DD}+\Delta V$) to the bitline during write '1' on the cell. This technique results in significant improvement in the Write Margin (WM) and the Write Time (WT). In this technique, coupling capacitances are used to produce boosted voltages.

The remainder of the paper is organized as follows. In Section 2, a brief survey of existing asymmetric SRAM cells is presented. In Section 3, the basic concept of the proposed asymmetric cell and the proposed boosted bitline (BBL) technique is presented and validated by mathematical analysis. The efficacy of the BBL technique on the proposed 6T-SRAM cell is shown in Section 4 through simulations. Finally, conclusions are drawn in Section 5.

2. State of the art

In this section, the existing asymmetric SRAM cell and the write assist techniques which can improve its inability to write '1' are discussed.

2.1. Asymmetric SRAM cell

Asymmetric SRAM topologies use asymmetric sizing of the cross-coupled inverters to increase RSNM of the standard 6T-SRAM cell with the same size at the cost of WM reduction during write '1' on the cell. Considering the fact that RSNM limits the SRAM operation at lower supply voltages, the RSNM improvement allows scaling down the operating supply voltage. Decreasing the minimum supply voltage together with single-ended access in asymmetric SRAM cells reduces the leakage power consumption. The asymmetric 5T-SRAM cell in [12] is shown in Fig. 2. Two different sizing scenarios used in [12] shown in Fig. 2 are 1) maximum RSNM (RSNM Max) and 2) maximum WM (WM Max). In this cell, asymmetric sizing is used for the cross-coupled inverters. The strong pull down transistor (DL) connected to the access transistor decreases the increment in the voltage of storage node (V_Q) during read. Moreover, using minimum size pull down transistor (DR) in the inverter with its input connected to Q (right hand) increases its trip point. The above changes including the lower increase in V_Q and higher trip point in the right hand inverter significantly improve RSNM of the asymmetric 5T-SRAM cell. The main drawback of the asymmetric SRAM cell during write mode is when writing '1' without any write assist. This is attributed to the strong pull down transistor and the very large bitline capacitance.

2.2. Write assist techniques

In order to improve write margin of SRAMs, several write assist techniques have been proposed. Some of these techniques rely on cell V_{DD} collapse [14–17], Negative Bit-Line (NBL) [18–22], Boosted Word-Line (BWL) and cell GND boost [23]. Amongst the existing proposed techniques, NBL write assist is the most effective one to reduce SRAM minimum supply voltage, especially when considering dynamic failure metrics [25]. This technique improves the writeability of the cell while writing '0'. However, the NBL technique is appropriate for the dual bitline cells (e.g. standard 6T/8T) as they always have one low-going store node connected to the bitline while it cannot be applied to the 5T-SRAM cell during write '1' operation.

The BWL technique increases the word line voltage (V_{WL}) connected to the gate of AC transistor (Fig. 2) during write operation. This increases the gate source voltage of AC ($V_{GS\text{-}AC}$) and improves its driveability. However, when writing '1' in asymmetric 5T-SRAM cell, $V_{GS\text{-}AC}$ is determined by the word-line and store node voltages ($V_{GS\text{-}AC}=V_{WL}-V_Q$). Hence, during write '1' operation, $V_{GS\text{-}AC}$ will be decreased by increasing V_Q which leads to significant decrease in access transistor driveability. As a result, the BWL technique is not an effective method to deal with the write '1' weakness of asymmetric 5T-SRAM cells. Hence, there is a need for a write assist technique to improve the writeability of asymmetric SRAM cells which suffer from inability to write '1'.

Cell V_{DD} collapse and cell GND boost techniques can be used in asymmetric single-ended cells in order to improve write '1' and write '0' margins. However, these are much less effective than the NBL write assist technique [25]. On the other hand, these techniques degrade the Hold Static Noise Margin (HSNM) of the half-selected cells and are not suitable for low voltage applications.

To this end, a new asymmetric 6T-SRAM cell is proposed in the following section that improves the write margin and write time. In this cell, a transmission gate is used as the access device.

Therefore, the 5T-SRAM cell is converted to a 6T-SRAM cell. At the same time the drawbacks of 5T-SRAM cell during write '1' are resolved. A new write assist circuit is also proposed that improves write margin and allows the SRAM cell to work properly at lower supply voltages.

3. The proposed asymmetric 6T-SRAM cell and write assist technique

In this paper a new asymmetric 6T-SRAM cell with improved write margin and write time and a new write assist technique that improves write margin are proposed.

3.1. The proposed asymmetric 6T-SRAM cell

The proposed asymmetric 6T-SRAM cell is shown in Fig. 3. Unlike the standard 6T-SRAM cell, back to back inverters are asymmetrically sized to improve the RSNM of the cell. To resolve the issue of write '1' in the standard 5T-SRAM cell and to keep the RSNM sufficiently high, two modifications are applied to the proposed cell. First, the NMOS access device is replaced with a transmission gate. To elucidate the advantage of using a transmission gate, suppose that the store node Q holds '0' and it needs to change to '1'during a write cycle. In the standard 5T-SRAM cell, when the write cycle starts, the strength of the access transistor (AC) is maximized ($V_{GS\text{-}AC}=V_{WL}$). As soon as the voltage of node Q='0' starts to increase, $V_{GS\text{-}AC}$ starts to decrease. As a result, the strength of AC is reduced and the access transistor enters the cut off region at $V_Q=V_{WL}-V_{TH\text{-}AC}$.

However, by replacing the NMOS access device with a transmission gate, one of the NMOS or PMOS transistors would always continue to conduct during the write mode with the maximum strength. Furthermore, paths for read and write '1'are separated from each other. In typical SRAM cells, the bit-lines are precharged to V_{DD} and then the access devices of the target cell are enabled to perform the read operation. The storage node that holds '0' discharges its relevant bit-line and the sense amplifier detects the data stored on the cell. However, in the proposed asymmetric 6T-SRAM cell, the bit-line is precharged to GND and then the transmission gate access device is enabled. As a result, if Q='1', the BL will be charged to V_{DD} through the cell (instead of discharging) during the read cycle. By using this approach, a minimum size pull-down transistor can be used which eases writing '1'.

During read: 1) The BL is discharged to ground. 2) The PMOS access device turns on while NMOS is kept OFF to achieve a higher RSNM. In case, node Q stores '1', the BL will be charged through transistors AP and UL. Hence, RSNM improvement can be achieved by the use of a stronger pull-up transistor (UL) that will ease writing '1'. This means that, in the proposed cell, RSNM and write margin can be simultaneously improved.

In order to make PMOS access device (AP) stronger during a write cycle, its bulk can be connected to node Q (body biasing technique). In this way, while writing '1' on the cell, since the bulk of AP is connected to $V_Q=0$, the current through AP increases. This, in turn, improves the writeability of the cell with a negligible effect on read cycle. The main drawbacks of this technique are the area overhead due to the bulk connected to the storage node and the leakage power. However, the body biasing technique is not used in our simulations to reduce the area and leakage of the proposed cell.

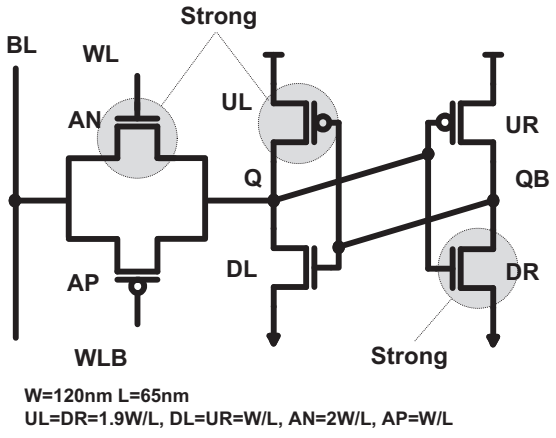

Fig. 3. The proposed asymmetric 6T-SRAM cell.

3.2. The proposed write assist technique

As mentioned in Section 2.2, NBL and BWL techniques are not appropriate for improving the write margin of the 5T- and proposed 6T-SRAM cells when writing '1'. The write '1' operation of the proposed 6T-SRAM cell is mainly done through the PMOS transistor AP (Fig. 3). Hence, increasing the driveability of AP leads to write '1' margin improvement. This can be done by either of the following four techniques: 1) applying a negative voltage to the gate of AP (similar to the BWL technique for NMOS access device), 2) boosting the BL to voltages higher than V_{DD} (similar to the NBL technique for NMOS access device), 3) cell V_{DD} collapse [14–17] or 4) cell GND boost [23]. Simulation results indicate that the two proposed write assist techniques (1 and 2 above) are better than existing approaches (3 and 4).

Since the best write assist technique is found to be the boosting bitline approach, this approach is chosen and described below. Fig. 4 shows the proposed asymmetric 6T-SRAM array and the implementation of the proposed write assist circuit which boosts the BL voltage to $V_{DD}+\Delta V$. The minimum ΔV voltage has to be chosen in such a way that sufficient write '1' improvement is achieved. However, there is an upper limit to ΔV since increasing it leads to an increase in the leakage current of half-selected cells. Simulations show that $\Delta V=0.2V_{DD}$ is optimal. The replica column consists of $2n$ turned off transmission gate cells (TG-cells) plus the replica column driver for an $n\times m$ array. The write assist circuit consists of a capacitor, $C_{P\text{-}boost}$, to produce the boosting voltage. The boosting capacitor ($C_{P\text{-}boost}$) is chosen in such a way that after coupling it to the bit-line, the BL voltage will be boosted to $V_{DD}+\Delta V$. Hence, it is mainly determined by the capacitance of the BL (C_{BL}) and the desired boosting voltage (ΔV). The replica column is used to determine the best time for connecting the boosting capacitor to BL. The transmission gates are of the same size as the ones used in the cells in order to form an equivalent capacitance twice that of the bit-line ($2C_{BL}$) [17]. Therefore, when the replica column bitline (RBL) charges to $V_{DD}/2$, BL is charged to V_{DD}. Suppose that the data which needs to be written on the selected cell is '1' (Data='1'). When the write cycle starts, WR signal is enabled and RBL starts to charge at t_0. Meanwhile, transistor MP in the write assist circuit turns on and starts to charge $C_{P\text{-}boost}$ with a polarity shown in Fig. 4. On the other hand, C2 control signal is enabled (C1 is disabled) and BL starts to charge to V_{DD} through WD2. When replica bitline is charged to $V_{DD}/2$ (BL charged to V_{DD}), RP is enabled at t_1. As a result, MP is turned off and the control signal C1 is enabled (C2 is disabled). These make a boosted voltage ($V_{DD}+\Delta V$) on V_B. This is done through the charges stored on $C_{P\text{-}boost}$ and the output voltage (V_{DD}) of the left hand side inverter (WD1) connected to it. This boosted voltage is transferred to BL through WD1. Hence, the absolute value of the gate-source voltage of the PMOS transistor of the transmission gate of the selected cell connected to BL (AP) will increase. This makes the

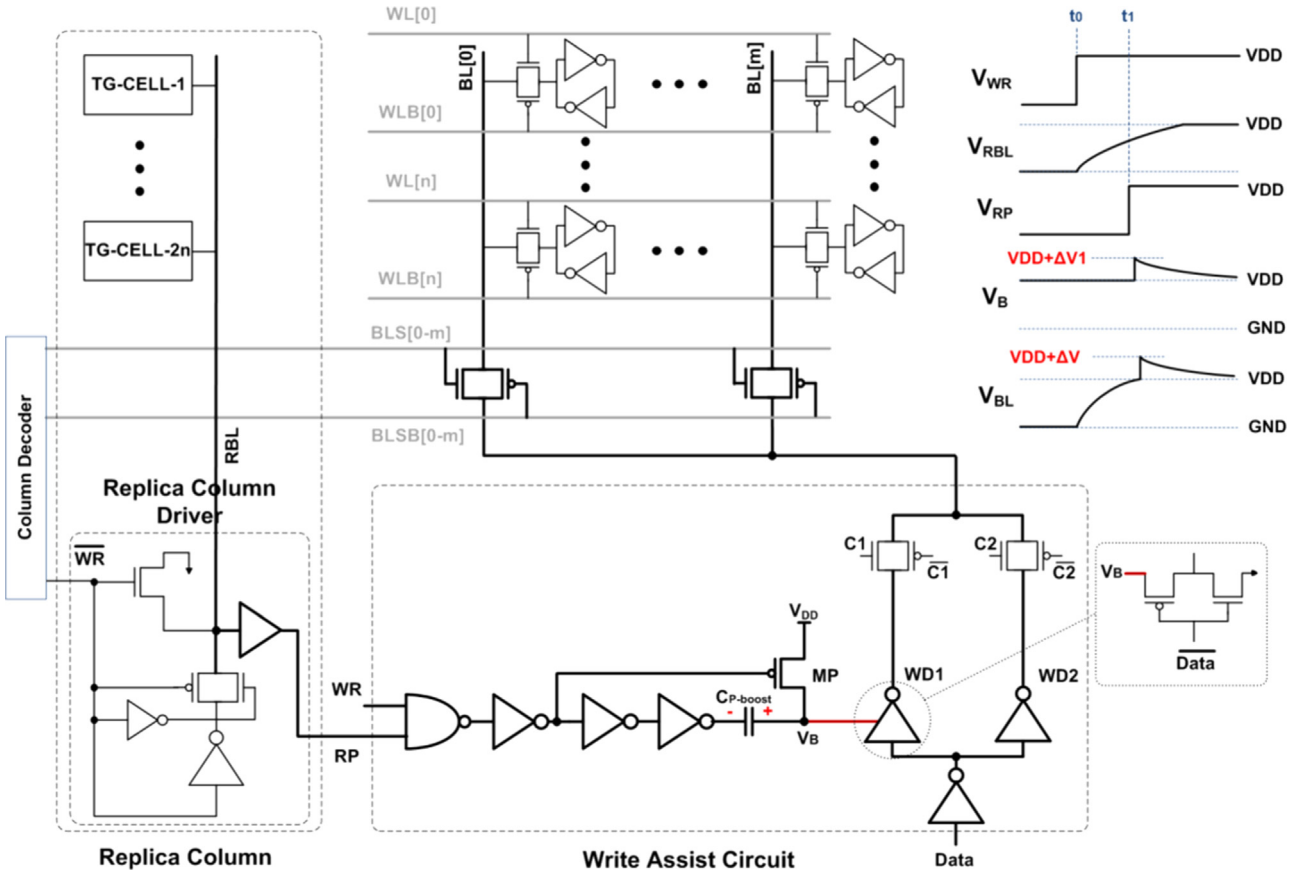

Fig. 4. The proposed asymmetric 6T-SRAM $n \times m$ array and the boosted bitline write assist scheme.

PMOS access device stronger and improves the writeability of the cell while writing '1'.

Boosting the BL voltage level can increase the leakage current of the half-selected cells (the cells connected to the boosted BL) during write '1' operation. This is due to the fact that the PMOS access transistor of half-selected cells is at subthreshold region ($V_{GS\text{-}AP}$=0.2 V). However, the write power consumption increase due to leakage current is negligible compared with the hold mode leakage current improvement achieved by the proposed write assist technique and asymmetric 6T-SRAM cell. On the other hand, applying the proposed write assist technique to the proposed asymmetric 6T-SRAM cell lets it work at lower supply voltages and this leads to more leakage power reduction.

3.3. Control signals

The implementation of the control signals is depicted in Fig. 5. In order to improve the read stability of the SRAM cell, WL is disabled during a read cycle and only the WLB is enabled. This is done by the control signal circuit shown in Fig. 5(a). The RD signal is enabled during a read operation. This prevents activation of the WL signal. Therefore, during read, the NMOS transistor of the transmission gate in the proposed 6T-SRAM cell is turned off and this weakens the access device. This, in turn, results in read stability improvement.

Fig. 5(b) shows the implementation of the control signals C1 and C2. When write cycle starts, prior to asserting RP ($t_0 < t < t_1$), RP='0' and WR is equal to '1'. Therefore, signals C2 and C1 are enabled and disabled, respectively. This will result in charging BL to V_{DD} via WD2. When RP goes high at $t=t_1$, C2 is disabled and C1 is enabled to connect the boosted voltage to BL via WD1. Hence,

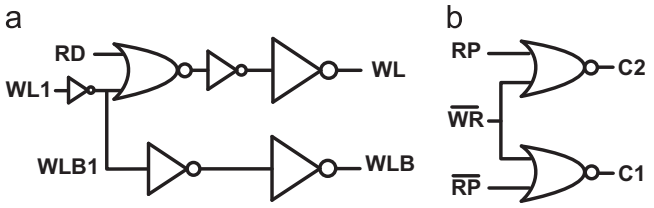

Fig. 5. Control signals implementation (a) WL and WLB (b) C1 and C2.

the boosted capacitor ($C_{P\text{-}boost}$) will connect to BL at the most appropriate time (i.e. immediately after charging to V_{DD}).

3.4. Mathematical analysis

The mathematical analysis for the behavior of the proposed cell is presented in this section in order to explore the effect of the proposed 6T-SRAM cell and the write assist circuit on write '1' operation. The equivalent simplified circuit of the proposed asymmetric 6T-SRAM cell at the side of BL and node Q from time t_1 on (Fig. 4) is shown in Fig. 6(a) and (b), respectively. When a write cycle starts, the pull down transistor DL is in triode region ($V_{GS\text{-}DL}=V_{DD}$ and $V_{DS\text{-}DL}=0$) and can be considered as a resistor (R_{DL}). C_Q is the total capacitance at node Q. Access transistors, AN and AP, are in saturation region and can be considered as current sources (I_{AN} and I_{AP}). C_{BL} and $C_{P\text{-}boost}$ are the total capacitance of the BL and the boosting capacitor of the write assist circuit, respectively. V_{BL} is an exponentially decreasing function of time from t_1 on (it decays from $V_{DD}+\Delta V$) with a time constant that is mostly determined by the boosting capacitance ($C_{P\text{-}boost}$) and the write current. In fact, the boosting capacitance charges the storage node capacitance (C_Q) to V_{DD} in order to perform write '1'

operation. Considering the large capacitance of $C_{P\text{-boost}}$ compared with C_Q, V_{BL} can be assumed to be constant to simplify the equations. A KCL at node Q gives

$$C_Q\frac{dV_Q}{dt}=I_{AN}+I_{AP}-I_{R_{DL}} \tag{1}$$

$$I_{R_{DL}}=\frac{V_Q}{R_{DL}} \tag{2}$$

$$I_{AN}=\frac{\beta_{AN}}{2}(V_{DD}-V_Q-V_{thn})^2 \tag{3}$$

$$I_{AP}=\frac{\beta_{AP}}{2}(|V_{BL}|-|V_{thp}|)^2 \tag{4}$$

$$R_{DL}=\frac{1}{\beta_{DL}(V_{DD}-V_{thn})} \tag{5}$$

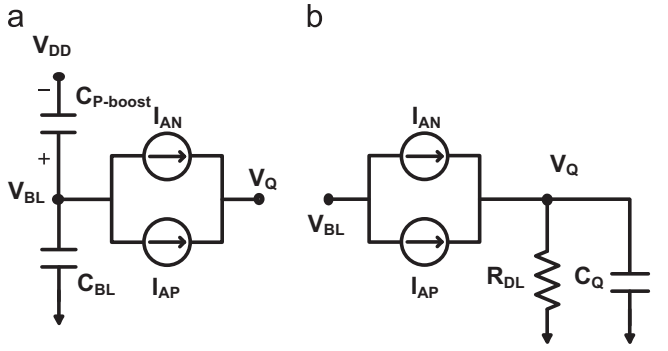

Fig. 6. The equivalent simple circuit of asymmetric 6T-SRAM cell at (a) the side of BL (b) the side of node Q.

Using (1)–(5), Eq. (1) can be written as follows:

$$C_Q\frac{dV_Q}{dt}=aV_Q{}^2+bV_Q+c \tag{6}$$

where

$$a=\frac{\beta_{AN}}{2}$$

$$b=-\left[\beta_{AN}(V_{DD}-V_{thn})+\frac{1}{R_{DL}}\right]$$

$$c=\frac{\beta_{AN}}{2}(V_{DD}-V_{thn})^2+\frac{\beta_{AP}}{2}(|V_{BL}|-|V_{thp}|)^2$$

Considering that $V_Q=0$ at $t=0$, the V_Q voltage is calculated from (6) as follows:

$$V_Q(t)=\frac{\left(|b|+\sqrt{b^2-4ac}\right)\left(1-e^{\frac{\sqrt{b^2-4ac}}{aC_Q}t}\right)}{2a\left(1-\frac{|b|+\sqrt{b^2-4ac}}{|b|-\sqrt{b^2-4ac}}e^{\frac{\sqrt{b^2-4ac}}{aC_Q}t}\right)} \tag{7}$$

Eq. (7) shows the voltage equation for node Q holding '0' while writing '1' on it in the proposed asymmetric SRAM cell. This has to be considered that (7) is valid in the first moments of write operation before the positive feedback of the back to back inverters speed up the write operation. The parameters a and c are positive while b is negative. When writing '1', the BL voltage is higher than the absolute value of the PMOS threshold voltage ($|V_{BL}|>|V_{thp}|$). As a result, by boosting the voltage on BL using the proposed write assist technique, the value of c will increase. The effect of an increase in c on V_Q can be explored by (6) at time zero.

Since $V_Q=0$ at time 0, we get the following from Eq. (6):

$$\frac{dV_Q}{dt}|t=0=\frac{c}{C_Q} \tag{8}$$

This indicates that an increase in the value of c will result in an increased rate of change of V_Q. The effect of boosting in the value c on the speed of V_Q rise is very high at the first moments of write

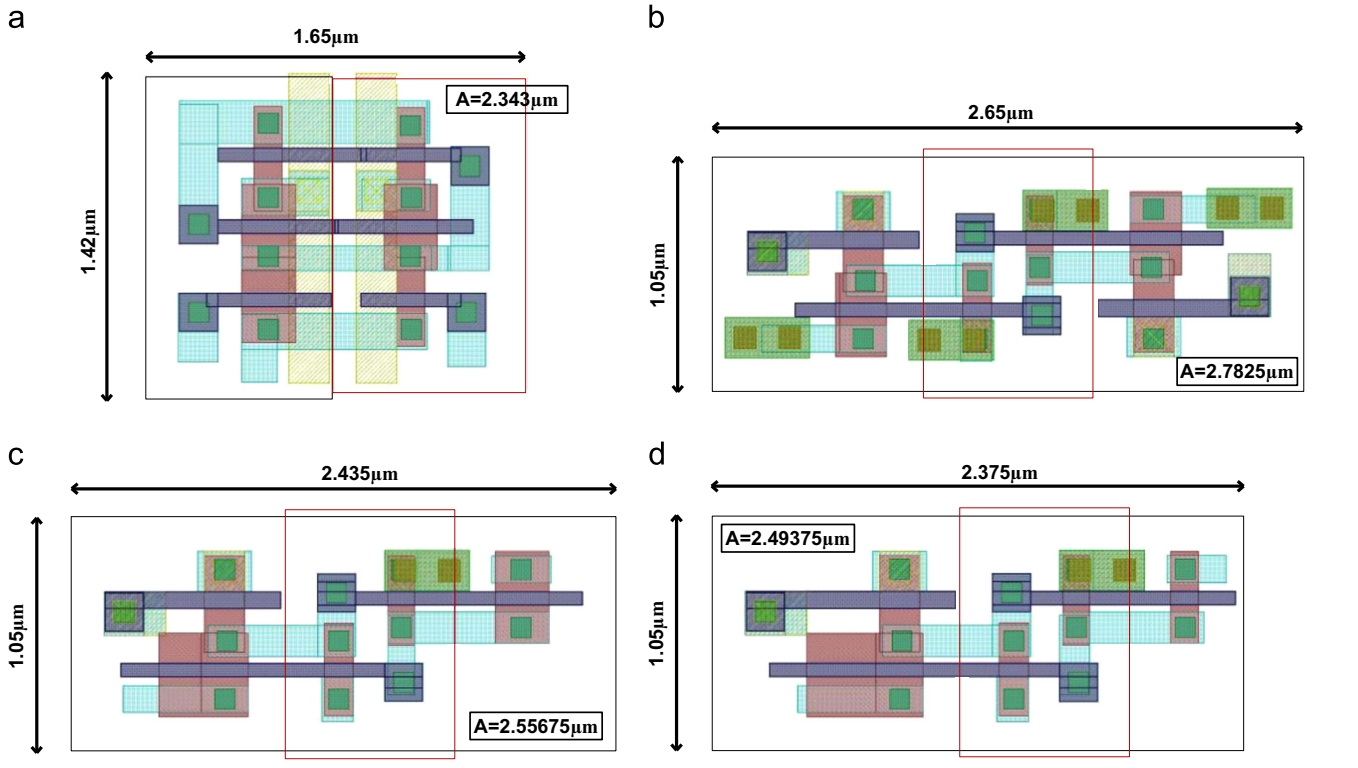

Fig. 7. The layout and area of (a) the proposed asymmetric 6T (b) standard 6T (c) standard 5T (WM Max) (d) standard 5T (RSNM Max) showing an area improvement of the cell of the proposed design.

operation when V_Q is low. On the other hand, the write operation will be speeded up through positive feedback of the back to back inverters for $V_Q > V_{thn\text{-}DR}$ (Fig. 3) and the cell enters an irreversible process. This shows the importance of improving the speed of V_Q rise by the proposed write assist technique.

3.5. Layout and area

In order to compare the area of the proposed cell with standard 5T- and 6T-SRAM cells, their layout are drawn in this section. The layouts have been drawn using digital design rules for 65 nm CMOS technology. Fig. 7 shows the layout of the proposed 6T, standard 6T, and standard 5T-SRAM (WM Max and RSNM Max) cells. In the proposed asymmetric 6T-SRAM cell, the equal number of NMOS and PMOS transistors leads to a lower area overhead as shown in the layout of Fig. 7(a). The proposed cell shows 19%, 9%, and 6% area savings compared to the standard 6T, 5T (WM Max), and 5T (RSNM Max) SRAM cells, respectively, while the total size of the transistors used in the cells are equal in all designs. Alternatively, at iso-area conditions, the proposed cell read or write performance can be improved even further by upsizing its transistors.

The area overhead of the replica column and the write assist circuit are not considered in the above comparisons. The standard 5T-SRAM cell utilizes two write assist circuits in order to perform write '1' operation including boosted WL and cell V_{DD} collapse techniques. The proposed 6T-SRAM cell utilizes the boosted BL write assist technique. Considering the fact that there is only one write assist circuit for the whole $n \times m$ array in the proposed design, its area overhead is negligible for large memories. The area overhead of the cells used in the replica column is 40% of the proposed 6T-SRAM cell. The replica column driver has nearly 5% area overhead. Thus, the area overhead of the $2n$ replica column and the replica column driver equals 85% of one column in the array. Therefor, the area overhead of the $2n$ replica column is 2.6% for an 8 Kb SRAM array (256×32) used in this paper. The overall area reduction in die area is 6.3% and 16.3% as compared with array designs with asymmetric 5T- and standard 6T-SRAM cells.

4. Simulation results

Simulation results for the proposed asymmetric 6T-SRAM cell in TSMC 65 nm CMOS technology with Cadence confirm that there is 77% RSNM improvement over the standard 6T-SRAM cell while it allows writing '1' on the cell without write assist circuit at $V_{DD}=1$ V. In addition, the scalability of operating supply voltage of the proposed cell can be improved by 10% and 21% compared to 5T- and 6T-SRAM cells, respectively. Subsequently, it has 21% and 53% lower leakage power consumption while it has less area overhead. The optimized sizing is considered for the 6T-SRAM cell in order to improve its RSNM ($W_{PD}/W_{PU}=1.92$ and $W_{PD}/W_{AC}=1.28$). On the other hand, the optimized sizing of asymmetric 5T-SRAM cell and the proposed 6T-SRAM cell in order to improve write '1' operation is used in simulations (Figs. 2 and 3). Note that the total size of the transistors used in the cells is equal in all simulations. Hence, the improvements of the proposed cell were achieved using less die area. The proposed cell is used in an 8 Kb SRAM array (256×32) with the proposed write assist circuit in order to improve its writeability. The boosting capacitor, $C_{P\text{-}boost}$, is implemented by a MOSCAP with $L_{CP\text{-}boost}=1$ μ, and $W_{CP\text{-}boost}=2.5$ μ. Simulations are performed at 1 V supply voltage and Temp=27 °C.

4.1. RSNM and WM

A metric to evaluate the read stability of an SRAM cell is RSNM. It is defined as the length of the side of the largest square which can fit into the lobes of the butterfly curve. Butterfly curve is

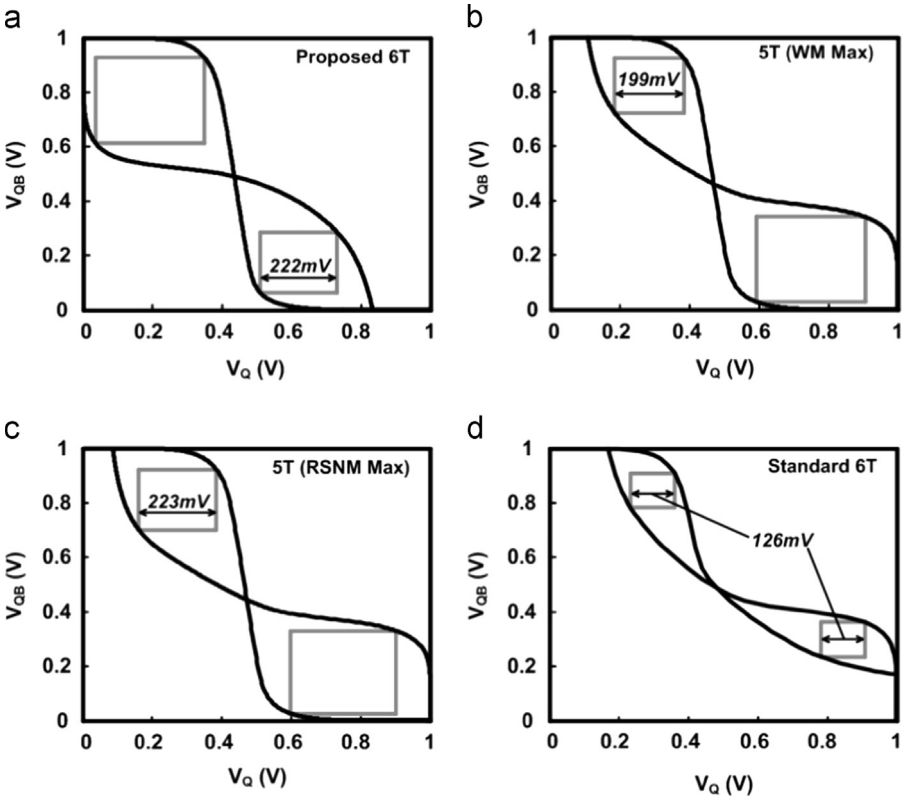

Fig. 8. Butterfly curves for (a) the proposed 6T- (b) 5T- (WM Max) (c) 5T- (RSNM Max) (d) standard 6T-SRAM cells.

obtained by drawing and mirroring the inverter characteristics while the access transistors are ON and the bitlines are precharged to V_{DD} (for standard 6T- and 5T-SRAM cells) and GND (for proposed cell) [26]. WM is calculated by the Word-Line (WL) voltage sweep method [27]. In this method the bitline will be connected to the appropriate voltage to enable flipping the data on the storage node. Then WL and WLB are swept from 0 V to 1 V and 1 V to 0 V, respectively. WM is calculated as the difference between V_{DD} and WL voltage when the data stored in the cell is flipped.

Fig. 8 shows RSNM for the proposed 6T-, asymmetric 5T- and standard 6T-SRAM cells and Fig. 9 shows RSNM, WM while writing '1' (WM1), and WM while writing '0' (WM0) for the proposed 6T-SRAM cell in comparison with 5T- and 6T-SRAM cells with the same size. In the proposed 6T-SRAM cell, we decreased WM0 in order to get a higher WM1 with no RSNM degradation. This is in contrast with 5T-SRAM cell that has a large WM0 but cannot perform write '1' without write assist (WM1=0) as shown in Fig. 9. As a result, we achieved an improved balance between these three features in the proposed cell. RSNM of the proposed 6T- and 5T-SRAM (RSNM Max) cells is 77% higher than that of standard 6T-SRAM cell. Asymmetric sizing leads to change in the trip point of the inverter with its input connected to the store node (right hand side inverter) in a way that it resists against flipping the cell during the read operation. Besides, weaker access device compared with the transistor of the inverter in the read path (UL in the proposed design and DL in the 5T-SRAM) increases RSNM.

In general, the standard 6T-SRAM cell has a strong writeability while it suffers from very weak RSNM. In contrast, the standard 5T-SRAM cell has improved RSNM while it suffers from very weak writeability (WM1=0). However, the proposed cell achieves RSNM improvement over the standard 5T-SRAM cell while it has an acceptable writeability which could be improved significantly with the proposed write assist technique. It has to be mentioned that RSNM improvement in standard 6T-SRAM cell with read assist circuits is very difficult and is not appropriate for scaled supply voltages. On the other hand, the focus of this paper is on write '1' margin improvement compared with the asymmetric 5T-SRAM cell.

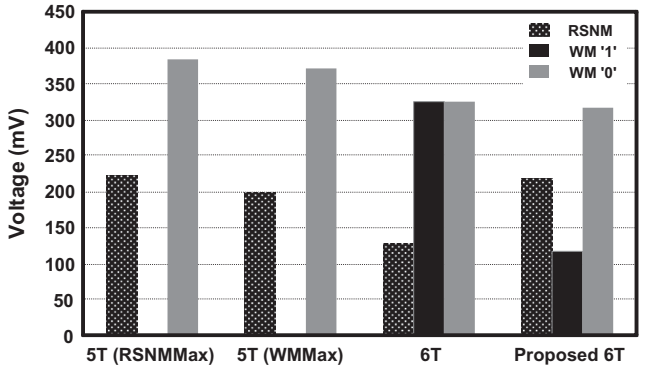

Fig. 9. RSNM, WM while writing '1', and WM while writing '0' for 5T-, 6T-, and proposed 6T-SRAM cells. Note that the WM'1' is zero for 5T-SRAM cells.

4.2. Comparison of write assist techniques

In this section, the effect of the proposed write assist techniques in Section 3.2 is compared with existing cell V_{DD} collapse and cell GND boost techniques. Fig. 10 shows the write '1' margin (WM1) for the proposed 6T-SRAM cell when utilizing 1) negative WLB ($V_{WLB}=-0.2$ V); 2) boosted BL ($V_{BL}=1.2$ V); 3) cell V_{DD} collapse ($V_{DD}=0.8$ V), and; 4) cell GND boost ($V_{GND}=0.2$ V) techniques. A 20% voltage increase for boosting BL and cell GND boost techniques is considered while a 20% voltage decrease is used for cell V_{DD} collapse and negative WLB techniques in order to make a fair comparison.

The WM1 of the proposed write assist techniques (1 and 2) is higher than the existing techniques (3 and 4) with that of the boosting BL technique having the highest of all. The WM1

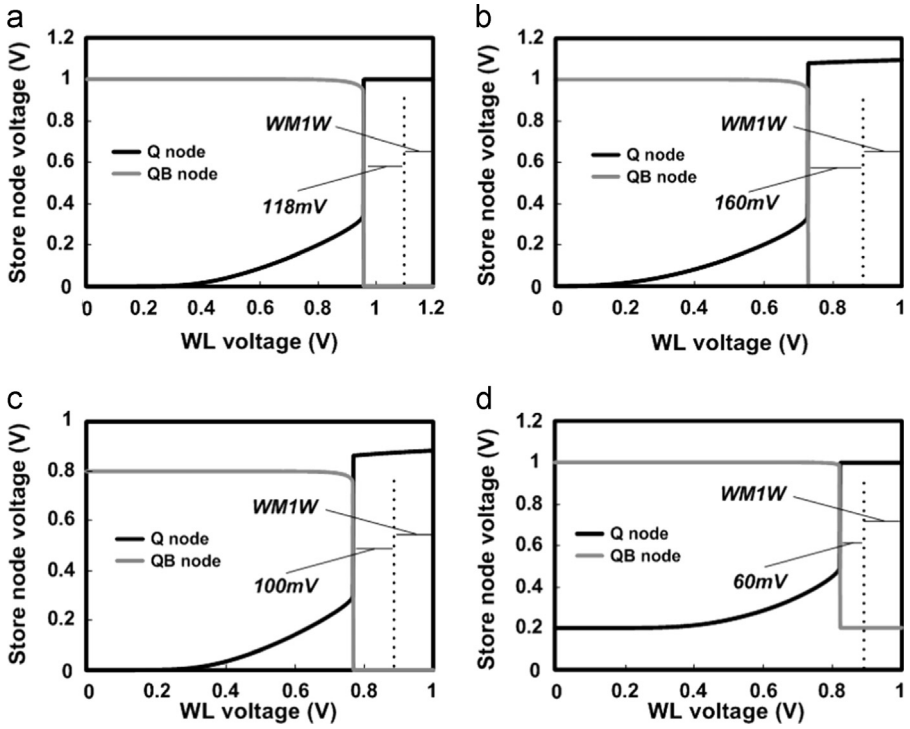

Fig. 10. WM1 of the proposed 6T-SRAM cell when utilizing (a) negative WLB with $V_{WLB}=-0.2$ V (b) proposed boosted BL technique with $V_{BL}=1.2$ V (c) cell V_{DD} collapse technique with $V_{DD}=0.8$ V (d) cell GND boost with $V_{GND}=0.2$ V. The difference between V_{DD} (1 V) and the dashed line shows the write '1' margin of the proposed 6T-SRAM cell without the write assist technique (WM1W).

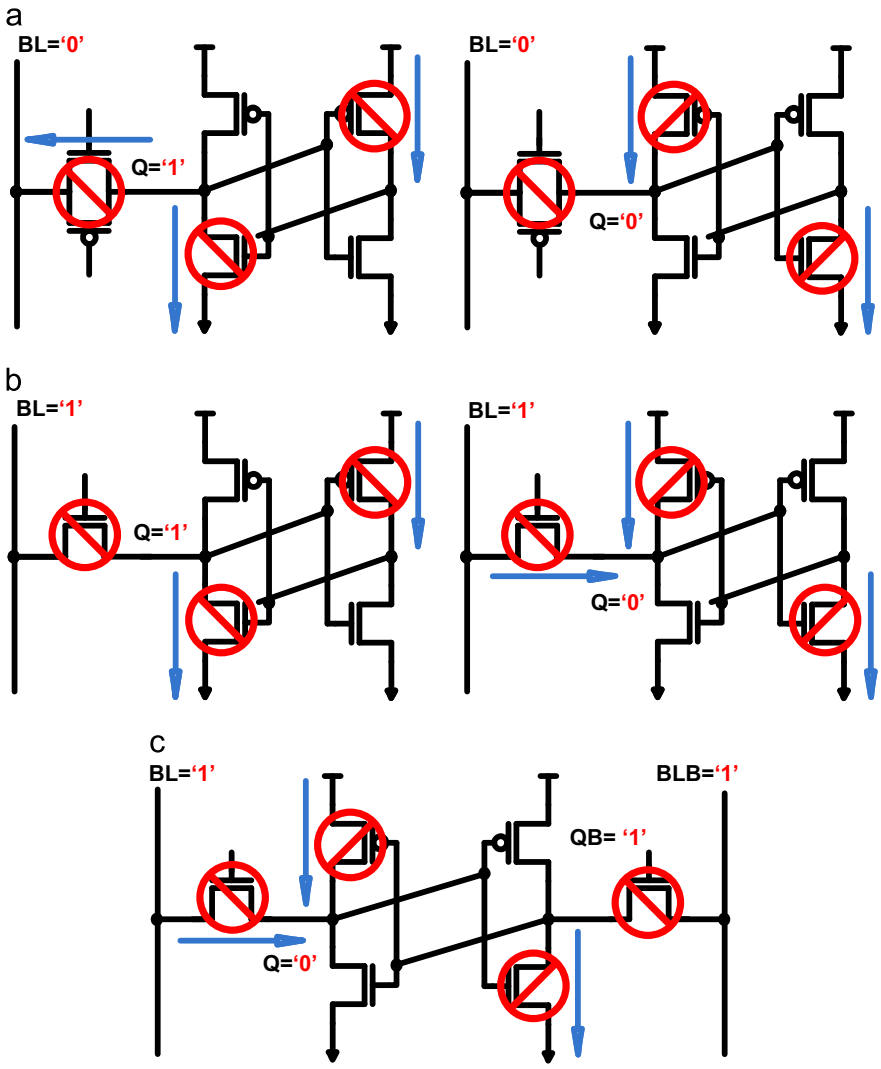

Fig. 11. The leakage current paths in (a) proposed 6T- (b) 5T- (c) standard 6T-SRAM cells.

improvements of negative WLB, boosted BL, cell V_{DD} collapse and cell GND boost techniques over the cell without write assist technique are 100%, 136%, 85% and 51%, respectivly. The boosted BL technique has the highest WM1 improvement. This is due to the fact that boosted BL technique increases both V_{GS} and V_{DS} of the AP access device while the negative WLB just increases V_{GS} of the AP. Increasing V_{DS} leads to further increase in write current due to the channel length modulation effect which leads to WM1 improvement. Cell GND boost has the minimum WM1 improvement. This is due to the fact that boosting cell GND decreases V_{DS} of the AP access device and increases the trip point of the right hand side inverter (Fig. 3). The cell V_{DD} collapse technique decreases the trip point of the right hand side inverter. However, this technique does not have any effect on the access transistors and node Q.

4.3. Leakage power consumption

In order to compare the leakage power consumption of the cells, leakage current of the cells is calculated in this section. The cell leakage current includes subthreshold leakage and gate leakage of pull up, pull down, and access transistors. Fig. 11 shows the leakage currents for the proposed 6T-, 5T-, and standard 6T-SRAM cells while Q='0' and '1'. In the standard 6T-SRAM cell, due to symmetry, the leakage current is equal for Q='0' and Q='1'. However, it is data dependent for asymmetric structures. Hence, the corresponding leakage current of the standard 6T-SRAM cell is shown just for Q='0'. The leakage currents can be categorized in two groups: first, the current flowing via access device between storage node and bitline (bitline leakage) and second, the current that flows through turned off transistors in cross-coupled inverters. Simulation results show that the overall bitline leakage in the proposed 6T- and 5T-SRAM cells is less than that of the standard 6T-SRAM cell due to single-ended bitline. However, the asymmetric structures have higher inverter leakage due to the use of larger transistors.

Fig. 12 shows the leakage power consumption for the proposed 6T-, 5T-, and standard 6T SRAM cells. The proposed 6T-SRAM cell shows minimum average leakage power consumption among these designs. It is due to the fact that, unlike 5T-SRAM cell, large transistors are not used in the proposed 6T-SRAM structure and this results in lower inverter leakage. Furthermore, single-ended access in the proposed 6T-SRAM cell compared with standard 6T-SRAM cell results in lower bitline leakage. However, the proposed cell has higher leakage power when holding '1'. This is attributed to the discharged bitline during hold cycle and the use of two transistors in parallel as access device. The average leakage currents of the proposed 6T-, standard 6T-, 5T- (RSNM Max) and 5T- (WM Max) are 7.42 nA, 7.7 nA, 7.83 nA and 7.91 nA, respectively. The average leakage current of 5T-SRAM cell is higher than

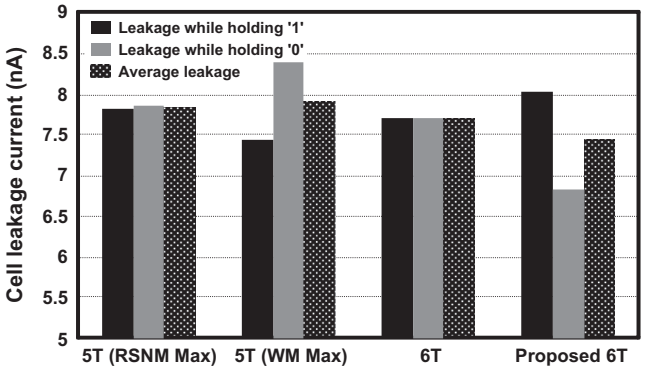

Fig. 12. Cell leakage current for the proposed 6T-, 5T- and standard 6T-SRAM cells.

that of the proposed 6T- and standard 6T-SRAM cells due to the very large pull-down transistor (DL) in its structure.

4.4. The effect of process variations on boosted BL voltage

In order to see the effect of process variations on write operation for the proposed asymmetric 6T-SRAM cell with the boosted BL write assist technique, a Monte Carlo (MC) analysis with 1000 iterations at T=27 °C is used. Fig. 13(a) shows the boosted voltage level variations due to process variations and Fig. 13(b) illustrates its histogram and the fitted Gaussian function. The mean value and the standard deviation of the boosted voltage level are 1.2 V and 0.91 mV, respectively. The variations in boosted voltage level result from mismatches between transistors in the write assist circuit, mismatch between write driver circuit in the

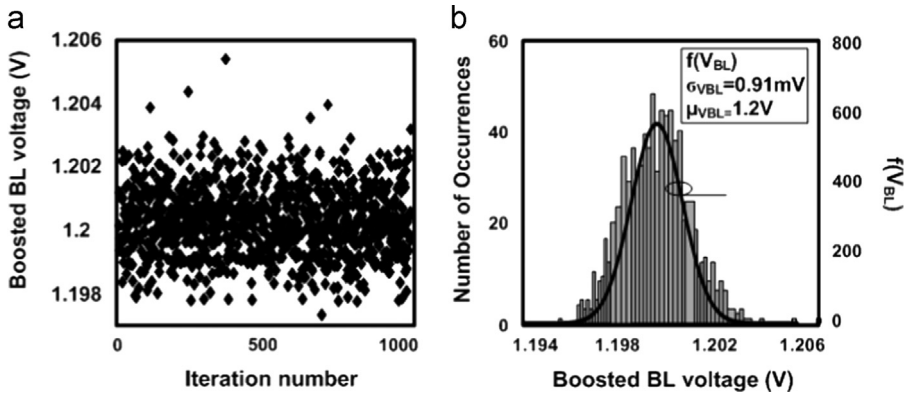

Fig. 13. (a) The effect of process variations on the boosted BL voltage level using a Monte Carlo simulation with 1000 iterations (b) boosted BL voltage level histogram and its fitted Gaussian function.

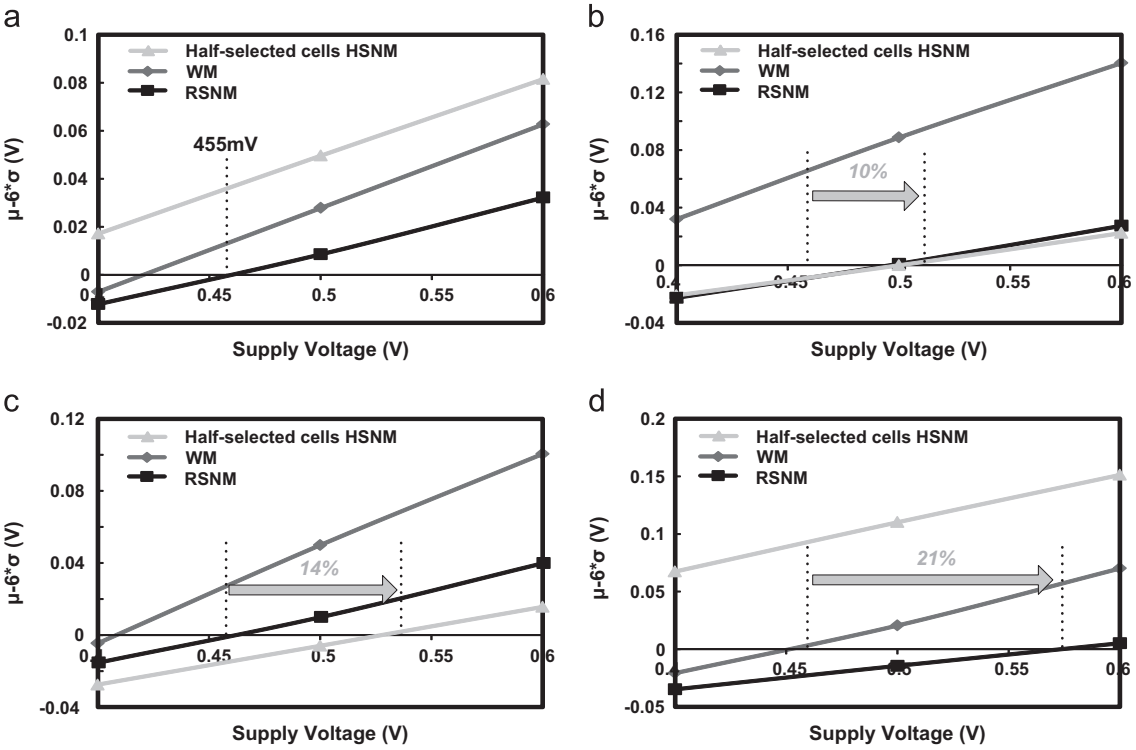

Fig. 14. Noise margin comparison under statistical variations for different supply voltages for (a) the proposed asymmetric SRAM cell (b) the standard 5T-SRAM cell (WM max) (c) the standard 5T-SRAM cell (RSNM max) (d) the standard 6T-SRAM cell.

replica column and the write assist circuit, and $C_{P\text{-}boost}$ variations. As can be seen from Fig. 13, the effect of process variations on BL voltage level is very small and its effect on WM is negligible.

4.5. Supply voltage scalability in the presence of process variations

In this section, the operation of different SRAM cells under scaled supply voltage is studied. Supply voltage scaling is used to reduce the total power consumption of an SRAM array. Therefore, the behavior of different SRAM cells at very low supply voltages under process variations is explored. Monte-Carlo simulation is used to study the effect of process variations and mismatch on SRAM operation at scaled supply voltages. A Monte Carlo analysis with 1000 iterations is used for supply voltages 0.6 V, 0.5 V, and 0.4 V and then $\mu-6\sigma$ of RSNM, WM, and half-selected (HSNM) values are calculated for different cells as shown in Fig. 14. Boosted WL ($1.2\times V_{DD}$) and collapsed supply voltage ($0.5\times V_{DD}$) write assist techniques are used to improve the write margin of the 5T-SRAM cell. However, for the proposed cell, boosted BL voltage to $1.2\times V_{DD}$ and collapsed supply voltage to $0.75\times V_{DD}$ are used.

As it can be seen from Fig. 14(a), RSNM limits the supply voltage scaling for the proposed 6T-SRAM cell and it fails at $V_{DD}=455$ mV, while WM and half-selected HSNM fail at lower supply voltages. In the 5T-SRAM cell, the half-select HSNM limits the lowest supply voltage to $V_{DD}=505$ mV and 528 mV for WM Max and RSNM Max sizing, respectively (Fig. 14(b) and (c)). Finally, in the 6T-SRAM cell, read is the first failure observed at $V_{DD}=575$ mV (Fig. 14(d)). It shows that the supply voltage of the proposed cell can be decreased by 10%, 14%, and 21% compared with 5T- (WM Max), 5T- (RSNM Max), and 6T-SRAM cells. Simulations show that the mentioned supply voltage scalability improvement leads to a 21%, 28%, and 53% less leakage power in the proposed cell compared with 5T- (WM Max), 5T- (RSNM Max), and 6T-SRAM cells.

Half-selected HSNM reduction in 5T-SRAM cell attributed to the collapsed supply voltage to $V_{DD}/2$. In fact, the half-selected HSNM of all the cells in a row or a column is sacrificed to improve the write '1' capability of the cell.

5. Conclusion

In this paper a new asymmetric 6T-SRAM cell is proposed for low-voltage and robust operation in the presence of existing process variations. A new write assist technique is proposed to enhance the writeability of the proposed SRAM cell. The proposed cell achieves the same RSNM of the 5T-SRAM cell and 77% higher RSNM than the standard 6T-SRAM cell, while it is able to perform write operation without any write assist at typical supply voltages. Using the proposed cell, 21% supply voltage scalability and 19% less cell area are achieved, and this can decrease the leakage power up to 53%. The overall area overhead reduction of the proposed memory array design (256×32) considering the write assist circuit, replica column and replica column driver is 16.3% compared with standard 6T-SRAM cells.

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