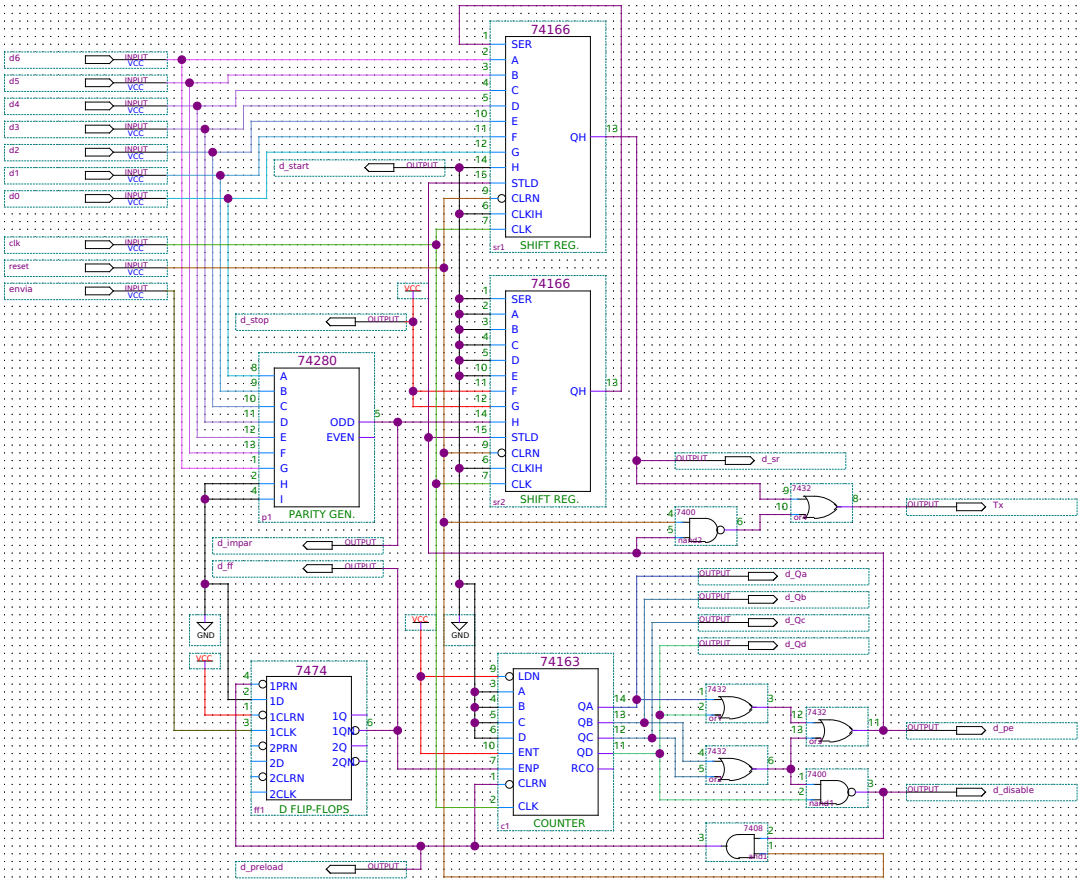
74166
SER
A
B
C
D
E
F
G
H
STLD
CLRN
CLKIH
CLK
QH
SHIFT REG.
sr1
sr2
d6
d5
d4
d3
d2
d1
d0
clk
reset
envia
INPUT
VCC
d_start
d_stop
OUTPUT
74280
ODD
EVEN
I
PARITY GEN.
p1
d_impar
d_ff
GND
7474
1PRN
1D
1CLRN
1CLK
2PRN
2D
2CLRN
2CLK
1Q
1QN
2Q
2QN
D FLIP-FLOPS
ff1
d_preload
74163
LDN
ENT
ENP
RCO
COUNTER
c1
d_sr
7432
7400
7408
Tx
d_Qa
d_Qb
d_Qc
d_Qd
d_pe
d_disable