Nuno M.C. Paulino

PhD in Electrical and Computer Engineering

+351 919533968
nmcp@fe.up.pt

Summary

Name	Nuno Miguel Cardanha Paulino
Date of Birth	20th July 1988
e-mail	nmcp@fe.up.pt
ORC-ID	https://orcid.org/0000-0001-5547-0323
Ciência ID	BB19-5511-AF8E
ResearchGate	https://www.researchgate.net/profile/Nuno_Paulino2
Google Scholar	https://scholar.google.com/citations?user=cSGirLUAAAAJ
Personal Website	https://paginas.fe.up.pt/~nmcp/

Short Bio

Nuno Paulino received a M.Sc. degree in Electrical and Computer Engineering from the Faculty of Engineering of the University of Porto in 2011. He received his Ph.D. in the same field from the same institution in 2015, where he currently is an Invited Assistant Professor. He has been a researcher at INESC Technology and Science since 2015, where he has participated in five research projects. He has supervised two MSc thesis, co-supervised three MSc theses, and is currently supervising and co-supervising three MSc theses. His research interests include run-time reconfigurable systems, edge computing in FPGAs, co-processor hardware acceleration, tools for hardware/software co-design automation, new heterogeneous computing architectures in the RISC-V ecosystem, and wireless telecommunications. He has written two national project proposals as PI, and is currently leading a consortium for a European project proposal.

Education & Experience

2018-Present **Auxiliary Researcher**, *INESC-TEC (Instituto de Engenharia de Sistemas e Computadores, Tecnologia e Ciência)*, Porto, Portugal

Research on the PEPCC project (completed January 2022), and on Innovation Actions with national companies, via the WHERE.IS and SLID projects. Organization of several public events and supervision of theses.

2016-2018 **Post-Doc Researcher (BI Grant)**, *INESC-TEC (Instituto de Engenharia de Sistemas e Computadores, Tecnologia e Ciência)*, Porto, Portugal
Research on the SMILES and PEPCC projects, focusing on computing for HPC and techniques for generation of heterogenous systems.

2012-2015 **PhD in Electrical and Computer Engineering**, *University of Porto, Faculty of Engineering (FEUP)*, Porto, Portugal, *Cum Laude (Grade–17.88/20)*
Relevant areas: Embedded Systems, Hardware Accelerators, FPGA Design, Robotic Manipulators and Mobile Robotics, Microelectronics and Micromechanics, Image Recognition, Computer Vision, and Machine Learning

2009-2012 **MSc in Electrical and Computer Engineering**, *University of Porto, Faculty of Engineering (FEUP)*, Porto, Portugal *(Grade–16.46/20)*
Relevant areas: VLSI Circuits and Digital Systems, Microprocessors, Peripherals and Interfaces, Computer Networks, Semiconductors and Optoelectronics

2011 **FCT Research Grant (BI/FhP-11/003)**, *Fraunhofer AICOS*, Porto, Portugal
Design and implementation of a hardware and software infrastructure of a large scale web-interactive wall-mounted LED clock for Fraunhofer AICOS. The project entailed PCB design, development and integration of the website and backend control software residing in the embedded control system composed by microcontroller and an FPGA.

Scientific and Technological Development

Publication Summary

Year	Conference	ACM/IEEE	Journal	Q1/Q2	Citations
2010-2016	4	3	4	3	99
2017-2021	8	7	5	4	23
Total	12	10	9	6	122

Summarized are all publications in conferences and journals, with a discriminated subset of ACM/IEEE conference publications and Q1/Q2 journal articles. For three quarters of the listed publications, Paulino was first author, and principal developer and researcher of the scientific and technological contributions.

International Journal Publications

1 **Nuno Paulino**, Luís Pessoa, André Branquinho, Rafael Almeida, Igor Ferreira. 2022. *"Optimizing Packet Reception Rates for Low Duty-Cycle BLE Relay Nodes"*, in IEEE Sensors (Under Review)

2 **Nuno Paulino**, João Bispo, João Canas Ferreira, and João M. P. Cardoso. 2021. *"A Binary Translation Framework for Automated Hardware Generation"*, in IEEE Micro: Special Issue on FPGAs in Computing, July 2021, 8 pages

3 **Nuno Paulino**, João Canas Ferreira, and João M. P. Cardoso. 2020. *"Improving Performance and Energy Consumption in Embedded Systems via Binary Acceleration: A Survey"*, ACM Comput. Surv. 53, 1, Article 6 (February 2020), 36 pages

4 **Nuno Paulino**, João Canas Ferreira, and João M. P. Cardoso. 2020. *"Optimizing OpenCL Code for Performance on FPGA: k-Means Case Study With Integer Data Sets"*, in IEEE Access, vol. 8, pp. 152286-152304, 2020

5 **Nuno Paulino**, João C. Ferreira, and João M.P. Cardoso. *"Dynamic Partial Reconfiguration of Customized Single-Row Accelerators"*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 27, no. 1, pp. 116-125, Jan. 2019

6 **Nuno Paulino**, João C. Ferreira, and João M.P. Cardoso. *"Generation of Customized Accelerators for Loop Pipelining of Binary Instruction Traces"*, in IEEE Transactions on Very Large Scale Integration Systems, vol. 25, no. 1, pp. 21-34, Jan. 2017

7 **Nuno Paulino**, João Canas Ferreira, and João M. P. Cardoso. 2013. *"A Reconfigurable Architecture for Binary Acceleration of Loops with Memory Accesses"*, ACM Trans. Reconfigurable Technol. Syst. 7, 4, Article 29 (December 2014), 20 pages

8 João Bispo, **Nuno Paulino**, João M. P. Cardoso and João C. Ferreira, *"Transparent Runtime Migration of Loop-Based Traces of Processor Instructions to Reconfigurable Processing Units"*, International Journal of Reconfigurable Computing, 2013

9 João Bispo, **Nuno Paulino**, João C. Ferreira and João M. P. Cardoso, *"Transparent Trace-Based Binary Acceleration for Reconfigurable HW/SW Systems"*, IEEE Transactions on Industrial Informatics, vol. 9, no. 3, pp. 1625-1634, Aug. 2013

International Conference Publications

1 P. F. Silva, J. Bispo and **N. Paulino**, *"FPGAs as General-Purpose Accelerators for Non-Experts via HLS: The Graph Analysis Example"*, 2021 International Conference on Field-Programmable Technology (ICFPT), 2021, pp. 1-4

2 T. Santos, **N. Paulino**, J. Bispo, J. M. P. Cardoso and J. C. Ferreira, *"On the Performance Effect of Loop Trace Window Size on Scheduling for Configurable Coarse Grain Loop Accelerators"*, 2021 International Conference on Field-Programmable Technology (ICFPT), 2021, pp. 1-4

3 L. Sousa, **N. Paulino**, J. C. Ferreira, and J. Bispo, *"A Flexible HLS Hoeffding Tree Implementation for Runtime Learning on FPGA"*, 2021, at LATTE'2021 (an ASPLOS'2021 Workshop), arXiv preprint arXiv:2112.01875

4 L. Sousa, **N. Paulino**, J. C. Ferreira, and J. Bispo, *"A Flexible HLS Hoeffding Tree Implementation for Runtime Learning on FPGA"*, 2021, LATTE'2021 (an ASPLOS'2021 Workshop), at LATTE'2021 (an ASPLOS'2021 Workshop)

1 P. Silva, J. Bispo, and **N. Paulino**, *"Building Beyond HLS: Graph Analysis and Others"*, 2021, . arXiv preprint arXiv:2104.02676

5 **Nuno Paulino**, Luís M. Pessoa, André Branquinho, and Edgar Gonçalves. 2021. *"Evaluating a Novel Bluetooth 5.1 AoA Approach for Low-Cost Indoor Vehicle Tracking via Simulation"*, in Proc. of the 2021 Joint EuCNC & 6G Summit, Virtual Conference (Portugal), 6 pages

6 **Nuno Paulino**, João C. Ferreira, João Bispo, and João M.P. Cardoso. *"Executing ARMv8 Loop Traces on Reconfigurable Accelerator via Binary Translation Framework"*, In Proceedings of the 30th International Conference on Field-Programmable Logic and Applications (FPL), 2020

7 **Nuno Paulino**, Luís Reis, and João M.P. Cardoso. *"On Coding Techniques for Targeting FPGAs via OpenCL"*, In Proceedings of the 2017 International Conference on Parallel Computing (ParCo), 2017

8 **Nuno Paulino**, João C. Ferreira, and João M.P. Cardoso. *"Transparent acceleration of program execution using reconfigurable hardware"*, In Proceedings of the 2015 Design, Automation & Test in Europe Conference & Exhibition (DATE), 2015

9 **Nuno Paulino**, João C. Ferreira, and João M.P. Cardoso. *"Trace-Based Reconfigurable Acceleration with Data Cache and External Memory Support"*, In IEEE Intl. Symp. on Parallel and Distributed Processing with Applications (ISPA), pp. 158–165, 2014

10 **Nuno Paulino**, João C. Ferreira and João M. P. Cardoso. *"Architecture for Transparent Binary Acceleration of Loops with Memory Accesses"*, In Proc. of the 9th Intl. Conf. on Reconfigurable Computing: Architectures, Tools, and Applications (ARC'13), pp. 122-133, 2013

11 João Bispo, **Nuno Paulino**, João M. P. Cardoso and João Canas Ferreira, *"From Instruction Traces to Specialized Reconfigurable Arrays"*, In Proc. of the Intl. Conf. on Reconfigurable Computing and FPGAs (ReConFig), pp.386-391, 2011

National Conference Publications

1 **Nuno Paulino**, João C. Ferreira and João M. P. Cardoso, *"Transparent Binary Acceleration via Automatically Generated Reconfigurable Processing Units"*, XI Jornadas sobre Sistemas Reconfiguráveis, Fev. 5-6, 2015

2 **Nuno Paulino**, João C. Ferreira and João M. P. Cardoso, *"Generation of Coarse-Grained Reconfigurable Processing Units for Binary Acceleration"*, VII Jornadas sobre Sistemas Reconfiguráveis, pp.11-19, Fev. 9 2012-Fev. 10, 2012

Participation in Research Projects

2019-present **SLID - Stock Live IDentification**, *Researcher, National Project*, INESC-TEC (in partnership with Wavecom), Funded by ERDF, Grant POCI-01-0247-FEDER-045388

The SLID project focuses on the development of a product that can be used in cargo vehicles and indirectly track the location and movement of all products in stock, in all logistical scenarios. The project explores the use of Bluetooth 5.2 Low Energy for indoor location and tracking using Angle-of-Arrival technology with antenna arrays in mobile receivers. The solution is expected to improve the logistical efficiency of industrial processes.

2018-2019 **WHERE.IS - Localização e tracking de equipamentos em ambiente indoor**, *Researcher, National Project*, INESC-TEC (in partnership with Wavecom), Funded by ERDF, Grant POCI-01-0247-FEDER-024191

The WHERE.IS project focused on the development of the hardware and software infrastructure of an ad-hoc mesh network of Bluetooth 4.1 beacons and receivers/re-transmitters for the location of an arbitrary number of valuable assets in multiple scenarios, such as inventory management (Casa de Música, Porto) or and real-time equipment tracking (Hospital de Braga)

2018-present **PEPCC - Power Efficiency and Performance for Embedded and HPC Systems with Custom CGRAs**, *Researcher, National Project*, INESC-TEC, Funded by FCT, Grant PTDC/EEI-HAC/30848/2017

The goal of this project is to devise efficient techniques for dynamically mapping computations extracted from execution behavior to the resources of specialized re-configurable accelerators. The techniques will identify program hot-spots at run-time. The use of specialized circuits reduces resource usage and improves performance. The methodologies and concepts to explore are relevant for emergent edge computing applications due to performance and power consumption efficiency.

2016-2017 **TEC4Growth - RL SMILES - Smart, Mobile, Intelligent and Large scale Sensing and Analytics**, *Researcher, National Project*, INESC-TEC, Funded by the CCDRN (ERDF), NORTE2020, Grant NORTE-01-0145-FEDER-000020

2016-2017 **REFLECT: Rendering FPGAs to Multi-Core Embedded Computing**, *Researcher, International Project*, Faculdade de Engenharia da Universidade do Porto (FEUP), Funded by the FP7-ICT Programme, European Commission

Artifacts from Research Projects

PEPCC A compilation framework for exploration of future automated hardware design tools and methods.[1] I have been the main developer of the framework, which is now the host for on-going MSc theses on hardware compilation.

PEPCC A test harness for several implementation of the k-means algorithm in OpenCL, for execution on FPGA accelerator boards, publicly available at IEEE Code Ocean (`https://codeocean.com/capsule/2348736/tree/v1`)

PEPCC An Implementation of K-means written in C, publicly available at IEEE Code Ocean (`https://codeocean.com/capsule/3208075/tree/v1`)

PEPCC A Generator of Randomly Correlated N-Dimentional Clusters, publicly available at ResearchGate (`http://dx.doi.org/10.13140/RG.2.2.34866.43200`

PEPCC A Batch of Integer Datasets for Clustering Algorithms, publicly available at IEEE DataPort (`https://dx.doi.org/10.21227/smta-vv06`

PEPCC A C/C++ HLS-ready implementation of a Hoeffding Tree, publicly available at GitHub (`https://github.com/lm-sousa/Hoeffding-Tree`

WHERE.IS Blueooth 4.2 receiver/re-transmitter device for indoor asset tracking, currently in early commercial deployment.

REFLECT Internal report on acceleration opportunities and hardware designs for workload on a G.279 speech encoder application.

Patents

2020 André Branquinho, Franciso Pimenta, Igor Ferreira, José Ferreira, Luís Pessoa, **Nuno Paulino**, Rafael Almeida, *"Monitoring System for Determining the Location of Bluetooth Beacons"*, P904.4, n.º 20211000000460 (Patent Pending), 2020

Teaching and Pedagogic Activities

Teaching Experience

[1] The framework can be found at `https://github.com/specs-feup/specs-hw`

I have been Invited Assistant Professor of the Informatics Engineering Department (DEI) of the Faculty of Engineering (FEUP) of the University of Porto since 2017. I teach 3 to 4 hours per week of laboratory classes of first and second year subjects of the Master's Degree in Informatics and Computing Engineering (MIEIC). Prior, I was a teacher's assistant for first year programming classes for the Electric Engineering Deparment (DEEC) of the same institution.

2022 **Invited Class**, University of Porto, Faculty of Engineering (FEUP), Porto, Portugal
An invited class of the subject of Heterogenous System Architectures (M.EEC049) – part of the Master's on Electrical and Computer Engineering at FEUP – regarding code translation techniques, OpenCL acceleration on FPGAs, and research on DSLs for HDL generation.

2021-Present **Invited Assistant Professor**, *Laboratory Classes*, University of Porto, Faculty of Engineering (FEUP), Porto, Portugal
Assistant professor for the subjects of Fundamentals of Computing Systems (L.EIC004), focusing on binary representation, boolean algebra, circuit blocks, CPU organization, and ARMv8 assembly; and Computer Labs (L.EIC018), regarding C and assembly programming for peripheral interfaces in educational development kits (e.g. BeagleBoard).

2016-2021 **Invited Assistant Professor**, *Laboratory Classes*, University of Porto, Faculty of Engineering (FEUP), Porto, Portugal
Assistant professor for the subjects of *C/C++* Programming (EIC0012), focusing on data structures and their manipulation, and Computer Labs (EIC0020), regarding peripherals and device drivers in a MINIX environment.
EIC0020: Average 5.2/7.0 rating in a 4 year period, as per UP Pedagogical Surveys[2]
EIC0012: Average 4.6/7.0 rating in a 3 year period, as per UP Pedagogical Surveys[2]

2011 **Programming class assistant (*"monitor"*)**, *Laboratory Classes*, University of Porto, Faculty of Engineering (FEUP), Porto, Portugal
Teaching aid during programming lab classes, according to the course plan for the MSc degree in Electrical and Computer Engineering (EEC0009), entailing: C programming and development methodologies, low-level programming, fundamental algorithmic concepts and data structures.

Teaching Material

2020 **LaTeX Template for Master's Thesis for the "Instituto de Ciências Biomédicas Abel Salazar (ICBAS)" from the University of Porto**, *Author*, University of Porto, Faculty of Engineering (FEUP)
An adaptation of FEUP's LaTeX Master's thesis template to conform with the formatting and typesetting requirements of the ICBAS institute. The template includes basic LaTeXinstructions and examples.[3]

2018-present **(The Very) Basics of C/C++**, *Author*, University of Porto, Faculty of Engineering (FEUP)
A (work-in-progress) introduction to the basics of C and C++. The document is intended to clarify most of the gaps in knowledge I identified in programming skills of 2nd (and later) year students. As per its introduction: *This document is a condensed overview on basics of C programming, and on some concepts about compilation in general. The point of this document is to introduce you to some concepts that might not be familiar if your prior programming experience was not C/C++ or a compiled language.*[4]

[2] Overall average of all pedagogical parameters for stated period
[3] The document can be found at `https://paginas.fe.up.pt/~nmcp/`
[4] The document can be found at `https://paginas.fe.up.pt/~nmcp/`

Supervisions (Theses, Internships, & Research Grants)

2021 **Design of embedded software for pre-processing and transmission of carrier phase data in Bluetooth module with antenna array**, *Master's Research Grant (Supervisor)*, INESC-TEC, David Cunha

This studentship was a contribution to the on-going SLID national project. Included the design of software for gathering and transmitting AoA data acquired by a Bluetooth module with antenna, and characterization of the transmission and reception quality of the module in anechoic chamber.

2021 **Design and comparison of different algorithms for AoA calculation from phase data from antenna array**, *Research Contract (Supervisor)*, INESC-TEC, Bruno Saraiva

This mentorship focused on developing diferent methods to compute the angle-of-arrival (AoA) of Bluetooth transmissions, based on experimentally acquired wave phase data.

2021-Present **Specializing RISC-V Cores for Performance and Power**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Henrique Veloso de Sousa

This MSc thesis is a contribution to the PEPCC national project, and contributes to the start of a research line on the RISC-V ecosystem.

2021-Present **Designing an Instruction Set Based Coarse Grain Accelerator**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Gonçalo de Albuquerque Ferreira

This MSc thesis is a contribution to the PEPCC national project, and contributes to the start of a research line on the RISC-V ecosystem.

2021 **Desenvolvimento de antena integrada para recetor Bluetooth Low Energy 5.1**, *CTM Summer Internship (Co-Supervisor)*, INESC-TEC, Margarida Costa

This internship was a contribution to the on-going SLID national project.

2021 **Angle-of-Arrival Estimation on FPGA from IQ Samples**, *CTM Summer Internship (Supervisor)*, INESC-TEC, Gabriella Pantaleão

This internship was a contribution to the on-going SLID national project.

2020-2021 **Design of Bluetooth Low Energy 5.1 Angle-of-Arrival Based Receiver for Indoor Asset Tracking**, *Scientific Initiation Studentship (Supervisor)*, INESC-TEC, Catarina Alexandre Marques

This studentship was a contribution to the on-going SLID national project.

2020-2021 **Acceleration of Applications with FPGA-based Computing Machines: Pathfinding Algorithm**, *MSc. Thesis (Co-Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Pedro Filipe Silva

This MSc thesis was a collaboration with the IT4Innovations National Supercomputing Center in the Czech Republic.

2020-Present **Generating Hardware Modules via Binary Translation of RISC-V Binaries**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), João Miguel Conceição

This MSc thesis is a contribution to the PEPCC national project.

2020-2021 **Runtime Management of Heterogeneous Compute Resources in Embedded Systems**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Luís Miguel de Sousa

This MSc thesis was a contribution to the PEPCC national project.

2020-2021 **Vehicle Tracking in Warehouses via Bluetooth Beacon Angle-of-Arrival**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Telmo Francisco Soares

This MSc thesis was a contribution to the on-going SLID national project.

2020 **Online Interactive Demonstrator of Binary Translation Tools**, *Summer Internship (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Gonçalo José Monteiro

Interactive demonstrator for compilation framework of hardware accelerators, developed for the PEPCC national project.[5]

2020 **Dynamically Reconfigurable Multi-Classifier Architecture on FPGA**, *MSc. Thesis (Co-Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Joana Lima Macedo

This MSc thesis was a contribution to the PEPCC national project.

2019 **Run-Time Selection of Customized Accelerators**, *MSc. Thesis (Co-Supervisor)*, University of Porto, Faculty of Engineering (FEUP), José Miguel Carvalho de Campos

2019 **Solar Powered Bluetooth Low Energy Tag PCB Design**, *CTM Summer Internship (Supervisor)*, INESC-TEC, João Pedro Loureiro, and José Pedro Carvalho

2016 **Embedded Scheduler for Dynamically Reconfigurable Accelerators**, *MSc. Thesis (Co-Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Carlos Jorge Matos Carneiro de Sousa

2014 **Implementing an HDMI Based Demo of Binary Acceleration Approach**, *Student Internship (Co-Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Cédric Gerval (ISEN, France)

Supervising the implementation of a demonstrator of developed binary acceleration techniques on FPGA.

Jury Participations

2021 **PDIS (EIC0087) Sessions**, *Jury Member*, University of Porto, Faculty of Engineering (FEUP), MIEIC Syllabus

Participation as jury member in Dissertation Planning sessions (president and examiner)

Interventions in the Scientific Community

Event Organization

2022-Present **CTM Open Day 2022**, *Organizing Committee (General Chair)*, INESC TEC, Porto, Portugal

General chair for organization of CTM Open Day 2022, and event with 2 days of interactive workshops for students, focusing on the scientific area's of work at INESC TEC's Center for Telecommunications and Multimedia

2021-Present **CTM Social Event 2022**, *Organizing Committee*, INESC TEC, Porto, Portugal

Organization of teambuilding social event for NESC TEC's Center for Telecommunications and Multimedia, including activities, catering, and scientific components.

2021 ***XVII Jornadas sobre Sistemas Reconfiguráveis (REC)***, *Local Committee*, INESC TEC, Porto, Portugal

Organization, scheduling, reviewing, supporting staff

[5] The demo site can be found at `http://specs.fe.up.pt/tools/btf/`

2021 **5th Edition of the CTM Summer Internships Programme (2021)**, *Organizing Committee*, INESC TEC, Porto, Portugal
Registration, scheduling, submission reviewing, supporting staff

2015 **1st Doctoral Congress in Engineering (DCE 2015)**, *Organizing Committee*, University of Porto, Faculty of Engineering (FEUP)
Web-chair, registration, graphic design, submission reviewing, supporting staff

2013 **23rd International Conference on Field Programmable Logic and Applications (FPL 2013)**, *Organizing Committee*, Porto, Portugal
Registration, supporting staff

Event Participation

2021 **AI For Good - Machine Learning in 5G Challenge**, *Team Supervisor*, Virtual, Worldwide Competition Organized by ITU and Xilinx Inc.
Supervision of 4-member team targeting a AI problem for 5G communication. The team was selected as the winner of a first contest phase on the topic of Machine Learning in 5G, and winner of a final phase among 32 finalists from 82 countries.

2020 ***XVI Jornadas sobre Sistemas Reconfiguráveis (REC)***, *Participation in Academia Panel*, Instituto Superior Técnico, Lisboa, Portugal
Panelist in session on FPGAs in Education

Apr. 2019 ***17ª Mostra da Universidade do Porto 2019***, *Participation in Exhibition Floor*, Porto, Portugal
Represented INESC-TEC in Exhibition hall

Jul. 2019 **4th Edition of the CTM Summer Internships Programme (2018)**, *Internship supervisor*, INESC TEC, Porto, Portugal
Tutoring and supervision of a one month internship project on the topic of solar energy harvesting for Bluetooth Low-Energy asset tracking tags.

2019 ***"ENE3 - Encontro Nacional de Estudantes de Engenharia Electrotécnica"***, *Participation in Industry Session*, University of Aveiro, Aveiro, Portugal
Represented INESC-TEC in Industry Session

2016 **Open Day CTM**, *Project Presentation*, INESC-TEC, Porto, Portugal
Presentation of image processing acceleration via FPGA

Apr. 2014 **Erasmus Intensive Program 2014 "BioElectronics for Medical Engineering (BELEM)"**, *Lecturer and supervisor*, University of Bordeaux, France
Tutoring and supervision of student projects for a 2 week course in the topics of analog and digital design in the field of BioElectronic applications.

Apr. 2014 **Demo session of "Transparent Binary Acceleration Using Reconfigurable Hardware"**, *Demo and Poster Presentation*, at the 10th International Symposium on Applied Reconfigurable Computing (ARC), Vilamoura, Algarve, Portugal
Hands-on demo and poster presentation of instruction trace based hardware generation.

2019 **Demo session of "Toolflow for Generation of Reconfigurable Processing Units from Binary Traces"**, *Demo and Poster Presentation*, at the 23rd International Conference on Field programmable Logic and Applications (FPL), Porto, Portugal

Jul. 2013 **9th Intl. Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES)**, *School attendance and poster presentation*, Fiuggi, Italy
Participation in two week summer school, and presentation of poster "Binary Acceleration Using Reconfigurable Hardware"

Scientific Reviews

Publons Profile `https://publons.com/researcher/3161219/nuno-paulino/`

Artifact Reviews EuroPAR 2021

Conference Reviews IEEE FPL, IEEE MWSCAS, IEEE ReConFig, REC'2020, REC'2021, ARCS'2021

Journal Reviews MDPI Electronics, IEEE VLSI, Hindawi IJRC, IEEE Access, Electronic Letters

Presentations

Jun. 2021 **FPGAs 101 for Software Engineers**, *Keynote*, at *XVII Jornadas sobre Sistemas Reconfiguráveis (REC'2021)*, `http://dx.doi.org/10.13140/RG.2.2.13302.11843`, Faculdade de Engenharia da Universidade do Porto
Porto, Portugal

Jun. 2021 **Evaluating a Novel Bluetooth 5.1 AoA Approach for Low-Cost Indoor Vehicle Tracking via Simulation**, *Conference paper presentation*, at 2021 Joint EuCNC & 6G Summit, Virtual Conference

Sep. 2020 **Executing ARMv8 Loop Traces on Reconfigurable Accelerator via Binary Translation Framework**, *Conference paper presentation*, at Field Programmable Logic and Applications (FPL), Virtual Conference

Feb. 2020 **A Binary Translation Framework for Automated Hardware Generation**, *Demo presentation*, at Design Automation & Test in Europe (DATE), Virtual Conference

Feb. 2020 **A Survey on Binary Acceleration Approaches in Embedded Systems**, *Keynote*, at *XVI Jornadas sobre Sistemas Reconfiguráveis (REC'2021)*, Instituto Superior Técnico
Lisboa, Portugal

Feb. 2019 **Dynamic Partial Reconfiguration of Customized Single-Row Accelerators**, *Keynote*, at *XV Jornadas sobre Sistemas Reconfiguráveis (REC)*, Universidade do Minho
Guimarães, Portugal

Sep. 2017 **On Coding Techniques for Targeting FPGAs via OpenCL**, *Conference paper presentation*, at International Conference on Parallel Computing, ParCO, Bologna, Italy

Feb. 2015 **Transparent Binary Acceleration via Automatically Generated Reconfigurable Processing Units**, *Conference paper presentation*, at *XI Jornadas sobre Sistemas Reconfiguráveis (REC)*, ISEP, Porto

Aug. 2014 **Trace-Based Reconfigurable Acceleration with Data Cache and External Memory Support**, *Conference paper presentation*, at IEEE Intl. Symposium on Parallel and Distributed Processing with Applications (ISPA), Milan, Italy

Jul. 2014 **Transparent Hardware Generation from Assembly Code at program Execution Time**, *Invited Talk*, at Ruhr University Bochum, Bochum, Germany
Invited talk on on-going PhD research.

Apr. 2014 **Overview of Digital System Design**, *Lecturer*, at Erasmus Intensive Program 2014 "BioElectronics for Medical Engineering (BELEM)", University of Bordeaux, France
Lecture on the basics of digital system design.

Sep. 2013 **Transparent Hardware Generation from Assembly Code at Program Execution Time**, *Conference paper presentation*, at Field Programmable Logic and Applications (FPL), Porto, Portugal

Jun. 2013 **Runtime Transparent Hardware Generation from Execution Instruction Traces**, *Student Conference Paper Presentation*, at 2nd PhD Students Conference in Electrical and Computer Engineering, University of Porto, Faculty of Engineering (FEUP), Porto, Portugal

Mar. 2013 **Architecture for Transparent Binary Acceleration of Loops with Memory Accesses**, *Conference paper presentation*, at International Symposium on Applied Reconfigurable Computing (ARC), Los Angeles, United States

Mar. 2013 **Generation of Coarse-Grained Reconfigurable Processing Units for Binary Acceleration**, *Conference paper presentation*, at *VIII Jornadas sobre Sistemas Reconfiguráveis (REC)*, Los Angeles, United States