Nuno M.C. Paulino

PhD in Electrical and Computer Engineering

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Summary

Name	Nuno Miguel Cardanha Paulino
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Google Scholar	`https://scholar.google.com/citations?user=-gY3OIYAAAAJ`
Personal Website	`https://nmcp88.github.io/`

Short Bio

Nuno Paulino received a M.Sc. degree in Electrical and Computer Engineering from the Faculty of Engineering of the University of Porto in 2011. He received his Ph.D. in the same field from the same institution in 2015, where he currently is an Invited Assistant Professor. He has been a researcher at INESC Technology and Science since 2015, where he has participated in 15 research projects. He has supervised and co-supervised over 20 MSc thesis, and is currently supervising and co-supervising 9 MSc theses and two PhD thesis. He has participated in four Horizon Europe projects (Chips JU or SNS JU), one National project, and taken a PI role in an on-going Exploratory National Project on heterogeneous computing. He further has participated in an on-going Chips JU project on edge compute, and is contributing to the preparation of a four additional proposals in the same funding programme, focusing on tools and designs for heterogeneous edge SoCs for AI workloads. His research interests include run-time reconfigurable systems, edge computing in FPGAs, co-processor hardware acceleration, tools for hardware/software co-design automation, new heterogeneous computing architectures in the RISC-V ecosystem, and wireless telecommunications.

Education & Experience

2018-Present **Auxiliary Researcher**, *INESC-TEC (Instituto de Engenharia de Sistemas e Computadores, Tecnologia e Ciência)*, Porto, Portugal

Research on the PEPCC project (completed January 2022), and on Innovation Actions with national companies, via the WHERE.IS and SLID national Co-Promotion projects, and via service contracts with LEs such as Amorim Cork. Further participation in four Horizon Europe projects (Chips JU or SNS JU), one National project, and PI role in an additional Exploratory National Project, with focus on heterogeneous and edge computing, via hardware acceleration on RISC-V systems. Participation in the preparation of over half a dozen Horizon Europe proposals and four national projects. Organization of several public events and supervision of over 20 MsC theses and two PhD theses.

2016-2018 **Post-Doc Researcher (BI Grant)**, *INESC-TEC (Instituto de Engenharia de Sistemas e Computadores, Tecnologia e Ciência)*, Porto, Portugal

Research on the SMILES and PEPCC projects, focusing on computing for HPC and techniques for generation of heterogeneous systems.

2012-2015 **PhD in Electrical and Computer Engineering**, *University of Porto, Faculty of Engineering (FEUP)*, Porto, Portugal, *Cum Laude (Grade–17.88/20)*

Relevant areas: Embedded Systems, Hardware Accelerators, FPGA Design, Robotic Manipulators and Mobile Robotics, Microelectronics and Micromechanics, Image Recognition, Computer Vision, and Machine Learning

2009-2012 **MSc in Electrical and Computer Engineering**, *University of Porto, Faculty of Engineering (FEUP)*, Porto, Portugal *(Grade–16.46/20)*

Relevant areas: VLSI Circuits and Digital Systems, Microprocessors, Peripherals and Interfaces, Computer Networks, Semiconductors and Optoelectronics

2011 **FCT Research Grant (BI/FhP-11/003)**, *Fraunhofer AICOS*, Porto, Portugal

Design and implementation of a hardware and software infrastructure of a large scale web-interactive wall-mounted LED clock for Fraunhofer AICOS. The project entailed PCB design, development and integration of the website and backend control software residing in the embedded control system composed by microcontroller and an FPGA.

Scientific and Technological Development

Publication Summary

Year	Conference	ACM/IEEE	Journal	Q1/Q2	Citations
2011-2015	3	4	3	3	108
2016-2021	8	4	4	7	67
2012-2027	6	3	2	7	73
Total	28	17	11	9	248

Summarized are all publications in conferences and journals, with a discriminated subset of ACM/IEEE conference publications and Q1/Q2 journal articles. For about half of the listed publications, I was first author, and principal developer and researcher of the scientific and technological contributions. According to Google Scholar, my h-index is currently 9.

International Journal Publications

1 **Nuno Paulino**, Luís Pessoa. 2022. *"Self-Localization via Circular Bluetooth 5.1 Antenna Array Receiver"*, IEEE Access, Volume 11 (2023)

2 Jose Rosa, Daniel Granhao, Guilherme Carvalho, Tiago Gonçalves, Monica Figueiredo, Luis Conde Bento, **Nuno Paulino**, Luís M. Pessoa. 2022. *"BacalhauNet: A tiny CNN for lightning-fast modulation classification"*, TU Journal on Future and Evolving Technologies, Volume 3 (2022), Issue 2

3 **Nuno Paulino**, Luís Pessoa, André Branquinho, Rafael Almeida, Igor Ferreira. 2022. *"Optimizing Packet Reception Rates for Low Duty-Cycle BLE Relay Nodes"*, in IEEE Sensors Journal, vol. 22, no. 13, pp. 13753-13762, 1 July1, 2022

4 **Nuno Paulino**, João Bispo, João Canas Ferreira, and João M. P. Cardoso. 2021. *"A Binary Translation Framework for Automated Hardware Generation"*, in IEEE Micro: Special Issue on FPGAs in Computing, July 2021, 8 pages

5 **Nuno Paulino**, João Canas Ferreira, and João M. P. Cardoso. 2020. *"Improving Performance and Energy Consumption in Embedded Systems via Binary Acceleration: A Survey"*, ACM Comput. Surv. 53, 1, Article 6 (February 2020), 36 pages

6 **Nuno Paulino**, João Canas Ferreira, and João M. P. Cardoso. 2020. *"Optimizing OpenCL Code for Performance on FPGA: k-Means Case Study With Integer Data Sets"*, in IEEE Access, vol. 8, pp. 152286-152304, 2020

7 **Nuno Paulino**, João C. Ferreira, and João M.P. Cardoso. *"Dynamic Partial Reconfiguration of Customized Single-Row Accelerators"*, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 27, no. 1, pp. 116-125, Jan. 2019

8 **Nuno Paulino**, João C. Ferreira, and João M.P. Cardoso. *"Generation of Customized Accelerators for Loop Pipelining of Binary Instruction Traces"*, in IEEE Transactions on Very Large Scale Integration Systems, vol. 25, no. 1, pp. 21-34, Jan. 2017

9 **Nuno Paulino**, João Canas Ferreira, and João M. P. Cardoso. 2013. *"A Reconfigurable Architecture for Binary Acceleration of Loops with Memory Accesses"*, ACM Trans. Reconfigurable Technol. Syst. 7, 4, Article 29 (December 2014), 20 pages

10 João Bispo, **Nuno Paulino**, João M. P. Cardoso and João C. Ferreira, *"Transparent Runtime Migration of Loop-Based Traces of Processor Instructions to Reconfigurable Processing Units"*, International Journal of Reconfigurable Computing, 2013

11 João Bispo, **Nuno Paulino**, João C. Ferreira and João M. P. Cardoso, *"Transparent Trace-Based Binary Acceleration for Reconfigurable HW/SW Systems"*, IEEE Transactions on Industrial Informatics, vol. 9, no. 3, pp. 1625-1634, Aug. 2013

International Conference Publications

1 Guilherme Oliveira, Vinicius Pirassoli, Luís Miguel Sousa, **Nuno Paulino**. 2025. *"RISC++: Towards an HLS Defined RISC-V SoC"*, 28th Euromicro Conference Series on Digital System Design (DSD)

2 Nelson Neto, José Pedro Ferreira, Pedro Gonçalo Correia, Juan Gallego, Alfonso Rodríguez, Andrés Otero, **Nuno Paulino**, and João Bispo. 2025. *"Towards Offloading C/C++ Kernels and ONNX Models to CGRAs through MLIR"*, 21st International Symposium on Applied Reconfigurable Computing (ARC)

3 **Nuno Paulino** *et al.* 2025. *"Human activity recognition with a 6.5 GHz reconfigurable intelligent surface for Wi-Fi 6E"*, 2025 EuCNC (European Conference on Networks and Communications)

4 **Nuno Paulino** *et al.* 2025. *"Design and Implementation of Scalable 6.5 GHz Reconfigurable Intelligent Surface for Wi-Fi 6E"*, 2025 European Conference on Antennas and Propagation (EuCAP)

5 F. B. Teixeira *et al.* 2024. *"CONVERGE: A Vision-Radio Research Infrastructure Towards 6G and Beyond"*, 2024 EuCNC & 6G Summit

6 Rafael Aguiar, **Nuno Paulino**, Luís Pessoa. 2024. *"A Deep Learning Approach in RIS-based Indoor Localization"*, 2024 EuCNC & 6G Summit

7 Mariana Oliveira, Francisco M. Ribeiro, **Nuno Paulino**, Okan Yurduseven, Luís M. Pessoa. 2024. *"SpecRF-Posture: Exploring Specular Reflections for Human Posture Recognition"*, IEEE International Mediterranean Conference on Communications and Networking (MeditCom)

8 Manuel da Silva, Luís Crespo, Nuno Neves **N. Paulino**, João Bispo, 2024, *"Multi-Target DSL and MLIR Dialect for Streaming"*, 16th Workshop on Rapid Simulation and Performance Evaluation for Design (RAPiDO 2024)

9 Miguel Henriques, João Bispo, **N. Paulino**, 2024, *"Using Source-to-Source to Target RISC-V Custom Extensions: UVE Case-Study"*, LATTE'2024 (an ASPLOS'2024 Workshop)

10 Manuel da Silva, **N. Paulino**, João Bispo, 2024, *"A DSL and MLIR Dialect for Streaming and Vectorisation"*, International Symposium on Applied Reconfigurable Computing (ARC 2024)

11 Rafael Aguiar, **Nuno Paulino**, Luís Pessoa. 2023. *"Enhancing NLoS RIS-Aided Localization with Optimization and Machine Learning"*, IEEE Globecom Workshops

12 João Bispo, **N. Paulino**, Luís Miguel, *"Challenges and Opportunities in C/C++ Source-To-Source Compilation"*, 14th Workshop on Parallel Programming and Run-Time Management Techniques for Many-Core Architectures and 12th Workshop on Design Tools and Architectures for Multicore Embedded Computing Platforms (PARMA-DITAM 2023), (Invited Paper)

13 Luís Miguel, João Bispo, **N. Paulino**, *"Retargeting Applications for Heterogeneous Systems with the Tribble Source-to-Source Framework"*, HiPEAC 2023, WRC: Workshop on Reconfigurable Computing (HiPEAC 2023)

14 **N. Paulino**, L. M. Pessoa, A. Branquinho and E. Gonçalves, *"Design and Experimental Evaluation of a Bluetooth 5.1 Antenna Array for Angle-of-Arrival Estimation"*, 2022 13th International Symposium on Communication Systems, Networks and Digital Signal Processing (CSNDSP)

15 L. M. Sousa, **N. Paulino**, J. C. Ferreira and J. Bispo, *"A Flexible HLS Hoeffding Tree Implementation for Runtime Learning on FPGA"*, 2022 IEEE 21st Mediterranean Electrotechnical Conference (MELECON)

16 P. F. Silva, J. Bispo and **N. Paulino**, *"FPGAs as General-Purpose Accelerators for Non-Experts via HLS: The Graph Analysis Example"*, 2021 International Conference on Field-Programmable Technology (ICFPT), 2021, pp. 1-4

17 T. Santos, **N. Paulino**, J. Bispo, J. M. P. Cardoso and J. C. Ferreira, *"On the Performance Effect of Loop Trace Window Size on Scheduling for Configurable Coarse Grain Loop Accelerators"*, 2021 International Conference on Field-Programmable Technology (ICFPT), 2021, pp. 1-4

18 L. Sousa, **N. Paulino**, J. C. Ferreira, and J. Bispo, *"A Position on Transparent Reconfigurable Systems"*, 2021, LATTE'2021 (an ASPLOS'2021 Workshop)

11 P. Silva, J. Bispo, and **N. Paulino**, *"Building Beyond HLS: Graph Analysis and Others"*, 2021, . arXiv preprint arXiv:2104.02676

19 **Nuno Paulino**, Luís M. Pessoa, André Branquinho, and Edgar Gonçalves. 2021. *"Evaluating a Novel Bluetooth 5.1 AoA Approach for Low-Cost Indoor Vehicle Tracking via Simulation"*, in Proc. of the 2021 Joint EuCNC & 6G Summit, Virtual Conference (Portugal), 6 pages

20 **Nuno Paulino**, João C. Ferreira, João Bispo, and João M.P. Cardoso. *"Executing ARMv8 Loop Traces on Reconfigurable Accelerator via Binary Translation Framework"*, In Proceedings of the 30th International Conference on Field-Programmable Logic and Applications (FPL), 2020

21 **Nuno Paulino**, Luís Reis, and João M.P. Cardoso. *"On Coding Techniques for Targeting FPGAs via OpenCL"*, In Proceedings of the 2017 International Conference on Parallel Computing (ParCo), 2017

22 **Nuno Paulino**, João C. Ferreira, and João M.P. Cardoso. *"Transparent acceleration of program execution using reconfigurable hardware"*, In Proceedings of the 2015 Design, Automation & Test in Europe Conference & Exhibition (DATE), 2015

23 **Nuno Paulino**, João C. Ferreira, and João M.P. Cardoso. *"Trace-Based Reconfigurable Acceleration with Data Cache and External Memory Support"*, In IEEE Intl. Symp. on Parallel and Distributed Processing with Applications (ISPA), pp. 158–165, 2014

24 **Nuno Paulino**, João C. Ferreira and João M. P. Cardoso. *"Architecture for Transparent Binary Acceleration of Loops with Memory Accesses"*, In Proc. of the 9th Intl. Conf. on Reconfigurable Computing: Architectures, Tools, and Applications (ARC'13), pp. 122-133, 2013

25 João Bispo, **Nuno Paulino**, João M. P. Cardoso and João Canas Ferreira, *"From Instruction Traces to Specialized Reconfigurable Arrays"*, In Proc. of the Intl. Conf. on Reconfigurable Computing and FPGAs (ReConFig), pp.386-391, 2011

Data Sets

1 Mariana Oliveira, Francisco Ribeiro, **Nuno Paulino**, Okan Yurduseven, Luís Pessoa, 2024, "SpecRF-Posture Dataset", GitHub Repository, https://github.com/franciscombr/SpecRF-Posture/

2 **Nuno Paulino**, November 18, 2022, "A Dataset of Phase Samples using an 8-Element Uniform Circular Antenna Array and a Bluetooth Low Energy 5.1 Nordic nRF52811 Based Receiver", IEEE Dataport, doi: https://dx.doi.org/10.21227/92ba-e365.

3 **Nuno Paulino**, July 28, 2020, "A Batch of Integer Data Sets for Clustering Algorithms", IEEE Dataport, doi: https://dx.doi.org/10.21227/smta-vv06.

National Conference Publications

1 Pedro Ramalho, Manuel Cerqueira da Silva, João Bispo, **Nuno Paulino**. 2024. *"Extendable and Decoupled Multi-Level Intermediate Representation (MLIR) Compilation with JavaScript"*, INForum 2024

2 Vinicus Pirassoli, Luís Sousa, **Nuno Paulino**, and João Bispo. 2024. *"RISC++: A 32-bit RISC-V Core via High-Level Synthesis of C/C++"*, XIX Jornadas sobre Sistemas Reconfiguráveis (REC)

3 José Rosa, Daniel Granhão, Guilherme Carvalho, Tiago Gonçalves, Monica Figueiredo, Luis Conde Bento, **Nuno Paulino** and Luis M. Pessoa, *"BacalhauNet: A Tiny CNN for Lightning-Fast Modulation Classification"*, XVIII Jornadas sobre Sistemas Reconfiguráveis, 4-5 July, 2022

4 **Nuno Paulino**, João C. Ferreira and João M. P. Cardoso, *"Transparent Binary Acceleration via Automatically Generated Reconfigurable Processing Units"*, XI Jornadas sobre Sistemas Reconfiguráveis, Fev. 5-6, 2015

5 **Nuno Paulino**, João C. Ferreira and João M. P. Cardoso, *"Generation of Coarse-Grained Reconfigurable Processing Units for Binary Acceleration"*, VII Jornadas sobre Sistemas Reconfiguráveis, pp.11-19, Fev. 9 2012-Fev. 10, 2012

Participation in Research Projects

2025-Present **POEMS: Portuguese Competence Centre in Semiconductors**, *Researcher, Chips JU*, INESC-TEC, Funded by the ERDF

The main objective of POEMS is to align with the Chips for Europe Initiative, and is meant to provide an aggregation and improvment of all semiconductor related competences and players at a national level. This aims to improve Portugal's capacity for semiconductor innovation and production, specifically focusing on microelectronics and semiconductors, pivotal for elevating the existing industrial and technological capacities to meet the key global challenges. POEMS leverages the diverse expertise of its 16 consortium partners, including leading research and academic institutions.

2025-Present **STREAM: Smart Tracking and Real-time Enhanced Asset Management**, *Researcher, I&DT EM COPROMOÇÃO*, INESC-TEC, Funded by ANI (Agência Nacional de Inovacão), via COMPETE2030

The main objective of STREAM is to augment factory operations with improved real-time localization systems based on WiFi-6 and novel reconfigurable antennas, with asset tracking capable of vertical localization of tagged assets, and to communicate all this information jointly to a central system equipped with digital twin based 3D visualization, further aided by natural language based queries from operators to the system, to improve overall efficiency.

2023-Present **CONVERGE: Telecommunications and Computer Vision Convergence Tools for Research Infrastructures**, *Researcher, European HORIZON*, INESC-TEC, Funded by ERDF

The main objective of the CONVERGE project is the development of an innovative toolset aligned with the motto "view-to-communicate and communicate-to-view". This toolset is a world-first and consists of vision-aided large intelligent surfaces, vision-aided fixed and mobile base stations, a vision-radio simulator and 3D environment modeler, and machine learning algorithms for multimodal data.

2023-Present **TERRAMETA: TERahertz ReconfigurAble METAsurfaces For Ultra-High Rate Wireless Communications**, *Researcher, European HORIZON-JU-SNS-2022-STREAM-B-01-02*, INESC-TEC, Funded by ERDF

TERRAMETA is a Horizon Europe project which aims to investigate revolutionary technologies for 6G and demonstrate the feasibility of Terahertz (THz) Reconfigurable Intelligent Surface (RIS) assisted ultra-high data rate wireless communications networks.

2023-Present **SUPERIOT (Truly Sustainable Printed Electronics-based IoT Combining Optical and Radio Wireless Technologies)**, *Researcher, European HORIZON-JU-SNS-2022-STREAM-B-01-03*, INESC-TEC, Funded by ERDF

SUPERIOT is a Horizon Europe project which aims to develop a truly sustainable and highly flexible internet of things (IoT) system based on the dual-mode use of optical and radio communications, combined with the exploitation of printed electronics technology.

2023-Present **AI-Q Ready**, *Researcher, European HORIZON-KDT-JU-2021-2-RIA Project*, INESC-TEC, Funded by ERDF

The AI-Q Ready project is a large European project with 50 partner institutions. INESC TEC is responsible for one of the deliverables of one of the eight supply chains. Specifically, we will focus on compilation tool-chains for RISC-V Based Heterogeneous AI Accelerators, and on development of tools for heterogeneous SoC development in general (e.g., HW/SW partitioning, CGRA APIs, etc).

2023-Present **TORIS (Towards fully printed Reconfigurable Intelligent Surfaces)**, *Researcher, National Project*, INESC-TEC (in partnership with INESC-ID/IST), Funded by FCT Grant 2022.09084.PTDC

This exploratory project aims to implement digital control of Reconfigurable Intelligent Surfaces (RIS), in order to achieve directional communication by controlled reflection of eletromagnetic wavefronts. It is an enabler technology for 5G/6G communications.

Scheduled for 2023 **UNIFY**, *Researcher, National Project*, INESC-TEC (in partnership with INESC-ID/IST), Funded by FCT

The UNIFY project addresses research of intermediate level representations and transformations in order to lower generic high-level source code into different heterogeneous targets, such as FPGAs, CGRAs, deep pipelines, or MPPAs. The objective is to allow easy compilation onto heterogeneous SoCs without developer effort or intervention. A contribution towards the LLVM-IR/MLIR ecosystem is expected.

2019-2022 **STRx - Transmission and reception system of electronically oriented signals for next generation satellite constellations**, *Researcher, National Project*, INESC-TEC (in partnership with Sinuta SA.), Funded by FEDER, POCI-01-0247-FEDER-033623

The STRx project is focused on developing new beamforming technologies, from the device level (i.e., planar antenna arrays) to the computation level (e.g., algorithms, including hardware accelerated implementations), for future MIMO 5G/6G systems.

2019-2022 **SLID - Stock Live IDentification**, *Researcher, National Project*, INESC-TEC (in partnership with Wavecom), Funded by ERDF, Grant POCI-01-0247-FEDER-045388

The SLID project focuses on the development of a product that can be used in cargo vehicles and indirectly track the location and movement of all products in stock, in all logistical scenarios. The project explores the use of Bluetooth 5.2 Low Energy for indoor location and tracking using Angle-of-Arrival technology with antenna arrays in mobile receivers. The solution is expected to improve the logistical efficiency of industrial processes.

2018-2019 **WHERE.IS - Localização e tracking de equipamentos em ambiente indoor**, *Researcher, National Project*, INESC-TEC (in partnership with Wavecom), Funded by ERDF, Grant POCI-01-0247-FEDER-024191

The WHERE.IS project focused on the development of the hardware and software infrastructure of an ad-hoc mesh network of Bluetooth 4.1 beacons and receivers/re-transmitters for the location of an arbitrary number of valuable assets in multiple scenarios, such as inventory management (Casa de Música, Porto) or and real-time equipment tracking (Hospital de Braga)

2018-present **PEPCC - Power Efficiency and Performance for Embedded and HPC Systems with Custom CGRAs**, *Researcher, National Project*, INESC-TEC, Funded by FCT, Grant PTDC/EEI-HAC/30848/2017

The goal of this project is to devise efficient techniques for dynamically mapping computations extracted from execution behavior to the resources of specialized re-configurable accelerators. The techniques will identify program hot-spots at run-time. The use of specialized circuits reduces resource usage and improves performance. The methodologies and concepts to explore are relevant for emergent edge computing applications due to performance and power consumption efficiency.

2016-2017 **TEC4Growth - RL SMILES - Smart, Mobile, Intelligent and Large scale Sensing and Analytics**, *Researcher, National Project*, INESC-TEC, Funded by the CCDRN (ERDF), NORTE2020, Grant NORTE-01-0145-FEDER-000020

2016-2017 **REFLECT: Rendering FPGAs to Multi-Core Embedded Computing**, *Researcher, International Project*, Faculdade de Engenharia da Universidade do Porto (FEUP), Funded by the FP7-ICT Programme, European Commission

Artifacts from Research Projects

SLID A Dataset of Phase Samples using an 8-Element Uniform Circular Antenna Array and a Bluetooth Low Energy 5.1 Nordic nRF52811 Based Receiver, publicly available at IEEE DataPort (`https://dx.doi.org/10.21227/92ba-e365`)

PEPCC A compilation framework for exploration of future automated hardware design tools and methods.[1] I have been the main developer of the framework, which is now the host for on-going MSc theses on hardware compilation.

PEPCC A test harness for several implementation of the k-means algorithm in OpenCL, for execution on FPGA accelerator boards, publicly available at IEEE Code Ocean (`https://codeocean.com/capsule/2348736/tree/v1`)

PEPCC An Implementation of K-means written in C, publicly available at IEEE Code Ocean (`https://codeocean.com/capsule/3208075/tree/v1`)

PEPCC A Generator of Randomly Correlated N-Dimentional Clusters, publicly available at ResearchGate (`http://dx.doi.org/10.13140/RG.2.2.34866.43200`)

PEPCC A Batch of Integer Datasets for Clustering Algorithms, publicly available at IEEE DataPort (`https://dx.doi.org/10.21227/smta-vv06`)

PEPCC A C/C++ HLS-ready implementation of a Hoeffding Tree, publicly available at GitHub (`https://github.com/lm-sousa/Hoeffding-Tree`)

WHERE.IS Blueooth 4.2 receiver/re-transmitter device for indoor asset tracking, currently in commercial deployment.

[1] The framework can be found at `https://github.com/specs-feup/specs-hw`

REFLECT Internal report on acceleration opportunities and hardware designs for workload on a G.279 speech encoder application.

Patents

2020 André Branquinho, Franciso Pimenta, Igor Ferreira, José Ferreira, Luís Pessoa, **Nuno Paulino**, Rafael Almeida, *"Monitoring System for Determining the Location of Bluetooth Beacons"*, P904.4, n.º 20211000000460 (Patent Pending), 2020

Teaching and Pedagogic Activities

Teaching Experience

I have been Invited Assistant Professor of the Informatics Engineering Department (DEI) of the Faculty of Engineering (FEUP) of the University of Porto since 2017. I teach 3 to 4 hours per week of laboratory classes of first and second year subjects of the Master's Degree in Informatics and Computing Engineering (MIEIC). Prior, I was a teacher's assistant for first year programming classes for the Electric Engineering Department (DEEC) of the same institution.

2022 **Invited Class**, University of Porto, Faculty of Engineering (FEUP), Porto, Portugal
An invited class of the subject of Heterogeneous System Architectures (M.EEC049) – part of the Master's on Electrical and Computer Engineering at FEUP – regarding code translation techniques, OpenCL acceleration on FPGAs, and research on DSLs for HDL generation.

2021-2024 **Invited Assistant Professor**, *Laboratory Classes*, University of Porto, Faculty of Engineering (FEUP), Porto, Portugal
Assistant professor for the subjects of Fundamentals of Computing Systems (L.EIC004), focusing on binary representation, boolean algebra, circuit blocks, CPU organization, and ARMv8 assembly; and Computer Labs (L.EIC018), regarding C programming for design of device drivers in a VM environment (Minix).

2016-2024 **Invited Assistant Professor**, *Laboratory Classes*, University of Porto, Faculty of Engineering (FEUP), Porto, Portugal
Assistant professor for the subjects of *C/C++* Programming (EIC0012), focusing on data structures and their manipulation, and Computer Labs (EIC0020), regarding peripherals and device drivers in a MINIX environment.
EIC0020: Average 5.2/7.0 rating in a 4 year period, as per UP Pedagogical Surveys[2]
EIC0012: Average 4.6/7.0 rating in a 3 year period, as per UP Pedagogical Surveys[2]

2011 **Programming class assistant ("monitor")**, *Laboratory Classes*, University of Porto, Faculty of Engineering (FEUP), Porto, Portugal
Teaching aid during programming lab classes, according to the course plan for the MSc degree in Electrical and Computer Engineering (EEC0009), entailing: C programming and development methodologies, low-level programming, fundamental algorithmic concepts and data structures.

Teaching Material

2020 **Slides for Invited Class on Heterogeneous System Architectures**, *Author*, University of Porto, Faculty of Engineering (FEUP)
Slides for the above mentioned invited class of the subject of Heterogeneous System Architectures (M.EEC049) – part of the Master's on Electrical and Computer Engineering at FEUP.[3]

[2] Overall average of all pedagogical parameters for stated period

2018-present **(The Very) Basics of C/C++**, *Author*, University of Porto, Faculty of Engineering (FEUP)

A (work-in-progress) introduction to the basics of C and C++. The document is intended to clarify most of the gaps in knowledge I identified in programming skills of 2nd (and later) year students. As per its introduction: *This document is a condensed overview on basics of C programming, and on some concepts about compilation in general. The point of this document is to introduce you to some concepts that might not be familiar if your prior programming experience was not C/C++ or a compiled language.*[4]

2020 **LaTeX Template for Master's Thesis for the "Instituto de Ciências Biomédicas Abel Salazar (ICBAS)" from the University of Porto**, *Author*, University of Porto, Faculty of Engineering (FEUP)

An adaptation of FEUP's LaTeX Master's thesis template to conform with the formatting and typesetting requirements of the ICBAS institute. The template includes basic LaTeXinstructions and examples.[5]

Supervisions (Theses, Internships, & Research Grants)

2025-Present **Desenho de uma Cache L1 para um SoC RISC-V Sintetizável a partir de Alto Nível**, *Summer/Curricular Internship)*, INESC-TEC, João Teixeira

This internship extends a RISC-V core design written entirely in C/C++ with an L1 cache sub-system to allow for greater system complexity and SoC integration.

2025-Present **Aceleração de IA num SoC RISC-V Sintetizável a partir de Alto Nível**, *Summer/Curricular Internship)*, INESC-TEC, Henrique Sousa, José Paradela

This internship improves a RISC-V core design written entirely in C/C++, suitable for hardware synthesis. The work explores the implementation of custom instructions in logarithmic number system format, to achieve higher edge inference of language models at the edge.

2025-Present **Extensão da ferramenta de conversão ONNX-para-DFG para aceleração da IA**, *Summer/Curricular Internship)*, INESC-TEC, António Abílio

This internship is about extending a tool for conversion of AI models stored as ONNX graphs into graph formats suitable for offloading onto, or generation of, custom hardware accelerators.

2025-Present **Customização e Simulação de um System-on-Chip com core RISC-V**, *Summer/Curricular Internship)*, INESC-TEC, Vanessa Queirós

This internship topic is on extending a co-simulation system composed of a RISC-V SoC written in SystemVerilog, and an arbitrary number of high-level simulators of hardware accelerators. The internship expands the co-simulation flow to support communication via custom RISC-V instructions.

2024-Present **Implementation of Embedded Controllers for Scalable RIS Assemblies**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Francisco Marques Mesquita

This work addresses the implementation and test of software for scalable assemblies of reconfigurable intelligent surfaces, where different physical layouts can be supported by the same firmware layer, and where global or partial control of the surface can allow for multiple focusing beams or sensing approaches.

[3] The document can be found at `https://nmcp88.github.io/material/ashclass/`

[4] The document can be found at `https://nmcp88.github.io/material/basicsofc/`

[5] The document can be found at `https://nmcp88.github.io/material/icbastemplate/`

2024-Present **Design and Evaluation of CGRA-based Accelerators for Embedded RISC-V Systems**, *MSc. Thesis (Co-Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Francisco Marques Mesquita

This work is about the porting and testing of a CGRA design from partners from UPM withn the European project AI-Q Ready. The CGRA design is ported to another target SoC with a hard RISC-V core, and evaluated for performance versus soft-core implementations.

2024-Present **Improving Compilation Flows for RISC-V Machine Learning Custom Instructions**, *MSc. Thesis (Co-Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Guilherme Soares Sequeira

This work focuses on researching and refining a more lightweight approach for mapping computation to RISC-V custom instructions, in the context of machine-learning acceleration. It is framed in the context of an european project, A-IQ Ready.

2024-Present **Mapping Computations to a Stream-Oriented Domain Specific Language**, *MSc. Thesis (Co-Supervisor)*, University of Porto, Faculty of Engineering (FEUP), André Costa Lima

This work focuses on automatically mapping certain kinds of computations (e.g., well-behaved loops) to a high-level stream-oriented representation. It is framed in the context of a national project, UNIFY.

2024-2025 **Automated Integration of High-Level Simulators for RISC-V SoC Co-Simulation**, *MSc. Thesis (Co-Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Pedro Miguel Moreira Ramalho

This work extends a state-of-the-art RISC-V SoC simulation platform to allow for a more integrated communication with an external accelerator simulator, including memory access via DMA.

2024-Present **Design and Test of a 28Ghz Reconfigurable Intelligent Surface**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Francisco Gonçalves Vilarinho

This work addresses the design of a reconfigurable intelligent surface tuned for a central frequency of 28GHz, which includes also the study and implementation of the best unit cell design, and validation of the tile's beamforming capablities in an anechoic chamber.

2024-2025 **Designing an SoC with an HLS-Based RISC-V Core**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Guilherme Vareiro de Oliveira

This work deals with the integration of a C/C++ based RISC-V core into an in-house System-on-chip for deployment onto FPGA targets, considering also integration with accelerators external to the core.

2024-Present **Optimizing Large Language Model Inference on FPGAs**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), João Pedro Reis Teixeira

This work deals with implementing an architecture in FPGA that allows the energy-efficient execution of the inference step of an LLM, for edge-AI use cases.

2024-Present **Source Analysis for Automated Hardware/Software Partitioning**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), José Luís Nunes Osório

This work deals with using source analysis to identify portion of an application that are suitable for hardware acceleration, and with applying necessary transformations to make them ammenable for processing with HLS tools.

2023-2024 **RISC++: Designing an Accelerator-Ready RISC-V Core via High-Level-Synthesis of C/C++**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Vinicius Dutra Pirassoli

This thesis implemented a RISC-V core written entirely in C/C++, and lowered to hardware via HLS methods. The core was validated as a simulator through conventional C/C++ compilation, and as a hardware core by instantiation on an FPGA target.

2023-2024 **Simulation Infrastructure for Coupling CGRA Accelerator to RISC-V Processor**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Antonio Francisco Rente Ribeiro

A co-simulation framework was set up between two Unix processes: a state-of-the-art RISC-V SoC and an in-house CGRA simulator. The work will allow for further development of co-simulation of CGRA based heterogeneous systems and DSE flows.

2023-2024 **Support for Streaming SIMD Paradigms via MLIR**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Manuel Cerqueira da Silva

This work developed a DSL and MLIR dialects to lower general purpose C code into a streaming and vectorization engine coupled to a RISC-V via a custom extension, and its validation via simulation.

2023-2024 **Human Perception through Reconfigurable Intelligent Surfaces**, *MSc. Thesis (Co-Supervisor)*, University of Porto, Faculty of Sciences (FCUP), Mariana Silva Fonseca Barros Oliveira

This thesis dealt with human pose and activity estimation in simulated scenarios and real-world experimental campaigns using a in-house reconfigurable intelligent surface intelligent surface design.

2023-2024 **Design, integration and experimental validation of a 2-bit Reconfigurable Intelligent Surface**, *MSc. Thesis (Co-Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Ricardo Carvalho Araújo

This work included the implementation and characterization of a reconfigurable intelligent surface control circuit based on varactor diodes, and performance comparision versus a PIN diode based solution.

2023-2024 **Indoor Localization using Reconfigurable Intelligent Surfaces**, *MSc. Thesis (Co-Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Rafael Amaral Aguiar

This thesis addressed the modeling of a channel in WiFi band for a setup with a reconfigurable intelligent surface, generation of simulated data, and implementation of machine learning models for localization estimation in indoor scenarios.

2022-2023 **Accelerated Pattern Matching for Big Data**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Pedro Miguel Ribeiro Alves

This MSc thesis addresses the acceleration of RegEx matching using FPGA acceleratatio. The work targets server-grade FPGA accelerator cards, and continues a prior thesis with the objectives of generating more compact automata by automata prefix merging, and improving backreference support. The design space exploration of specialization of the engines versus programmability and the respective hardware performance and costs is addressed.

2022-2023 **CrispyHDL - Java Inner DSL for Verilog**, *Curricular Internship (L.EEC026)*, INESC-TEC, Luís Saraiva

This internship contributes to the on-going development of a Java DSL for programmatic generation of Verilog code. The Internship addresses automated generation of testbench modules, and functional verification of the generated HDL versus its high-level Java description.

2022-2023 **Desenvolvimento de Controlador Eletrónico para uma Smart Antenna**, *Curricular Internship (L.EEC026)*, INESC-TEC, Francisco Vilarinho

This internship addresses the porting and testing of existing code for control of antenna array elements onto an FPGA device, testing the scalability of software-only digital control of an external peripheral which emulates the antenna array, and hardware implementation of time-critical components of the algorithm.

2022-2023 **A Machine Learning Model for Indoor Positioning of Bluetooth Receivers**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Francisco Pêgo dos Santos Monteiro

This MSc thesis is a continuation of the research lines resulting from the SLID national project on indoor localization with low-power beacons for tracking, focusing on neutral network models for position estimation.

2021 **Design of embedded software for pre-processing and transmission of carrier phase data in Bluetooth module with antenna array**, *Master's Research Grant (Supervisor)*, INESC-TEC, David Cunha

This studentship was a contribution to the on-going SLID national project. Included the design of software for gathering and transmitting AoA data acquired by a Bluetooth module with antenna, and characterization of the transmission and reception quality of the module in anechoic chamber.

2021 **Design and comparison of different algorithms for AoA calculation from phase data from antenna array**, *Research Contract (Supervisor)*, INESC-TEC, Bruno Saraiva

This mentorship focused on developing diferent methods to compute the angle-of-arrival (AoA) of Bluetooth transmissions, based on experimentally acquired wave phase data.

2021-2022 **Specializing RISC-V Cores for Performance and Power**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Henrique Veloso de Sousa

This MSc thesis is a contribution to the PEPCC national project, and contributes to the start of a research line on the RISC-V ecosystem.

2021-2023 **Designing an Instruction Set Based Coarse Grain Accelerator**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Gonçalo de Albuquerque Ferreira

This MSc thesis is a contribution to the PEPCC national project, and contributes to the start of a research line on the RISC-V ecosystem.

2021 **Desenvolvimento de antena integrada para recetor Bluetooth Low Energy 5.1**, *CTM Summer Internship (Co-Supervisor)*, INESC-TEC, Margarida Costa

This internship was a contribution to the on-going SLID national project.

2021 **Angle-of-Arrival Estimation on FPGA from IQ Samples**, *CTM Summer Internship (Supervisor)*, INESC-TEC, Gabriella Pantaleão

This internship was a contribution to the on-going SLID national project.

2020-2021 **Design of Bluetooth Low Energy 5.1 Angle-of-Arrival Based Receiver for Indoor Asset Tracking**, *Scientific Initiation Studentship (Supervisor)*, INESC-TEC, Catarina Alexandre Marques

This studentship was a contribution to the on-going SLID national project.

2020-2021 **Acceleration of Applications with FPGA-based Computing Machines: Pathfinding Algorithm**, *MSc. Thesis (Co-Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Pedro Filipe Silva

This MSc thesis was a collaboration with the IT4Innovations National Supercomputing Center in the Czech Republic.

2020-Present **Generating Hardware Modules via Binary Translation of RISC-V Binaries**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), João Miguel Conceição

This MSc thesis is a contribution to the PEPCC national project.

2020-2021 **Runtime Management of Heterogeneous Compute Resources in Embedded Systems**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Luís Miguel de Sousa

This MSc thesis was a contribution to the PEPCC national project.

2020-2021 **Vehicle Tracking in Warehouses via Bluetooth Beacon Angle-of-Arrival**, *MSc. Thesis (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Telmo Francisco Soares

This MSc thesis was a contribution to the on-going SLID national project.

2020 **Online Interactive Demonstrator of Binary Translation Tools**, *Summer Internship (Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Gonçalo José Monteiro

Interactive demonstrator for compilation framework of hardware accelerators, developed for the PEPCC national project.[6]

2020 **Dynamically Reconfigurable Multi-Classifier Architecture on FPGA**, *MSc. Thesis (Co-Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Joana Lima Macedo

This MSc thesis was a contribution to the PEPCC national project.

2019 **Run-Time Selection of Customized Accelerators**, *MSc. Thesis (Co-Supervisor)*, University of Porto, Faculty of Engineering (FEUP), José Miguel Carvalho de Campos

2019 **Solar Powered Bluetooth Low Energy Tag PCB Design**, *CTM Summer Internship (Supervisor)*, INESC-TEC, João Pedro Loureiro, and José Pedro Carvalho

2016 **Embedded Scheduler for Dynamically Reconfigurable Accelerators**, *MSc. Thesis (Co-Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Carlos Jorge Matos Carneiro de Sousa

2014 **Implementing an HDMI Based Demo of Binary Acceleration Approach**, *Student Internship (Co-Supervisor)*, University of Porto, Faculty of Engineering (FEUP), Cédric Gerval (ISEN, France)

Supervising the implementation of a demonstrator of developed binary acceleration techniques on FPGA.

Jury Participations

2021 **Daniel Zheng Dong, "Multi-technology Indoor Localization with Data Fusion", Master's Thesis, FCUP**, *Jury Member*, University of Porto, Faculty of Sciences (FCUP)

Participation as jury member in evaluation of Master's thesis.

[6] The demo site can be found at `http://specs.fe.up.pt/tools/btf/`

2021 **PDIS (EIC0087) Sessions**, *Jury Member*, University of Porto, Faculty of Engineering (FEUP), MIEIC Syllabus
Participation as jury member in Dissertation Planning sessions (president and examiner)

Awards

Dec. 2024 **Prémio ANACOM-URSI Portugal 2024**, *Researcher*, Porto, Portugal, 18.º Congresso do Comité Português da URSI
Received the 2024 award given by the Portuguese national regulatory body on communications, *"Autoridade Nacional de Comunicações"*, focusing on use of emergent radio based technologies for sensing of human posture and human gesture classification using radio-frequency data.

2021 **AI For Good - Machine Learning in 5G Challenge**, *Team Supervisor*, Virtual, Worldwide Competition Organized by ITU and Xilinx Inc.
This is the winning submission of the ITU-ML5G-PS-007 "AI for Good Machine Learning in 5G Challenge", where Neural Networks deployed to FPGAs are used to classify radio signal modulations, using the DeepSig RadioML 2018 dataset. The submission won first place in two evaluation rounds, consisting of over 30 teams from all over the world. The submission presentation is publicly available.

Interventions in the Scientific Community

Event Organization

2023-2024 **14th International Symposium on Highly Efficient Accelerators and Reconfigurable Technologies (HEART'24)**, *Organizing Committee*, University of Porto, Faculty of Engineering (FEUP), Porto, Portugal
Local Chair

2023-2024 **XIX Jornadas sobre Sistemas Reconfiguráveis (REC)**, *Programme Committe*, *FEUP/INESC-TEC*, Porto, Portugal
Organization, reviewing, supporting staff

2024 **8th Edition of the CTM Summer Internships Programme (2024)**, *Organizing Committee*, INESC TEC, Porto, Portugal
General Chair (registration, scheduling, submission reviewing, supporting staff)

2022-2023 **34th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP'23)**, *Organizing Committee*, University of Porto, Faculty of Engineering (FEUP), Porto, Portugal
Webchair & Registration Chair

2022-2023 **7th Edition of the CTM Summer Internships Programme (2023)**, *Organizing Committee*, INESC TEC, Porto, Portugal
Webchair, registration, scheduling, submission reviewing, supporting staff

2022 **CTM Open Day 2022**, *Organizing Committee (General Chair)*, INESC TEC, Porto, Portugal
General chair for organization of CTM Open Day 2022, and event with 2 days of interactive workshops for students, focusing on the scientific area's of work at INESC TEC's Center for Telecommunications and Multimedia

2021-2022 **CTM Social Event 2022**, *Organizing Committee*, INESC TEC, Porto, Portugal
Organization of teambuilding social event for NESC TEC's Center for Telecommunications and Multimedia, including activities, catering, and scientific components.

2021 **XVII Jornadas sobre Sistemas Reconfiguráveis (REC)**, *Local Committee*, INESC TEC, Porto, Portugal
Organization, scheduling, reviewing, supporting staff

2021 **5th Edition of the CTM Summer Internships Programme (2021)**, *Organizing Committee*, INESC TEC, Porto, Portugal
Registration, scheduling, submission reviewing, supporting staff

2015 **1st Doctoral Congress in Engineering (DCE 2015)**, *Organizing Committee*, University of Porto, Faculty of Engineering (FEUP)
Web-chair, registration, graphic design, submission reviewing, supporting staff

2013 **23rd International Conference on Field Programmable Logic and Applications (FPL 2013)**, *Organizing Committee*, Porto, Portugal
Registration, supporting staff

Event Participation

2024 **Industry Booth in Wireless Meeting 2024 (https://wireless-meeting.com/)**, *Participation in Exhibition Floor*, Porto, Portugal
Showcase of results of TERRAMETA and CONVERGE projects (SNS JU projects funded by EFRD).

2022 **Participation in Industry Booth at VISUM Summer School**, *https://visum.inesctec.pt/*, Porto, Portugal

2022 **Speaker in Scientific Session of Wireless Meeting 2022 (https://wireless-meeting.com/)**, *Invited Speaker*, Aveiro, Portugal
Intervention of results of the SLID national project at the annual Wireless Meeting event, 2022 edition; https://www.youtube.com/watch?v=Rr3whfEhWOE

2021 **AI For Good - Machine Learning in 5G Challenge**, *Team Supervisor*, Virtual
Supervision of 4-member team targeting a AI problem for 5G communication. The team was selected as the winner of a first contest phase on the topic of Machine Learning in 5G, and winner of a final phase among 32 finalists from 82 countries.

2020 **XVI Jornadas sobre Sistemas Reconfiguráveis (REC)**, *Participation in Academia Panel*, Instituto Superior Técnico, Lisboa, Portugal
Panelist in session on FPGAs in Education

Apr. 2019 **17ª Mostra da Universidade do Porto 2019**, *Participation in Exhibition Floor*, Porto, Portugal
Represented INESC-TEC in Exhibition hall

Jul. 2019 **4th Edition of the CTM Summer Internships Programme (2018)**, *Internship supervisor*, INESC TEC, Porto, Portugal
Tutoring and supervision of a one month internship project on the topic of solar energy harvesting for Bluetooth Low-Energy asset tracking tags.

2019 **"ENE3 - Encontro Nacional de Estudantes de Engenharia Electrotécnica"**, *Participation in Industry Session*, University of Aveiro, Aveiro, Portugal
Represented INESC-TEC in Industry Session

2016 **Open Day CTM**, *Project Presentation*, INESC-TEC, Porto, Portugal
Presentation of image processing acceleration via FPGA

Apr. 2014 **Erasmus Intensive Program 2014 "BioElectronics for Medical Engineering (BELEM)"**, *Lecturer and supervisor*, University of Bordeaux, France
Tutoring and supervision of student projects for a 2 week course in the topics of analog and digital design in the field of BioElectronic applications.

Apr. 2014 **Demo session of "Transparent Binary Acceleration Using Reconfigurable Hardware"**, *Demo and Poster Presentation*, at the 10th International Symposium on Applied Reconfigurable Computing (ARC), Vilamoura, Algarve, Portugal
Hands-on demo and poster presentation of instruction trace based hardware generation.

2019 **Demo session of "Toolflow for Generation of Reconfigurable Processing Units from Binary Traces"**, *Demo and Poster Presentation*, at the 23rd International Conference on Field programmable Logic and Applications (FPL), Porto, Portugal

Jul. 2013 **9th Intl. Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems (ACACES)**, *School attendance and poster presentation*, Fiuggi, Italy
Participation in two week summer school, and presentation of poster "Binary Acceleration Using Reconfigurable Hardware"

Scientific Reviews

Web of Science Profile: `https://www.webofscience.com/wos/author/record/1876421`

Artifact Reviews: EuroPAR 2021

Conference Reviews: IEEE FPL, IEEE MWSCAS, IEEE ReConFig, REC'2020, REC'2021, ARCS'2021

Journal Reviews: MDPI Electronics, IEEE VLSI, Hindawi IJRC, IEEE Access, Electronic Letters, IEEE Sensors Journal

Presentations

March 2025 **Design and Implementation of Scalable 6.5 GHz Reconfigurable Intelligent Surface for Wi-Fi 6E**, *Conference paper presentation*, at 19th European Conference on Antennas and Propagation (EuCAP), Stockholm, Sweden

Jul. 2022 **Design and Experimental Evaluation of a Bluetooth 5.1 Antenna Array for Angle-of-Arrival Estimation**, *Conference paper presentation*, at Field Programmable Logic and Applications (CSNDSP), Porto, Portugal

Jun. 2021 **FPGAs 101 for Software Engineers**, *Keynote*, at *XVII Jornadas sobre Sistemas Reconfiguráveis (REC'2021)*, `http://dx.doi.org/10.13140/RG.2.2.13302.11843`, Faculdade de Engenharia da Universidade do Porto
Porto, Portugal

Jun. 2021 **Evaluating a Novel Bluetooth 5.1 AoA Approach for Low-Cost Indoor Vehicle Tracking via Simulation**, *Conference paper presentation*, at 2021 Joint EuCNC & 6G Summit, Virtual Conference

Sep. 2020 **Executing ARMv8 Loop Traces on Reconfigurable Accelerator via Binary Translation Framework**, *Conference paper presentation*, at Field Programmable Logic and Applications (FPL), Virtual Conference

Feb. 2020 **A Binary Translation Framework for Automated Hardware Generation**, *Demo presentation*, at Design Automation & Test in Europe (DATE), Virtual Conference

Feb. 2020 **A Survey on Binary Acceleration Approaches in Embedded Systems**, *Keynote*, at *XVI Jornadas sobre Sistemas Reconfiguráveis (REC'2021)*, Instituto Superior Técnico
Lisboa, Portugal

Feb. 2019 **Dynamic Partial Reconfiguration of Customized Single-Row Accelerators**, *Keynote*, at *XV Jornadas sobre Sistemas Reconfiguráveis (REC)*, Universidade do Minho
Guimarães, Portugal

Sep. 2017 **On Coding Techniques for Targeting FPGAs via OpenCL**, *Conference paper presentation*, at International Conference on Parallel Computing, ParCO, Bologna, Italy

Feb. 2015 **Transparent Binary Acceleration via Automatically Generated Reconfigurable Processing Units**, *Conference paper presentation*, at *XI Jornadas sobre Sistemas Reconfiguráveis (REC)*, ISEP, Porto

Aug. 2014 **Trace-Based Reconfigurable Acceleration with Data Cache and External Memory Support**, *Conference paper presentation*, at IEEE Intl. Symposium on Parallel and Distributed Processing with Applications (ISPA), Milan, Italy

Jul. 2014 **Transparent Hardware Generation from Assembly Code at program Execution Time**, *Invited Talk*, at Ruhr University Bochum, Bochum, Germany
Invited talk on on-going PhD research.

Apr. 2014 **Overview of Digital System Design**, *Lecturer*, at Erasmus Intensive Program 2014 "BioElectronics for Medical Engineering (BELEM)", University of Bordeaux, France
Lecture on the basics of digital system design.

Sep. 2013 **Transparent Hardware Generation from Assembly Code at Program Execution Time**, *Conference paper presentation*, at Field Programmable Logic and Applications (FPL), Porto, Portugal

Jun. 2013 **Runtime Transparent Hardware Generation from Execution Instruction Traces**, *Student Conference Paper Presentation*, at 2nd PhD Students Conference in Electrical and Computer Engineering, University of Porto, Faculty of Engineering (FEUP), Porto, Portugal

Mar. 2013 **Architecture for Transparent Binary Acceleration of Loops with Memory Accesses**, *Conference paper presentation*, at International Symposium on Applied Reconfigurable Computing (ARC), Los Angeles, United States

Mar. 2013 **Generation of Coarse-Grained Reconfigurable Processing Units for Binary Acceleration**, *Conference paper presentation*, at *VIII Jornadas sobre Sistemas Reconfiguráveis (REC)*, Los Angeles, United States