Centro de Informática - CIn
Universidade Federal de Pernambuco

CAN Bit Timing

Bus Synchronization

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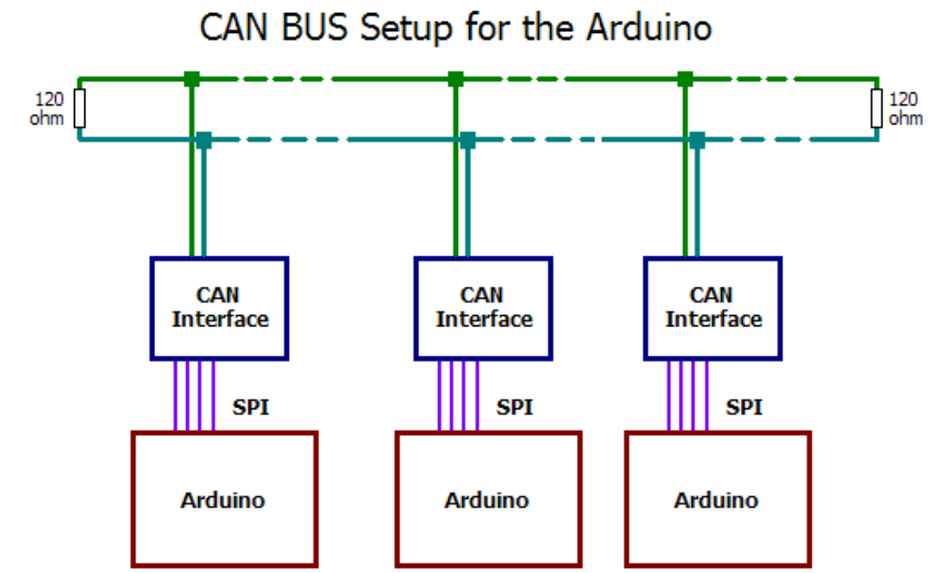
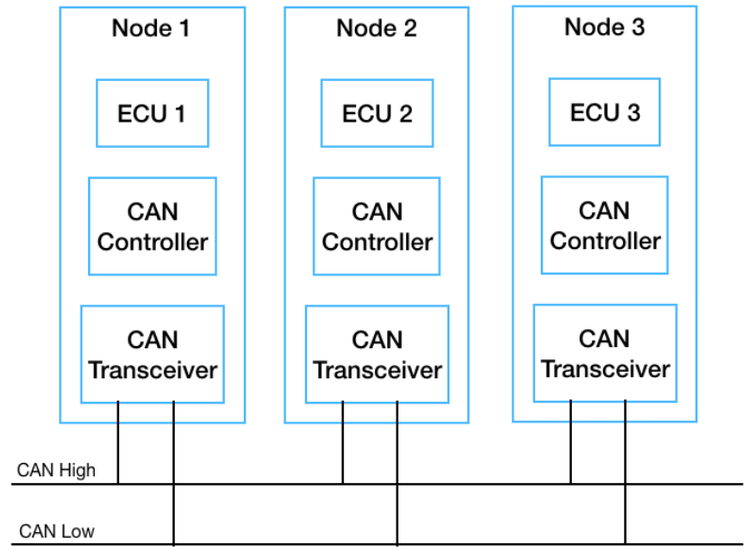
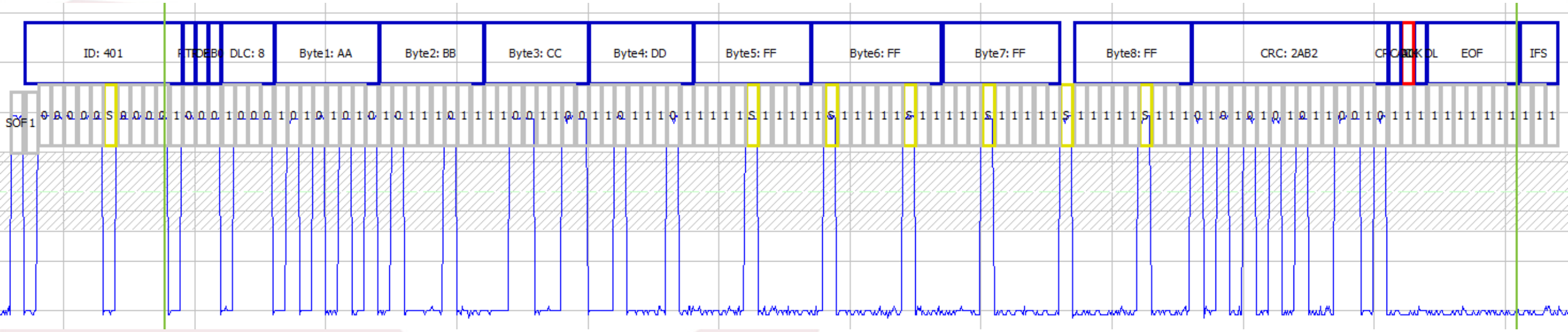
CAN Bit Timing

- Consider a CAN/CAN FD bus



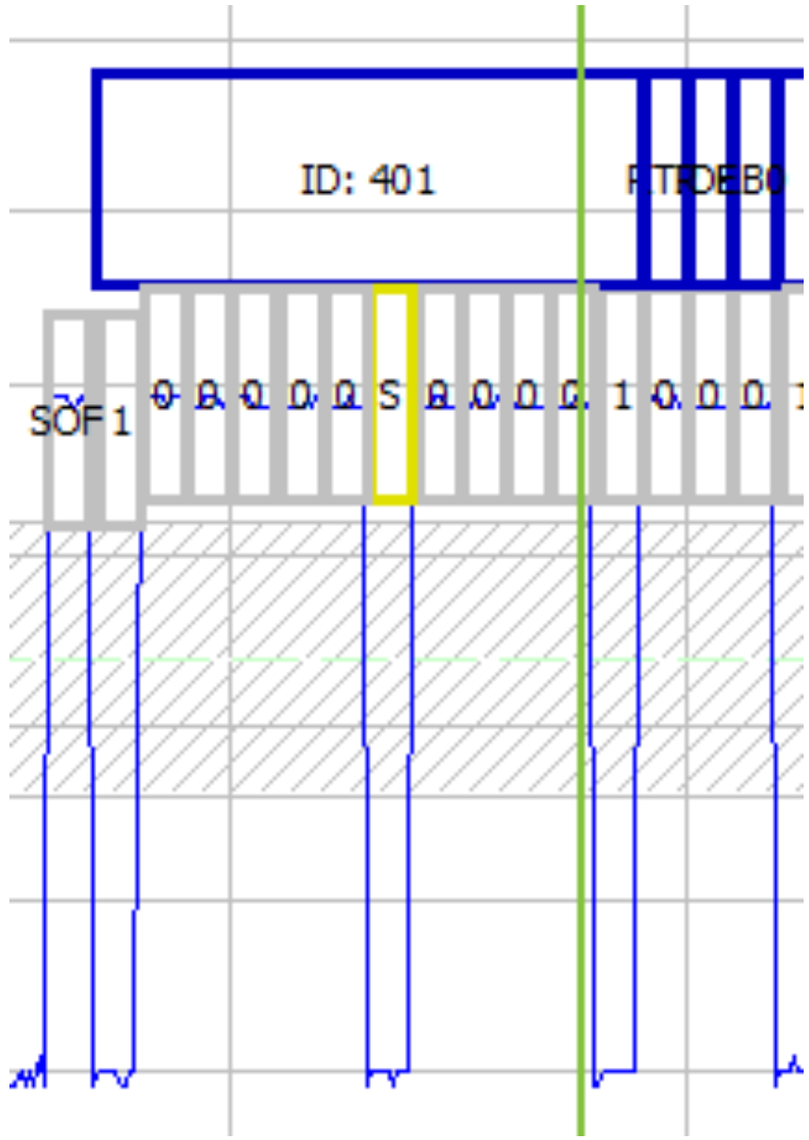


- This is what each node “sees":



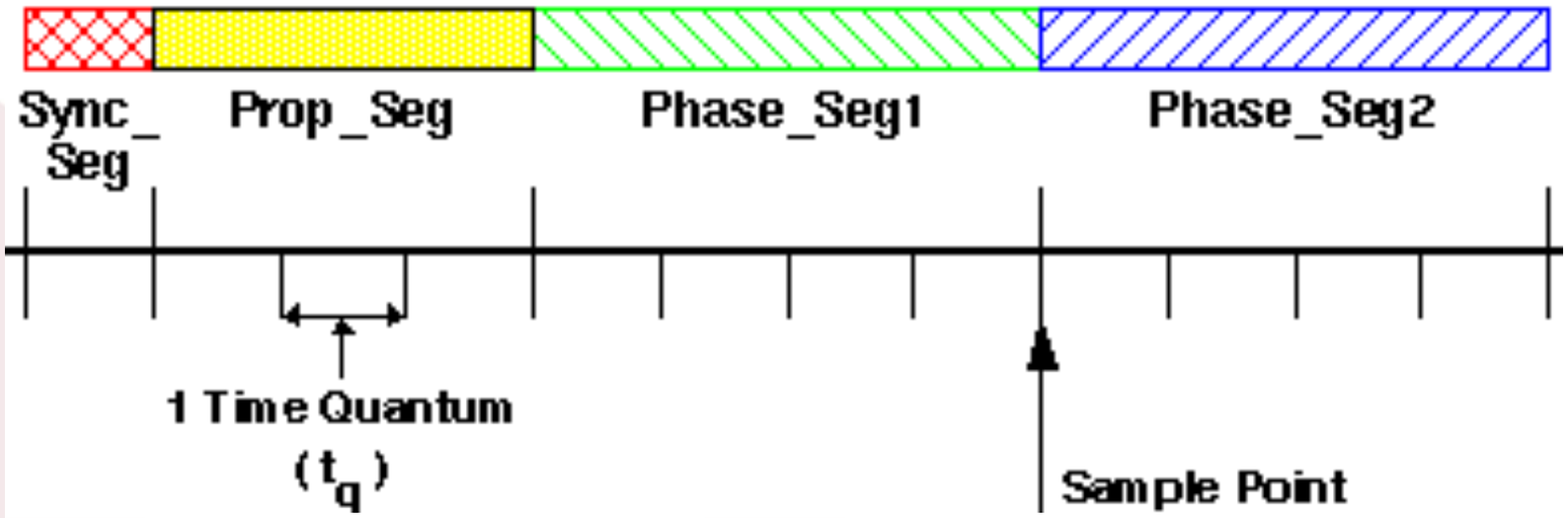
CAN Bit Timing

- When the node can read or write a bit?
- How does it know the right moment to do so?
- In the case of consecutive dominant or recessive bits, how does it know when one bit ends and the other starts?
- How the node configures itself to operate in the bus bit rate?



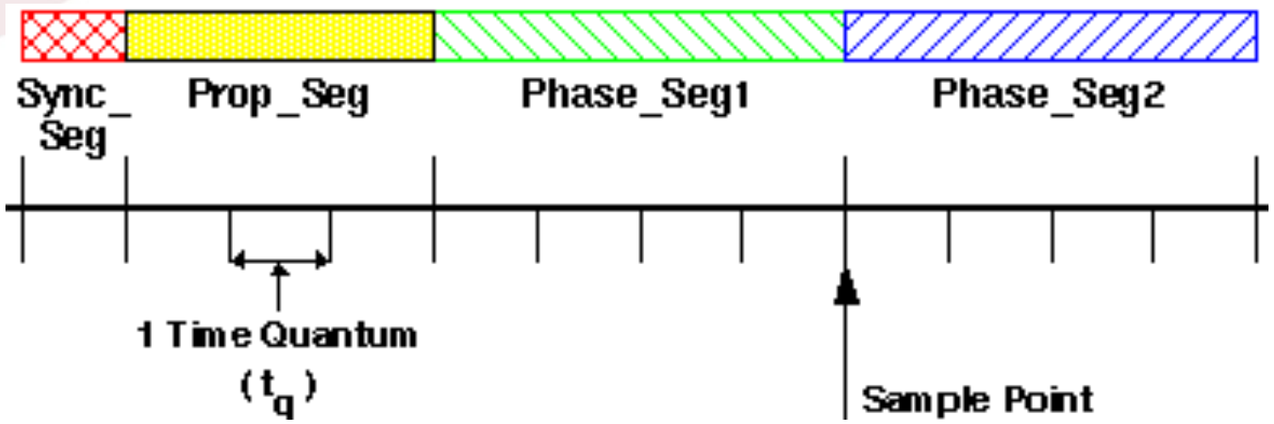
CAN Bit Timing

- A bit in a CAN/CAN network can be divided into four time segments
- Each of these segments is composed by a multiple of a fixed unit of time derived from the local oscillator called time quantum
- The time quantum “size" is fixed
- However, the segments may have different amounts of time quanta
- This configuration and the size of the time quantum is what defines the network bit rate



CAN Bit Timing

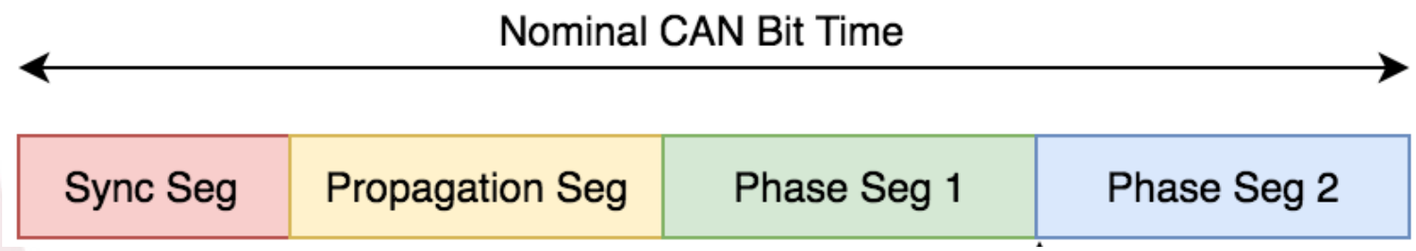
- Sample configuration



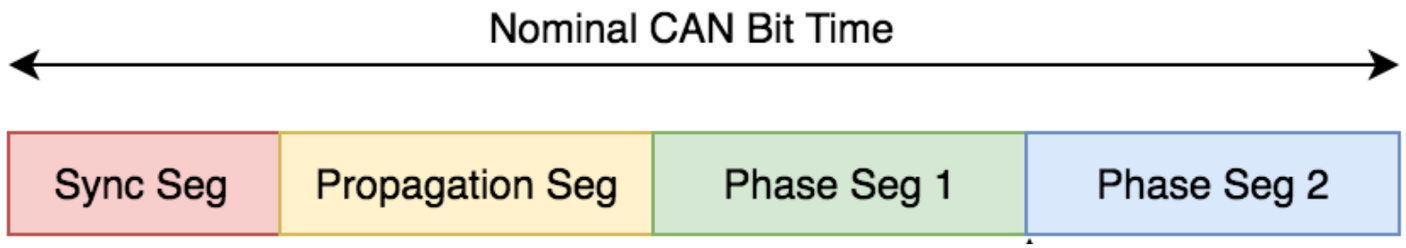
Bit Rate, kbps	Nominal bit time	TQ per bit	Sample point	TQ length	ck_tq, MHz
1000	1 µs	8	6 TQ	125 ns	8
800	1.25 µs	10	7 TQ	125 ns	8
500	2 µs	16	13 TQ	125 ns	8
250	4 µs	16	13 TQ	250 ns	4
125	8 µs	16	13 TQ	500 ns	2
62.5	16 µs	16	13 TQ	1 µs	1
50	20 µs	16	13 TQ	1.25 µs	0.8
20	50 µs	16	13 TQ	3.125 µs	0.32
10	100 µs	16	13 TQ	6.25 µs	0.16

CAN Bit Timing

- Bit rates are achieved through bit timing configurations
- A CAN network operates with a single bit rate that can reach up to 1Mbps
- Thus, it has a single bit timing configuration called: Nominal CAN Bit Time
- A CAN FD network, however, may switch between two bit rates and reach up to 10Mbps.
- Thus, it has two bit timing configurations called: Nominal Bit Time, for the arbitration phase, and Data Bit Time, for the data phase.

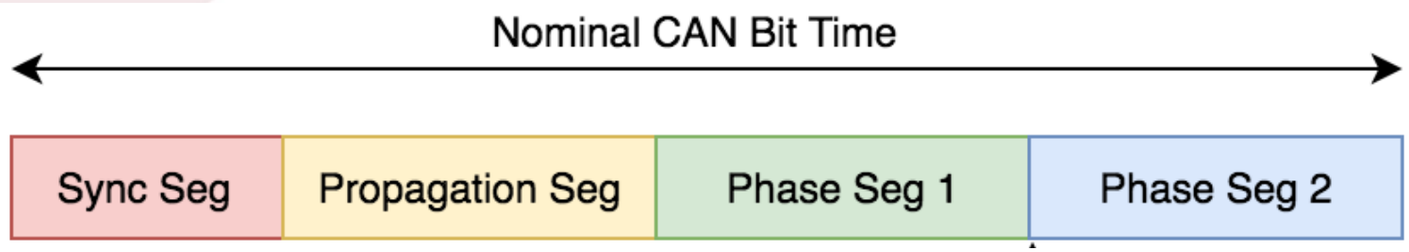


CAN Bit Timing



- Synchronization segment (Sync Seg)
  - Formed by a single time quantum
  - It is the portion of the bit time in which the various nodes in the bus must synchronize
  - The leading edge of a bit is expected to be positioned within this segment

CAN Bit Timing



- Propagation Segment (Prop Seg)
  - Used to compensate for physical delay times within the network
    - It is twice the sum of the signal propagation time on the bus line, the input comparator delay and the output driver delay
- Phase Segment 1 and 2 (Phase Seg 1/2)
  - Used to compensate for edge phase errors by being lengthened or shortened during resynchronizations

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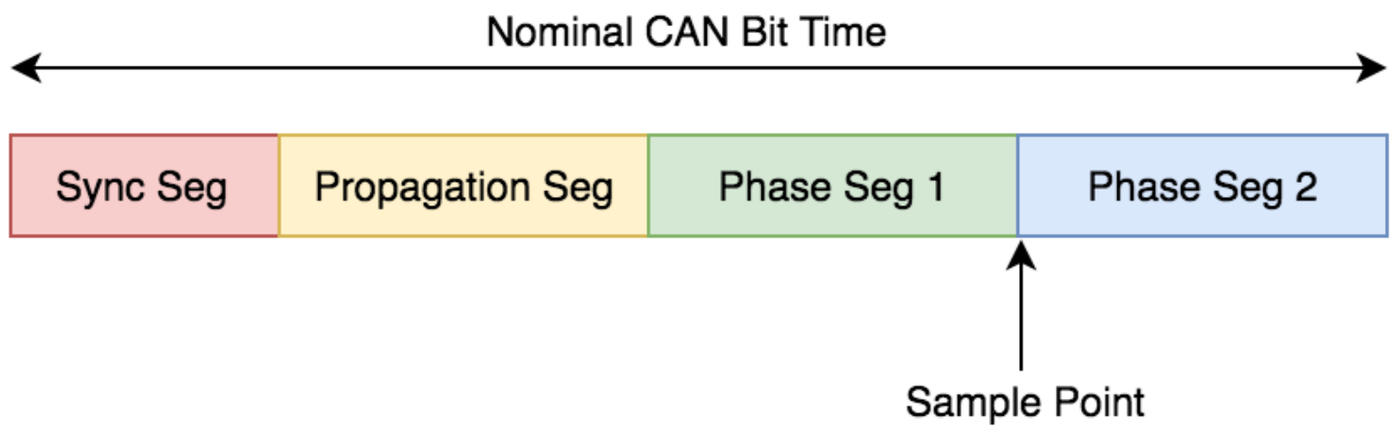
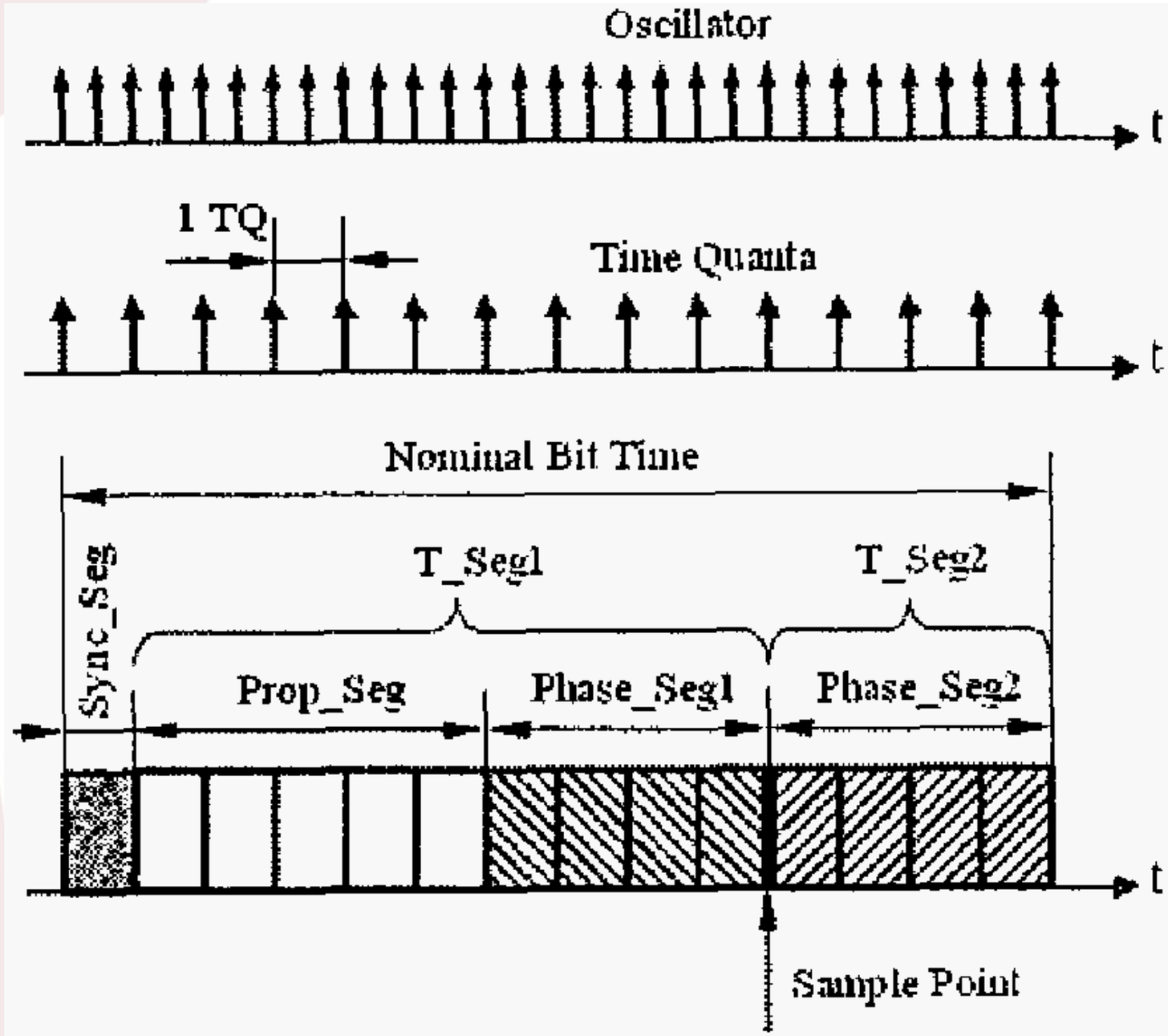
- Between the phase segments 1 and 2 there is the Sample Point
- The moment in which the bus level should be read and interpreted as the value of that respective bit
- A write operation, however, should occur in the beginning of the bit, that is in the beginning of the Sync Seg



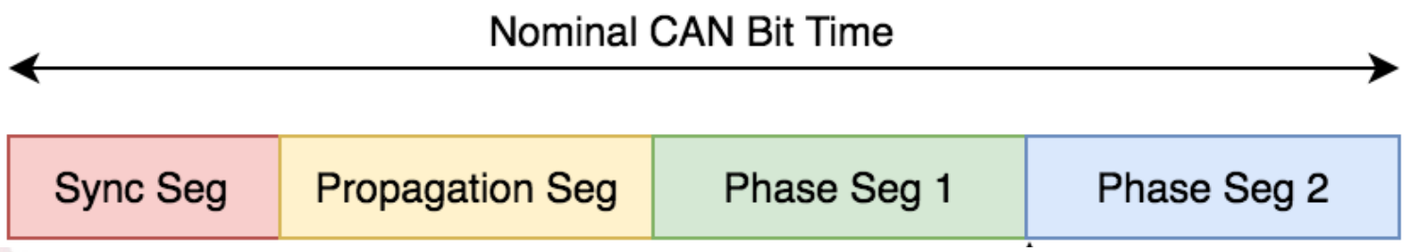
CAN Bit Timing

- Sum up



CAN Bit Timing

- To correctly read the bus level, the distance between sample points and edges must be controlled
- This is done through synchronizations that occur on falling edges, in transitions from recessive bits (logical 1) to dominant bits (logical 0)
- The edges are supposed to occur within the Sync Seg
- If they lie in any other segment, there is a phase error that must be compensated for by a synchronization

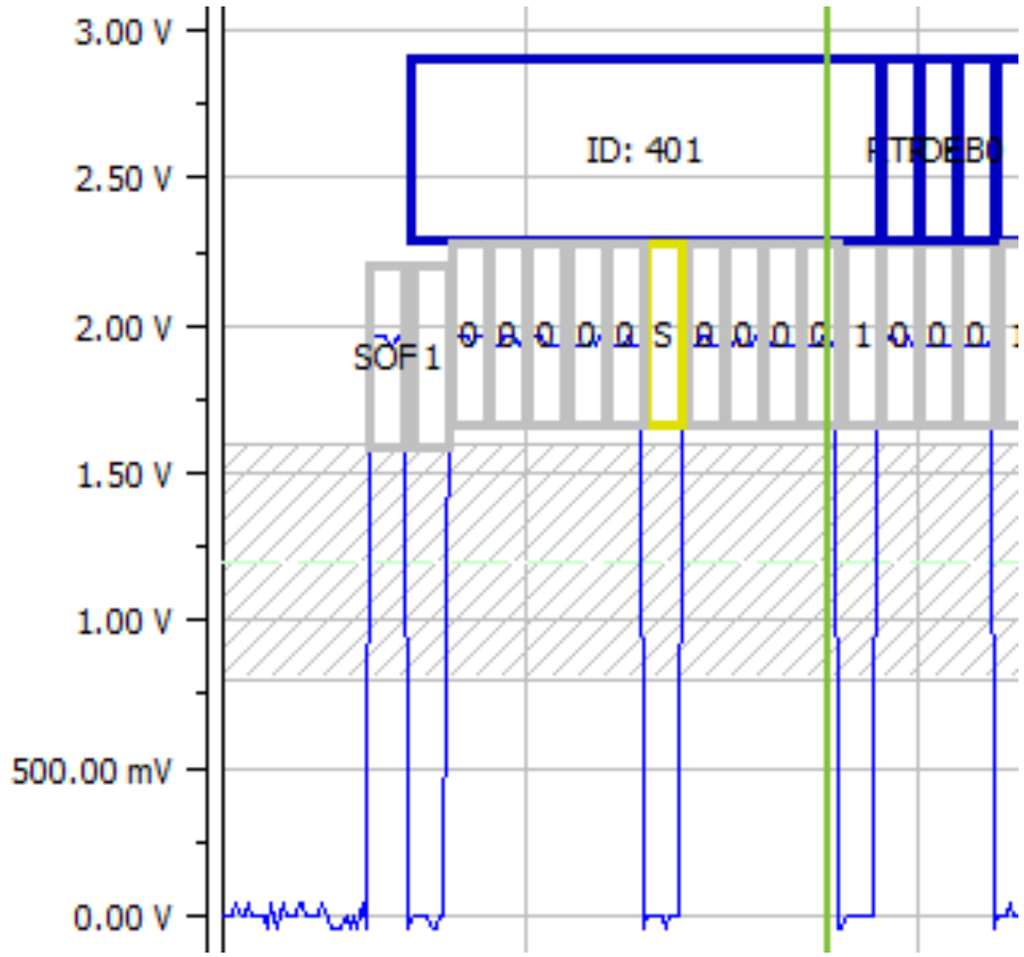


CAN Bit Timing

- There are two types of synchronizations: Hard Synchronization and Resynchronization

- Hard Synchronizations occur in the beginning of the frame, in the falling edge caused by the transition from bus idle to the start of frame bit

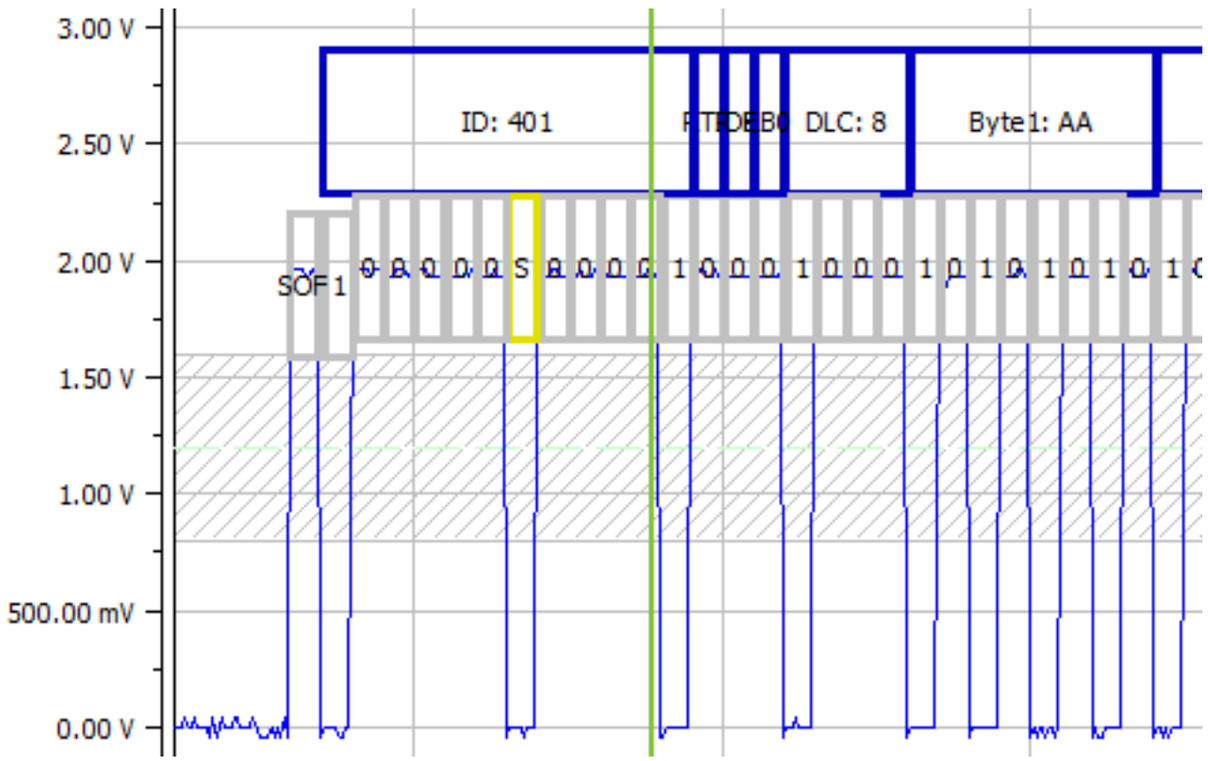
- The Hard Sync restarts the Bit Time with the end of the Sync Seg regardless of the phase error



CAN Bit Timing

- Resynchronizations occur at every other recessive to dominant edge within a frame

- It leads to a compression or an expansion of the bit time such that the position of the sample point is altered with regard to the edge



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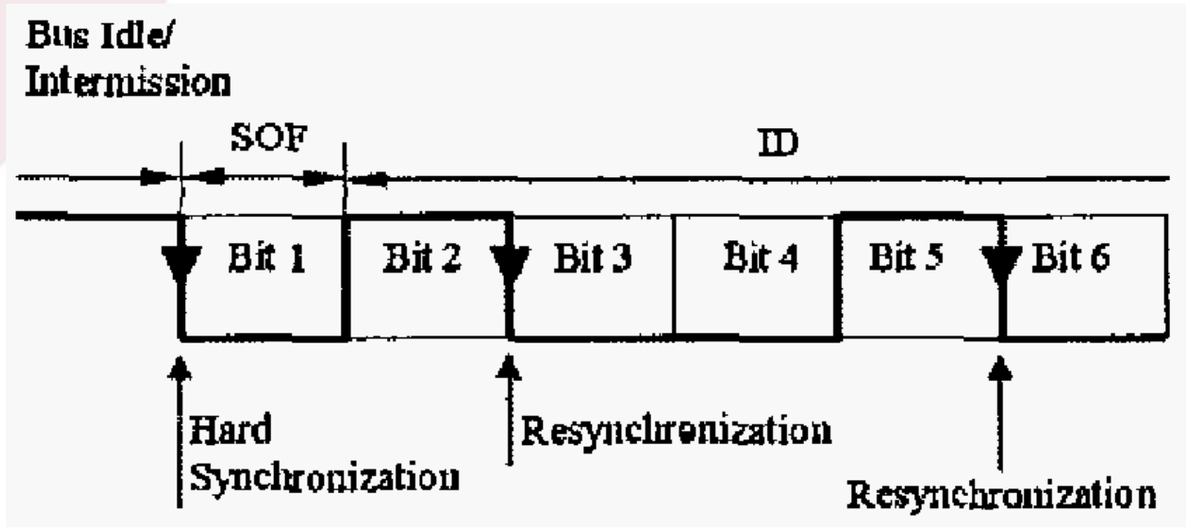
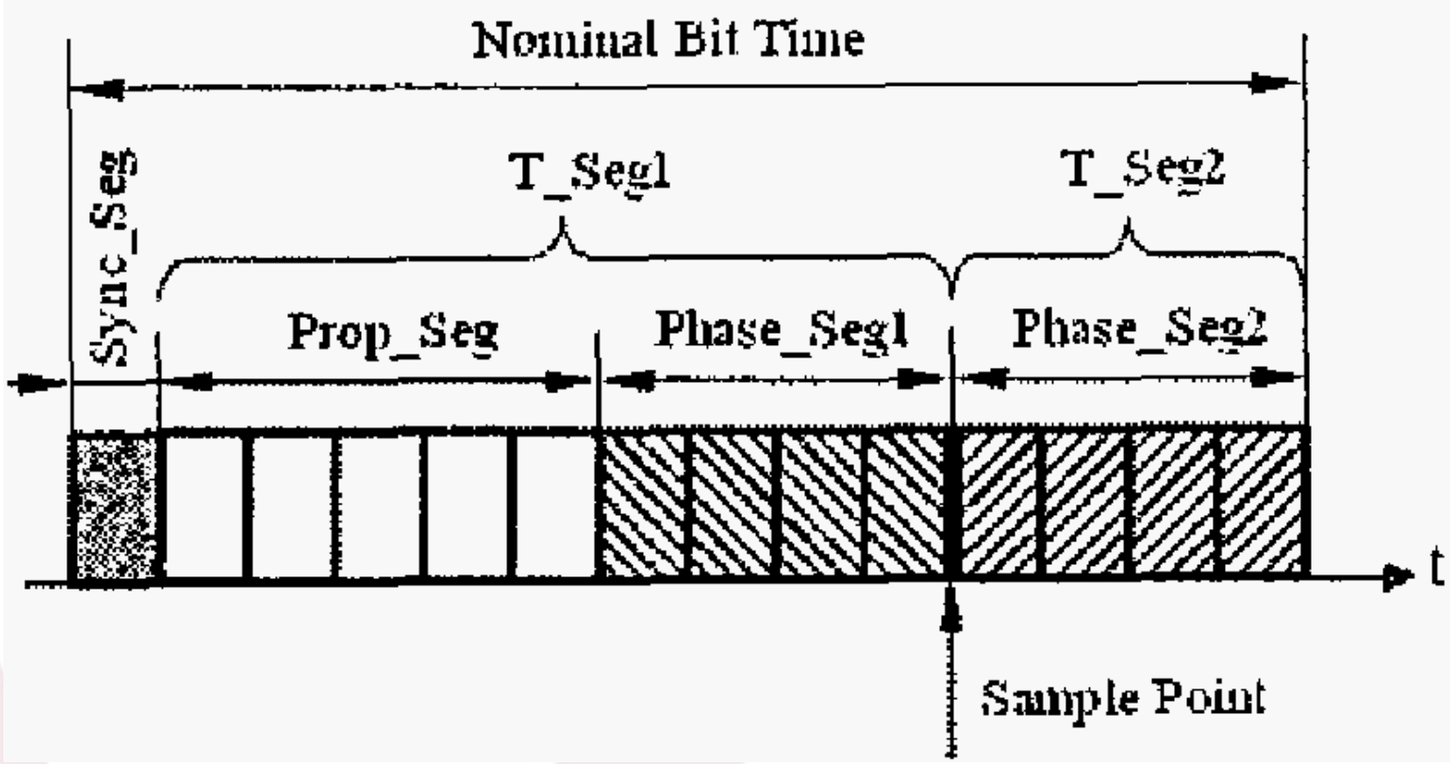




CAN Bit Timing

- If the falling edge lies before the sample point, the phase error is said to be positive and Phase Seg 1 is lengthened to compensate for the phase error by an amount up to a parameter called synchronization jump width (SJW)

- If the edge lies after the sample point, the phase error is said to be negative and Phase Seg 2 is shortened to compensate for the phase error by an amount up to SJW

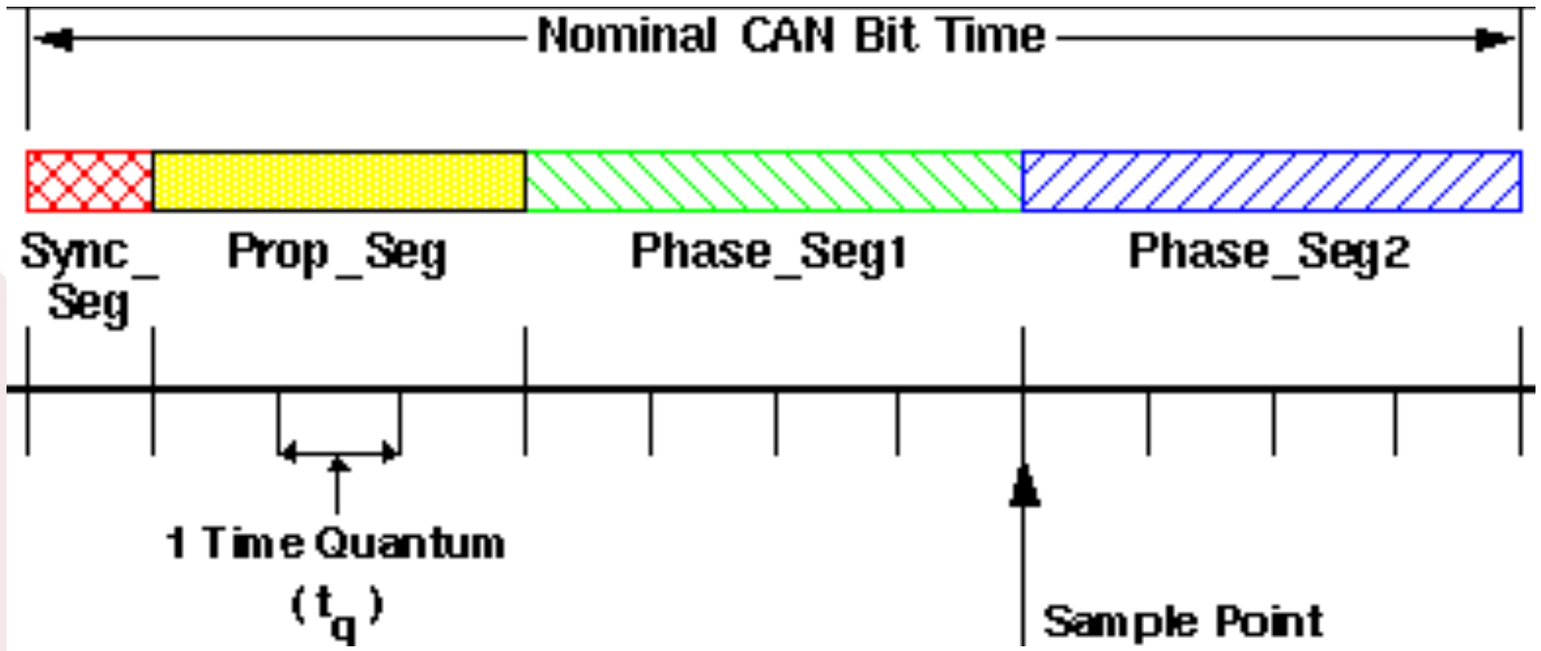
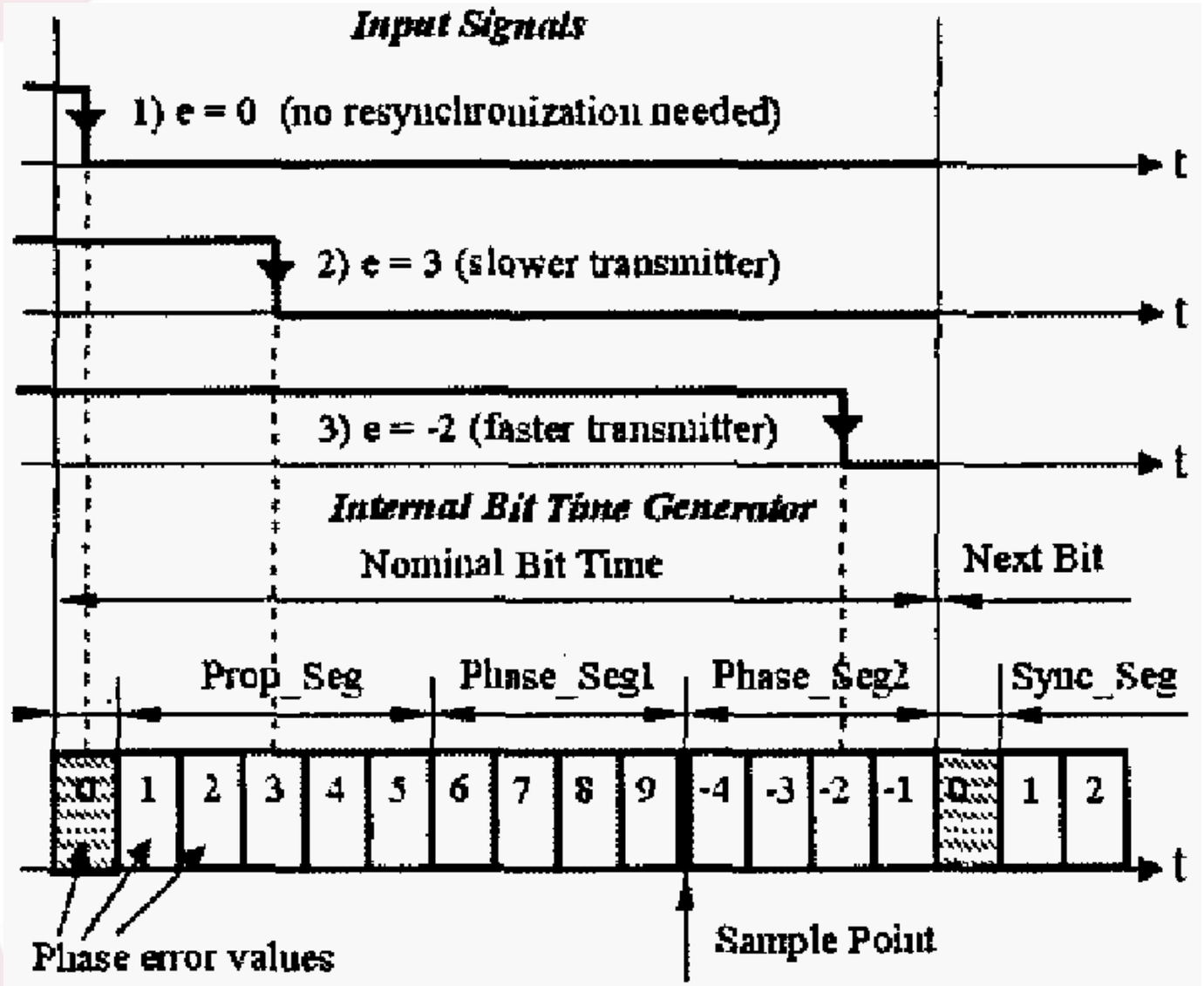


Figure 1 : Bit Timing

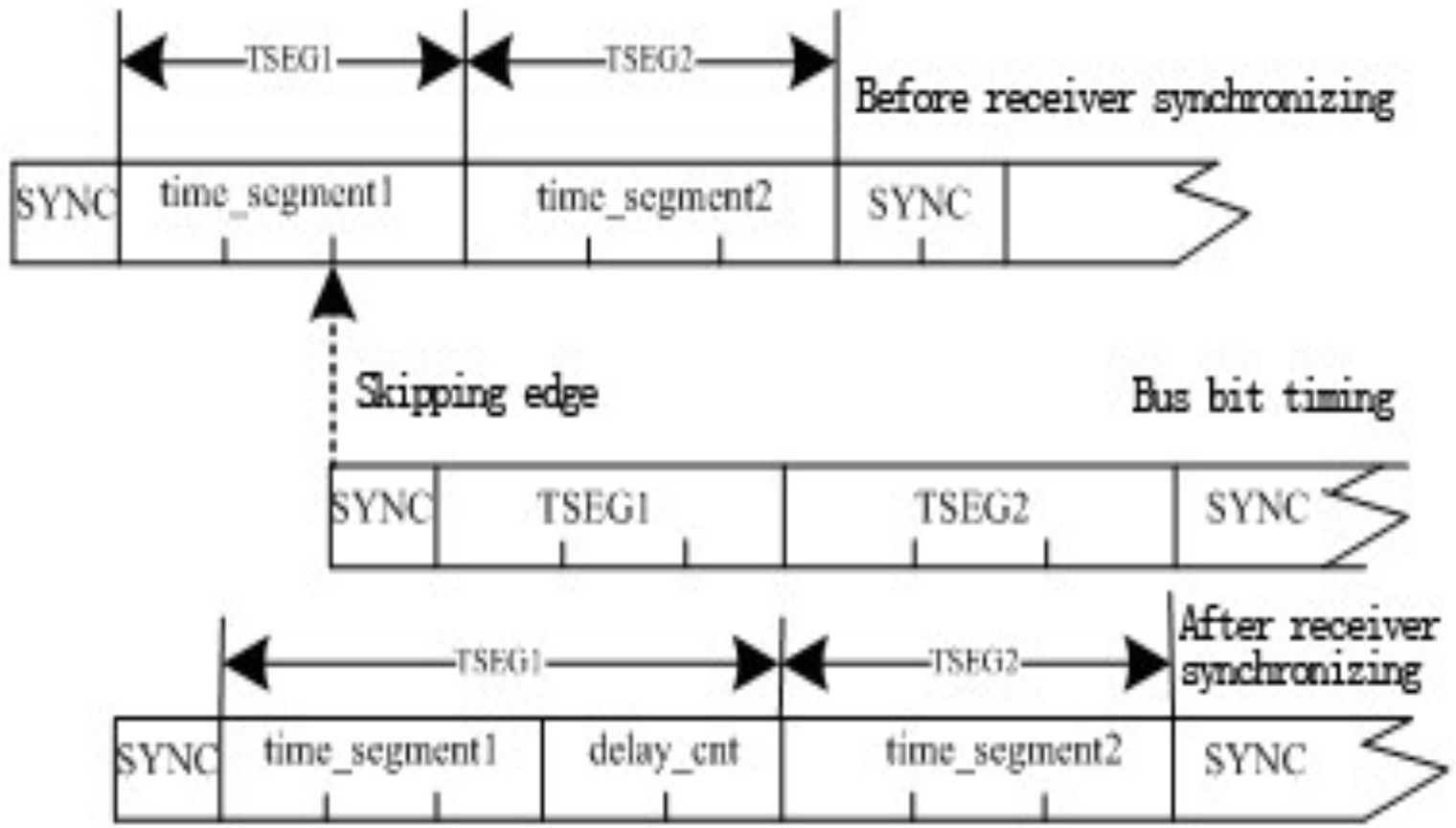
CAN Bit Timing

- Phase Error of Received Edges



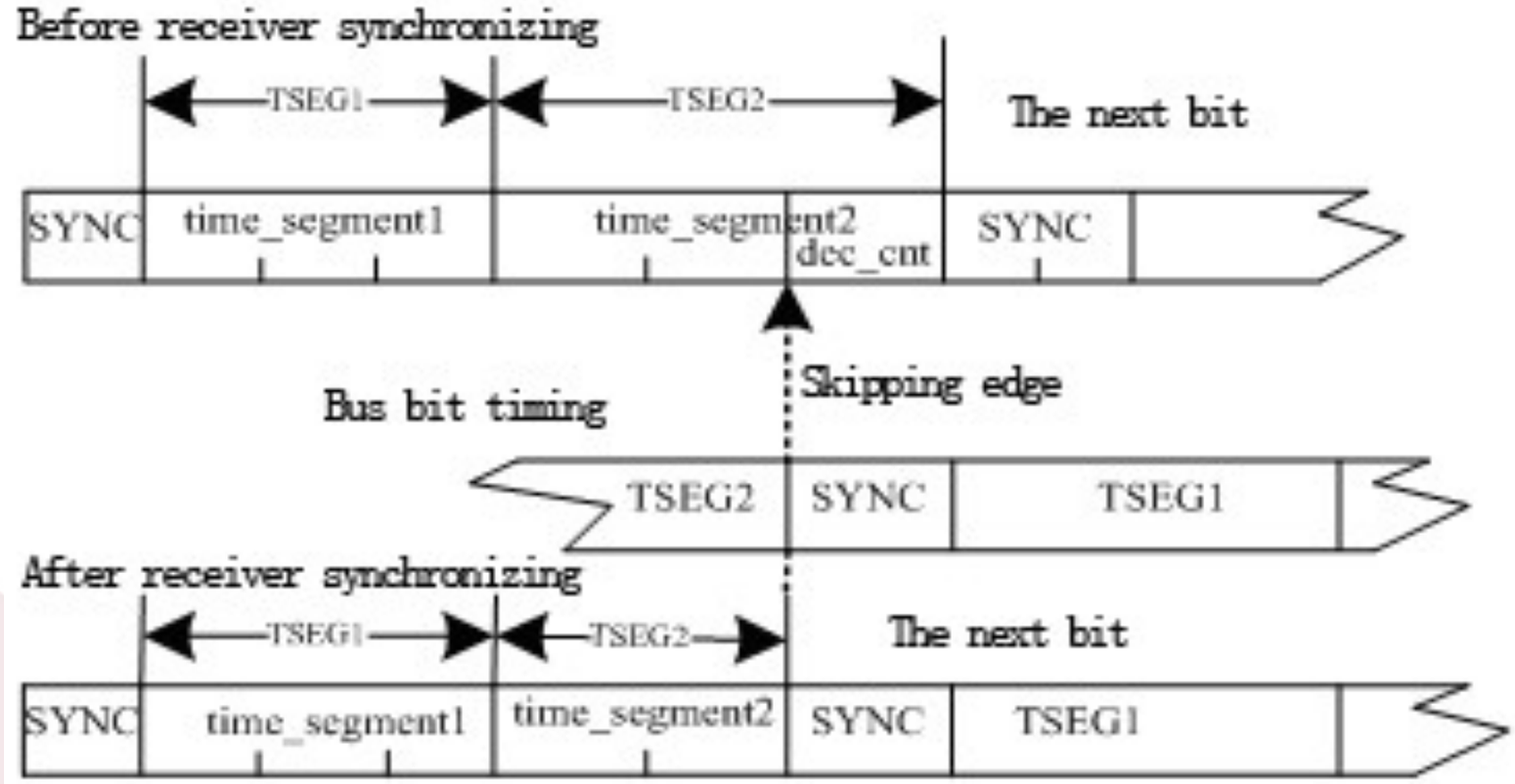
CAN Bit Timing

- A State Machine handles the synchronizations



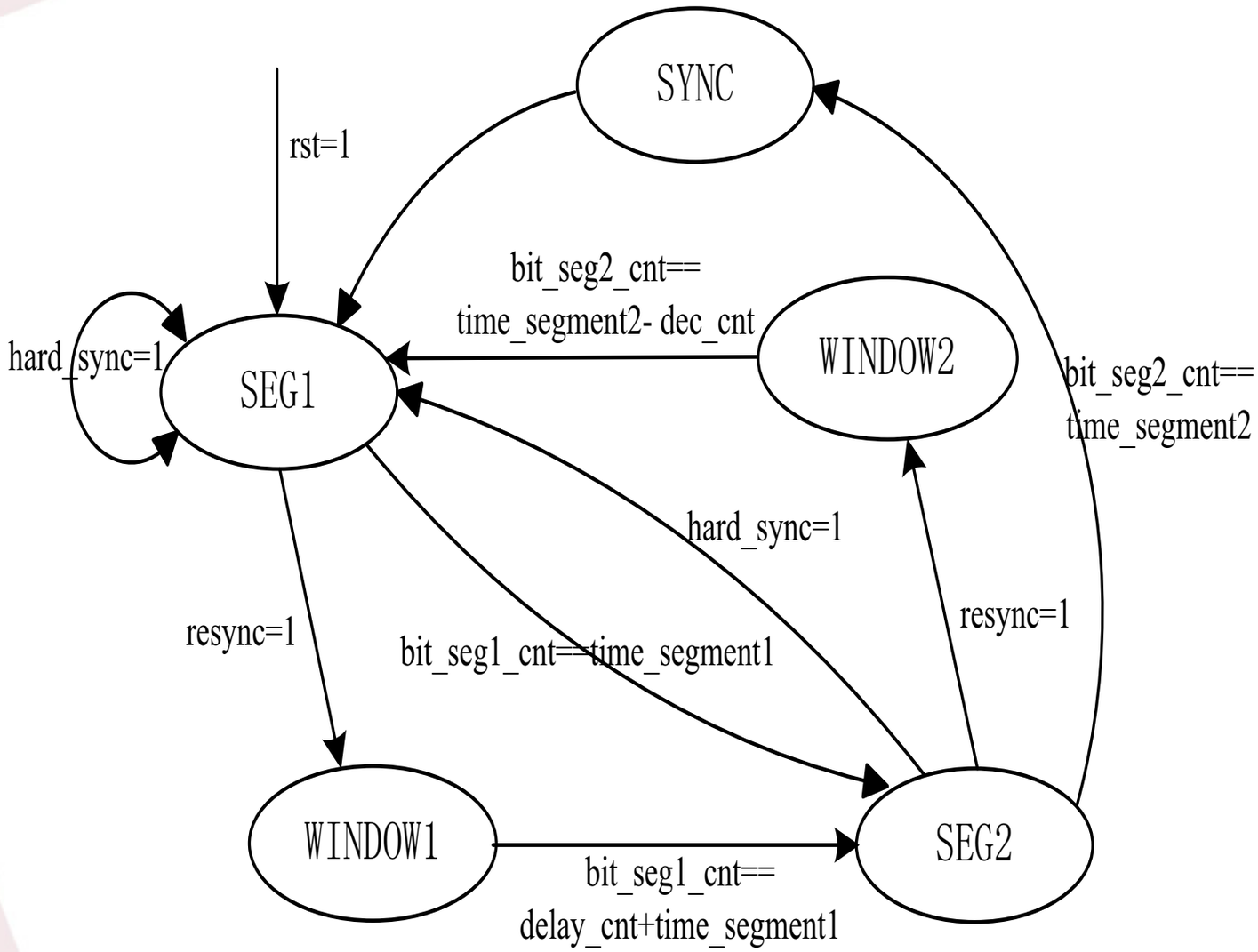
CAN Bit Timing

- A State Machine handles the synchronizations



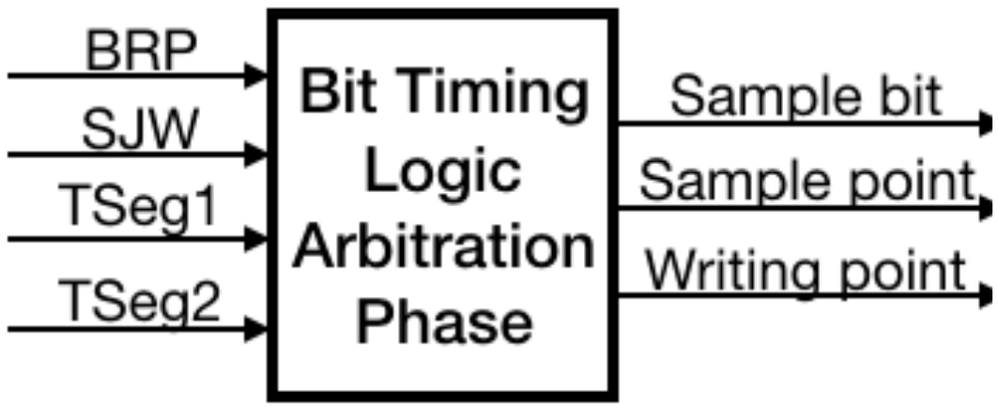
CAN Bit Timing

- A State Machine handles the synchronizations



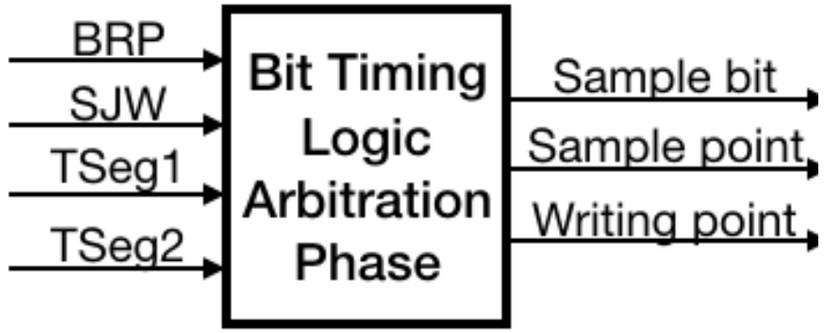
CAN Bit Timing

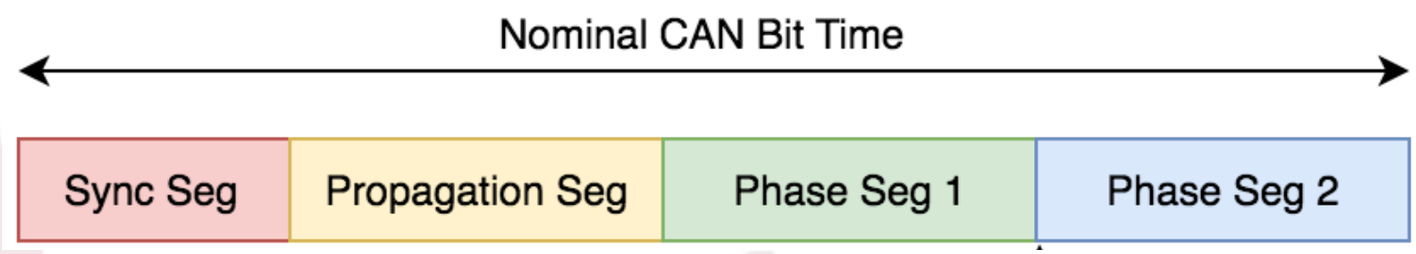
- A Module responsible for the Bit Timing may have the following inputs and outputs:
  - BRP (Baudrate Pre-scalar): To divide the input system clock
  - SJW (Synchronization Jump Width): The maximum allowed compensation for a edge that does not lie within the Sync Seg, defines the maximum change in the Phase Seg sizes
  - TSeg1 and TSeg2: Define the amount of time quanta in the (Prop Seg + Phase Seg 1) and in the Phase Seg 2



CAN Bit Timing

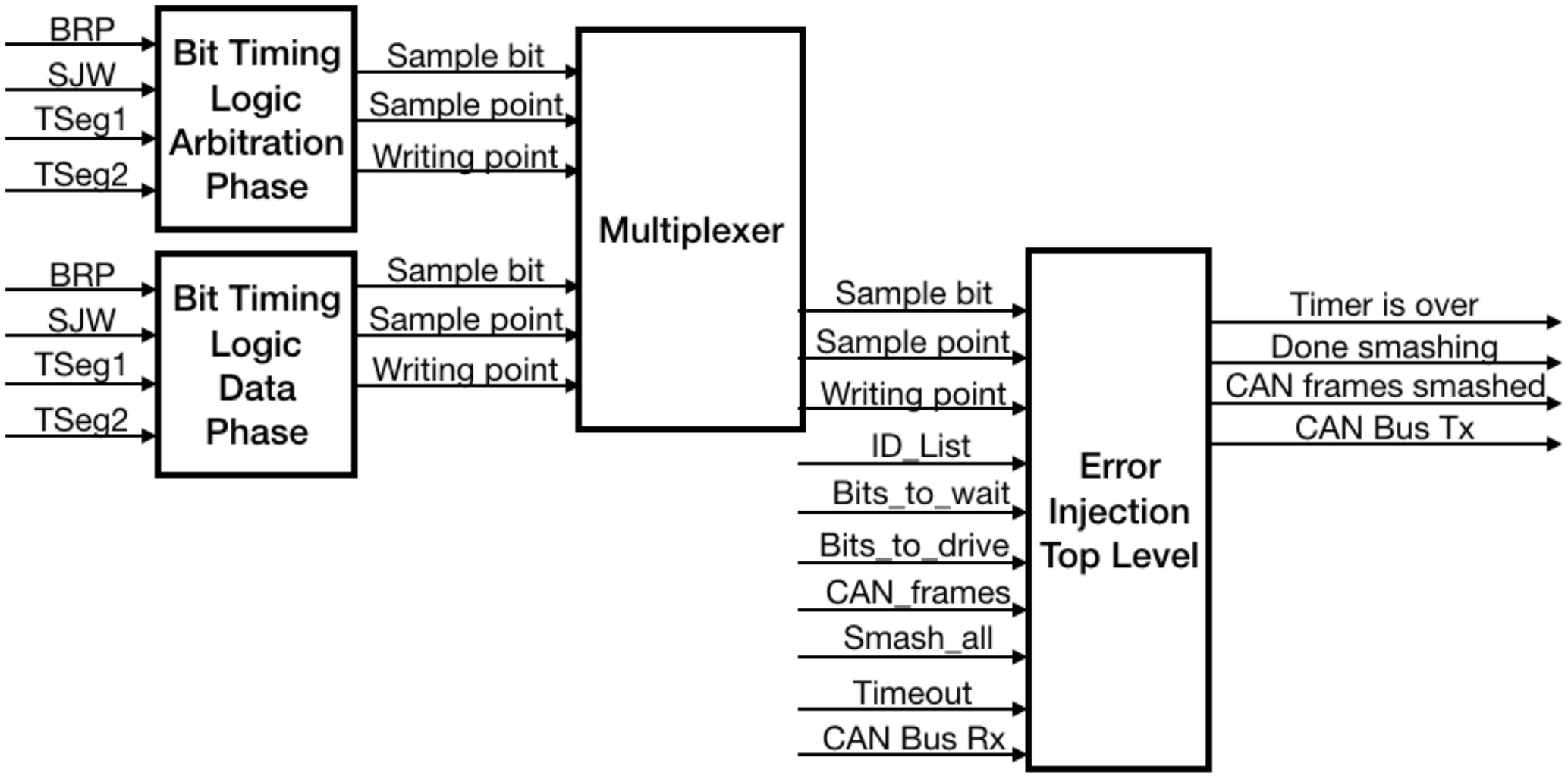
- A Module responsible for the Bit Timing may have the following inputs and outputs:
  - Sample Bit: Bit sampled in the sample point
  - Sample Point: Transition between the Phase Seg 1 and Phase Seg 2
  - Writing Point: Beginning of the frame





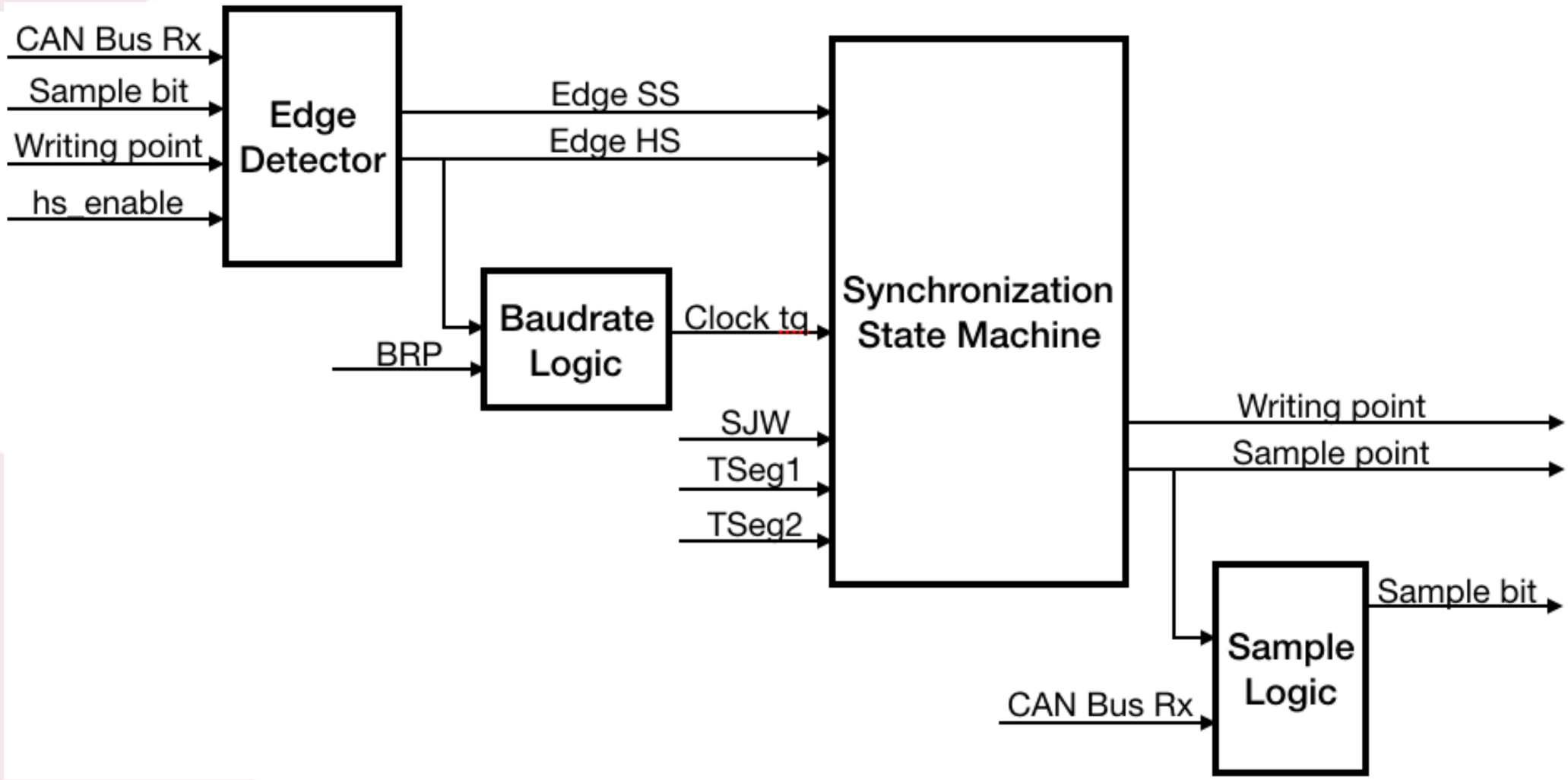
CAN Bit Timing

- Two Bit Timing Logic Modules in order to support CAN FD



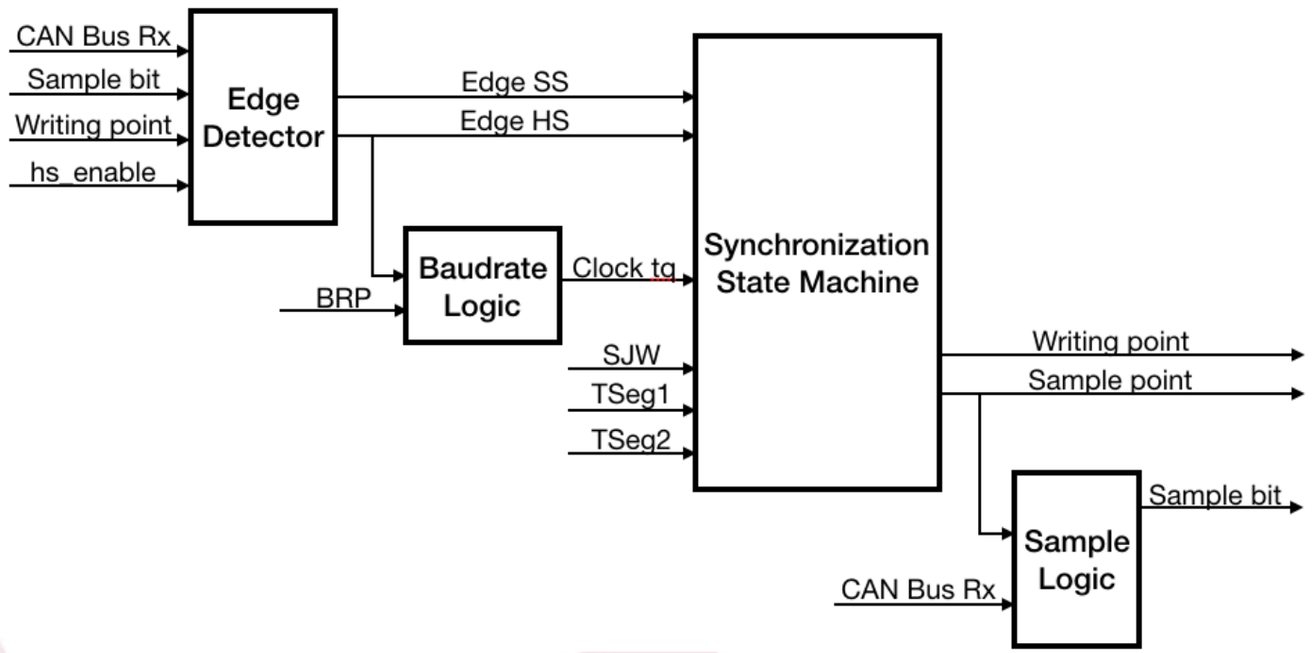
CAN Bit Timing

- Modules that compose each Bit Timing Logic Module



CAN Bit Timing

- Edge Detector: we need to detect the edges in which the synchronizations should occur
- Baudrate Logic: just a clock divider
- Synchronization State Machine: it is the core of the bit timing module, it performs the hard and soft synchronizations
- Sample Logic: samples the bus value in the sample point



Homework

- Study the support material that will be uploaded
- Do the list of exercises that will be uploaded

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Thank you!
Question?

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