Bit Timing Logic - Block Diagram

MODULES

Baud Rate Prescaler: Baud Rate Prescaler module must convert the *sys_clk* coming from the microcontroller oscillator into *clk* with period of 1 *time quanta*.

Reading Logic: Reading Logic module must implement the logic of the state machine. It tells other modules when the *writing point* and *sample point* happens ,via *wp* and *sp* respectively, and must handle the *synchronizations* itself.

Writing Logic: Writing Logic must send the bit coming from controller to the bus exactly at the *writing point*. It works as a valve that opens when the *writing point* happens.