BIT TIMING LOGIC - STATE MACHINE

This document explain the variables,flags and states of our synchronous state machine ,refreshed every *time quanta*, designed to implement the bit timing logic of CAN protocol.

VARIABLES AND FLAGS

tq_cnt: tq_cnt is a global variable for the state machine. It counts the number of *time quanta* since the beginning of the bit.

tq_cnt_seg1: tq_cnt_seg1 is a variable that can be accessed from SEG1 and PESTATE1 states. It counts the number of *time quanta* since the beginning of the SEG1.

tq_cnt_seg2: tq_cnt_seg2 is a variable that can be accessed from SEG2 and PESTATE2 states. It counts the number of *time quanta* since the beginning of the SEG1.

SJW: Synchronization Jump Width represents the maximum allowed amount of *time quanta* which the *sample point* position can be moved. In this project SJW is set to 1.

hard_sync: hard_sync is a flag that represents a *Hard Synchronization* defined by CAN protocol must happen.

resync: resync is a flag that represents a *resynchronization* (or *soft synchronization*) defined by CAN protocol must happen.

STATES

SYNC: SYNC state represents the *synchronization segment* of CAN bit timing. At the beginning of this state the CAN Controller must reset tq_cnt to 0 and indicate the *writing point*. *Synchronization Segment* must lasts 1 *time quanta*.

SEG1: SEG1 state represents 2 segments of CAN bit timing that were merged to ease the implementation, the *propagation segment* and *phase buffer segment 1*. At the beginning of this state the CAN Controller must reset tq_cnt_seg1 to 0 and set tq_cnt to 1 (because this state can be reached after a *hard synchronization*). In this project the *propagation segment* and *phase buffer segment 1* must last 1 *time quanta* and 7 *time quanta*, if no synchronization happens.

SEG2: SEG2 state represents the *phase buffer segment 2*. At the beginning of this state the CAN Controller must reset tq_cnt_seg2 to 0 and indicate the *sample point*. In this project the *phasse buffer segment 2* must lasts 7 *time quanta*, if no synchronization happens.

PESTATE1: *Phase Error State 1* state is reached if a *resynchronization* is required in SEG1 (positive phase error). PESTATE1 always extends the SEG1 by 1 *time quanta* (SJW = 1).

PESTATE2: *Phase Error State 2* state is reached if a *resynchronization* is required in SEG2 (negative phase error). PESTATE2 always shorten the SEG2 by 1 *time quanta* (SJW = 1).