ATARI Pokey reconstructed schematics

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Version 1.3

The logic of these schematics was reverse engineered from the actual chip die layout. The style and graphic representation was done following the original schematics, barely readable, as present in the chip datasheet.

The graphic is close, but not exactly identical to the original schematics. Original signal names or similar, when they were readable at all, were used in most cases.

The actual logic on the chip layout is almost identical to the original schematics, at the extent that the latter is readable. The differences don’t seem to be significant, and most of them are noted here.

In the original schematics there seems to be an optional, dotted line, to bypass the first inverter after the CS pad.

We are not sure what is the purpose of this, and this bypass is not present in the actual die. There is small text that probably describes the purpose, but it is unreadable. A possible purpose could be a different version of Pokey with an alternate CS scheme.

There are 3 extra dynamic flops, carrying the delayed output of the polys, at the last sound channel. These flops are unused, their output is not connected to anything. They are not present in the original schematics.

There is a feedback to positive power transistor present in both keyboard input pins. The initial purpose seems to be to avoid the input being floating. In the actual die layout, and contrary to the schematics the output of these transistors is disconnected. Probably a last minute change.

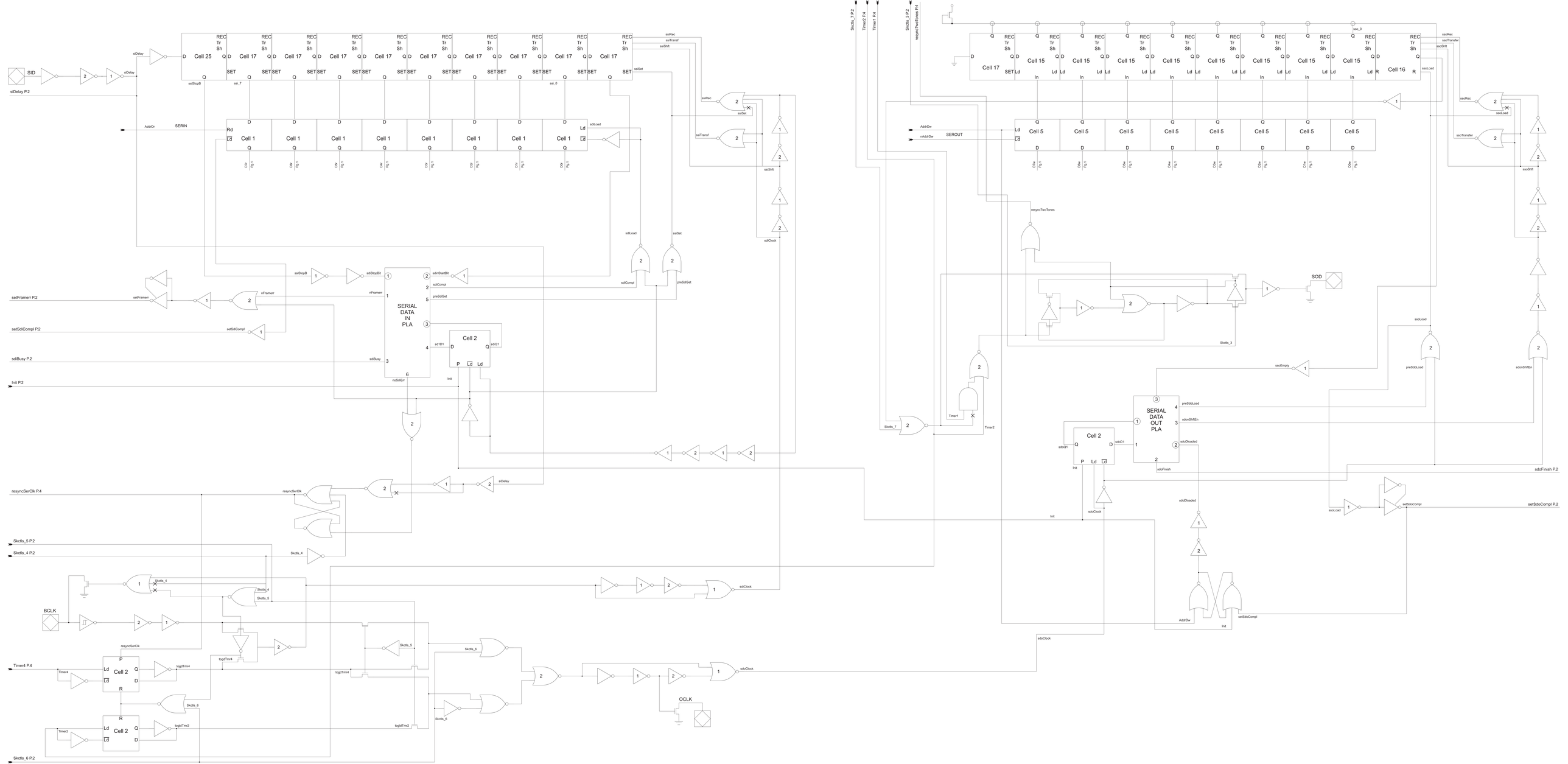
As noted in the original schematics, the die has a separate POT (analog) ground. But both ground pads are bonded to the same, and only, ground pin.

D0
Cell 7
D0r
D0r
D0w
D1
Cell 7
D1r
D1w
D2
Cell 7
D2r
D2w
D3
Cell 7
D3r
D3w
D4
Cell 7
D4r
D4w
D5
Cell 7
D5r
D5w
D6
Cell 7
D6r
D6w
D7
Cell 7
D7r
D7w
PreS01
Phi2B
PreS01
PreS01
Phi2B
csWr
RW
CS0
CS1
bA3
bA2
bA1
bA0
nA3
nA2
nA1
nA0
PreS01
PreS01
A3
A2
A1
A0
PreS01
AddrFr
AddrEr
AddrDr
AddrAr
Addr9r
Addr8r
Addr7r
Addr6r
Addr5r
Addr4r
Addr3r
Addr2r
Addr1r
Addr0r
Phi2B
Cell 22
Option 1
IN
C
Q
$\overline{Q}$
AddrFw
nAddrFw
Cell 22
IN
C
Q
$\overline{Q}$
AddrEw
nAddrEw
Cell 22
IN
C
Q
$\overline{Q}$
AddrDw
nAddrDw
Cell 22
IN
C
Q
$\overline{Q}$
AddrBw
Cell 21
IN
C
Q
AddrAw
Cell 21
IN
C
Q
Addr9w
Cell 22
Option 1
IN
C
Q
$\overline{Q}$
Addr8w
nAddr8w
Cell 22
IN
C
Q
$\overline{Q}$
Addr7w
nAddr7w
Cell 22
IN
C
Q
$\overline{Q}$
Addr6w
nAddr6w
Cell 22
IN
C
Q
$\overline{Q}$
Addr5w
nAddr5w
Cell 22
IN
C
Q
$\overline{Q}$
Addr4w
nAddr4w
Cell 22
IN
C
Q
$\overline{Q}$
Addr3w
nAddr3w
Cell 22
IN
C
Q
$\overline{Q}$
Addr2w
nAddr2w
Cell 22
IN
C
Q
$\overline{Q}$
Addr1w
nAddr1w
Cell 22
IN
C
Q
$\overline{Q}$
Addr0w
nAddr0w

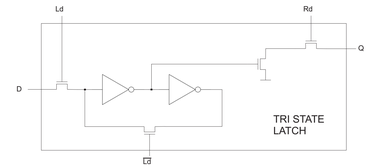

KEYBOARD CONTROL PLA
KR1
KR2
K0
K1
K2
K3
K4
K5
Cell 2
Cell 3
Cell 6
Cell 4
Cell 1
Cell 12
Cell 9
Cell 5
IRQEN
IRQST
IRQ
KBCODE
SKCTLS
SKSTAT
SKRES
WR BRK SDO
Tmr 2 SDO
2 Tone Serout
Fast Scan Select
keybClk P.3
setSdiCompl P.5
setSdoCompl P.5
Timer4 P.4
Timer2 P.4
Timer1 P.4
Skctls_7 P.5
Skctls_6 P.5
Skctls_5 P.5
Skctls_4 P.5
Skctls_3 P.5
setFramerr P.5
Skctls_2 P.3
Init P.3,4,5
sdoFinish P.5
sdiBusy P.5
siDelay P.5

Addr8r
Addr7r
Addr6r
Addr5r
Addr4r
Addr3r
Addr2r
Addr1r
Addr0r
ALLPOT
D0r P.1
D1r P.1
D2r P.1
D3r P.1
D4r P.1
D5r P.1
D6r P.1
D7r P.1
Rd
RdK
Cell 1
Cell 8
Q
D
Ld
Pot8nLd
Pot7nLd
Pot6nLd
Pot5nLd
Pot4nLd
Pot3nLd
Pot2nLd
Pot1nLd
Pot0nLd
Pot8Ld
Pot7Ld
Pot6Ld
Pot5Ld
Pot4Ld
Pot3Ld
Pot2Ld
Pot1Ld
Pot0Ld
Cell 23
CR
BOR
P
potPreset
nPotClk
Skctls_2
keybClk
Cell 26
In
P6
P7
P4
P5
P2
P3
P0
P1
AddrBw
POTGO
Init
audClock
sel15Khz
HSYNC
64 KHZ
keybClk
audClock P.4
sel15Khz P.4
Init P.2
keybClk P.2
Skctls_2 P.2


4 BIT POLY
5 BIT POLY
9/17 BIT POLY
AUDF1
AUDF2
AUDF3
AUDF4
AUDC1
AUDC2
AUDC3
AUDC4
AUDCTL
Cell 24
Option 1
Cell 24
Cell 20
Cell 5
Cell 12
Cell 11
Cell 2
Cell 9
RANDOM
Resync
Timers
STIMER
AUD


SID
sdDelay
sdDelay P.2
AddrDr
SERIN
Rd
Cell 1
Cell 25
Cell 17
Cell 2
Cell 5
Cell 15
Cell 16
REC
Tr
Sh
SET
Ld
ssiStopB
ssi_7
ssi_0
ssiRec
ssiTransf
ssiShift
ssiSet
sdLoad
sdClock
ssiStopBit
sdiStartBit
sdiCompl
preSdiSet
SERIAL
DATA
IN
PLA
nFramerr
setFramerr
setFramerr P.2
setSdiCompl
setSdiCompl P.2
sdiBusy
sdiBusy P.2
sdiD1
sdiQ1
noSdiErr
Init
Init P.2
resyncSerClk P.4
resyncSerClk
Skctls_5 P.2
Skctls_4 P.2
Skctls_4
Skctls_5
Skctls_6
BCLK
Timer4 P.4
Timer4
togdTmr4
Timer2
togdTmr2
Skctls_6 P.2
OCLK
sdoClock
Skctls_1 P.2
Timer2 P.4
Timer1 P.4
Skctls_3 P.2
resyncTwoTones P.4
resyncTwoTones
sso_0
ssoRec
ssoTransfer
ssoShift
ssoLoad
AddrOw
nAddrOw
SEROUT
SOD
Skctls_3
Skctls_7
Timer1
Timer2
ssoEmpty
preSdoLoad
sdonShftEn
SERIAL
DATA
OUT
PLA
sdoQ1
sdoD1
sdoDloaded
sdoFinish
sdoFinish P.2
setSdoCompl
setSdoCompl P.2
sdoClock
Init
AddrOw

1



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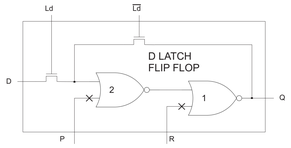

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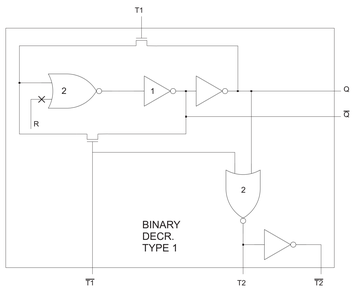

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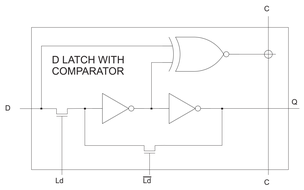

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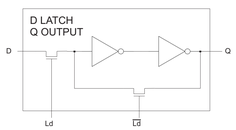

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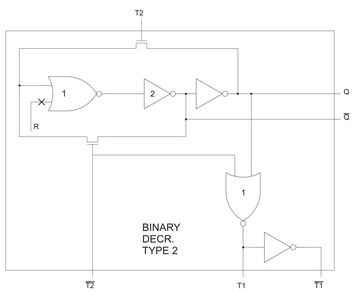

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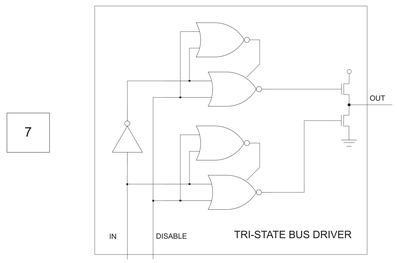

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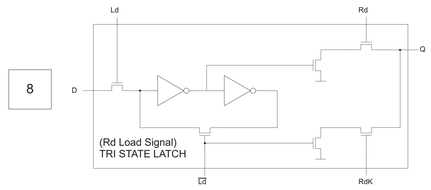

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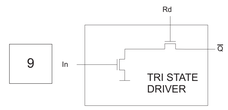

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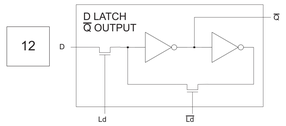

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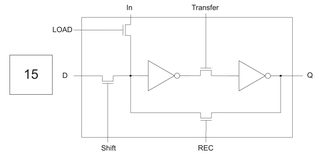

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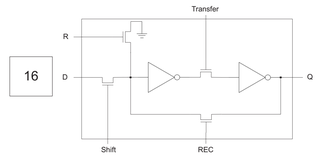

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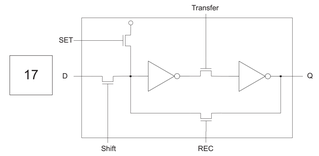

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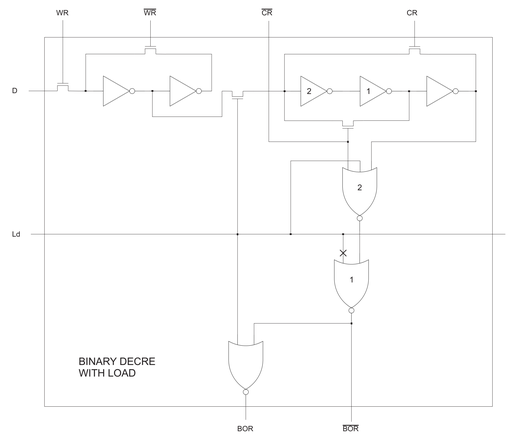

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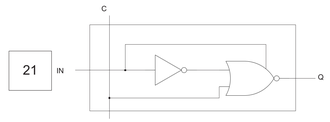

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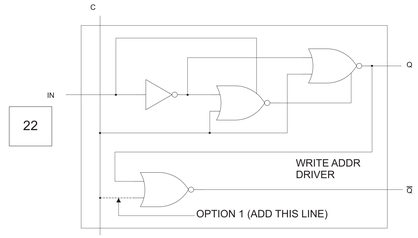

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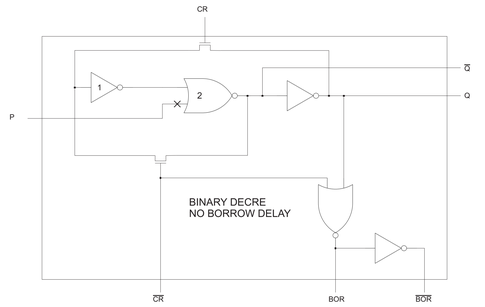

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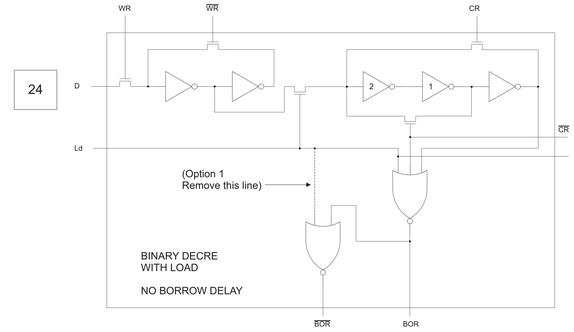

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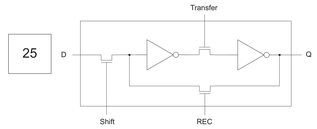

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