

# ATARI Pokey reconstructed schematics

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The logic of these schematics was reverse engineered from the actual chip die layout. The style and graphic representation was done following the original schematics, barely readable, as present in the chip datasheet.

The graphic is close, but not exactly identical to the original schematics. Original signal names or similar, when they were readable at all, were used in most cases.

The actual logic on the chip layout is almost identical to the original schematics, at the extent that the latter is readable. The differences don't seem to be significant, and most of them are noted here.

In the original schematics there seems to be an optional, dotted line, to bypass the first inverter after the CS pad.

We are not sure what is the purpose of this, and this bypass is not present in the actual die. There is small text that probably describes the purpose, but it is unreadable. A possible purpose could be a different version of Pokey with an alternate CS scheme.

There are 3 extra dynamic flops, carrying the delayed output of the polys, at the last sound channel. These flops are unused, their output is not connected to anything. They are not present in the original schematics.

There is a feedback to positive power transistor present in both keyboard input pins. The initial purpose seems to be to avoid the input being floating. In the actual die layout, and contrary to the schematics the output of these transistors is disconnected. Probably a last minute change.

As noted in the original schematics, the die has a separate POT (analog) ground. But both ground pads are bonded to the same, and only, ground pin.















