ELEN 605 Final Project

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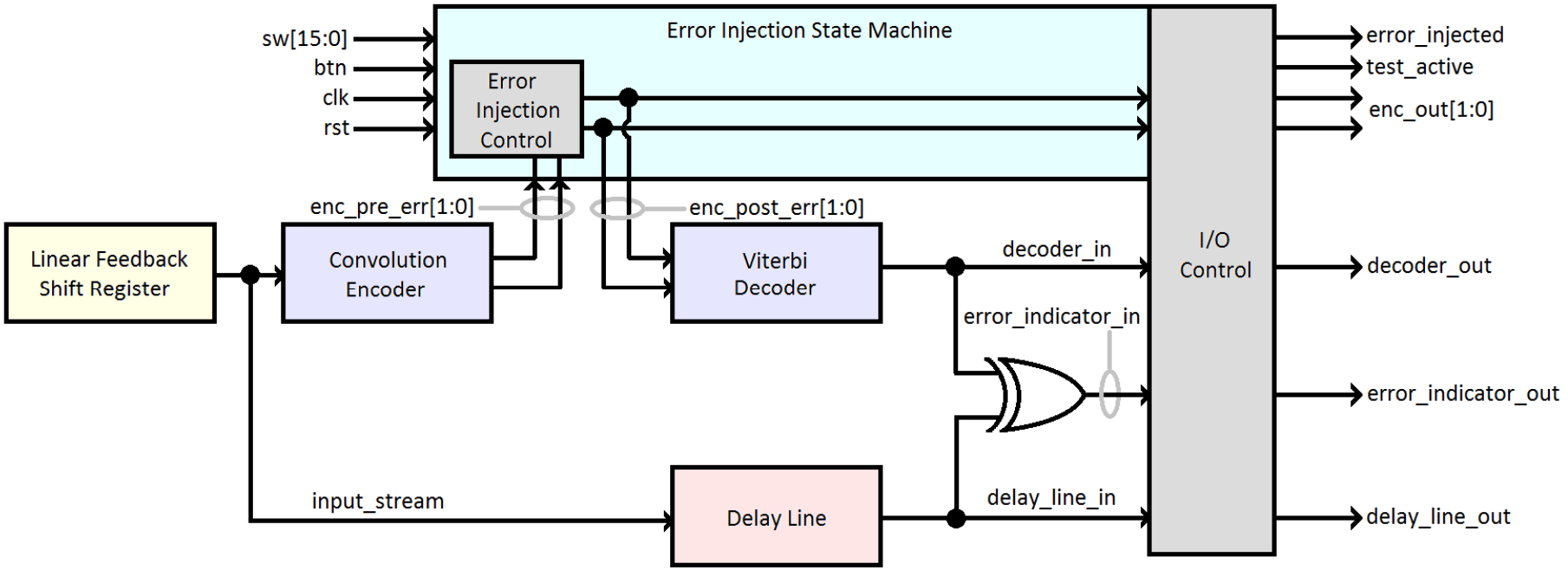
Objective

- Devise a state machine to perform error injection into a Viterbi decoder that can be used in FPGA fabric
- Understand the various steps required to implement a design on a Basys 3 FPGA development board
- Implement the HLS version of the Viterbi decoder along with its corresponding state machine in an FPGA for real-time experimentation
- Observe the error correction capabilities of the Viterbi decoder in actual hardware

Solution

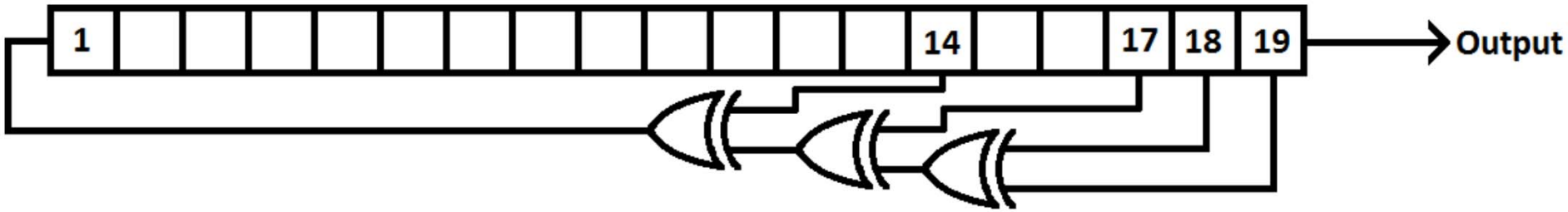
- Create the state machine which is basically a hardware testbech that can run the decoder and inject various types of errors
- Variable amounts of error injection, or no error injection at all, should also be a functionality of the state machine
- Error injection should be configurable for one encoded bit stream or both encoded bit streams
- Error injection should be of the burst error type and be configurable for stuck at 0, stuck at 1 or inverted bits
- Internal signals as well as output signals should be visible to the outside world for observation

System Layout



Linear Feedback Shift Register (LFSR)

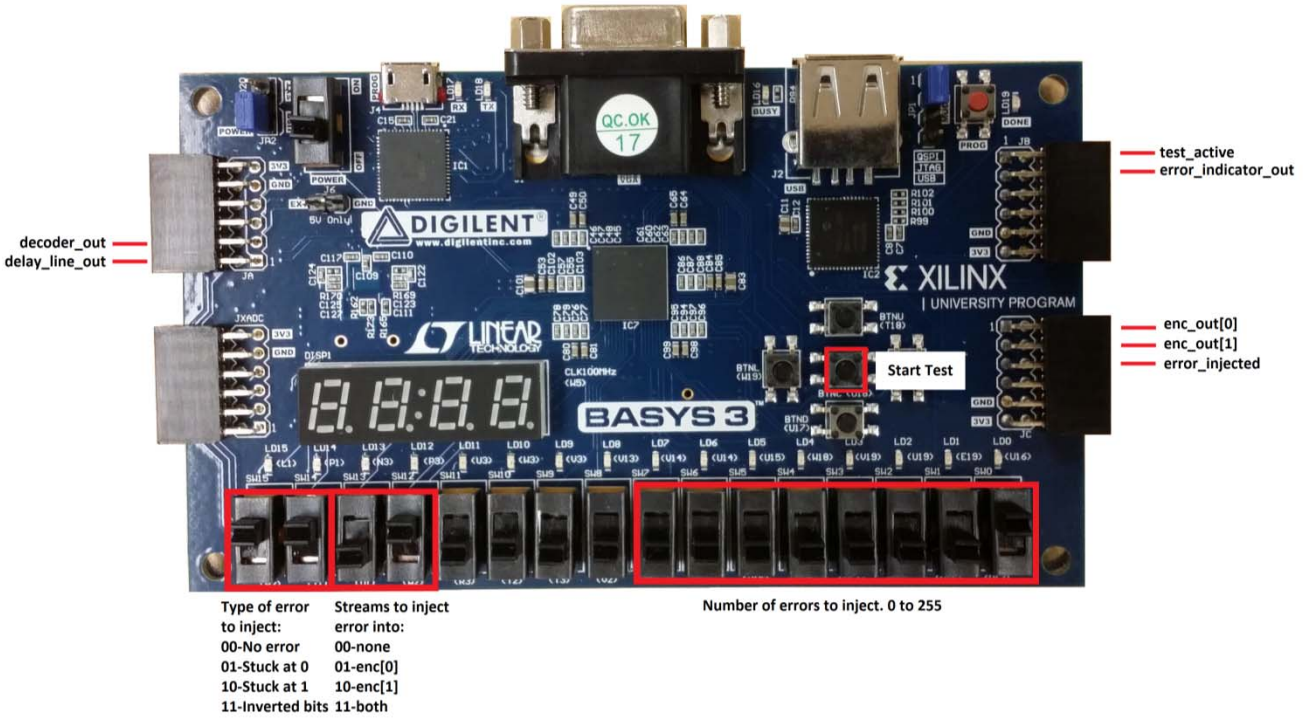
- Random input data is needed to stimulate the system
- A 19^{th} order maximal LFSR was chosen for this purpose
- The polynomial equation for the LFSR is: $x^{19} + x^{18} + x^{17} + x^{14} + 1$



Delay Line

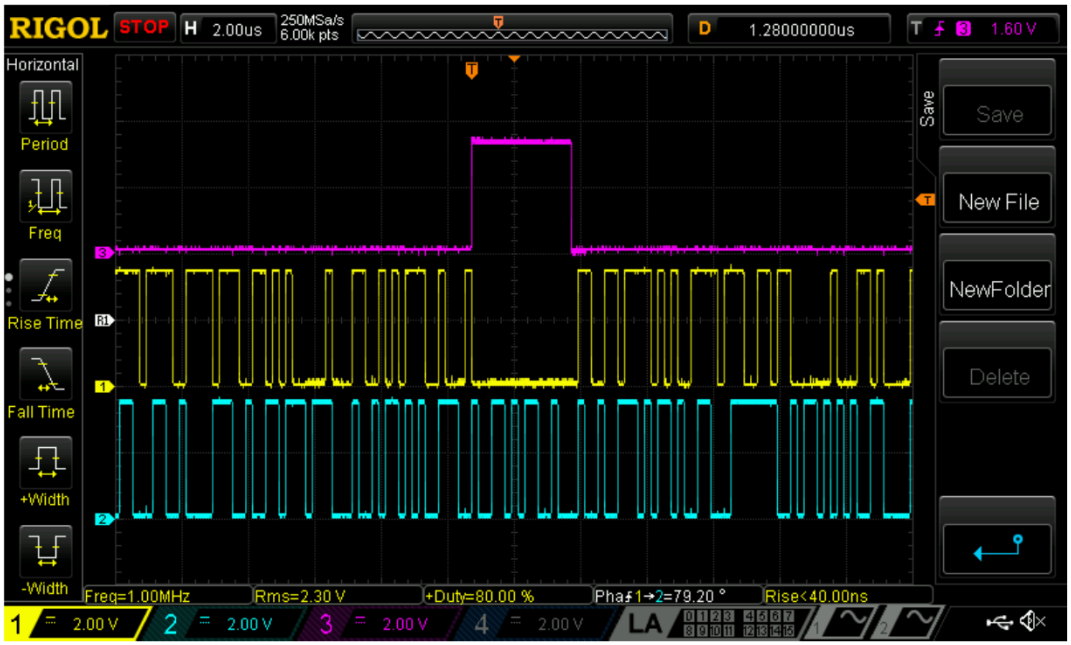
- A delay line was used in Project 3 to align the input stream with the decoder output in the testbench
- A delay line is used for the same purpose in this project but it is an actual piece of implemented hardware
- The output of the delay line is XORed with the output of the decoder to allow easy identification of errors while running the decoder in hardware. It also gives a trigger point for an oscilloscope during waveform capture

Basys 3 Board Level Signals and Controls



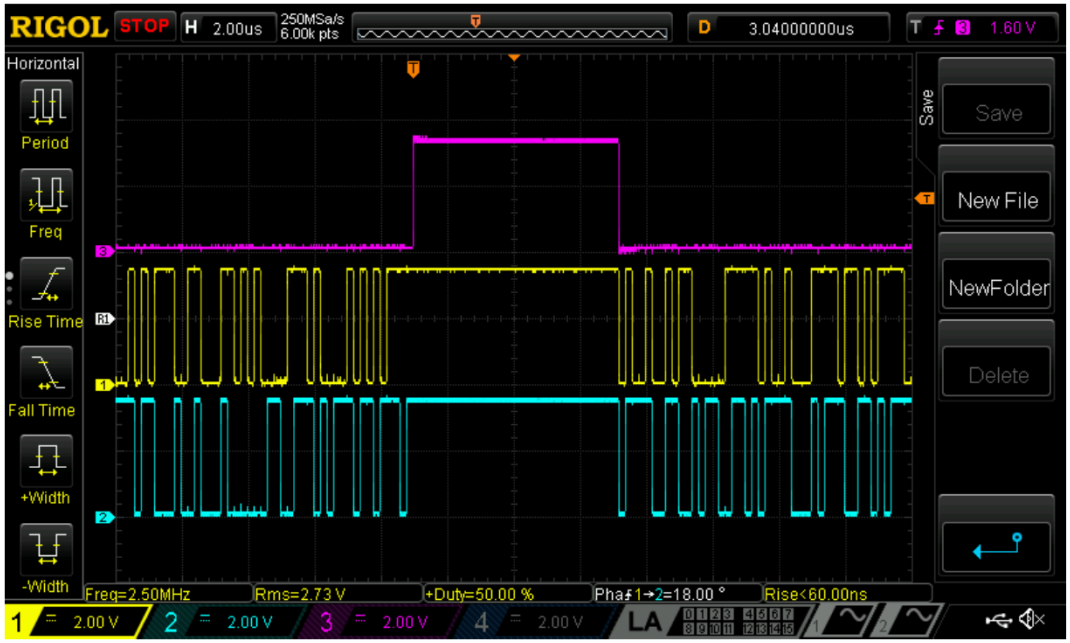
Results

- Ecoded bitstream 0 (yellow) and encoded bitstream 1 (light blue)
- Error injected indicator (purple)
- 15 error bits injected. Error type: stuck at 0 on bitstream 0



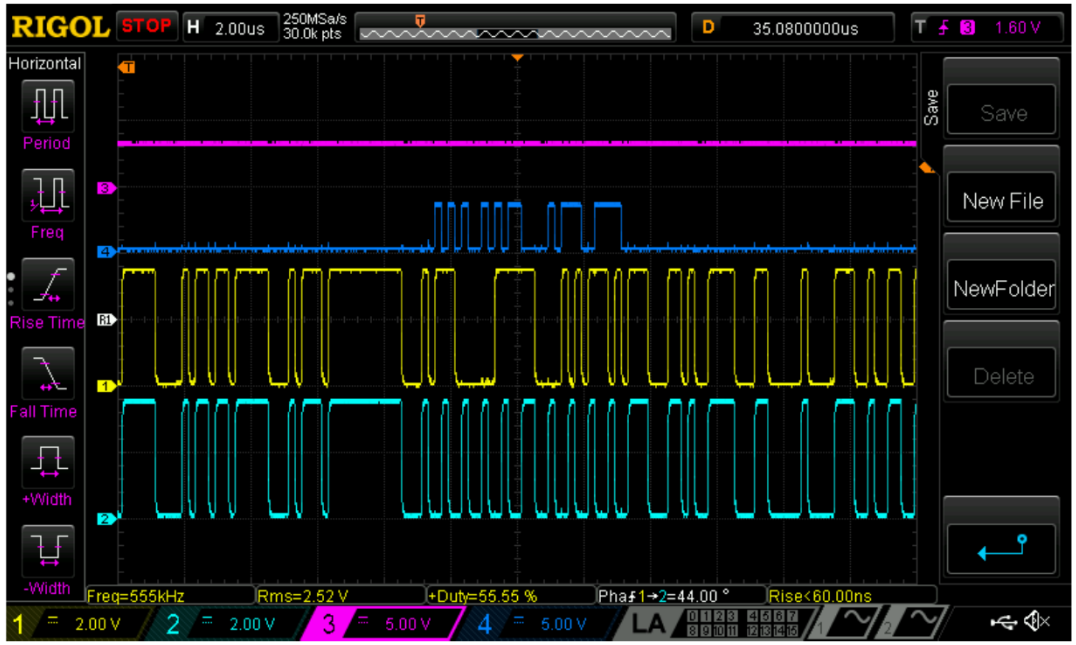
Results

- Ecoded bitstream 0 (yellow) and encoded bitstream 1 (light blue)
- Error injected indicator (purple)
- 31 error bits injected. Error type: stuck at 1 on both bitstreams



Results

- Delayed input (yellow) and decoder output (light blue)
- Test running indicator (purple), output error indicator (bark blue)
- 31 error bits injected. Error type: stuck at 1 on both bitstreams



Results

- Delayed input (yellow) and decoder output (light blue)
- Test running indicator (purple), output error indicator (bark blue)
- 2 error bits injected. Error type: stuck at 1 on bitstream 0 (no output error)

Analysis and Conclusion

- The system performed as expected under various error conditions
- When the error was limited to 2 bit on a single stream of encoded data, the decoder was able to recover the data with no errors
- When the burst error rate was increased to a larger number of bits, the output of the decoder contained errors
- The HLS Viterbi decoder was rapidly produced and shown to perform within specification under all given conditions
- The objectives stated from the start of the presentation were all successfully met