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CS 203: Advanced Computer Architecture
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Lab 3 Answers

1. Assuming a 512KB 4-way set associative cache with 16B block size, how many bits does the tag have? What is the total size, in bytes, of the cache including tag bits?

   The tag has 16 bits.

   Total size, in bytes, of the cache including tag bits (with LRU bits):

   $$512KB\ cache\ data\ //524288\ bytes$$
   $$+(32768\ cache\ blocks * 16\ tag\ bits\ per\ block)\ //65536\ bytes$$
   $$+(8192\ sets * 2\ LRU\ bits)\ //\ 2048\ bytes$$
   $$= 591872\ bytes\ \ or\ 578\ KB$$

   Total size, in bytes, of the cache including tag bits (without LRU bits):

   $$= 589824\ bytes\ \ or\ 576\ KB$$

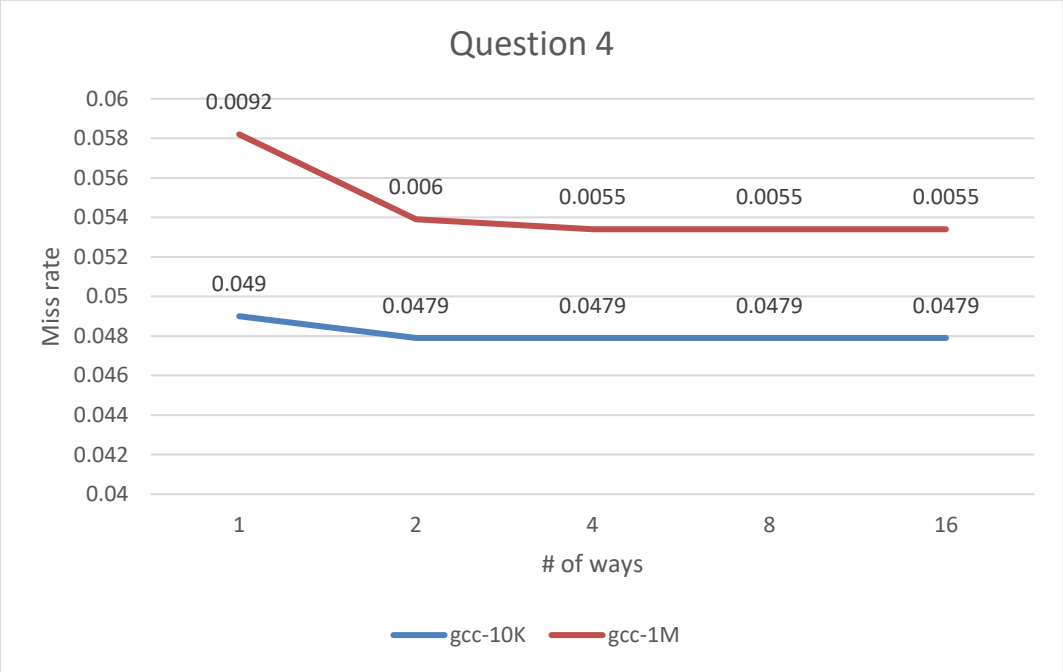
2. What is the cache miss rate of the given traces and cache configuration? Assume we have a 512KB cache and 16B block size.

Trace	Direct	2-way	4-way	Fully Assoc.
gcc-10K	0.0762	0.0756	0.0756	0.0756
gcc-1M	0.0124	0.0094	0.0092	0.0092

3. For the following configurations, how many bits are for tag, index, and offset fields? Assume we have a 256KB cache and 16B block size.

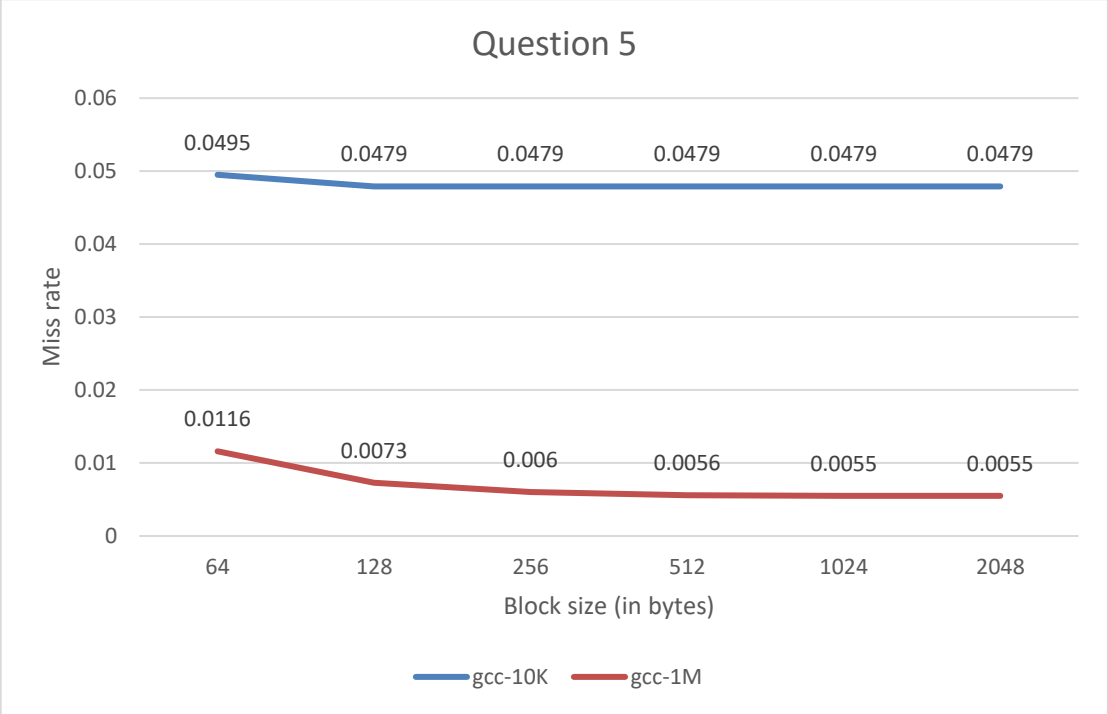
Trace	Direct	2-way	4-way	Fully Assoc.
gcc-10K	tag 14 index 14 offset 4	tag 15 index 13 offset 4	tag 16 index 12 offset 4	tag 28 index 0 offset 4
gcc-1M	tag 14 index 14 offset 4	tag 15 index 13 offset 4	tag 16 index 12 offset 4	tag 28 index 0 offset 4

4. Assuming a 256KB cache and 32B block size. How does increasing the number of ways affect cache miss rate? Plot the number of ways (1,2,4,8,16) vs miss rate for the two traces. What do you observe and why?



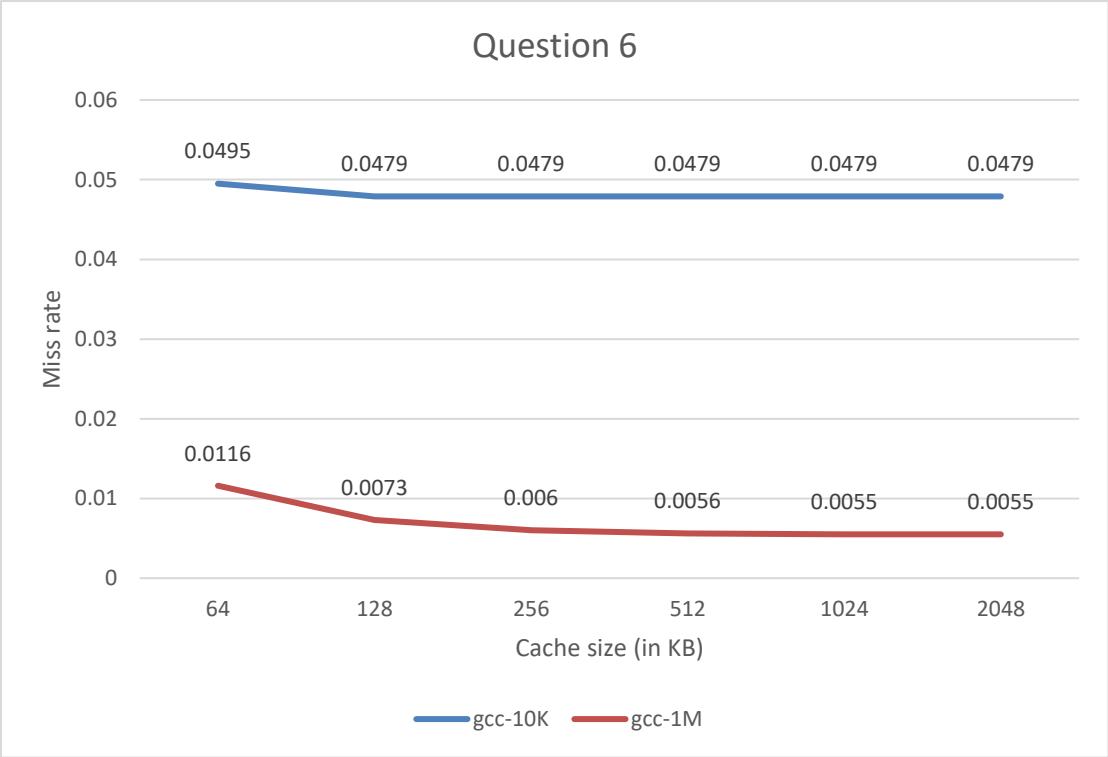
Increasing the number of ways lowers the hit rate. There are diminishing returns however after a certain point. This is likely due to the number of ways that are no longer needed for a "popular" index.

5. Assuming a 256KB 2-way set associative cache. How does varying the size of the block affect cache miss rate? Plot the block size (2B, 4B, 8B, 16B, 32B, 64B) vs miss rate for the two traces. What do you observe and why?



The miss rate again decreases as the block size increases. This causes the number of blocks to decrease, allowing the cache to warm up faster and cause more collisions.

6. Assuming a 2-way set associative cache and 32B block size. How does varying the size of the cache affect cache miss rate? Plot the cache size (64K, 128K, 256K, 512K, 1M, 2M) vs miss rate for the two traces. What do you observe and why?



The miss rate decreases but we see diminishing returns more quickly as we increase the cache size. This means that the number of available sets is increasing, but there is little need to do so after a certain threshold.

7. Measuring cold, capacity, and conflict misses. (See "Measuring/Classifying Misses" in slides). In this problem, we will identify the types of misses for an 8KB, 4-way set associative cache with block size of 32B. For the gcc-1M trace, provide a breakdown of the type of cache misses. *You can provide the breakdown in terms of the miss rate.* For example, if the 8KB, 4-way cache has a 20% miss rate, an infinite size cache have a 1% miss rate, and a fully associative cache have a 10% miss rate, then 1% is due to cold misses, 9% is due to capacity misses, and 10% is due to conflict misses.

Cold misses: simulating a fully associate cache of infinite size, we see 8454 misses.

$$8{,}454\ cold\ misses$$

Capacity misses: simulating a fully associate cache using the specs above, we see 68443 misses.

$$68443 - 8454 = 59{,}989\ capacity\ misses$$

Conflict misses: simulating target cache configuration, we see 76609 misses.

$$76609 - 59989 - 8454 = 8{,}166\ capacity\ misses$$