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Large-scale sensor systems based on graphene electrolyte-gated field-effect transistors†

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This work reports a novel graphene electrolyte-gated field-effect transistor (EGFET) array architecture along with a compact, self-contained, and inexpensive measurement system that allows DC characterization of hundreds of graphene EGFETs as a function of V_{DS} and V_{GS} within a matter of minutes. We develop a reliable graphene EGFET fabrication process capable of producing 100% yield for a sample size of 256 devices. Large sample size statistical analysis of graphene EGFET electrical performance is performed for the first time. This work develops a compact piecewise DC model for graphene EGFETs that is shown capable of fitting 87% of I_{DS} *vs.* V_{GS} curves with a mean percent error of 7% or less. The model is used to extract variations in device parameters such as mobility, contact resistance, minimum carrier concentration, and Dirac point. Correlations in variations are presented. Lastly, this work presents a framework for application-specific optimization of large-scale sensor designs based on graphene EGFETs.

Introduction

Graphene is a two-dimensional carbon allotrope consisting of sp^2-bonded carbon atoms arranged in a hexagonal lattice.[1–4] Graphene exhibits a number of desirable mechanical, optical, electrical, and chemical properties making it well suited for chemical and biological sensing applications. Electrically, graphene boasts high carrier mobility, which is an advantage for many chemical sensing applications.[5] Graphene FETs have demonstrated reasonable voltage gain making them suitable amplifiers in electrogenic cell sensing experiments.[6] Graphene's inertness also enables sensors to directly interface with the electrolytic environments found in many chemical and biological sensing applications and to take advantage of the high electric double layer capacitance.[7–11] In addition, graphene exhibits a wide electrochemical potential window in solutions mimicking physiological conditions such as phosphate buffered saline.[12] In terms of optical properties, graphene's extreme thinness allows for minimal absorption in the visible spectrum making graphene suitable for applications requiring transparent sensors.[13–15] In terms of mechanical properties, graphene possesses high strength and flexibility making it potentially useful in flexible and smart skin sensing applications.[16–19] Finally, graphene's atomically thin carbon composition meaning makes it intrinsically low cost. Chemical vapor deposition growth processes also enable large-area and economical production.[20,21]

A number of previous works explore the use of graphene as the channel material in electrolyte-gated field-effect transistors (EGFETs). These works include applications to chemical sensing, electrogenic cell sensing, and the development of electronic models.[22–27] Sample size and yield, however, are always very limited – often limited to tens of devices at best. In addition, the limited works containing statistical information regarding electrical performance typically do not provide data on the underlying device parameter variations responsible for variations in electrical performance. A few previous papers provide insight into graphene variation using Raman spectroscopy scanning tunnelling microscopy, and THz time-domain spectroscopy.[28–30] For sensing applications involving graphene EGFETs, however, variation data obtained directly from measurements of actual graphene EGFETs is clearly the most relevant.

This work develops a chip architecture and custom measurement system capable of accessing an array of N^2 devices using only 2N wires. Our specific implementation produces a sample size of 256 graphene EGFETs using a 16 × 16 array, which is accessed using 32 wires. This enables statistical analysis of graphene EGFET electrical performance parameters such as drain–source current, transconductance, output conductance, and voltage gain. We have also developed a compact model for graphene EGFETs, which enables the timely extraction of graphene EGFET device parameters such as mobility, minimum carrier concentration, contact resistance, and Dirac point.

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Sensor array system design

Measurement system design

The measurement system developed in this work is depicted in Fig. 1A, B and consists of a personal computer, microcontroller, custom-designed printed circuit board (PCB), and insertable graphene EGFET array chip. The personal computer primarily functions to record and process measured data and to program the microcontroller. The microcontroller supplies power to the PCB and provides digital control signals to manage row and column selection in the graphene EGFET array. The microcontroller is equipped with two 12-bit digital-to-analog (DAC) outputs that control the drain–source voltage V_{DS} and gate–source voltage V_{GS}.

The custom-designed PCB forwards the microcontroller-generated V_{DS} and V_{GS} biases to the appropriate graphene EGFET within the array. The V_{DS} bias is applied to the appropriate row *via* a 16-channel low-impedance analog multiplexer. The PCB then amplifies the resulting graphene EGFET I_{DS} currents across the entire row using a two-stage low-noise transimpedance amplifier (Fig. 1G). The gains of the first and second stages are −1000 V/I and −10 V/V, respectively. Another 16-channel analog multiplexer performs column selection and forwards the amplified I_{DS} signal to the microcontroller.

The amplified I_{DS} signals are routed from the PCB to a 12-bit analog-to-digital converter (ADC) on the microcontroller. All data is transmitted back to the personal computer *via* USB. The benchtop system is capable of characterizing I_{DS} as a function of V_{DS} and V_{GS} for 256 graphene EGFETs within a matter of minutes. The measurement system also readily incorporates Ag/AgCl and saturated calomel reference electrodes for chemical and biological sensing applications requiring stable reference potentials.

Graphene EGFET array fabrication

Graphene EGFETs consist of a graphene channel between two conductive source–drain contacts, typically metals. A diagram of a graphene EGFET diagram and a microscope image of an actual device are depicted in Fig. 1C and D, respectively. The fabrication process begins with a no. 2 coverslip with dimensions 2.2 cm × 2.2 cm and 0.2 mm thickness. The coverslip is coated with 25 nm of Al_2O_3 using atomic layer deposition (ALD). This ensures excellent photoresist adhesion in the subsequent metal lift-off process used to form Ti/Au (10 nm/150 nm) contact leads and array rows. Another 25 nm of Al_2O_3 is deposited as interlayer dielectric. BCl_3 plasma is used to etch windows into the interlayer dielectric to allow contact between first and second metal layers where appropriate. Array columns are formed by depositing a second layer of Ti/Au (10 nm/150 nm) using electron beam evaporation and lift-off photolithography.

Commercial graphene covered in poly methyl methacrylate (PMMA) from ACS Material is transferred over the array and nitrogen dried to remove any underlying water. The transferred graphene/PMMA film is baked for 15 minutes at 80 °C and for two hours at 130 °C. This allows the PMMA to reflow, which helps promote adhesion between the graphene and substrate. The sample is immersed in acetone for several hours to remove the PMMA. The sample is then annealed for three hours at 350 °C in 700 sccm H_2 and 400 sccm Ar to reduce PMMA residue and to further promote adhesion between the graphene and the substrate. The graphene channel regions are defined using MMA/SPR3012 resist stacks and oxygen plasma etching. The sample is immersed in acetone for several hours to remove the resists. The sample is then coated with approximately 2.4 μm of SU-8 2002. Windows are defined in the SU-8 over the graphene channel regions to allow electrolyte gating. The sample is baked at 150 °C for five minutes to remove cracks in the SU-8 and enhance its chemical resistance. The sample is coated with PMMA to protect the graphene from particulates and high-pressure water during subsequent die sawing, which trims the coverslip to the appropriate size for the measurement setup. The sample is immersed in acetone for several hours to remove the protective PMMA layer.

The graphene EGFET array is designed as an insertable chip containing wire sharing to the extent possible while maintaining the ability to access individual devices. This allows N^2 devices to be accessed using 2N wires. The design shown in Fig. 1E is based on the fact the currents sum in

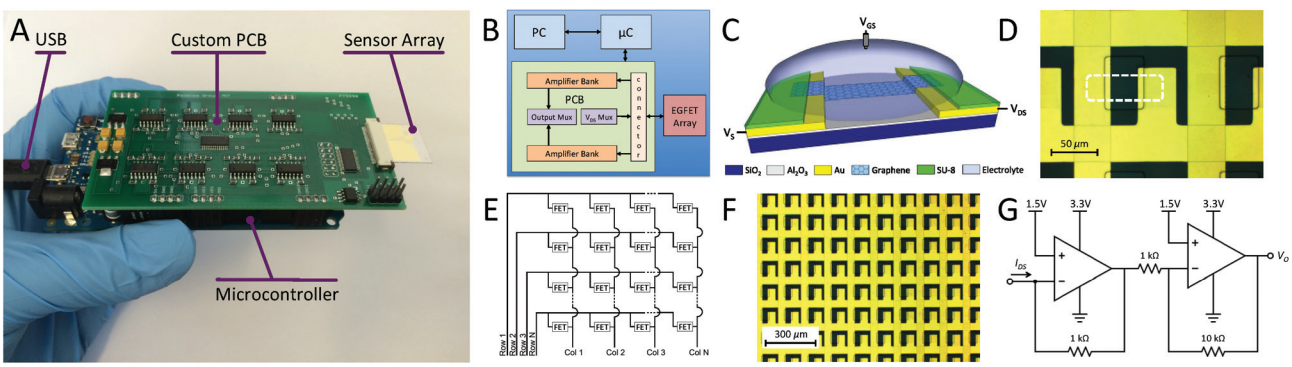

Fig. 1 (A) Complete measurement system and sensor array insert, (B) system overview, (C) graphene EGFET diagram, (D) microscope image of graphene EGFET with channel region outlined in white (dashed), (E) sensor array architecture, (F) microscope image of graphene EGFET sensor array, (G) transimpedance amplifier schematic.

parallel, which allows all output currents from a single column to be tied together as one output. Row multiplexing biases one device per column such that the entire output current for a given column stems from one device. Individual columns are replicated row-wise. The implementation of the arrayed structure is shown in Fig. 1F.

Compact piecewise DC graphene EGFET model

The measurement system developed in this work is capable of performing DC characterization on a large number of graphene EGFETs. This provides data on the variation in source–drain current I_{DS}, transconductance g_m, output conductance g_o, and intrinsic gain G_V. Many times, however, it is also desirable to extract the variations in device and material properties responsible for the variation in electrical performance. These device properties include mobility μ, top-gate capacitance C_{TOP}, minimum carrier concentration n_o, contact resistance R_C, and Dirac point V_o. From a practical standpoint, extracting the parameter variations for a large number of devices requires the development of a compact graphene EGFET model.

Fitting a graphene EGFET model to a single experimental I_{DS} *vs.* V_{GS} dataset typically requires an iterative optimization over a 5-parameters space: μ, C_{TOP}, R_C, n_o, V_o. In our case, each experimental I_{DS} *vs.* V_{GS} dataset contains roughly 100 points because V_{GS} spans approximately 1.0 V in 10 mV increments. If an iterative process is required to calculate individual I_{DS} values, it results in a nested iterative fitting process. This greatly increases the overall fitting time, which makes parameter extraction for a large number of devices impractical. Thus, developing a compact, yet accurate, model is imperative.

Three relevant models have been previously developed: one for graphene electrolyte-gated FETs[26] and two for metal-oxide-gated FETs.[31,32] The model for graphene electrolyte-gate FETs (EGFETs) incorporates the graphene quantum capacitance and solves I_{DS} by iteratively computing the potential profile spatially along the graphene channel until the applied V_{DS}, V_{GS}, and I_{DS} are all in agreement. The model has been shown capable of fitting experimental data with great accuracy, but is computationally expensive. This prohibits its use in fitting a large number of devices. The previously developed model is given by eqn (1) and may be thought of, in some sense, as the basis for the derived compact model. W is the channel width, L is the channel length, V is the potential along the channel, and v_{sat} is the saturation velocity. Equations detailing the voltage-dependent top-gate capacitance are omitted as our model will approximate $C_{TOP}(V)$ with a constant to reduce the computational expense. The other key assumptions made are constant and equivalent electron and hole mobilities along with symmetric contact resistances.

$$I_{DS} \approx \frac{\mu \frac{W}{L} \int_{I_{DS}R_C}^{V_{DS}-I_{DS}R_C} \sqrt{(qn_o)^2 + \left[C_{Top}(V)[V_{GS} - V - V_o]\right]^2}\,dV}{1 + \left|\frac{\mu(V_{DS} - 2I_{DS}R_C)}{Lv_{sat}}\right|} \quad (1)$$

In addition, the saturation velocity is neglected because graphene EGFETs are typically biased at low voltages to avoid oxidation–reduction reactions. Graphene quantum capacitance is also neglected to produce a constant top-gate capacitance. The form of the integrand in eqn (1) does not have a physical basis but serves to produce a nice rounding near the minimum carrier concentration and provide symmetry. We instead assume an abrupt transition near the minimum carrier concentration, which has a stronger physical foundation. This transforms eqn (1) into a simpler albeit piecewise equation (ESI†). I_{DS} remains present on both sides of the equation, but with a little manipulation, may now be isolated to the left-hand-side. This results in the compact model given by eqn (2). A number of variables are combined and renamed due to space limitations. The new variables include $k = \mu W/L$, $C = C_{TOP}$, $V_X = V_{GS} - V_o$, $n'_o = qn_o$, and $M = kCR_C^2$. Although the model may appear daunting, it is in fact readily coded and computationally inexpensive.

The three segments of the piecewise model correspond to scenarios in which the graphene channel is p-type, n-type, or a mixture of the two. Fig. 2 shows the derived piecewise model produces smooth and continuous transitions between each of the segments and ultimately yields graphene EGFET curves with all key features intact.

$$I_{DS} \approx \begin{cases} \dfrac{kV_{DS}\left[C\left(\frac{V_{DS}}{2} - V_X\right) + n'_o\right]}{1 + 2kR_C\left[C\left(\frac{V_{DS}}{2} - V_X\right) + n'_o\right]} & \text{when } V_X < I_{DS}R_C \\ \dfrac{1 + kR_C(CV_{DS} + 2n'_o) - \sqrt{[1 + kR_C(CV_{DS} + 2n'_o)]^2 - 4M\left[\frac{1}{2}kC\left[(V_{DS} - V_X)^2 + V_X{}^2 + kn'_oV_{DS}\right]\right]}}{2M} & \text{when } I_{DS}R_C \le V_X \le V_{DS} - I_{DS}R_C \\ \dfrac{kV_{DS}\left[C\left(V_X - \frac{V_{DS}}{2}\right) + n'_o\right]}{1 + 2kR_C\left[C\left(V_X - \frac{V_{DS}}{2}\right) + n'_o\right]} & \text{when } V_X > V_{DS} - I_{DS}R_C \end{cases} \quad (2)$$

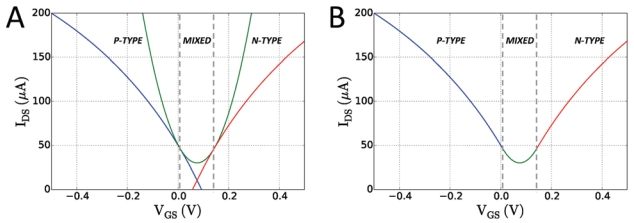

Fig. 2 (A) Different segments of the compact piecewise model and (B) the stitching together of segments in order to produce the overall I_{DS} *vs.* V_{GS} curve. Parameters are V_{DS} = 150 mV, W/L = 30 μm/30 μm, μ = 450 cm^2 V^{-1} s^{-1}, C_{TOP} = 9.0 μF cm^{-2}, R_C = 5 kΩ μm, n_o = 1 × 10^{12} cm^{-2}, and V_o = 0.0 V.

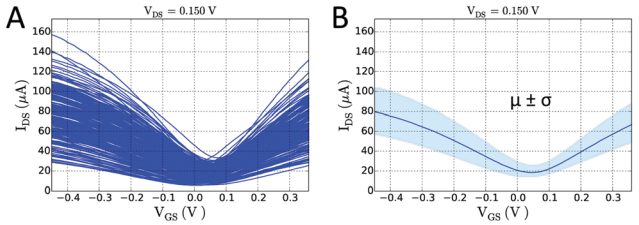

Fig. 4 (A) Individually measured graphene EGFET I_{DS} *vs.* V_{GS} curves, (B) mean I_{DS} *vs.* V_{GS} plus or minus one standard deviation.

Results & discussion

Variation in electrical performance

Individual graphene EGFETs within the array were characterized using 100 mM aqueous NaCl as the electrolyte and a Au plated wire as a pseudoreference gate electrode. V_{DS} was swept from 10 mV to 150 mV in increments of 10 mV. V_{GS} was swept from −0.5 V to 0.7 V in increments of 10 mV with a sweep rate of 10 mV s^{-1}. A 30 s hold time was applied at the beginning of each V_{GS} sweep. This provides sufficient time for ion migration so the electrical double layer may reach steady state. Data post processing was performed to correct drift in the Dirac point, which reduced the V_{GS} range. Plots of the acquired I_{DS} *vs.* V_{GS} data are presented in Fig. 4. Mean and standard deviations for source–drain current, transconductance, output conductance, and intrinsic voltage gain are given in Fig. 3.

Transconductance g_m and output conductance g_o are defined as $\partial I_{DS}/\partial V_{GS}$ and $\partial I_{DS}/\partial V_{DS}$, respectively. Partial derivatives are calculated numerically using finite differences. Intrinsic voltage gain G_V, also referred to simply as gain, is defined as the transconductance divided by the output conductance.

Graphene EGFET parameter variations

Variations in process-dependent parameters μ, R_C, n_o, and V_o are extracted using the compact graphene EGFET model. The top-gate capacitance C_{TOP} is approximated with 3 μF cm^{-2} based on electrochemical impedance spectroscopy (EIS) measurement of the graphene–electrolyte interface capacitance. A number of previous works provide extensive examination of graphene's electric double layer and quantum capacitance.[11,23,33,34] For V_{DS} = 150 mV, the mean percent error between model and experimental I_{DS} *vs.* V_{GS} curves was 7% or less for 87% of devices. Cases failing to meet this accuracy criterion were considered outliers and discarded. Because the model contains simplifying assumptions and inevitably fits experimental data with some degree of error, extracted device parameters and distributions represent approximations. This work, nonetheless, provides insight into parameter distributions for graphene EGFETs for the first time (Fig. 5). Variations do not exhibit strong spatial trends (ESI†). The 100% yield is also indicative of excellent graphene transfer and a uniformly processed array. Table 1 compares extracted parameter values with those previously reported in literature.

Correlation coefficients are computed to reveal relationships between parameter variations (Table 2). Mobility and minimum carrier concentration are found inversely corre-

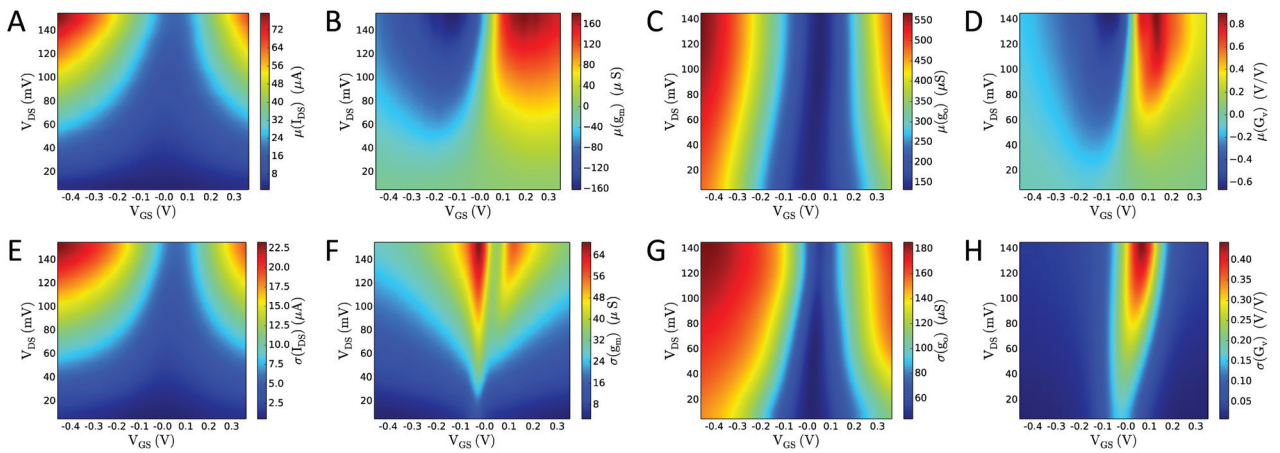

Fig. 3 Experimentally derived (A) mean source–drain current I_{DS}, (B) mean transconductance g_m, (C) mean output conductance g_o, (D) mean intrinsic voltage gain G_V, (E) standard deviation in source–drain current I_{DS}, (F) standard deviation in transconductance g_m, and (G) standard deviation in output conductance g_o. (H) Model derived standard deviation in intrinsic voltage gain G_V.

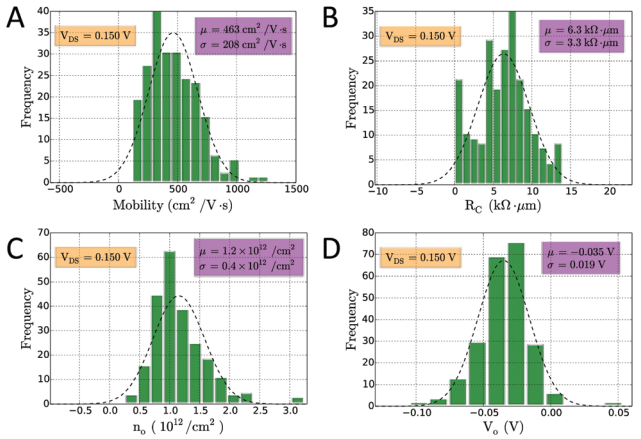

Fig. 5 Extracted graphene EGFET distributions for (A) mobility, (B) contact resistance, (C) minimum carrier concentration, and (D) Dirac point.

Table 1 Extracted parameters

	Units	Mean	S.D.	Reported	Ref.
μ	cm^2 V^{-1} s^{-1}	463	208	300–451	26 and 36
R_C	kΩ μm	6.3	3.3	11.5	26
n_o	10^{12} cm^{-2}	1.2	0.4	0.2–4.0	26, 31 and 35
V_o	mV	−35	19	N/A	N/A

Table 2 Process parameter correlation coefficients

	μ	R_C	n_o	V_o
μ	1	0.53	−0.52	0.40
R_C	0.53	1	−0.55	0.15
n_o	−0.52	−0.55	1	0.14
V_o	0.40	0.15	0.14	1

lated.[35] Minimum carrier concentration was found correlated with the Dirac point and contact resistance was found correlated with both minimum carrier concentration and mobility.

Performance optimization & trade-offs

Before performing optimization, the impact of the input variables on the loss function should be studied. This is especially important for problems with a physical basis such as graphene EGFET performance optimization. As an example of application-specific optimization, we have chosen the use of graphene EGFET arrays in a common-source amplifier configuration for the monitoring of electrogenic cells such as neurons or cardiac cells. In this application, we primarily wish to optimize the voltage gain. By investigating how the design parameters (V_{DS}, V_{GS}, W, L) and process-dependent parameters (μ, C_{TOP}, R_C, n_o, V_o) affect gain, we can develop some intuition regarding performance.

We investigate trends in gain performance by strategically modifying the design parameters and process-dependent parameters. At most, we may visualize three-dimensional data. For this reason, only two input parameters are varied at a time while all remaining parameters are fixed to some baseline value. Baseline parameter values are set based on the values extracted from our fabrication process (Table 3). Note that V_{GS} has no single baseline value. This is because gain is calculated across a V_{GS} range of ±1 V. The reported "gain" values depicted in Fig. 6 are in fact the maximum attainable gain given that the designer is free to manipulate V_{GS} to any value within ±1 V in order to maximize the gain. This allows gain to be plotted as a function of two variables without continually sacrificing one dimension to V_{GS}. A V_{GS} range of ±1 V is chosen because it is approximately the range of the graphene's electrochemical potential window in phosphate buffered saline.[12] Outside of this range, substantial oxidation–reduction reactions occur which may damage the graphene or alter its electrical properties.

The V_{DS} bias is limited to a maximum value of 200 mV to ensure I_{DS} values generated by the model for short channel lengths are sustainable in actual graphene EGFETs. Limiting V_{DS} also avoids model inaccuracies due to velocity saturation.

Fig. 6A shows the optimal V_{GS} does not vary significantly with changing channel length. Fig. 6B shows that the gain is also virtually independent on channel width provided that all other parameters remain constant. This is because increasing the channel width increases the transconductance and output conductance equally, leaving the overall gain unaffected. This suggests we may be able to reduce the optimization parameter space by eliminating the need to optimize the channel width. Gain also falls off as channel length is reduced. This is because at shorter channel lengths, contact resistance has a more pronounced effect on the transconductance while keeping the output conductance relatively constant because it is dominated by the graphene. Fig. 6C shows that if an application requires higher gain, one can simply increase the V_{DS} bias.

Now that we have investigated the effects of design parameters on the intrinsic voltage gain, we turn to analysing the process-dependent parameters. As the name indicates, these parameters are largely dependent on fabrication processes and more difficult for a designer to control. In some cases, however, it may be worthwhile to modify the fabrication process or perform some post-fabrication treatment of devices in order to achieve better performance.

Table 3 Baseline input parameters

Parameter	Units	Value
V_{DS}	mV	200
V_{GS}	mV	N/A
W	μm	30
L	μm	30
μ	cm^2 V^{-1} s^{-1}	463
C_{TOP}	μF cm^{-2}	3.0
R_C	kΩ μm	6.3
n_o	10^{12} cm^{-2}	1.2
V_o	mV	−35

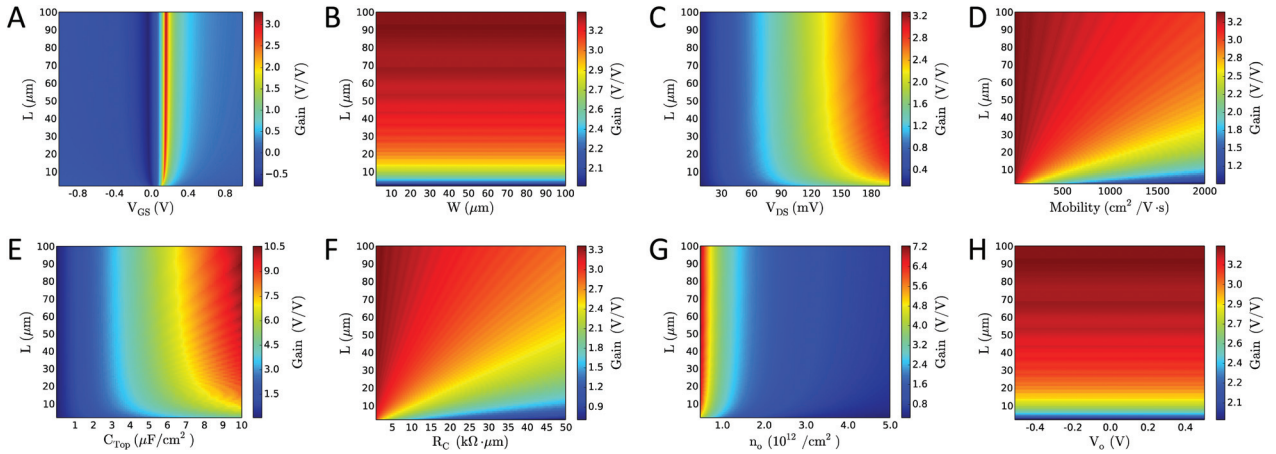

Fig. 6 Model derived trends for the intrinsic voltage gain as a function of (A) V_{GS} and L, (B) W and L, (C) V_{DS} and L, (D) mobility and L, (E) C_{TOP} and L, (F) R_C and L, (G) n_o and L, and (H) V_o and L.

Fig. 6D shows that increasing mobility reduces gain provided all other parameters are held constant. This stems from the fact that increasing mobility increases output conductance to a greater extent than transconductance. This effect becomes more pronounced at short channel lengths where contact resistance has a greater effect. Another interpretation is that high mobility increases the importance of having low contact resistance. It is important to note that it may not be possible to increase mobility to the extent simulated while keeping all other parameters constant as is assumed. For instance, higher mobilities are likely accompanied by lower values in minimum carrier concentration n_o, which is also supported by our correlation data in Table 2. Decreasing n_o has its own affect on gain. In any event, increasing mobility by a reasonable few hundred $cm^2\ V^{-1}\ s^{-1}$ does not greatly diminish gain except at very short channel lengths where contact resistance plays a greater role.

Increasing the top-gate capacitance is found to produce higher gain as shown in Fig. 6E. Larger top-gate capacitances more effectively translate V_{GS} signals into the graphene channel. In practice, however, the top-gate capacitance is limited by graphene's quantum capacitance and hydrophobicity.[23,26,37,38] Nonetheless, it becomes desirable to perform measurements in electrolytes that maximize the top-gate capacitance to the extent possible.

Lower contact resistances are found to produce higher gain provided all other parameters are fixed. This is shown in Fig. 6F. Lower contact resistances produce higher transconductances while having little effect on the output conductance, which is mostly determined by the graphene channel. This effect becomes more pronounced at small channel lengths where contact resistance has a greater effect on performance. Because contact resistance is a parasitic and provides absolutely no benefit, it should be minimized.

Fig. 6G shows that decreasing n_o increases gain. Decreasing n_o likely has little effect on the transconductance. It does, however, lower the output conductance, especially in the region around the minimum conduction point on the I_{DS} *vs.* V_{GS} curve. This is the region where the maximum gain is typically found. Ultimately, decreasing n_o decreases g_o while keeping g_m relatively constant, leading to increased gain.

Gain was found to increase with channel length in every case. General trends for optimizing gain in graphene EGFETs are summarized in Table 4.

Now that some intuition exists regarding gain performance of graphene EGFETs, it is possible to move on to a more thorough procedure for optimizing gain performance. Instead of optimizing purely for gain, it is possible to include penalties for variability in gain as well as increases in device area, noise, and power consumption. Minimizing variability in gain performance may be especially important for applications where all devices are gated using a common V_{GS}. Eqn (3) describes the objective function including these penalty terms. The fact that gain is a function of design and process parameters is omitted for readability. Eqn (3) also assumes the likely scenario in which the designer is free to manipulate the design parameters but has no control over the process-dependent parameters.

$$H(V_{DS}, V_{GS}, W, L) = \mu(\text{Gain}) + k_1\sigma(\text{Gain}) + k_2WL + k_3I_{DS} \quad (3)$$

where μ(Gain) and σ(Gain) are the mean and standard deviation of the intrinsic voltage gain, respectively. Constants k_1, k_2, and k_3 should be negative values because increases in variation, area, noise, and power consumption are typically undesirable. Optimization algorithms are typically designed to

Table 4 Gain optimizing parameter trends

Parameter	V_{DS}	V_{GS}	W	L	μ	C_{TOP}	R_C	n_o	V_o
Desired	↑	N/A	↕	↑	↓[a]	↑	↓	↓	↕

[a] Counterintuitive result.

minimize a loss function. Eqn (3) may be transformed into the appropriate loss function by taking the negative logarithm. The standard deviation in gain term may be approximated using a multivariate normal distribution in conjunction with the parameter variation data and covariance data. The loss function may then be minimized using a standard optimization algorithm capable of handling non-convex problems. This example provides a framework for optimizing the performance of graphene EGFET arrays for specific applications under a number of design constraints and trade-offs. Although this example deals with optimizing voltage gain, the method may be readily applied to the optimization of other electrical characteristics, such as transconductance.

Conclusions

Large-scale sensor arrays based on graphene EGFETs represent a promising technology for both chemical and biological sensing applications. This work reports a reliable fabrication process by producing a large-scale graphene EGFET array with 256 devices and 100% yield. The developed array architecture in conjunction with a compact and self-contained measurement system enables DC characterization of 256 graphene EGFETs as a function of V_{DS} and V_{GS} within minutes. These technological advancements represent a milestone in the development of graphene EGFET sensors by enabling the convenient and rapid acquisition of high quality data for a large number of devices. Large sample size statistical data on the electronic performance of graphene EGFETs is provided for the first time. This includes mean and standard deviations for drain–source current, transconductance, output conductance, and intrinsic gain.

This work has also developed a compact piecewise DC graphene EGFET model that is shown capable of fitting 87% of graphene EGFET I_{DS} *vs.* V_{GS} curves with a mean percent error of 7% or less. The compact model enables the extraction of device parameters for a large number of graphene EGFETs for the first time. By extension, this enables the extraction of parameter distributions for mobility, contact resistance, minimum carrier concentration, and Dirac point. It is now possible to characterize the impact of different fabrication processes on device parameter distributions. This is an important step in the development of any sensor technology based on graphene EGFETs.

Lastly, this work provides some intuition regarding the impacts of design parameters and process-dependent parameters on the intrinsic voltage gain of graphene EGFETs. Graphene EGFETs exhibit reasonable gain making them suitable for use as amplifiers or buffers in certain sensing applications. To maximize performance, this work provides a framework for application-specific optimization of large-scale sensor arrays under a number of design constraints and trade-offs. The sum of these contributions make this work a resource for the development of future chemical and biological sensor systems based on graphene EGFETs.

Note added after first publication

This article replaces the version published on 12th January 2016, which contained errors in Fig. 1 and Table 2.

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