Graphene Chip Tester PCB Documentation

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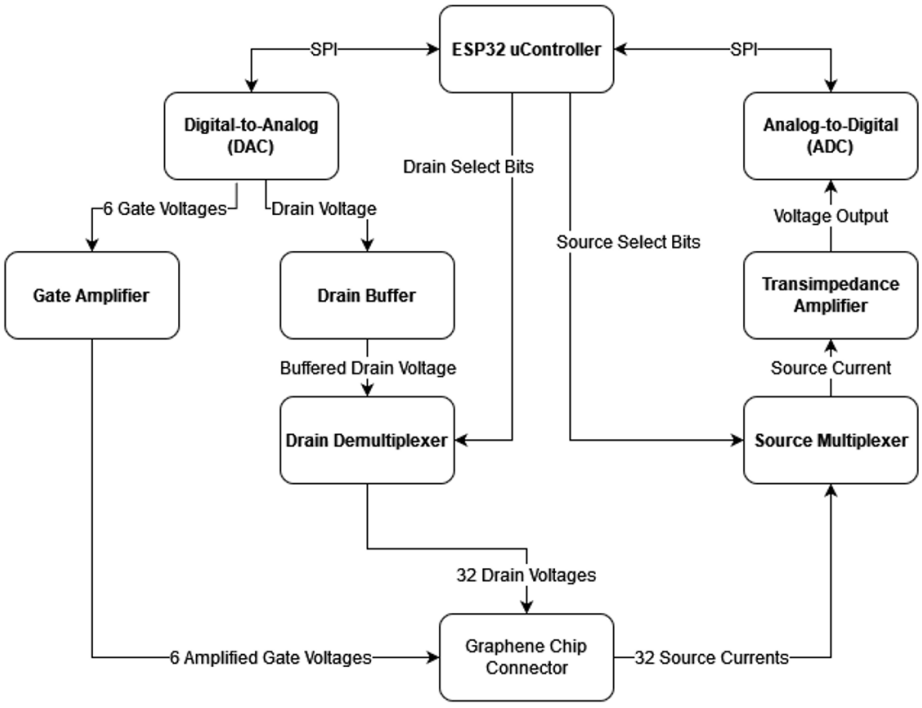
1 PCB Block Diagram



2 PCB Input and Output Specs

Supply Voltage	V_{GS} **Range**	V_{DS} **Range**	I_{DS} **Resolution**	I_{DS} **Range**
5V (from USB)	$-1V$ to $+1V$ (pre-amplification) $-21V$ to $+19V$ (w/ amplification*)	$-1V$ to $+1V$	$0.49\mu A$	$-0.98mA$ to $0.96mA$

*Positive and negative V_{GS} thresholds can be adjusted lower using the gate potentiometers to protect the chip from dangerous voltages.

3 Chief Components

3.1 Microprocessor

The microcontroller on this PCB is an ESP32-DEVKIT V1-DOIT. The ESP32 was chosen because it has many GPIO pins, several hardware SPI peripherals, and integrated WiFi, the last of which would be useful for a wireless version of this PCB. Compared to the Arduino Due, which was being used on a previous version of this PCB, the ESP32 has a faster clock speed (84 vs 240 MHz) and a much lower cost. The faster clock speed means faster digital reads and writes on GPIO pins. From testing, the ESP32 can toggle a GPIO pin on and off using digitalWrite 1 million times in 273 ms (so a single toggle takes on average 273 ns).

The ESP32 is powered by 5V from USB. On this PCB, the ESP32 has two main functions: interfacing with the ADC and DAC, and controlling the two multiplexers. For the ADC and the DAC, the ESP32 uses its VSPI interface for $MOSI$, $MISO$, and SCK, and two extra GPIO pins for selecting the two chips. For each multiplexer, the ESP32 uses 5 GPIO pins for choosing 1 of the 32 multiplexer channels, as well as 1 extra GPIO for enabling the multiplexer.

A small modification was made to the ESP32: a 100nF capacitor was soldered from the EN pin to GND. This enables us to flash the ESP32 without having to press the BOOT button each time.

3.2 Voltage References

There are several voltage regulators on the PCB, all of which take 5V from USB as input. The table below lists all the voltage regulators:

Voltage	**Part No.**	**Use**
$1V$	AP7365-10EG-13	Voltage reference for gate amplifiers and transimpedance amp
$2V$	NCP1117ST20T3G	Voltage reference for ADC and DAC
$3.3V$	LDL1117S33R	Power for ADC, DAC, multiplexers, transimpedance and drain buffer op-amp
$\pm 20V$	LT1945EMS#PBF	Powering gate amplifier and gate threshold op-amps

One issue that came up during testing the PCB was that the voltage output of the 1V regulator was not staying at 1V, instead jumping as high as 2V. The issue is that the gate amplifier op-amps on the PCB are trying to sink a small amount of current (about 1 mA) into the 1V regulator. However, the 1V regulator chosen cannot handle any amount of sink current. Therefore, this issue was solved by placing

a $1k\Omega$ resistor from 1V to GND to draw some current, so there there would be a net source current from the 1V regulator.

3.3 Digital to Analog Converter (DAC)

The DAC on this PCB is the AD5328BRUZ. This is a 12-bit DAC with 8 analog output channels, although on this board only 7 channels are used: 6 for gate voltages, and 1 for the drain voltage. The DAC is given a voltage reference of 2V, so it can produce voltages between 0V and 2V, in increments of $\frac{2}{2^{12}} \approx 0.49$ mV. Since the source of the graphene FETs is 1V, this allows for equal positive and negative V_{DS} and V_{GS} swing. The DAC interfaces with the ESP32 via SPI; $MOSI$ from the ESP32 is connected to the DIN pin of the DAC, which is used to write serial data to the DAC's input registers.

Two additional pins on the DAC are $\overline{SYNC}$ and $\overline{LDAC}$. When $\overline{SYNC}$ goes low, the DAC begins reading serial data from the DIN pin, so this pin is connected to the DAC Chip Select pin on the ESP32. Meanwhile, pulsing $\overline{LDAC}$ low transfers the contents of the DAC's input registers to its output pins. Therefore, $\overline{LDAC}$ is connected to a separate GPIO on the ESP32, which is pulsed low whenever we want to update all the DAC outputs at once.

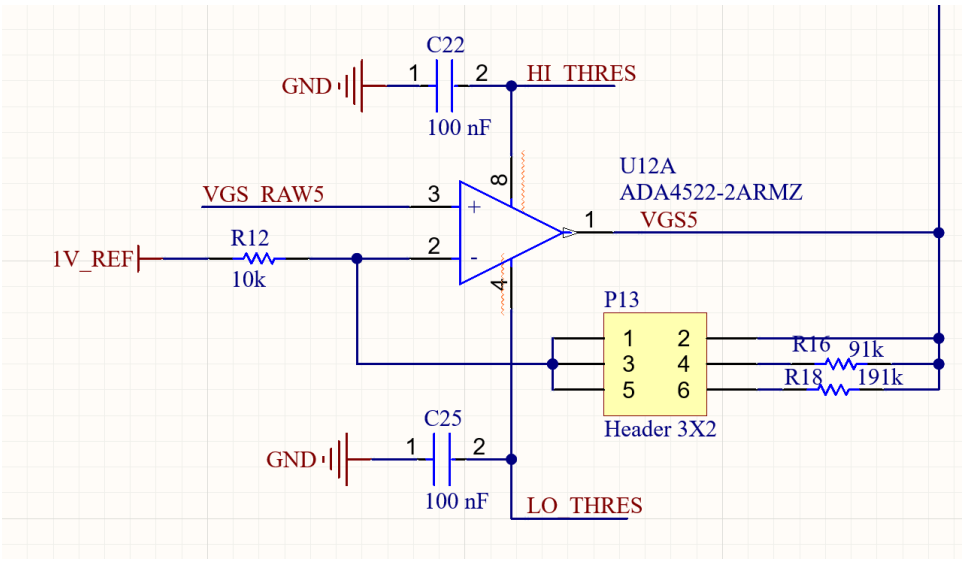
3.4 Multiplexers

There are two analog multiplexers on this PCB, both of which are the ADG732BSUZ. The drain (de)multiplexer connects the buffered drain voltage from the DAC to 1 of 32 drain connections on the graphene chip. The source multiplexer connects 1 of 32 source connections from the graphene chip to the transimpedance amplifier. If the graphene chip being tested has less than 32 drain and source connections, the code can be modified so that only some of the channels are addressed. For example, for a smaller 16x16 graphene chip, the code sets $A4$ (the most significant address bit) low for both multiplexers.

Since the transimpedance amplifier will be measuring I_{DS} current from the source connection, it is important that the impedance of the multiplexers is much lower than the impedance of our graphene FETs, or else the measured current would be lower than expected. For a 3V supply, the typical on-resistance of each ADG732 is 7Ω, while the impedance of the FETs is around 1000Ω. Therefore, the error in our current measurement will be around $\frac{14}{1000} = 1.4\%$. Another important spec is the switching frequency of the multiplexers. For a 3V supply, the ADG732 has max output transition time of 62 ns, so we can theoretically switch the drain and source channels at up to 16MHz. On the actual PCB, we are limited by the GPIO read/write speed of the ESP32.

3.5 Gate Amplifiers

The V_{GS} voltages produced by the DAC have a range from -1V to +1V. Op-amps on the PCB allow us to choose to amplify each gate voltage by either 1X, 10X, 20X (the 1X simply acts as a buffer). This is done through a non-inverting topology, shown below.



To choose our desired amplification, we place a jumper in one of three locations on the 3x2 header. This jumper will either put a 91k resistor between the op amp's inverting input and its output (for x10 amplification), a 191k resistor (for x20 amplification), or directly connect input to output (for x1 amplification).

3.6 Gate Potentiometers

The gate amplifiers can amplify the V_{GS} voltages up to -21V to +19V. However, some graphene chips that we test might not be able to handle these high voltages, and could get damaged if the wrong amplification is accidentally set. To prevent this, we can adjust high and low V_{GS} thresholds by adjusting two potentiometers on the PCB. Adjusting these potentiometers changes the voltage output of two resistor dividers. These voltages are buffered and then used to power the supply rails of the gate amplification op-amps. Because the op-amp cannot produce a voltage higher than its positive supply rail or lower than its negative supply rail, the potentiometers can be used to limit the voltage range of the gate amplifiers.

The high V_{GS} threshold can be set anywhere from +19V to +1.14V, while the low V_{GS} threshold can be set from -21V to -3.14V. The difference in the high and low ranges is due to the fact that the source voltage is at 1V. To check that the V_{GS} thresholds are properly set, the user should measure

each voltage threshold with respect to the 1V reference (i.e. red lead of the multimeter on the threshold voltage, black lead on 1V reference).

3.7 Gate Switches

As an additional failsafe measure, if the user wishes to immediately turn off any of the gate voltages, there are mechanical switches on the PCB that allow them to do so. These are single-pole, double-throw switches. The "on" configuration passes the amplified gate voltage directly to the gate on the graphene chip, while the "off" configuration passes a 1V reference instead. Since the source voltage is 1V with respect to the ground, turning the switch "off" sets the V_{GS} of that gate to 0V.

3.8 Transimpedance Amplifier

A transimpedance amplifier is current to voltage converter, and the one on this PCB is implemented using the OPA2388IDR rail-to-rail op-amp. It converts the I_{DS} current coming into the op-amp's inverting input into a voltage output of $1 - 1000I_{DS}$. Therefore, this transimpedance amplifier has a gain of 1000V/A. This gain is set by a 1k resistor between the inverting input and the output of the op-amp. Having the op-amp be rail-to-rail is important since it allows us to measure the maximum possible current; otherwise, the voltage output of the op-amp would saturate at a lower measured current.

During initial testing with the PCB, there was a large amount of variation in the measured current across the different FETs of the graphene chip. This issue was fixed by placing a compensation capacitor is parallel with the gain resistor of the transimpedance amplifier. This capacitor helps attenuate high-frequency noise, since the new gain of the amplifier is

$$Z_R||Z_C = \frac{R}{1 + j\omega RC}$$

By trial and error, the compensation capacitor was set to 330 pF. This gives our amplifier a pole at $\frac{1}{2\pi RC} \approx 482$ kHz.

3.9 Analog to Digital Converter (ADC)

The ADC on this PCB is the MCP3201. This is a 12-bit ADC. The ADC is given a voltage reference of 2V, so it can read analog voltages between 0V and 2V, with a resolution of $\frac{2}{2^{12}} \approx 0.49$ mV. The ADC is taking in the analog voltage from the transimpedance amplifier, and outputting serial data on

its $DOUT$ pin whenever its chip select pin $\overline{CS}$ is pulled low. Therefore, $DOUT$ is connected to $MISO$ on the ESP32, and $\overline{CS}$ is connected the ESP32's ADC Chip Select pin.

3.10 Maximum and Minimum I_{DS}

I_{DS} is converted into a voltage by the transimpedance amplifier, and then converted from an analog voltage to a digital serial output by the DAC. The miminmum detectable I_{DS} is limited by the DAC. The DAC can measure voltages with a resolution of 0.49 mV. Since the transimpedance amplifier has a gain of 1000, this means the current resolution is 0.49 μA. The DAC can have up to ± 2 bits of offset error and ± 1 bits of gain error, so the smallest I_{DS} we can reliably measure is around 3 μA.

The maximum positive I_{DS} measurable is limited by the transimpedance amplifier's output voltage swing. When the negative supply rail of the OPA2388IDR connected to ground, the op-amp can produce voltages as low as 40 mV. Since the equation for our transimpedance amplifier is $1 - 1000 I_{DS}$, this means the maximum I_{DS} measurable is 0.96 mA.

The maximum negative I_{DS} measurable is limited by the DAC's reference voltage of 2V. This limits the maximum negative I_{DS} to -1 mA (in practice, around -0.98 mA).