



## Digital Signal Processing - IP and Algorithms

[Register](#) [Sign In](#) [Help](#)[Xilinx User Community Forums](#)[Xilinx Products](#)[DSP Solutions](#)[Digital Signal Processing - IP and Algorithms](#)[Need help for FIR filter](#)[Reply](#)[Topic Options](#)[Message Listing](#)[Previous Topic](#)[Next Topic](#)[Previous](#) [1](#) [2](#) [Next](#)[rashidi](#)

Visitor



Posts: 4

Registered: 01-04-2011

[0](#)

### Need help for FIR filter

[Options](#)

01-04-2011 06:59 AM

Hi;

I am a beginner to filter design and I want to implement FIR filter with 300 tap and complex coefficient value. I want to use this FIR filter for implement MATCHED filter in virtex-4 fpga. I designed this FIR filter in MATLAB and when I want to generate COE file for xilinx, process stopped and displayed error to create COE file with complex value for xilinx.

Please help me to solve this problem and implement FIR and MATCHED filter.

Regards

Message 1 of 19 (7,296 Views)

[Reply](#)

Xilinx Employee



Posts: 2,979

Registered: 11-28-2007

[1](#)

### Re: Need help for FIR filter

[Options](#)

01-05-2011 09:23 PM

The FIR compiler (in CoreGen or SysGen) doesn't accept complex data or coefficient. What application are you working on? In general, you need to split the complex data into the real and imaginary parts and then process them using your algorithm. For RF signal processing, you normally get separate I/Q (real/imaginary) data, so you can pass them through 2 sets of FIR filters and each set of filter uses real coefficients.

rashidi wrote:

Hi;

I am a beginner to filter design and I want to implement FIR filter with 300 tap and complex coefficient value. I want to use this FIR filter for implement MATCHED filter in virtex-4 fpga. I designed this FIR filter in MATLAB and when I want to generate COE file for xilinx, process stopped and displayed error to create COE file with complex value for xilinx.

Please help me to solve this problem and implement FIR and MATCHED filter.

Regards

Cheers,  
Jim

Message 2 of 19 (7,274 Views)

[Reply](#)[rashidi](#)

Visitor



Posts: 4

Registered: 01-04-2011

[0](#)

### Re: Need help for FIR filter

[Options](#)

01-05-2011 10:05 PM

Thank you very much, Jim

I think this solution is reasonable but I have another question about oversampling for filter. Let me to try to implementing filter and if I can't find good response, I ask other question.

Regards

Message 3 of 19 (7,268 Views)

Reply

**XILINX eschei**  
Xilinx Employee



Posts: 32  
Registered: 02-09-2009

0

### Re: Need help for FIR filter

Options

01-05-2011 10:14 PM

Hi,

There is a big difference between a complex filter and filtering separate I and Q channels. So first I would confirm that you really need to implement complex filtering. If you do require complex coefficients, then you can still use the FIR compiler to implement a complex filter, but some additional work is required. A complex filter can be built out of 4 separate filters. For example, if you have the following equations:

$$I' = I * CI - Q * CQ ; Q' = I * CQ + Q * CI,$$

then you can implement this with four filters as follows:

Filter 1 =  $I * CI$  ; Filter2 =  $I * CQ$  ; Filter 3 =  $Q * CI$  ; Filter 4 =  $Q * CQ$

This would require that you use an additional adder and subtract after the filters. If your sample rate is slow and you have many clock cycles to process the data, then it may be possible to use one filter with re-loadable coefficients to save resources.

Cheers,  
-es

Message 4 of 19 (7,265 Views)

Reply

**rashidi**  
Visitor



Posts: 4  
Registered: 01-04-2011

0

### Re: Need help for FIR filter

Options

01-08-2011 08:06 AM

Hi [eschei](#):

thanks for your notice. Really I need 4 filter as you noticed, but I think :  $I' = I * CI + Q * CQ$  ;  $Q' = I * CQ - Q * CI$ .

My project sample rate is slow but I don't have many clock cycle to proceed. I think, I want 4 separate fir filter with real and imaginary coefficient value with high input clock for filter to reduce DSPSlice. My project fpga contain other process and it doesn't have enough DSPSlice for implement fir filter with low clock frequency and I have another question about this overclocking. Imagine I have 50 coefficient value for my fir filter and " fir clock input = 25\*data sample input ". what consideration need to generate and work with this core? Is true that load COE file with 50 value? Or must to multiply that to 25?

Thanks for your attention and notice

Message 5 of 19 (7,220 Views)

Reply

**XILINX ywu**  
Xilinx Employee



Posts: 2,979  
Registered: 11-28-2007


0

### Re: Need help for FIR filter [ Edited ]

Options

01-10-2011 07:40 AM - edited 01-10-2011 07:41 AM

I highly recommend you use the FIR compiler (CoreGen or SysGen) to create the FIR filters. Below is a snapshot of the FIR compiler GUI in CoreGen. Regarding the overclocking, you can just enter your input sampling frequency and the FPGA clock frequency in the "Hardware Oversampling Specification" section (in red square) and the tool will take care of optimizing the hardware resource required. Based on your description, it looks like each FIR can be implemented with just one multiplier assuming the coefficients are symmetric and 25x oversampling.



# FIR Compiler

5.0

Component Name

### Filter Coefficients

Select Source :

Coefficient Vector :

Coefficients File :

Number of Coefficient Sets :  Range: 1..256

Number of Coefficients (per set) : 21

### Filter Specification

Filter Type :

Rate Change Type :

Interpolation Rate Value :  Range: 1..1

Decimation Rate Value :  Range: 1..1

Zero Pack Factor :  Range: 1..1

Number of Channels :  Range: 1..64

### Hardware Oversampling Specification

Select format :

Input Sampling Frequency :  Range: 0.000001..550.0 MHz

Clock Frequency :  Range: 0.001..550.0 MHz

Input Sample Period :  Range: 1..100000000 Clock cycles

Page 1 of 4

rashidi wrote:

Hi [eschei](#):

thanks for your notice. Really I need 4 filter as you noticed, but I think :  $I' = I * CI + Q * CQ$  ;  $Q' = I * CQ - Q * CI$ .

My project sample rate is slow but I don't have many clock cycle to proceed. I think, I want 4 separate fir filter with real and imaginary coefficient value with high input clock for filter to reduce DSPSlice. My project fpga contain other process and it doesn't have enough DSPSlice for implement fir filter with low clock frequency and I have another question about this overclocking. Imagine I have 50 coefficient value for my fir filter and " fir clock input = 25\*data sample input ". what consideration need to generate and work with this core? Is true that load COE file with 50 value? Or must to multiply that to 25?

Thanks for your attention and notice

Cheers,  
Jim

[mahadevanna](#)

Regular Visitor



Posts: 37

Registered: 12-28-2010

0

Message 7 of 19 (7,162 Views)

### Re: Need help for FIR filter

01-12-2011 12:33 AM

is it possible to implement cross correlation using **Distributed Arithmetic FIR Filter(DAFIR)**

[Options](#)

[Reply](#)

 [XILINX](#) [chrisar](#)

Xilinx Employee



Posts: 403

Registered: 08-01-2007

0

Message 8 of 19 (7,142 Views)

### Re: Need help for FIR filter

01-12-2011 03:40 PM

Yes you should be able to use the DA FIR for this, but it's quite old and I would recommend moving to the FIR Compiler.

Chris

Video Solutions Center: <http://www.xilinx.com/support/answers/56851.htm>

[Options](#)

[Reply](#)

[mahadevanna](#)

Regular Visitor



Posts: 37

Registered: 12-28-2010

0

Message 9 of 19 (7,124 Views)

### Re: Need help for FIR filter

01-13-2011 06:53 AM

thanks for the reply .. can u plz tell in detail how can i implement cross correlation of two signals.

[Options](#)

[Reply](#)

[mahadevanna](#)

Regular Visitor



Posts: 37

Registered: 12-28-2010

0

Message 10 of 19 (7,102 Views)

### Re: Need help for FIR filter

01-13-2011 09:11 PM

can u please tell how cross correlation of two signals can be implemented by both DAFIR and also BY FIR complier.

waiting for your reply

[Options](#)

[Reply](#)

[Previous](#)   [1](#)   [2](#)   [Next](#)

[Message Listing](#)

[Previous Topic](#)

[Next Topic](#)