**Table 1: Project Chart**

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| **#** | **Activity** | **Predecessor** | **Duration**  **(days)** | **Responsibility** |
| 0.1 | Create a System Boundary Diagram | - | 1 | John |
| 0.2 | Create a Mission Scenario | 0.2 | 2 | Matt |
| 0.3 | Create Project Chart and Network Flow Diagram | 0.1, 0.2 | 3 | Natalie |
| 0.4 | Recommendation Report | 0.1, 0.2, 0.3 | 10 | All |
| 0.5 | Project Plan, including WBS and brief SOW | 0.1, 0.2, 0.3, 0.4 | 15 | All |
| 0.6 | Requirements Document | 0.1, 0.2, 0.3, 0.4, 0.5 | 15 | All |
| 0.7 | System Requirements (SRR) | 0.1, 0.2, 0.3, 0.4, 0.5, 0.6 | 10 | All |
| 0.8 | Preliminary Design Review (PDR) | 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7 | 7 | All |
| 0.9 | System Requirements Specification | 0.1, 0.2, 0.3, 0.4, 0.5, 0.6 | 7 | All |
| 0.9a | Demo Presentation | 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7 | 2 | Natalie |
| 1.1 | Determine interface method between product and guitar (Considerations discussed thus far are: 1/4th inch to USB and custom pick-up) | 0.1, 0.2 | 5 | All |
| 1.2 | Determine interface method product and amp | 0.1, 0.2 | 30 | All |
| 1.3 | Determine which development platform (Considerations discussed thus far are: Zync 7020 (FPGA/Arm) on Zedboard, several Adruinos and a software application on Windows/Mac/Linux) | 0.1, 0.2 | 5 | Natalie/John |
| 1.4 | Create several input samples for simulation and developing | - | 5 | Dave/Natalie |
| 1.5 | Research and decide on a shifting algorithm with minimal artifacts and latency | - | 15 | Dave/Matt |
| 1.6 | Research note detection algorithms | 1.4 | 20 | Dave/Matt |
| 2.0 | Implement single string retuning simulation in MATLAB | 1.4, 1.5 | 30 | Dave/Matt |
| 2.1 | Implement electronic capo mode simulation in MATLAB | 1.4, 1.5 | 30 | Dave/Matt |
| 2.2 | Create a developers GUI for note detection to speed up development time and showcase results for demonstrations | 1.4 | 5 | Natalie/Jon |
| 2.3 | Create a GUI to simulate the user’s general experience. | 1.4, 1.5 | 5 | Natalie/Jon |
| 3.0 | Implement single string retuning on either an Zynq 7020, microprocessors or software | 1.2, 1.3, 2.0 | 60 | Natalie/John |
| 3.1 | Implement electronic capo mode on either an Zynq 7020, microprocessors or software | 1.2, 1.3, 2.1 | 60 | Natalie/John |
| 3.2 | PCB design research for production unit | 4 | 20 | All |
| 3.3 | ADC/DAC Implementation | - | 30 | Jon/Matt |
| 4.0 | Design a user interface for the prototype. | 3.0, 3.1 | 15 | Matt |