Post layout verification of the MTM-RISCV chip.

TABLE OF CONTENTS

Document history

17.05.2021 – v1.00 – RS - initial version
11.05.2022 – v1.01 – RS – 2022 update

1 POST-LAYOUT VERIFICATION

Note: ***All your actions regarding "TODO" items should be documented in the project report.***

The actions below will provide minimum verification for the designed chip.

All the necessary files are provided in the *master* branch in the repository.

1.1 POST-LAYOUT SIMULATION

The post-layout simulations use the netlist and the SDF (Standard Delay Format) file with minimum and maximum delays generated by the P&R tool (Innovus). There are three goals for the simulations:

- functional verification of the design, to prove that the optimization algorithms did not change the functionality,
- timing verification of the design, to crosscheck the timing information given by P&R tool,
- generation of activity data for estimation of the power consumption.

The post-layout simulations can be very time consuming, so it is important to reasonably split them into several stages, as listed below.

All the post-layout simulations are run in the ***sim_post*** directory.

1.1.1 Stage #1: environment debugging

At this stage, we do not care about the timing and do not dump any activity data. We want to make sure that SDF file is annotated properly, and the simulation gives correct results.

TODO: Run the simulation without timing checks and without TCF (Toggle Count File). See the *README* file and run script help for documentation. Check in the log the SDF statistics: both path delays and timing checks should have 100% annotation. The result of the simulation should be PASSED. Measure and report the simulation time (use *time ./run_post.sh*). Expected run times are in the range of minutes.

1.1.2 Stage #2: functional simulation and timing verification

At this stage, you will verify the design of the two timing corners: MIN (the fastest case) and MAX (the slowest case). All timing checks (setup, hold, recovery, removal) will also be checked.

TODO: Run the simulation for both corners with timing checks enabled (do not enable TCF dump yet). The result of the simulation should be "PASSED" in both cases, with no timing violations.

Note: you can ignore any errors or violations appearing before the reset signal is released.

Expect 30%-50% longer simulation time than in stage #1.

1.1.3 Stage #3: dumping switching activity

The activity file provides switching information (activity factor and other data) for each node in the design. Thus, read access to all nodes in the design is required and many optimization algorithms can not be used. This leads to very long simulations, but we have to do this only once.

TODO: Run the simulation without timing checks and with TCF dump enabled. Verify that the activity file **.tcf.gz* contains real data (not only zeros).

Expect the run times 15-20x slower than in stage #1 (this gives 1 hour for each 3 minutes in stage #1).

1.2 POWER CONSUMPTION ESTIMATION.

To estimate the power consumption, we will use the last database saved during the P&R session and the TCF file from the previous stage.

The setup is ready in the ***power*** directory.

TODO: Browse the scripts and run the analysis. Look for TODO keywords inside the script and follow the instructions.

TODO: Answer the following questions:

- What is the total power consumed for the simulated scenario?
- How much power is consumed by the clock network (total value and percent)?
- How much power is consumed by the I/O cells?
- How much power comes from leakage?