MOROP	European model railway standards **Digital control signal DCC** **Bit representation**	**NEM** **670** Page 1 of 3

Binding standard **2013 edition**
(replaces 2007 edition)

Note 1: NEM 670 corresponds in content to NMRA Standard S 9.1 (as of July 2004). This version is the basis for conformity tests.

NEM 670 follows the NMRA standard S 9.1. This version is the basis for conformance tests.

Note 2: According to this standard, there is no backward compatibility with older decoders with 14 speed steps and an additional function, as well as with older decoders whose internal timing does not override the times specified here.

Note 3: More detailed technical data can be found in RailCommunity's RCN-210.

1. Purpose of the standard

The subject of this standard is bit representation according to the DCC standard.

2. Bit representation

a) Data transmission in the DCC standard is carried out by transmitting a series of bits, which are represented by the voltage curve over time on the track (the **track signal**). A bit represents one of two states, which are called 1 and 0.

b) The DCC track signal consists of a sequence of transitions between two voltage levels of opposite polarity, called zero crossings[2)]. A zero crossing is the midpoint between two voltage levels of opposite polarity.

c) Two consecutive zero crossings in the same direction separate one bit from the next.

d) Consecutive zero crossings divide each bit into a first and a second, final part.

e) The decision as to whether such a bit represents a 0 or a 1 is determined by the time interval between the zero crossings.

2.1 The "1" bit, one bit

a) In a one bit, the first and second parts always have the same duration of 58 microseconds.

Duration of the partial one bit: t_{D1} **= 58 µs**

The duration of a one bit is therefore 116 µs (microseconds).

b) **Permissible tolerances of the partial one bit:**

for **the track signal** ± **3 µs,**

which means that the two parts of the transmitted one bit may each have a duration between 55 and 61 microseconds and, under load, may not differ by more than 3 microseconds within the tolerance range in the zero crossing range,

for **decoders** ± **6 µs,**

This means that decoders must recognize as valid one bits those received bits whose two parts each have a duration between 52 and 64 microseconds and which do not differ by more than 6 microseconds in the zero crossing range.

c) The deviations must be in the same direction for both parts (see also Figure 1).

[1)] The abbreviation is derived from Digital Command Control, the digital model railway control system based on the NMRA S9 standard.

[2)] Decoders in vehicles used on a track in any direction do not distinguish whether the first or second part of a bit has the positive polarity of the voltage.

[3]All time measurements are based on zero crossings, which are the midpoints between positive and negative signal amplitudes.

2.2 The "0" bit, zero bit

a) In a zero bit, the duration of the first and last parts between two zero crossings should be greater than or equal to 100 microseconds.

Duration of the partial zero bit: $t_{D0} \geq$ **100 µs**

b) In order to keep the DC components of the complete signal at zero, as with the one bits**,** both parts of the zero bit are **normally equal to each other. Equal** parts of the zero bit may be extended. [4)]

c) **Permissible tolerances of the zero bit:**

For **the track signal:** The duration of the partial zero bit must be between 95 and 9900 microseconds. The total duration of a zero bit must not exceed 12000 microseconds.

For **decoders:** A decoder must recognize bits received with a first or last part lasting between 90 and 10000 microseconds as valid zero bits (see also Figure 1).

3. Further technical data of the DCC track signal

The track signal, measured at the output of the control unit in the range from zero to the maximum permissible load, must meet the following conditions:

3.1 Steepness and ripple of zero crossings

3.1.1 Track signal

In the voltage range between ± 4 volts around zero crossing, the amount of voltage slope must be equal to or greater than 2.5 volts per microsecond.

Transmit slope (amount): $|S|_S|| \geq$ **2.5 V/µs** in the voltage range ± 4 V

In the zero-crossing range, the track signal may have a ripple of any amplitude, provided that the amplitude of this ripple is less than +/- 2 V. [5)]

3.1.2 Received DCC signal

For correct signal decoding, decoders must be able to detect zero crossings in the voltage range between ± 4 volts around the zero crossing with a voltage slope of 2 volts per microsecond or greater.

Reception slope (amount): $|S|_E|| \geq$ **2 V/µs** in the voltage range ± 4 V

A DCC decoder should recognize at least 95% of data packets addressed to it as valid according to NEM 671, even in the presence of noise and external interference and/or other signals with frequencies above 250 kHz. The total amplitude of these extraneous superimpositions must be less than 25% (1/4) of the amplitude of the DCC signal. [6)]

3.2 Internal interference

The exact form of the DCC signal must be designed in such a way that electromagnetic interference is minimized even when operating large systems in accordance with the DCC standard, so that the applicable CE or FCC regulations (for the USA and others) are complied with.

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[4]This generates a DC component of the DCC track signal for alternative control purposes, the polarity of which depends on an extended zero bit and the magnitude of which depends on the duration of the extension.

[5)] This standard specifies permitted non-DCC track signals for alternative control purposes and ensures that these signals are ignored by DCC decoders.

[6)] This measurement is made with a decoder connected to the track or a connecting line.

4. Power transmission and voltage limits

4.1 Power transmission

The typical power supply for traction vehicles and accessories, which must be ensured by all control devices and decoders, is provided by rectifiers in bridge circuits. To maintain this power supply, continuous transmission of the track signal is therefore required, except in certain cases for the repetition times defined in NEM 671· [7]

4.2 Voltage limits

a) The effective value of the DCC control signal measured at the track should not exceed the voltage specified in NEM 630 [8] by more than 2 volts. [9]

The amplitude of the digital control signal must not exceed ± 22 V.

b) The minimum peak value of the DCC control signal for operating the digital decoder is ± 8 V, measured at the track.

c) Decoders for nominal sizes N and smaller must have a DC voltage resistance of at least 24 V, measured at the track.

d) Decoders for nominal sizes > N must have a DC voltage resistance of at least 27 V, measured at the track.

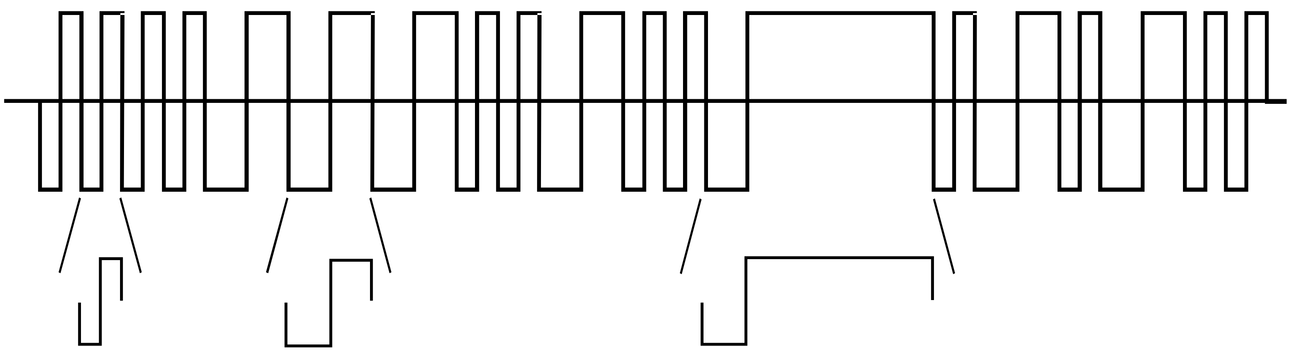

Figure 1: DCC representation

[7] Different methods of power supply are permitted, provided that the power modules are capable of generating the data packet described in NEM 671 and the decoders are capable of processing the track signal.

[8] The additional voltage serves to compensate for the voltage drop in the decoder to ensure that the maximum voltage specified in NEM 630 (Table 1) is available at the motor connections.

[9] All motors that are exposed to the DCC track signal for long periods of time must be designed to withstand the damaging effects of the higher amplitudes or have a sufficiently high impedance between 4 and 9 kHz to reduce the current to a normal operating level. These relationships are important for ironless bell-type armature motors or precision DC motors that have low load impedance, or for systems that use the DCC track signal with an amplitude greater than ± 18 V.