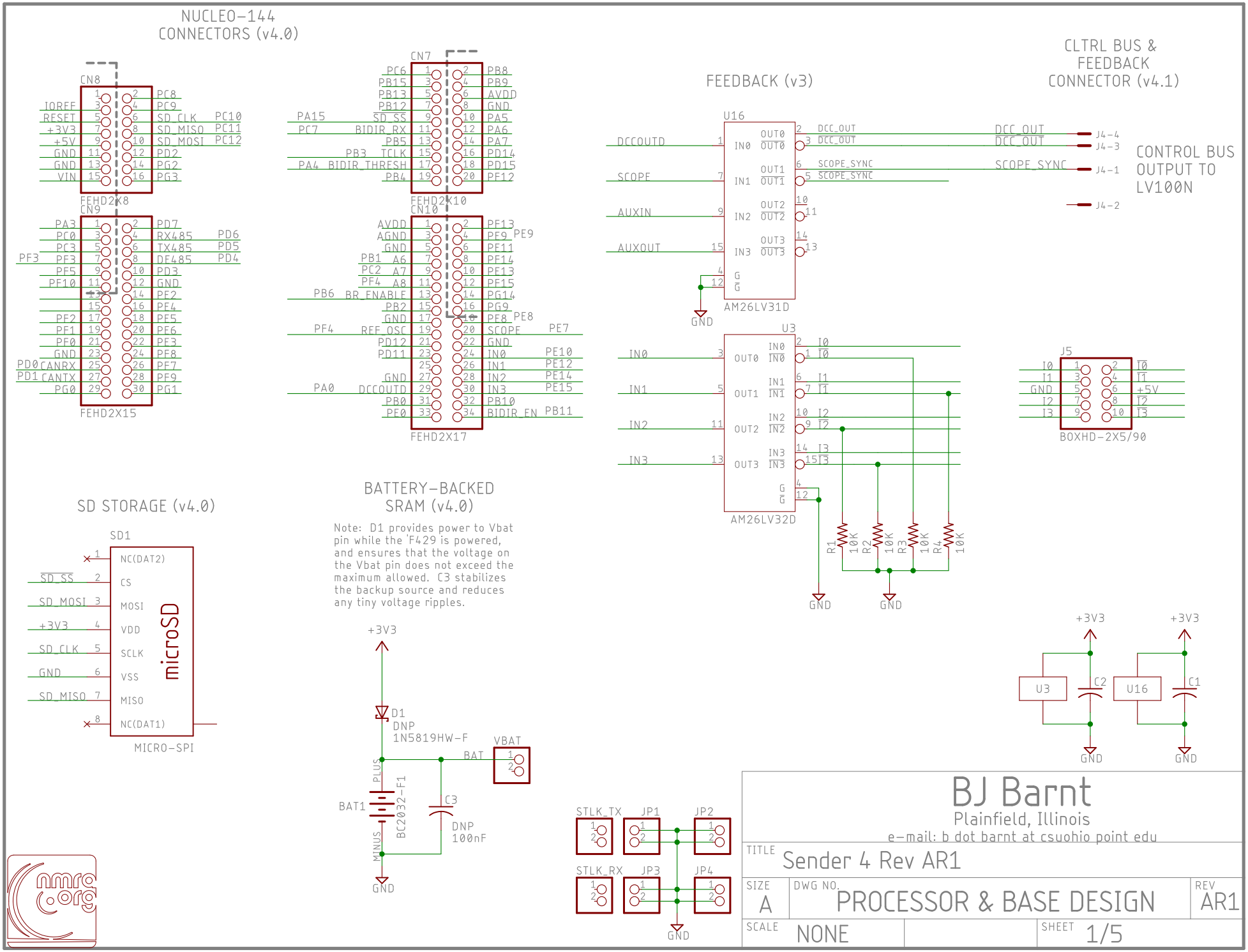
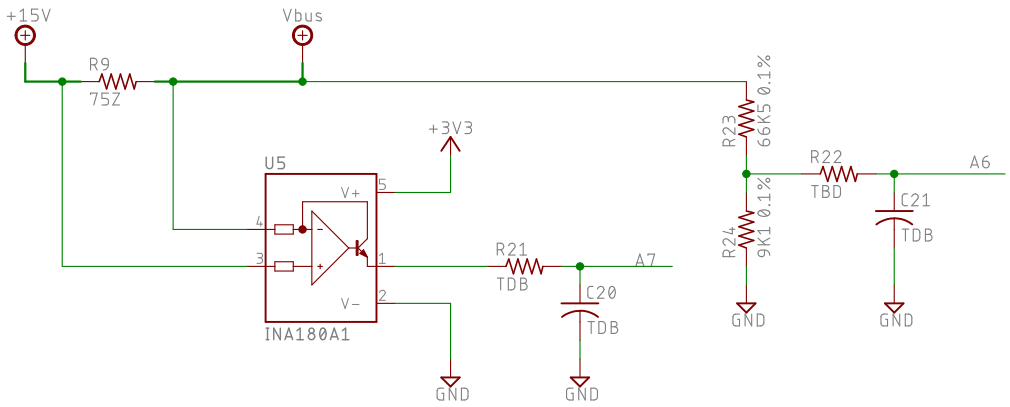

NUCLEO-144
CONNECTORS (v4.0)
CN8
FEHD2X8
CN9
FEHD2X15
CN7
FEHD2X10
CN10
FEHD2X17
FEEDBACK (v3)
U16
AM26LV31D
CLTRL BUS &
FEEDBACK
CONNECTOR (v4.1)
CONTROL BUS
OUTPUT TO
LV100N
U3
AM26LV32D
J5
BOXHD-2X5/90
SD STORAGE (v4.0)
SD1
MICRO-SPI
BATTERY-BACKED
SRAM (v4.0)
Note: D1 provides power to Vbat
pin while the 'F429 is powered,
and ensures that the voltage on
the Vbat pin does not exceed the
maximum allowed. C3 stabilizes
the backup source and reduces
any tiny voltage ripples.
D1
DNP
1N5819HW-F
BAT1
BC2032-F1
C3
DNP
100nF
VBAT
STLK_TX
STLK_RX
JP1
JP2
JP3
JP4
BJ Barnt
Plainfield, Illinois
e-mail: b dot barnt at csuohio point edu
Sender 4 Rev AR1
PROCESSOR & BASE DESIGN
A
AR1
NONE
1/5

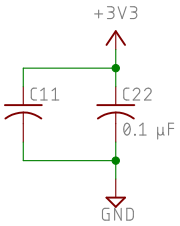


Calculations for Voltage Feedback:

Desired Range: 0–27v
A6 (max) = Vbus * (R24 / (R23+R24))
A6 (max) = Vbus * (9.1K / (66.5K+9.1K) = 3.25 V
A6 resolution = A6 (max) / 4096 = 3.25 / 4096 = 0.656 V

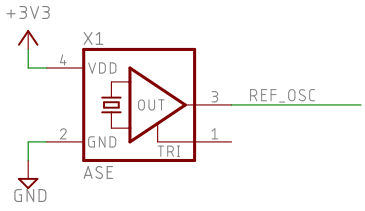
Calculations for Current Feedback:

Desired Range: 0–2 A
INA180A1 Gain: 20 V/V
Rsense < PDmax/ Imax * Imax
Rsense < 1/4 Ω
Vsp = Vs – 0.03 V » 3.27
Vsn = Vgnd + 0.005 » 0.005
Vsp > Imax * Rsense * Gain
Vsp > 2 * 0.075 * 20 » 3 [OK]
Vsn < Imin * Rsense * Gain
Vsn < 0 * 0.075 * 20 » 0 [OK]
A7 (max) = Imax * Rsense * Gain
A7 (max) = 2 * 0.075 * 20 » 3 V = 2 A
A7 resolution = A7 (max) / 4096 = 2 / 4096 = 0.5 mA per count



*FILTER CAPACITORS FOR: X1, IC1

REFERENCE CLOCK (v4.0)



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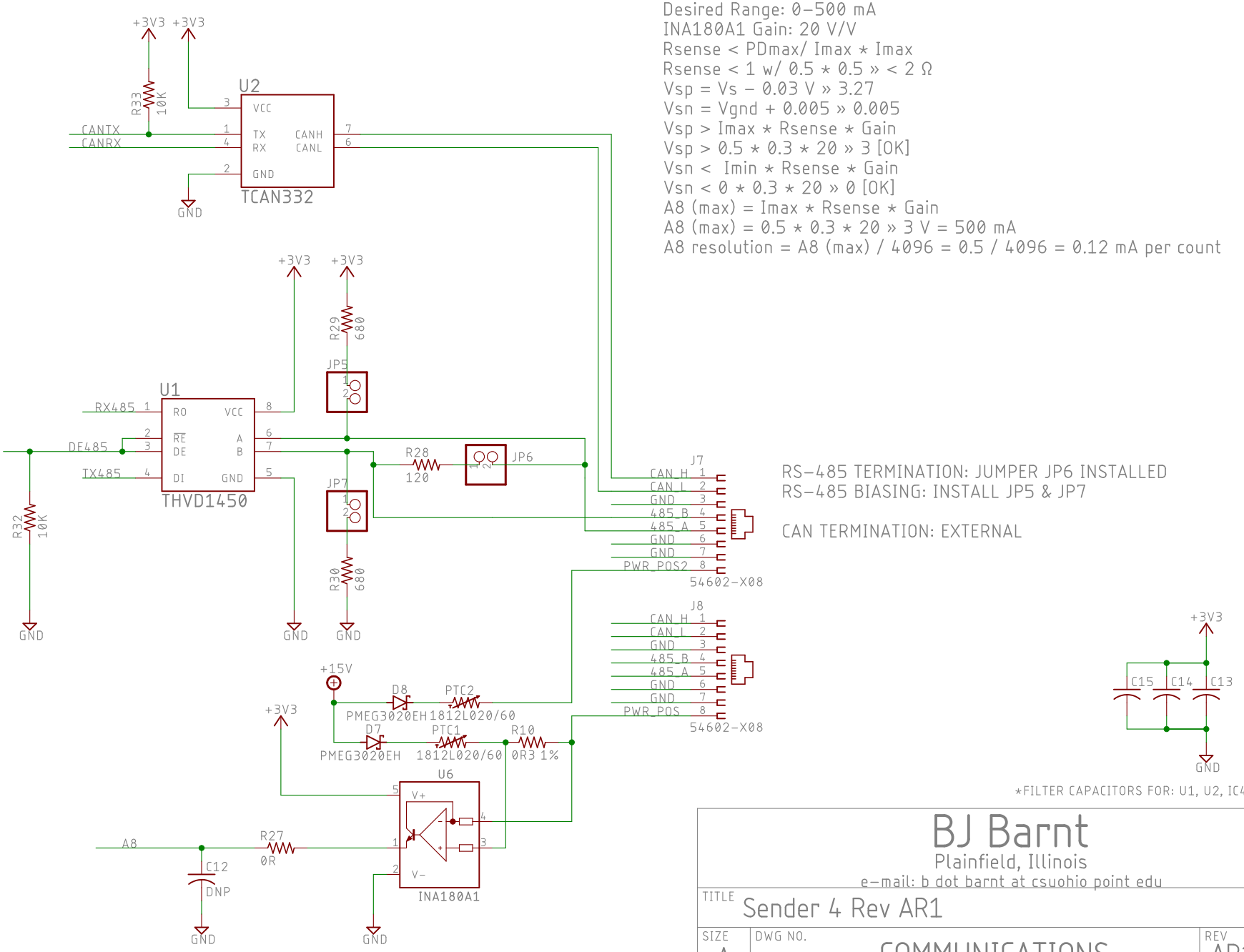
TITLE	Sender 4 Rev AR1	
SIZE A	DWG NO. SELF–TEST HARDWARE	REV AR1
SCALE NONE		SHEET 2/5

Calculations for CAN Current:

Desired Range: 0–500 mA
INA180A1 Gain: 20 V/V
Rsense < PDmax/ Imax * Imax
Rsense < 1 w/ 0.5 * 0.5 » < 2 Ω
Vsp = Vs – 0.03 V » 3.27
Vsn = Vgnd + 0.005 » 0.005
Vsp > Imax * Rsense * Gain
Vsp > 0.5 * 0.3 * 20 » 3 [OK]
Vsn < Imin * Rsense * Gain
Vsn < 0 * 0.3 * 20 » 0 [OK]
A8 (max) = Imax * Rsense * Gain
A8 (max) = 0.5 * 0.3 * 20 » 3 V = 500 mA
A8 resolution = A8 (max) / 4096 = 0.5 / 4096 = 0.12 mA per count



RS–485 TERMINATION: JUMPER JP6 INSTALLED
RS–485 BIASING: INSTALL JP5 & JP7

CAN TERMINATION: EXTERNAL

*FILTER CAPACITORS FOR: U1, U2, IC4

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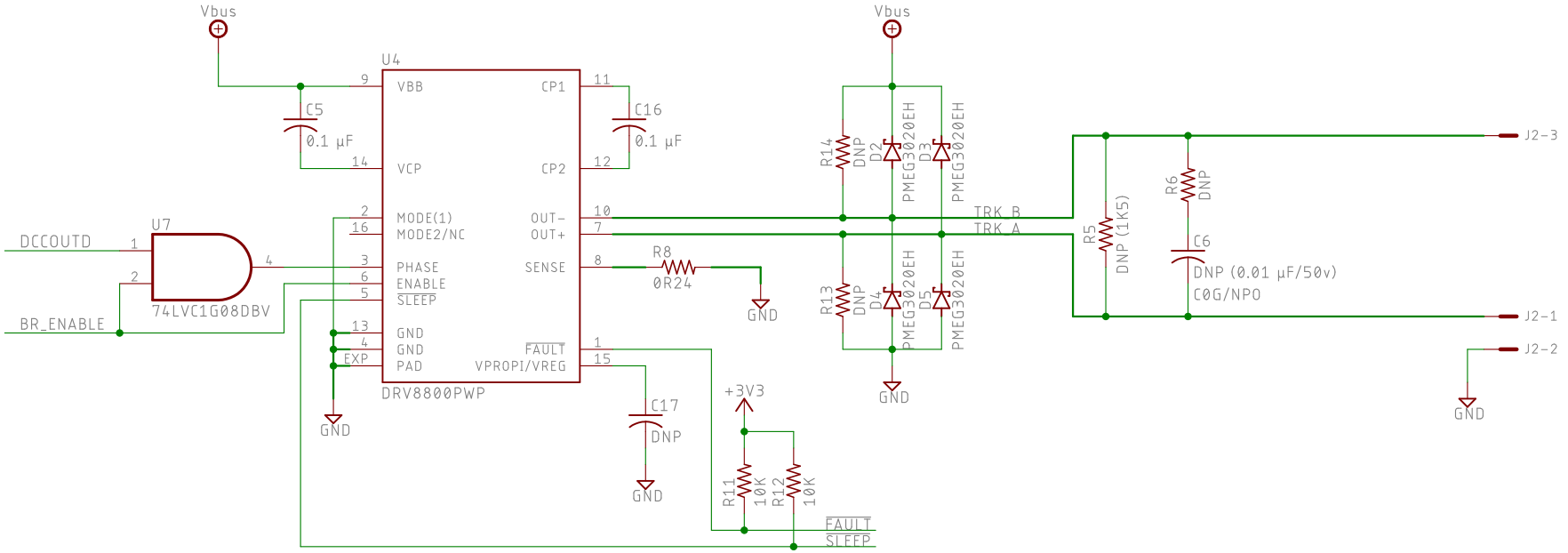
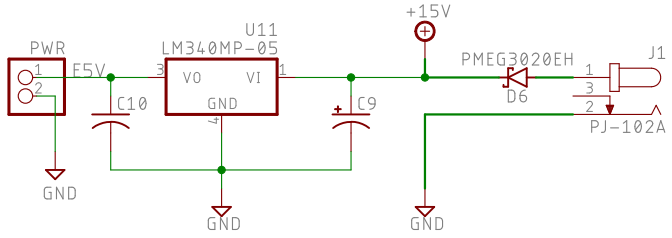
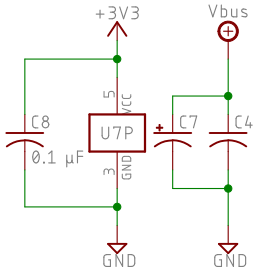
TITLE	Sender 4 Rev AR1	
SIZE A	DWG NO. COMMUNICATIONS	REV AR1
SCALE NONE		SHEET 3/5



POWER & REGULATOR (v4.1)





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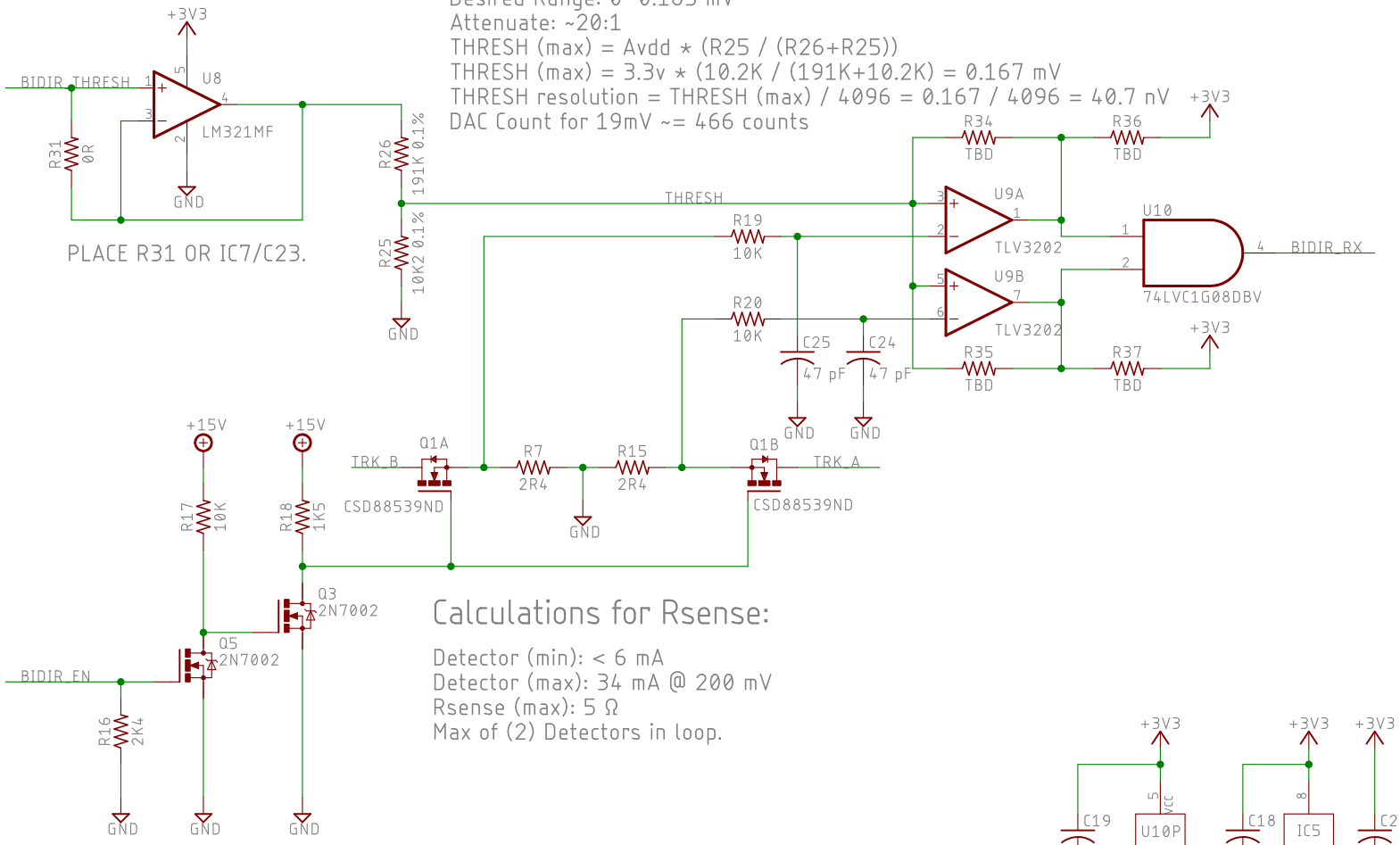
TITLE	Sender 4 Rev AR1	
SIZE A	DWG NO. POWER & PWR STATION	REV AR1
SCALE NONE		SHEET 4/5

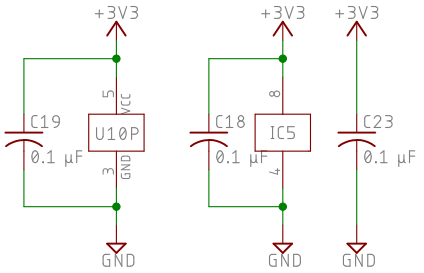
Calculations for Detector Threshold:

Desired Range: 0–0.165 mV
Attenuate: ~20:1
THRESH (max) = Avdd * (R25 / (R26+R25))
THRESH (max) = 3.3v * (10.2K / (191K+10.2K) = 0.167 mV
THRESH resolution = THRESH (max) / 4096 = 0.167 / 4096 = 40.7 nV
DAC Count for 19mV ~= 466 counts



Calculations for Rsense:

Detector (min): < 6 mA
Detector (max): 34 mA @ 200 mV
Rsense (max): 5 Ω
Max of (2) Detectors in loop.



*FILTER CAPACITORS FOR: IC5, IC6, IC7

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TITLE: Sender 4 Rev AR1		
SIZE: A	DWG NO.: BIDIRECTIONAL DETECTION	REV: AR1
SCALE: NONE		SHEET: 5/5