Standard	RCN-210 **DCC protocol** **Bit transmission**	RailCommunity
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Contents

1 General

1.1 Purpose of the standard

This standard describes bit transmission in the DCC protocol. It is based on the NMRA standard [S-9.1] and the MOROP standard [NEM 670]. DCC stands for *"Digital Command Control."* The packet structure based on this is described in [RCN-211].

1.2 Requirements

In order to comply with this standard, all times and levels specified for the respective device must be observed. To be less sensitive to interference, both polarities of the DCC track signal should be evaluated. In order not to interfere with other decoders, the decoder should avoid feedback to the DCC track signal and must have suitable countermeasures in place. A corresponding test procedure is currently being developed.

2 Bit representation

- Data transmission in the DCC protocol is carried out by transmitting a series of bits. A bit represents one of two states, which are called 1 and 0.
- A bit is represented by the voltage curve over time on the track (the DCC track signal).
- The DCC track signal consists of a sequence of transitions between two identical voltage levels of opposite polarity, called zero crossings.
- Two consecutive zero crossings in the same direction separate one bit from the next.
- The zero crossing in the opposite direction between them divides the bit into a first and second half.
- The decision as to whether such a bit represents a 0 or a 1 is determined by the time interval between the zero crossings.
- Since a vehicle can be positioned in any direction on the track, the receiver—hereinafter referred to as the decoder—does not know whether the first or second part of a bit has the positive polarity of the voltage.

2.1 The "1" bit, one bit

- In a single bit, the first and second halves must have a duration of 58 µs ± 3 µs.
- The duration of a one bit is therefore 116 µs ± 6 µs.
- Both bit halves must be of equal length with a tolerance of ± 3 µs.
- A decoder must accept a tolerance of ± 6 µs for one bit half.
- This means that a decoder must recognize as valid one bits those bits received whose two parts each have a duration between 52 µs and 64 µs.

2.2 The "0" bit, zero bit

- In a zero bit, the nominal duration of both halves is 100 µs.
- The minimum duration of half a zero bit is 95 µs.
- The maximum duration of half a zero bit is
  - 9900 µs if an analog locomotive is also to be controlled.
  - 116 µs to maintain compatibility with other protocols and protocol extensions.
- The total duration of a zero bit must not exceed 12000 µs.
- In order to keep the DC components of the complete DCC track signal at zero, as with the one bits, both parts of the zero bit are normally of equal length.
- In order to obtain a DC voltage component for alternative control purposes, only one half of a zero bit may be extended.
- A decoder must recognize such received bits as valid zero bits if their first or second part has a duration between 90 µs and 10000 µs.

All time measurements are based on zero crossings, which are the midpoints between positive and negative signal amplitudes.

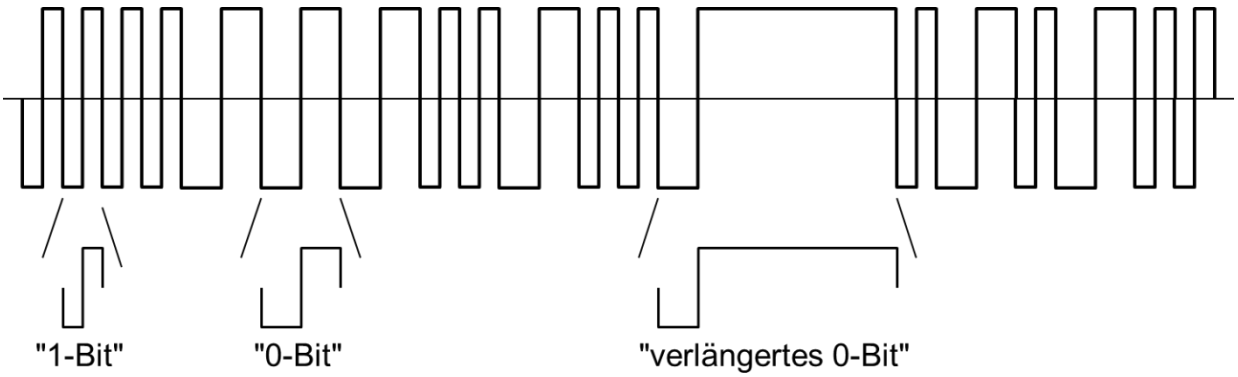

Figure 1: DCC bit representation

2.3 Polarity of the track signal

In principle, data is received independently of the polarity of the DCC track signal, i.e., regardless of how a vehicle is positioned on the track. However, there are applications that need to know the polarity of the DCC track signal. To ensure that all these applications interpret the polarity in the same way, the following is specified:

Phase position	First half-bit	Second half-bit
"positive"	V(R) > V(L)	V(R) < V(L)
"negative"	V(R) < V(L)	V(R) > V(L)

V(R) is the voltage on the right rail (red cable) V(L) is the voltage on the left rail (black cable)

This means that the phase angle corresponds to the voltage on the right rail relative to the left rail in the first half of a bit.

3 Further technical data for the DCC track signal

The DCC track signal, measured in the range from zero to maximum permissible load, must meet the following conditions:

- The DCC track signal must change at zero crossings in the voltage range from -4 V to +4 V at 2.5 V/µs or faster.
- The DCC track signal may have a ripple of 20% of the total amplitude in the zero-crossing range.

Decoders must recognize at least 95% of data packets addressed to them as valid under the following conditions according to [RCN-211] and [RCN-212] or [RCN-213]:

- Zero crossings with a steepness of 2 V/µs or steeper in the voltage range −4 V to +4 V.
- Noise, interference, and/or other signals whose total amplitude is less than 25% of the amplitude of the DCC track signal.

4 Energy transmission and voltage limits

4.1 Energy transmission

Since the DCC track signal also serves to supply power to the traction vehicles and accessories, continuous transmission of the bits is necessary to maintain this power supply.

4.2 Voltage limits

a) The effective value of the DCC track signal measured on the track should not exceed the voltage specified in [NEM 630] by more than 2 V. The additional 2 V serve to compensate for the voltage drop in the decoder to ensure that the maximum voltage specified in NEM 630 (Table 1).

b) The amplitude of the DCC track signal must not exceed ± 22 V.

c) The minimum peak value of the DCC track signal for operating the decoder is ± 8 V under rated load, with a load of 100 ohms at one output (or lower load if the decoder can supply less current) ± 7 V, measured at the track connections.

d) Decoders for nominal sizes N and smaller must have a DC voltage resistance of at least 24 V, measured at the track.

e) Decoders for nominal sizes > N must have a DC voltage resistance of at least 27 V, measured at the track.

5 Summary of technical data

(Voltages are given as the amplitude of the square wave signal)

	Output Control center	**Track output**	**Decoder input**
Half of a "1" bit nominal	58 µs		
Half of a "1" bit minimum	56 µs	55 µs	52 µs
Half of a "1" bit maximum	60 µs	61 µs	64 µs
Half of a "0" bit nominal	100 µs		
Half of a "0" bit minimum	97 µs	95 µs	90 µs
Half of a "0" bit maximum (if an analog locomotive is also to be controlled)	9898 µs	9900 µs	10000 µs
Half of a "0" bit maximum (compatibility with other protocols and protocol extensions)	114 µs	116 µs	119 µs
Slope in the range ± 4 V		≥ 2.5 V/µs	≥ 2.0 V/µs
Interference on the DCC track signal		≤ 0.2 U_{max}	<

			0.25 U_{max}
	Output Central	**Track output**	**Decoder input**
Recommended voltage range for nominal sizes Z or smaller		9 to 12 V	
Recommended voltage range for nominal sizes N and TT		14 to 16 V	
Recommended voltage range for nominal sizes H0 to 0		15 to 18 V	
Recommended voltage range for nominal size 1 and larger		19 to 22 V	
|**Voltage**| maximum (U_{max}) for nominal size ≤ N		≤ 22 V	≤ 24 V
|**Voltage**| maximum (U_{max}) for nominal size > N		≤ 22 V	≤ 27 V
|**Voltage**| minimum (U_{min}) under rated load		≥ 9 V	≥ 8 V
|**Voltage**| minimum (U_{min}) at a load of only 60 mA for the purpose of detecting data reception. Motor controllability is not required.			≥ 7 V

Annex A: References to other standards

A.1 Normative references

No other standards need to be complied with in order to meet this standard.

A.2 Informative references

The standards and documents listed here are for informational purposes only and are not part of this standard.

[RCN-211] RCN-211 DCC packet structure

[RCN-212] RCN-212 DCC Operating Commands for Vehicle Decoders

[RCN-213] RCN-213 DCC Operating Commands for Accessory Decoders [S-9.1] NMRA: S-9.1 DCC Electrical Standard

[NEM 630] MOROP: NEM 630 DC Train Control - Electrical Characteristics [NEM 670] MOROP: NEM 670 Digital Control Signal DCC Bit Representation

Appendix B: History

Date	Chapter	Changes since the previous version
Dec	2.1 5	Definition of equal length of bit halves Definition of load conditions at 7 V
Aug. 11	4.2 5	Second lower voltage limit at minimum load Correction: "with ≥ 100 kHz" removed. Addition of second lower voltage limit.
Dec. 2, 2018	1.2 2.3 3 5	Requirements for interference immunity and interference suppression New: Polarity of the DCC track signal Requirement: interference frequency greater than 100 kHz removed Correction in the table: "Half of a ...
May 3, 2013	All	First version