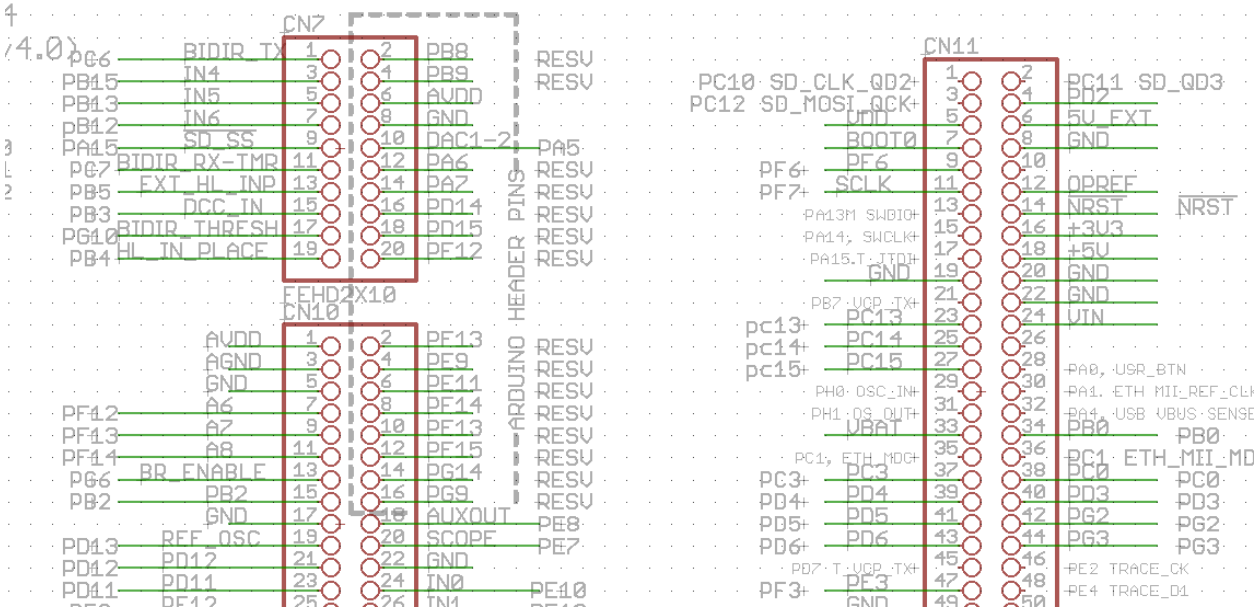
Ground Rules:

1. All Arduino Shield pins are reserved as far as possible.
2. All Nucleo internal connections on CN11 & CN12 are labeled, but have no green network wire on th schematic.
3. All function inputs & SUSI interface(s) are on a TBD mezzanine board to the right of the Nucleo. The Opto-isolators for functions & SUSI connections will be on this board. The connections to the processor are defined.



The network (wire) names are above the wire. To the left or right are the STM32 pin name(s). If the section above, CN7 pin 1 is port pin PC6, which is wired to the Bidirectional Transmit connection. On CN11, pint 1 is connected to pin PC10 and is used for the SD card D2 network. This particular connection is on a different Nucleo pin and is labeled so it does not get used again.
Nucleo connections are on CN7, CN8, CN9 & CN10. They *may* be duplicated on CN11 and CN12.

While checking the schematic, please verify that there are not duplicate green network wires between CN8-10 and CN11 & CN12.

a. BiDiCom cutout hardware interlock **Noted; in progress**
b. Separate edge connectors for track-out and track in as well as any aux features**. In place already**
c. Onboard jumpers to connect track out to track in? **use external jumpers to prevent errors in testing.**
d. Onboard LEDs jumper configurable to unused GPIO pins **Needs discussion**
e. BiDiCom decoder side circuit tx connected to PC6 (UART6) **Done**
f. MicroSD socket connected to SDHC pins PC8-12 **Done**
g. external pull up resistors to the SDHC interface **Done**
h. Remove pull up resistor on SDHC clock pin PC12 **Not done per g. above**
i. DAC output on pins PA4 & PA5. Using PA5 for BIDI_THRESH access to both. **DAC output reserved for Arduno Shield.**
j. Replace 6N167 Opto Isolator with H11 can run at 3.3v **Need discussion; no 6N167 parts**
k. 2 SPI channels for SUSI testing (main & secondary) SUSI Half duplex **Done SPI5 assigned**
unidirectional or bidirectional interface
i. need clock & one data line. 563 has 6 SPI channels, only 4 are available **Need discussion. Unclear.**
ii. MOSI is the only data line used in 2-wire mode. The data line can
rolls (input or output) via software configuration, so we only need MOSI. swap **unclear**
l. SUSI requires a few series resistors (470Ω) as well as pullups per S-9.4.1 **on mezz board**

NUCLEO-144 CONNECTORS (v4.0)

ARDUINO HEADER PINS

CN8 — FEHD2X8

	1	2	SD_QD0 — PC8
IOREF	3	4	SD_QD1 — PC9
RESET	5	6	SD_CLK_QD2 — PC10
+3V3	7	8	SD_MISO_QD3 — PC11
+5V	9	10	SD_MOSI_QCK — PC12
GND	11	12	IN9 — PD2
GND	13	14	IN10 — PG2
VIN	15	16	IN11 — PG3

CN9 — FEHD2X15

RESV — PA3	1	2	IN12 — PD7
RESV — PC0	3	4	RX485 — PD6
RESV — PC3	5	6	TX485 — PD5
RESV — PF3	7	8	DE485 — PD4
RESV — PF5	9	10	PD3 — PD3
RESV — PF10	11	12	GND
PB2 — PB2	13	14	PF2 — PE2
PE9 — PF9	15	16	PF4 — PE4
PF2 — PF2	17	18	PF5 — PE5
PF1 — PF1	19	20	PF6 — PE6
PF0 — PF0	21	22	PF3 — PE3
GND	23	24	PF8 — PD8
PD0 — CANRX	25	26	PF7 — PF7
PD1 — CANTX	27	28	PF9 — PD9
PG0 — PG0	29	30	PG1 — PG1

CN7 — FEHD2X10

PC6 — BIDIR_TX	1	2	PB8 — RESV
PB15 — IN4	3	4	PB9 — RESV
PB13 — IN5	5	6	AVDD
PB12 — IN6	7	8	GND
PA15 — SD_SS	9	10	DAC1-2 — PA5
PC7 — BIDIR_RX-TMR	11	12	PA6 — RESV
PB5 — EXT_HL_INP	13	14	PA7 — RESV
PB3 — DCC_IN	15	16	PD14 — RESV
PG10 — BIDIR_THRESH	17	18	PD15 — RESV
PB4 — HL_IN_PLACE	19	20	PF12 — RESV

CN10 — FEHD2X17

AVDD	1	2	PF13 — RESV
AGND	3	4	PF9 — RESV
GND	5	6	PF11 — RESV
A6	7	8	PF14 — RESV
PF12 — A7	9	10	PF13 — RESV
PF13 — A8	11	12	PF15 — RESV
PF14 — BR_ENABLE	13	14	PG14 — RESV
PG6 — PB2	15	16	PG9 — RESV
PB2 — GND	17	18	AUXOUT — PE8
PD13 — REF_OSC	19	20	SCOPE — PE7
PD12 — PD12	21	22	GND
PD11 — PD11	23	24	IN0 — PE10
PE2 — PE12	25	26	IN1 — PE12
GND	27	28	IN2 — PE6
PA0 — DCCOUTD	29	30	IN3 — PE15
PB0 — SD_QCMD	31	32	PB10 — PB10
PE0 — PE0	33	34	BIDIR_EN — PA3

ARDUINO HEADER PINS

CN11

PC10 SD_CLK_QD2	1	2	PC11 SD_QD3
PC12 SD_MOSI_QCK	3	4	PD2
VDD	5	6	5V_EXT
BOOT0	7	8	GND
PF6 — PF6	9	10	
PF7 — SCLK	11	12	OPREF
PA13M SWDIO	13	14	NRST — NRST
PA14, SWCLK	15	16	+3V3
PA15.T_JTDI	17	18	+5V
GND	19	20	GND
PB7 UCP_TX	21	22	GND
PC13 — pc13	23	24	VIN
PC14 — pc14	25	26	
PC15 — pc15	27	28	PA0, USR_BTN
PH0 OSC_IN	29	30	PA1. ETH MII_REF_CLK
PH1 OS_OUT	31	32	PA4, USB VBUS SENSE
VBAT	33	34	PB0 — PB0
PC1, ETH_MDC	35	36	PC1 ETH_MII_MDC
PC3 — PC3	37	38	PC0 — PC0
PD4 — PD4	39	40	PD3 — PD3
PD5 — PD5	41	42	PG2 — PG2
PD6 — PD6	43	44	PG3 — PG3
PD7 T_UCP_TX	45	46	PE2 TRACE_CK
PF3 — PF3	47	48	PE4 TRACE_D1
GND	49	50	PE5 TRACE_D1
	51	52	PF2 — PF2
PF0 — PF0	53	54	SDAT_IN — PF8
PD1 — PD1	55	56	SDAT_OUT — PF9
PD0 — PD0	57	58	PG1 — PG1
PG0 — PG0	59	60	GND
	61	62	PE6 TRACE_D3
PG9 — PG9	63	64	PG15 — PG15
PG12 — PG12	65	66	PG10 — PG10
PG13 ETH_MII_TX_EN	67	68	PG13 MII_TXD0
PD9 UART3_RX	69	70	PG11 ETG MII_TX_EN

CN12

PC9	1	2	PC8
PB8 — PB8	3	4	PC6
PB9 — PB9	5	6	PC5 MII_RXD1
VREFP	7	8	5V_STLK — 5V_STLK
GND	9	10	PD8 USART3_TX
PA5 — PA5	11	12	PA12 USB_FS_P
PA6 — PA6	13	14	PA11 USB_FS_N
PA7 ETH_MII_CRS_DV	15	16	IN12 — PB12
PB6 UART1_TX	17	18	NC — NC
PC7 — PC7	19	20	GND — GND
PA9 UUPD_DBN	21	22	IN13 — PB2
PA8 — PA8	23	24	IN14 — PB1
PB10 — PB10	25	26	PB15 MII_TXD1
PB4 — PB4	27	28	PB14 UPD_CC2
PB5 — PB5	29	30	PB13UPD_CC1
PB3 SWO — PA10	31	32	AGND — AGND
PA10	33	34	PC4 MII_RXD0
PA2 ETH_MII_MDIO	35	36	IN17 — PF5
PA3 — PA3	37	38	IN16 — PF4
GND	39	40	PE8 — PE8
PD13 — PD13	41	42	PE10 — PF10
PD12 — PD12	43	44	PE7 — PE7
PD11 — PD11	45	46	PD14 — PD14
PE10 — PE10	47	48	PD15 — PD15
PE12 — PE12	49	50	PF14 — PF14
PE14 — PE14	51	52	PE9 — PE9
PE15 — PE15	53	54	GND — GND
PE13 — PE13	55	56	PE11 — PE11
PF13 — PF13	57	58	PF3 — PF3
PF12 — PF12	59	60	PF15 — PF15
PG14 — PG14	61	62	PF11 — PF11
GND	63	64	PE0 — PE0
PD10 — PD10	65	66	PG8 — PG8
PG7 UPD_FLT	67	68	PG5 — PG5
PG4 — PG4	69	70	PG6 — PG6

SD STORAGE (v4.0)

microSD — MICRO-SD

	1	NC(DAT2) — SD2
SD_SS	2	CS(DAT3) — SD_SS
SD_MOSI_QCK	3	MOSI(CMD) — SD_MOSI
+3V3	4	VDD
SD_CLK_QD2	5	SCLK(CLK) — SD_CLK
GND	6	VSS
SD_MISO_QD3	7	MISO(DAT0) — SD_MISO
	8	NC(DAT1)

microSD — MICRO-SD

SD_CLK_QD2	1	NC(DAT2) — SD1
SD_MISO_QD3	2	CS(DAT3)
SD_QCMD	3	MOSI(CMD)
+3V3	4	VDD
SD_MOSI_QCK	5	SCLK(CLK)
GND	6	VSS
QD0	7	MISO(DAT0) — MICRO-SD
QD1	8	NC(DAT1)

QD1 — R40 10K — QD0 — R41 10K — SD_CLK_QD2 — R42 10K — SD_MISO_QD3 — R43 10K — SD_QCMD — R44 10K — SD_MOSI_QCK — 10K — +3V3

MODIFIED PER KK 21-FEB-25.

SJ1: DAC1-2 1 — 2 DAC

BATTERY-BACKED SRAM (v4.0)

Note: D1 provides power to Vbat pin while the 'F429 is powered, and ensures that the voltage on the Vbat pin does not exceed the maximum allowed. C3 stabilizes the backup source and reduces any tiny voltage ripples.

+3V3 — D1 DNP 1N5819HW-F — VBAT — BAT — PLUS — BAT1 BC2032-F1 — MINUS — GND

C3 DNP 100nF

+3V3 — R45 22K — X3 — HL_IN_PLACE 4 — EXT_HL_IN 5 — KLBR1

STLK_TX JP1 JP2

STLK_RX JP3 JP4

GND

J3 BOXHD-2X5

(F0f) IN4	1	2	IN5 (F0r)
(F1) IN6	3	4	IN7 (F2)
GND	5	6	+3V3
(F3) IN8	7	8	IN9 (F4)
(F5) IN10	9	10	IN11 (F6)

J6 BOXHD-2X5

(F7) IN12	1	2	IN13 (F8)
(F9) IN14	3	4	IN15 (F10)
GND	5	6	+3V3
(F11) IN16	7	8	IN17 (F12)
	9	10	

J4 BOXHD-2X5

(SUSI) SDAT_IN	1	2	SCLK (SUSI)
(SUSI) SDAT_OUT	3	4	DAC
GND	5	6	F5V
	7	8	
	9	10	

ADDED PER DCCWG MEETING 14-FEB-25.

JP8: TRK_A 1 2 — JP9: TRK_B 1 2

+3V3 — U3 — C2 — GND; +3V3 — U12 — C1 — GND

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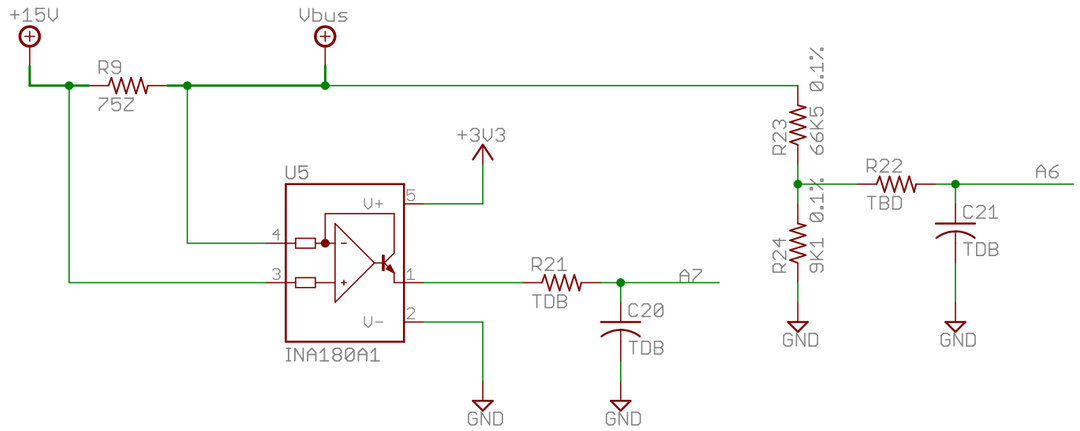
TITLE: Sender4p83 v7

SIZE: A | DWG NO.: PROCESSOR & BASE DESIGN | REV: R2

SCALE: NONE | SHEET: 1/6

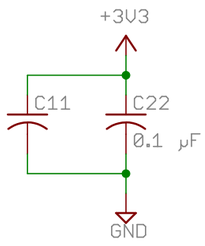
Calculations for Voltage Feedback:

Desired Range: 0-27v
A6 (max) = Vbus * (R24 / (R23+R24))
A6 (max) = Vbus * (9.1K / (66.5K+9.1K) = 3.25 V
A6 resolution = A6 (max) / 4096 = 3.25 / 4096 = 0.656 V



Calculations for Current Feedback:

Desired Range: 0-2 A
INA180A1 Gain: 20 V/V
Rsense < PDmax/ Imax * Imax
Rsense < 1/4 Ω
Vsp = Vs - 0.03 V » 3.27
Vsn = Vgnd + 0.005 » 0.005
Vsp > Imax * Rsense * Gain
Vsp > 2 * 0.075 * 20 » 3 [OK]
Vsn < Imin * Rsense * Gain
Vsn < 0 * 0.075 * 20 » 0 [OK]
A7 (max) = Imax * Rsense * Gain
A7 (max) = 2 * 0.075 * 20 » 3 V = 2 A
A7 resolution = A7 (max) / 4096 = 2 / 4096 = 0.5 mA per count

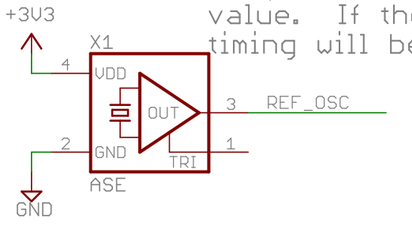


*FILTER CAPACITORS FOR: X1, IC1

Testing with X1:

X1 is used to validate the microprocessor timing. Measure the number of pulses during a calculated amount of time, and verify it against the theoretical value. If the STM32 clock is accurate, then all of the timing will be correct.

REFERENCE CLOCK (v4.0)



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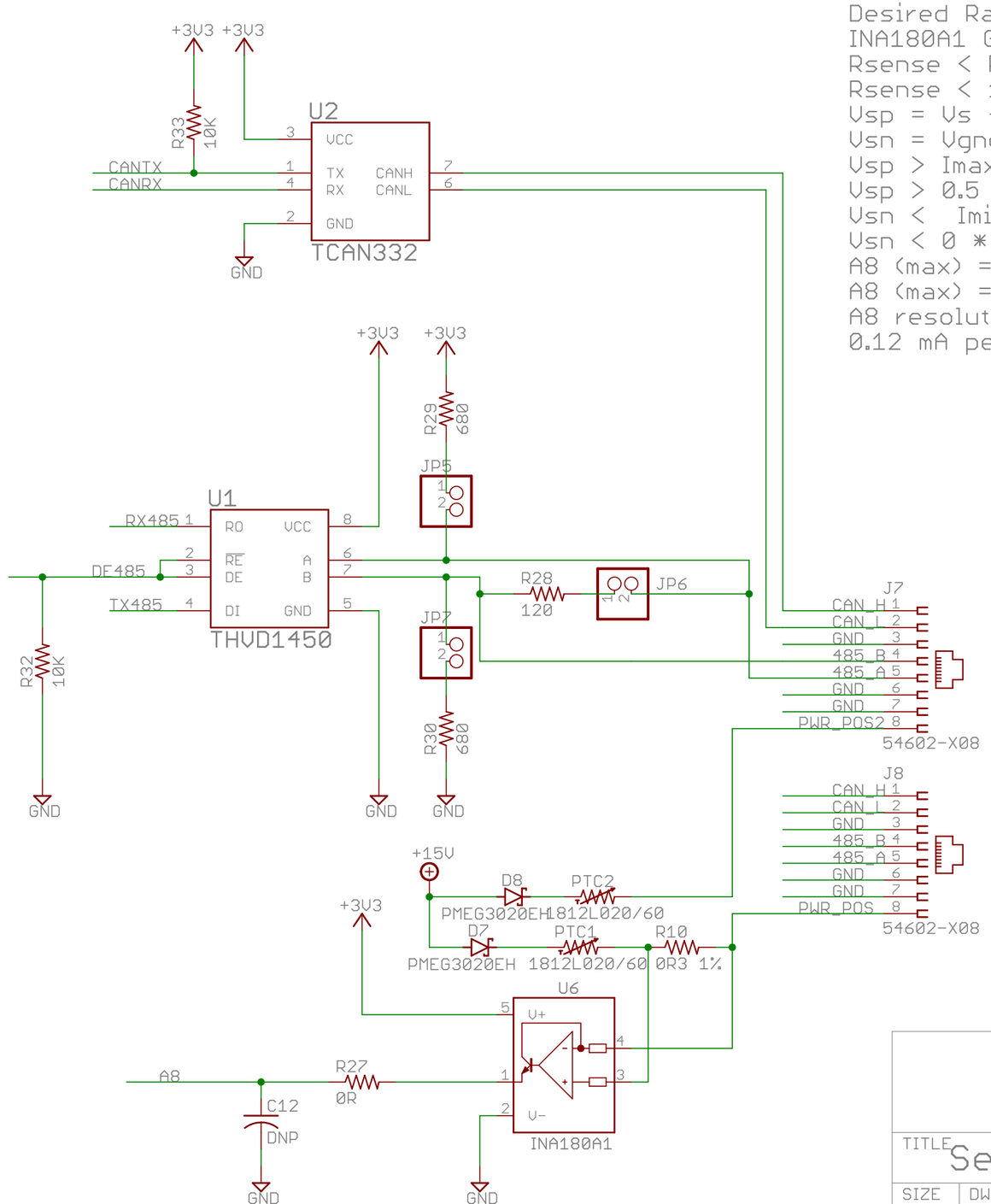
TITLE: Sender4p83 v7		
SIZE: A	DWG NO.: SELF-TEST HARDWARE	REV: AR2
SCALE: NONE		SHEET: 2/6



Calculations for CAN Current:

Desired Range: 0-500 mA
INA180A1 Gain: 20 V/V
Rsense < PDmax/ Imax * Imax
Rsense < 1 w/ 0.5 * 0.5 » < 2 Ω
Vsp = Vs - 0.03 V » 3.27
Vsn = Vgnd + 0.005 » 0.005
Vsp > Imax * Rsense * Gain
Vsp > 0.5 * 0.3 * 20 » 3 [OK]
Vsn < Imin * Rsense * Gain
Vsn < 0 * 0.3 * 20 » 0 [OK]
A8 (max) = Imax * Rsense * Gain
A8 (max) = 0.5 * 0.3 * 20 » 3 V = 500 mA
A8 resolution = A8 (max) / 4096 = 0.5 / 4096 = 0.12 mA per count

RS-485 TERMINATION: JUMPER JP6 INSTALLED
RS-485 BIASING: INSTALL JP5 & JP7

CAN TERMINATION: EXTERNAL

*FILTER CAPACITORS FOR: U1, U2, IC4

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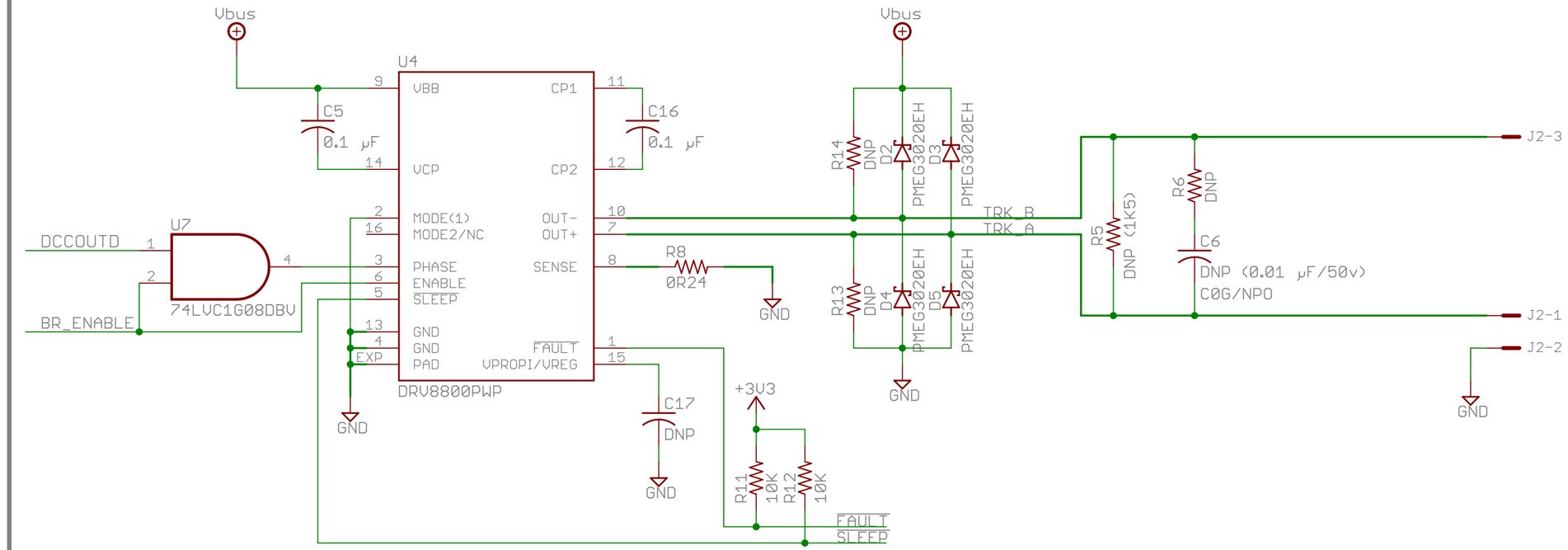
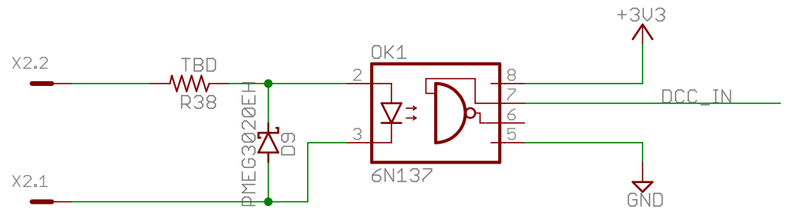
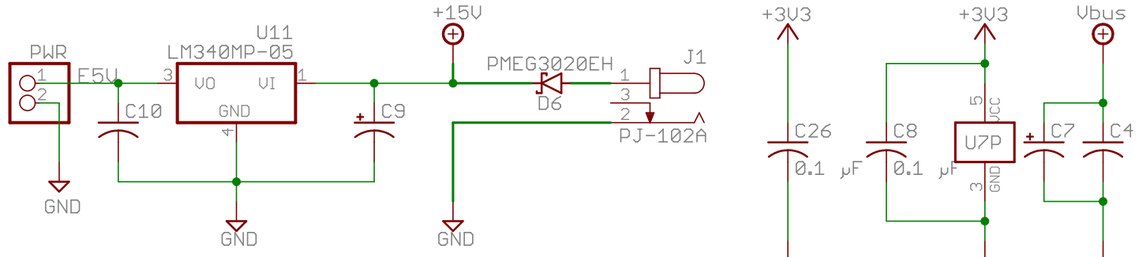
TITLE: Sender4p83 v7		
SIZE: A	DWG NO.: COMMUNICATIONS	REV: AR2
SCALE: NONE		SHEET: 3/6





POWER & REGULATOR (v4.1)



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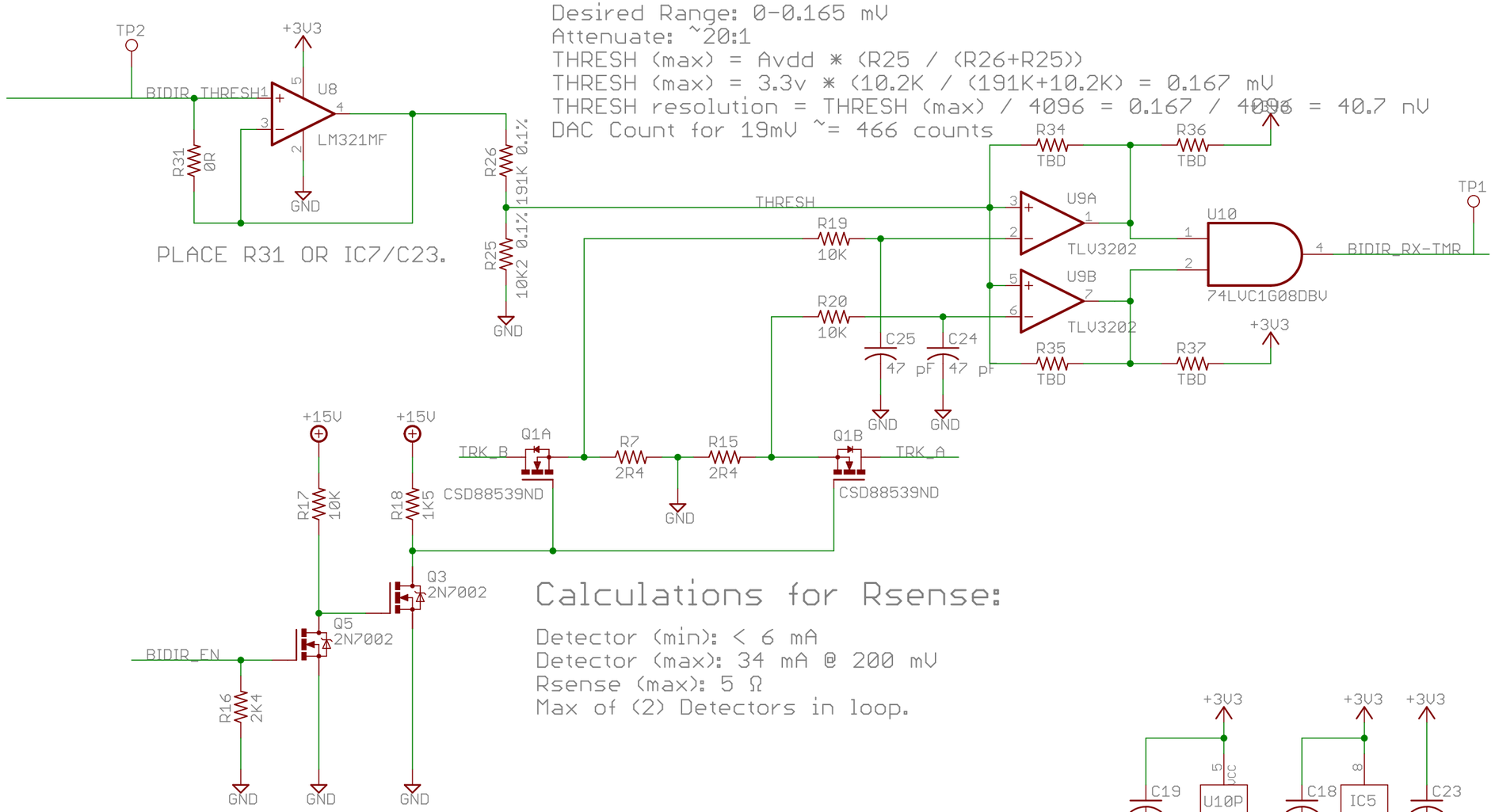
TITLE: Sender4p83 v7		
SIZE: A	DWG NO.: POWER & PWR STATION	REV: AR2
SCALE: NONE		SHEET: 4/6

Calculations for Detector Threshold:

Desired Range: 0-0.165 mV
Attenuate: ~20:1
THRESH (max) = Avdd * (R25 / (R26+R25))
THRESH (max) = 3.3v * (10.2K / (191K+10.2K) = 0.167 mV
THRESH resolution = THRESH (max) / 4096 = 0.167 / 4096 = 40.7 nV
DAC Count for 19mV ~= 466 counts



Calculations for Rsense:

Detector (min): < 6 mA
Detector (max): 34 mA @ 200 mV
Rsense (max): 5 Ω
Max of (2) Detectors in loop.

*FILTER CAPACITORS FOR: IC5, IC6, IC7

BRIEF THEORY OF OPERATION

DURING THE CUTOUT, THE H-BRIDGE IS DISABLED (BR_ENABLE = 0), AND THE DETECTOR IS ENABLED (BIDIR_EN = 1). Q5 IS TURNED ON, Q5 IS TURNED OFF, AND Q1A & Q1B ARE TURNED ON.

BIDIR CURRENT FLOWS FROM THE DECODER VIA TRK_A THROUGH R 15 & R7 TO TRK_B AND BACK TO THE DECODER, OR VICE-VERSA.

THE VOLTAAGE DROP ACROSS R15/R7 IS FILTERED BY R19/C25 AND R20/C24 AND FED TO U9. THE DAC OUTPUT OF THE MICROPROCESSOR SETS THE DESIRED SENSE THRESHOLD VOLTAGE.

THE OUTPUTS OF U9 ARE FED INTO U10; WHEN EITHER IS LOW, U10'S OUTPUT IS LOW. THAT SIGNAL IS FED BACK TO THE MICROPROCESSOR UART6, AND A TBD TIMER PIN.

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TITLE: Sender4p83 v7		
SIZE: A	DWG NO.: BIDIRECTIONAL DETECTION	REV: NR2
SCALE: NONE		SHEET: 5/6

To Do: Connect BIDIR_RX signal to a timer pin to measure the bit timing

CONTROL BUS & FEEDBACK CONNECTORS (v4.1)
PINOUT REVISED (v4.2)

FEEDBACK (v3)

U12

DCCOUTD 1
SCOPE 7
9
AUXOUT 15
4
12

IN0 OUT0
IN1 OUT1
IN2 OUT2
IN3 OUT3
G
G

AM26LV31D

GND

2 DCC_OUT
3 DCC_OUT
6 SCOPE_SYNC
5 SCOPE_SYNC
10
11
14 AUX_OUT
13

DCC_OUT J10-3
DCC_OUT J10-2
SCOPE_SYNC J10-1
AUX_OUT J10-4

CONTROL BUS OUTPUT TO LV100N

U13

IN0 3
IN1 5
IN2 11
IN3 13

IN0 OUT0
IN1 OUT1
IN2 OUT2
IN3 OUT3
G
G

AM26LV32D

2 I0
1 I0
6 I1
7 I1
10 I2
9 I2
14 I3
15 I3
4
12

GND

R46 10K
R47 10K
R48 10K
R49 10K

GND

J9

I0 1 2 I0
I1 3 4 I1
GND 5 6 +5V
I2 7 8 I2
I3 9 10 I3

BOXHD-2X5/90

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TITLE: Sender4p83 v7		
SIZE: A	DWG NO.: CONTRØLBUS & FEEDBACK	REV: AR2
SCALE: NONE		SHEET: 6/6