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1 General

Communication from a Digital Command Station to a Digital Decoder is accomplished by transmitting a series of bits that convey instructions. A bit is a signal which represents one of two conditions, which we will call "1" and "0". This portion of the standard covers the electrical characteristics of the digital command control signal that encodes these bits.

Please refer to Tables 2.1, 2.2 and 2.3 for definition and numerical values of parameters used throughout this document.

1.1 Introduction and Intended Use (Informative)

1.2 References

This standard should be interpreted in the context of the following NMRA Standards, Technical Notes, and Technical Information.

1.2.1 Normative

- S-9
- S-9.2

1.2.2 Informative

- None

1.3 Terminology

Term	Definition
Vehicle	Mobile model railroad device. This includes locomotives and other rolling stock.
Decoder (mobile)	DCC receiver for controlling vehicle animation.
Accessory Decoder	DCC receiver for controlling accessories.
Accessories	Fixed model railroad device. This includes turnouts, lights, signals and other devices not on the rails.
Power Station	A device that amplifies the low current DCC electrical signals transmitted by a Command Station for the purpose of providing high current DCC signals with sufficient power to operate model trains and any accessory decoders that are connected to the track. The power station may be a separate device or may be combined with the command station and/or throttle. Sometimes referred to as a booster.

2 Technique for Encoding Bits

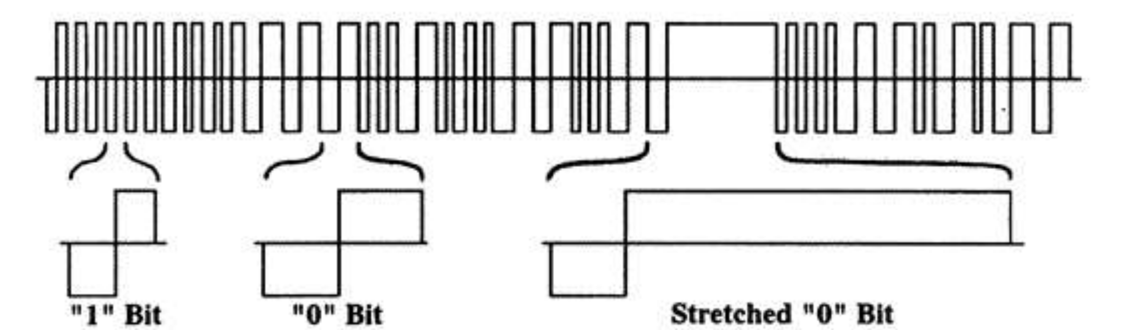
The NMRA baseline digital command control signal consists of a stream of transitions between two equal voltage levels that have opposite polarity[1]. Alternate transitions separate one bit from the next. The remaining transitions divide each bit into a first part and a last part. Digital Command Stations shall encode bits within this digital command control stream of transitions by varying the duration of the parts of the bits, or frequency of the transitions.

In a "1" bit, the first and last part of a bit shall have the same nominal duration, and that duration shall be **t1**[2], giving the bit a nominal total duration of **(2x t1)**. Digital Command Station components shall transmit "1" bits with the first and last parts each having a duration within the **t1** range. The duration difference between the first and last parts of a "1" bit shall not exceed **t1d**.

A Digital Decoder must accept bits whose first and last parts have a duration within the **tr1** range as a valid bit with the value of "1". Digital Decoders must accept "1" bits where the duration difference between the positive and negative components does not exceed **tr1d**.

In a "0" bit, the duration of the first and last parts of each transition shall nominally be greater than or equal to **t0**. To keep the DC component of the total signal at zero as with the "1" bits, the first and last part of the "0" bit are normally of equal duration. Digital Command Station components shall transmit "0" bits with each part of the bit having a duration within the **t0** range with the total bit duration of the "0" bit not exceeding **t0tot**. A Digital Decoder must accept bits, whose first or last parts have a duration within the **tr0** range as a valid bit with the value of "0". Figure 2.1 provides an example of bits encoded using this technique.

Figure 2.1: Bit Encoding



This is a differential signal with no ground. At the point where the signal line crosses the horizontal reference line, both rails will be at the same voltage.

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[1] Note that since a locomotive or piece of rolling stock can be placed upon a given section of track facing in either direction, it is impossible to define, from the point of view of a Digital Decoder, whether the first or last part of a bit will have the "positive" voltage polarity.

[2] All timing measurements are done between zero-volt crossings.

2.1 One Bit Timing

For Power **Station** Output under Load:

Relationship for One Bits	Result
Period A < ***(t1min.)*** or Period A > ***(t1max.)***	Bad
Period A = Period B	OK
|Period A – Period B| <= ***(t1dmax.)***	OK
|Period A – Period B| > ***(t1dmax.)***	Bad

Decoders must accept:

Relationship for One Bits	Result
Period A >= ***(tr1min.)*** & Period A <= ***(tr1max)***	OK
Period A = Period B	OK
|Period A – Period B| <= ***(tr1d_max.)***	OK

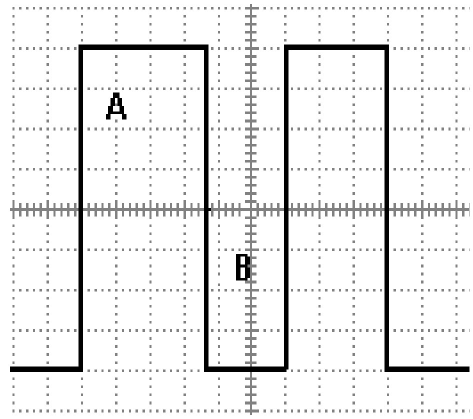

Table 2.1 – DCC Bit Timing

Parameter	Definition	Value			Unit	Comments
		Min.	Nominal	Max.		
t1	“1” Half Bit duration	55	58	61	µSec	Duration of a transmitted “1” half bit
tr1	“1” Half Bit received duration	52	58	64	µSec	Allowed Duration for a received “1” half bit
t0	“0” Half Bit duration	95	100	9900	µSec	Duration of a transmitted “0” half bit
t0total	stretched “0” Bit duration			12000	µSec	Max. total duration of stretched “0” bit
tr0	“0” Half Bit received duration	90	100	10000	µSec	Allowed Duration for a received “0” half bit
t1d	“1” half bit duration delta			3	µSec	Max. difference in duration between transmitted “1”bit half bits.
Tr1d	Received “1” half bit duration delta			6	µSec	Max. difference in duration between received “1” bit half bits.

2.2 Command Control Signal Shape

The NMRA digital signal applied to the track by any Digital Command Control system, as measured at the power station output, shall have the following characteristics, as measured under conditions ranging from no load to the maximum continuous load permitted by the power source. Transitions that cross the region between **VtrL** and **VtrH**[3] shall occur at the rate of **VtrA** or faster.

[3] 0 volts is the midpoint of the differential voltage.

This signal may contain non-monotonic distortion at the zero-crossing transitions, provided that this distortion shall have an amplitude of no greater than +/- **Vdist**[4].

Digital Decoders shall be designed to correctly decode signals with transitions whose slope is **VtrRA** or faster across the voltage range from **VtrL** to **VtrH**. A Digital Decoder shall correctly decode properly addressed baseline packets at a probability of **Pdecode** or higher, as defined in S-9.2, in the presence of noise (and/or other types of signals) at frequencies above **FNoise** with a total peak-to-peak amplitude of less than (**1/ Vsnr**) of the peak-to-peak amplitude of the NMRA digital signal[5].

Table 2.2 DCC Signal parameters Shape/ Amplitude

Parameter	**Definition**	**Value**			**Unit**	**Comments**
		Min.	Nominal	Max.		
VtrL	Transition region Vmin.		-4		Volt	Low limit of bit transition region
VtrH	Transition region Vmax.		4		Volt	High limit of bit transition region
VtrA	Transition rate	2.5			Volt/µSec	Transmitted bit voltage transition rate
Vdist	Distortion Amplitude			2	Volt	Distortion voltage during bit transition
VtrRA	Receive transition rate	2			Volt/µSec	Received bit voltage Transition rate
Pdecode	Decode probability	0.95				Percentage of packets decoded correctly
FNoise	Noise frequency	100			KHz	Frequency of noise or other signal
Vsnr	Peak Signal to Noise Amplitude Ratio	4				Peak DCC signal to peak FNoise

2.3 Power Transmission and Voltage Limits for Transmitting Power through the Rails

The baseline method for providing the power to operate locomotives and accessories, which shall be supported by all Digital Command Stations and Digital Decoders, is by full-wave rectification of the bipolar NMRA digital signal within the Digital Decoder[6]. In order to maintain power to the Digital Decoders, gaps in bit transmission are only allowed at specified times (see S-9.2, Section C).

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[4] This standard specifically permits super-imposing non-NMRA signals upon the rails for other purposes, provided that the NMRA Digital Decoder can reject these signals.

[5] This measurement is made with the Digital Decoder electrically connected to a track or accessory bus.

[6] Alternate means for supplying power are acceptable, provided that Digital Command Station power units are capable of producing the baseline track signal, and Digital Decoders are capable of operation from the baseline track signal as described by this standard.

The peak value of NMRA digital signal, as produced by the power station and measured at the track, shall be confined to the range of **VDCCp** for the applicable scale, as specified in Table 2.3[7]. In no case should the peak amplitude of the command control signal exceed **VDCCp_max** for the applicable scale.

Digital Decoders shall be designed to continuously operate and withstand, without permanent damage to the decoder; a peak maximum voltage within the range of **VDCCr** as specified in Table 2.3 for the applicable scale, measured at the track.

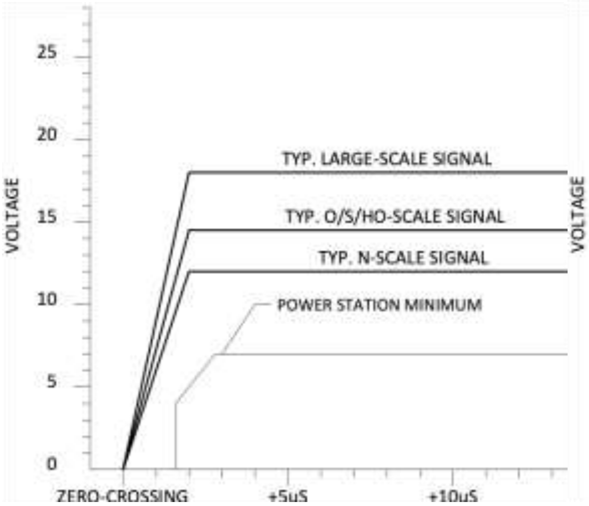
Table 2.3 – Power transmission and amplitude limit parameters

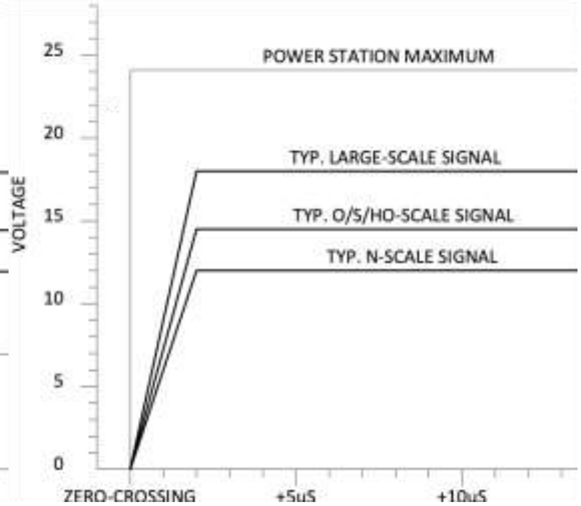
Parameter	Definition	Value			Unit	Comments
		Min.	Nominal	Max.		
VDCCp – N and smaller Scales	Voltage limits for track, N and smaller scales for power station	8.5	12	22	Volt	Voltage produced powering the track
VDCCp – HO/S/O Scales	Voltage limits for track HO/S/O scales for power station	8.5	15	22	Volt	Voltage produced powering the track
VDCCp – Large Scales	Voltage limits for track, large scales for power station	8.5	18	24	Volt	Voltage produced powering the track
VDCCr – N and smaller Scales	Voltage limits for track, N and smaller scales for digital decoders	7	12	24	Volt	Peak voltage decoder should operate in and withstand
VDCCr – HO/S/O Scales	Voltage limits for track HO/S/O scales for digital decoders	7	15	27	Volt	Peak voltage decoder should operate in and withstand
VDCCr – Large Scales	Voltage limits for track, large scales for digital decoders	7	18	27	Volt	Peak voltage decoder should operate in and withstand

Digital Decoders shall be designed to interpret a valid packet addressed to it whilst supplied a minimum voltage **VDDCr** as specified in Table 2.3 and to acknowledge the receipt of a command in that packet by some action E.G. turning on a low power output to illuminate an LED. The Digital Decoder is not required to turn the motor at this voltage. This an an indication of the Digital Decoder’s ability to read instructions addressed to it at the specified minimum voltage at the track.

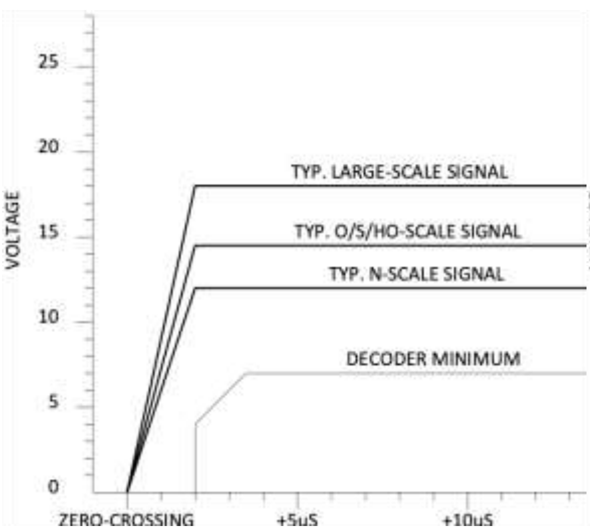
[7] Care should be taken to ensure that any motors exposed directly to the digital signal for extended periods have a stall rating that exceeds the amplitude of the signal, or sufficiently high impedance at 4-9 kHz to reduce the current to normal operating level. This appears to only be a concern for high-precision core-less can motors, which present a low impedance load, or for layouts using an NMRA digital signal with an amplitude in excess of ± 18 volts.

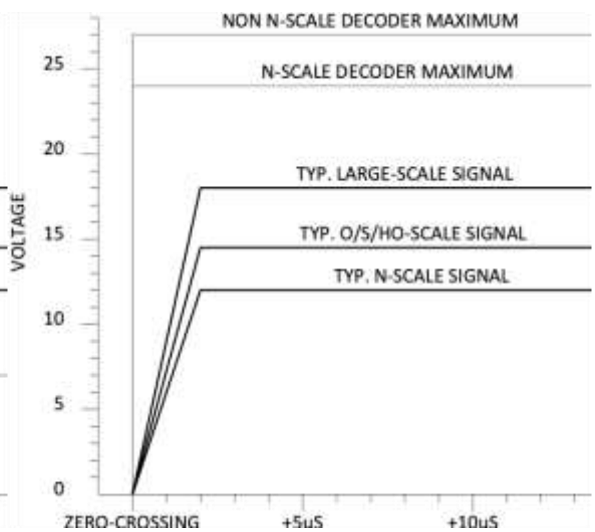
Minimum Voltage for Power Station **Maximum Voltage for Power Station**





Minimum Voltage for Decoders **Maximum Voltage for Decoders**





3 Document History

Date	Description
Jan 2019	Tabularized data, removing it from the text and replacing with a variable to make future revisions less prone to missing changes in the text. Cleaned up grammar and language.
Feb 2019	Table 3 increased large scale power station maximum voltage large to 24v from 22v.
Jan 21, 2021	Updated Graphs on Last Page to reflect higher max voltage on large scale. Removed requirement for FCC & CE certification to meet NMRA Standard.

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