

Experiment 1 - A.

Maximum Power Transfer Theorem

Aim: To verify the maximum power transfer theorem i.e. the specifications and relation between internal and external impedances to obtain the maximum output power.

Theory: Maximum power is transferred from a source of a given voltage and an initial impedance to the load $Z_L = R_L + jX_L$ in a circuit with internal resistance R_i and internal reactance X_i under two different conditions -

- ① When only X_L is adjustable - Here I (line current) should be maximum.

$$I = \frac{V_s}{(R_i + jX_i) + (R_L + jX_L)} \quad - (1)$$

$$\Rightarrow |I|_{\max} = \frac{V_s}{R_i + R_L} \quad \text{when } X_L = -X_i \quad - (2)$$

- ② When only R_L is adjustable - From the eqⁿ ① $P = |I|^2 R_L$

$$P = \frac{V_s^2}{(R_i + R_L)^2 + (X_i + X_L)^2} R_L \quad - (3)$$

Differentiating the eqⁿ ③ w.r.t R_L and equating to zero, the

value of $A \cdot R_L$ is obtained.

$$R_L = \sqrt{R_i^2 + (x_i + x_L)^2} \quad \text{--- (4)}$$

- (3) When both R_L and x_L are adjustable - ~~the required condition is satisfied~~
 Here both the eqⁿs (2) and (4) are satisfied simultaneously. Therefore

$$R_{L1} = R_i, \text{ so } x_{L2} = -x_i = 0$$

LTSpice Circuit Diagrams:

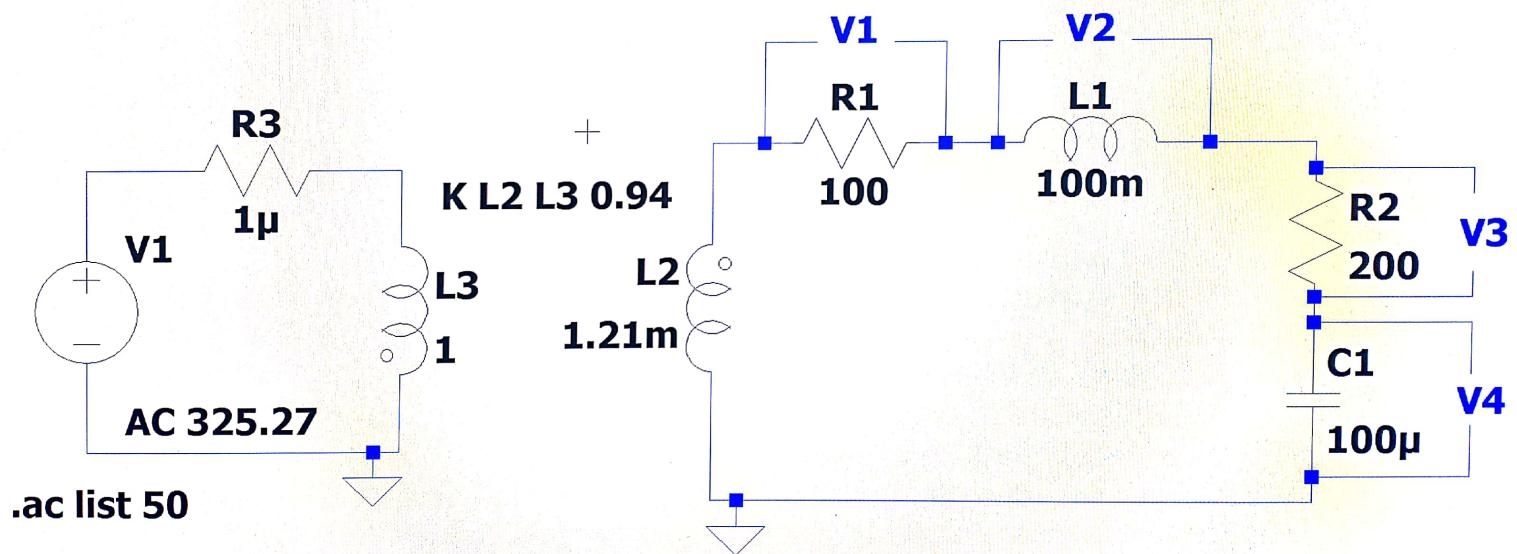
The diagrams for this experiment follow from the next page.

$$i_x - i_1 - i_2 = I$$

$$(i_x + i_2) + (i_1 + i_3)$$

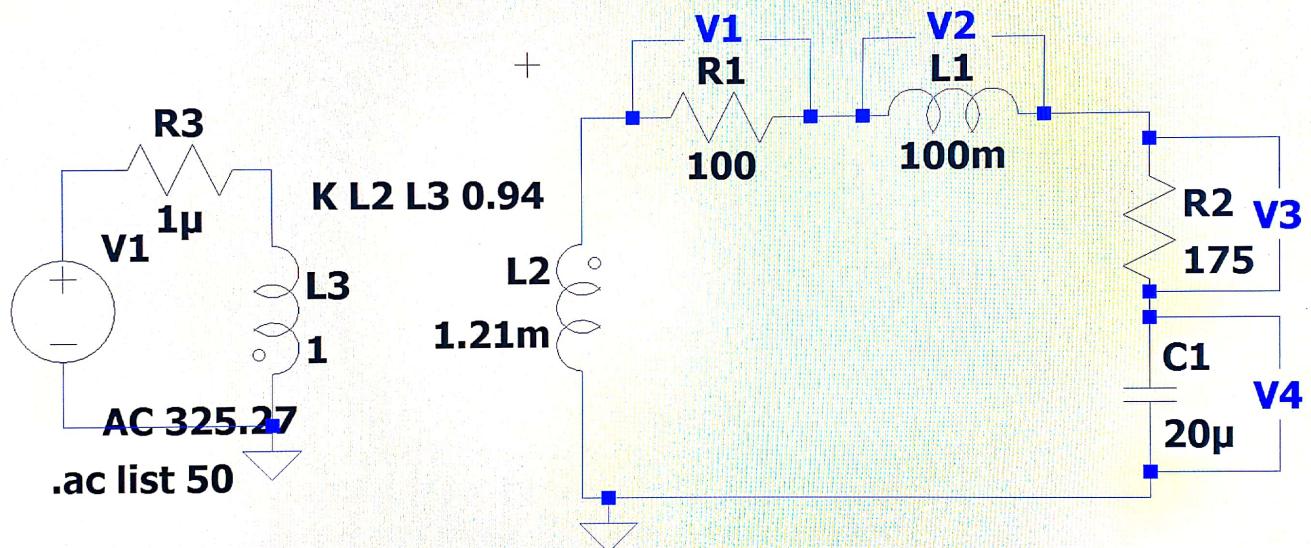
$$i_x - i_1 - i_2 = I$$

PART I (RESISTANCE KEPT CONSTANT AND ONLY CAPACITANCE IS ADJUSTABLE)

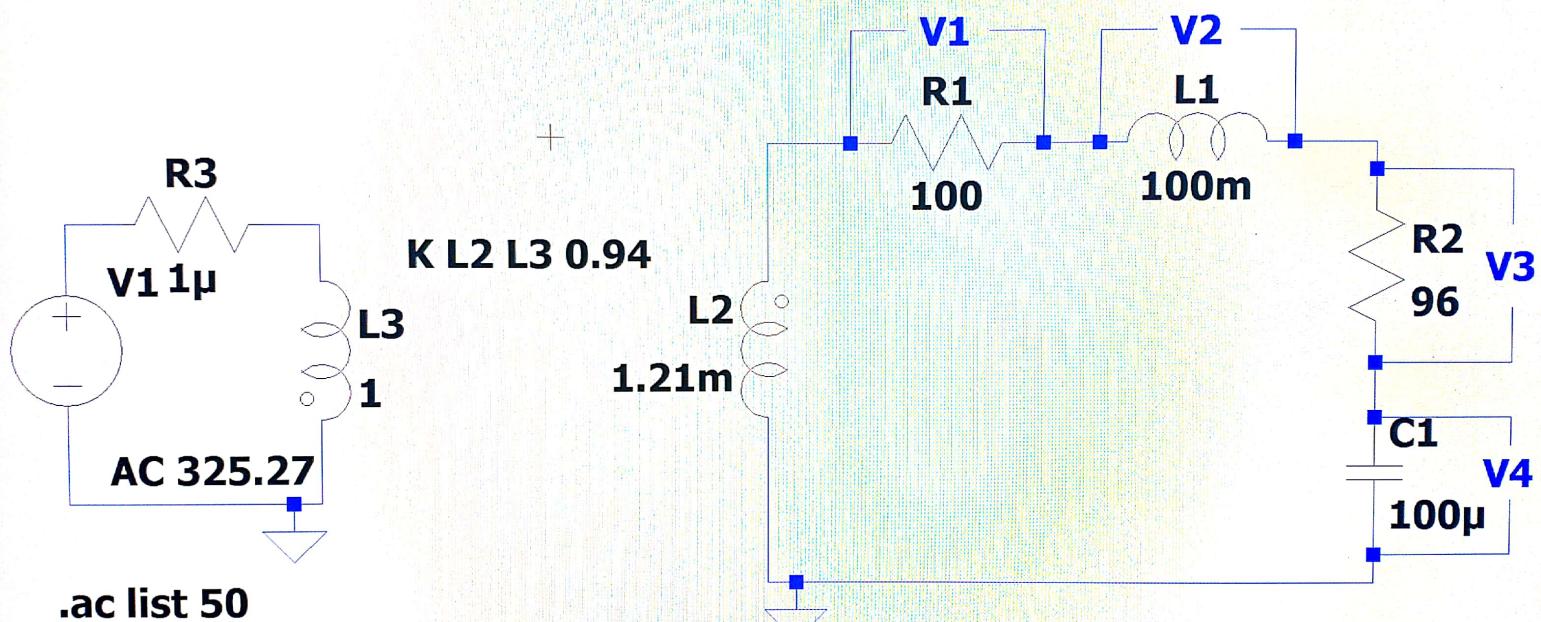


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PART II (CAPACITANCE KEPT CONSTANT AND ONLY RESISTANCE IS ADJUSTABLE)



PART III (BOTH CAPACITANCE AND RESISTANCE ARE ADJUSTABLE)



Observation Tables :

★ First Part

SNo.	C_L (4F)	V_1 (in V)	V_3 (in V)	$V_1 \cdot V_3$ (V^2)	Maximum of $V_1 \cdot V_3$ (V^2)
01.	20	3.2620	6.5240	21.28	21.28
02.	40	3.5000	7.0000	24.50	24.50
03.	60	3.5361	7.0722	25.10	25.10
04.	80	3.5438	7.0876	25.12	25.12
05.	100	3.5452	7.0904	25.14	25.14
06.	120	3.5447	7.0894	25.13	25.14
07.	140	3.5437	7.0874	25.11	25.14
08.	160.	3.5426	7.0852	25.10	25.14

★ Second Part

SNo.	R_L (Ω)	V_1 (in V)	V_3 (in V)	$V_1 \cdot V_3$ (in V^2)	Maximum of $V_1 \cdot V_3$ (V^2)
01.	35	5.7235	2.0032	11.464	11.464
02.	70	5.0022	3.5015	17.515	17.515
03.	105	4.4037	4.6239	20.362	20.362
04.	140	3.9122	5.4771	21.427	21.427
05.	175	3.5078	6.1386	21.533	21.533
06.	210	3.1723	6.6618	21.134	21.533
07.	245	2.8911	7.0832	20.478	21.533
08.	280	2.6531	7.4287	19.712	21.533

★ Third Part

SNo.	C_L (μF)	R_L (Ω)	V_1 (in V)	V_3 (in V)	$V_1 \cdot V_3$ (in V^2)	Maximum of $V_1 \cdot V_3$ (V^2)
01.	60	32	7.951	2.844	20.23	20.23
02.	80	64	6.477	4.145	26.85	26.85
03.	100	96	5.426	5.209	28.26	28.26
04.	120	128	4.664	5.970	27.84	28.26
05.	140	160	4.088	6.541	26.73	28.26
06.	160	192	3.639	6.987	25.448	28.26
07.	180	224	3.280	7.347	24.118	28.26
08.	200	256	2.985	7.642	22.818	28.26

For $C_L = 100 \mu F$ and $R_L = 96 \Omega$,
 $V_2 = 1.705 V$ and $V_4 = 1.727 V$.

Inference:

① First Part. Maximum output power was observed for $C_L = 100 \mu F$ while keeping R_L constant at 200Ω .

For $C_L = 100 \mu F$ and $R_L = 200 \Omega$,

$V_2 = 1.114 V$ and $V_4 = 1.128 V$.

Therefore at this point $V_2 \approx V_4$.

② Second Part.

Maximum output power was observed for $R_L = 175 \Omega$ while keeping C_L constant at $20 \mu F$.

Theoretically, $R_L = \sqrt{R_i^2 + (X_i + X_L)^2}$

$$X_i = L\omega = 0.1 \times 2\pi \times 50 = 31.41 \Omega$$

$$X_L = -1 \text{ p.u.} = -1 \frac{\Omega}{2\pi \times 50 \times 20 \times 10^{-6}} = -159.15 \Omega$$

$$R_L = [100^2 + (31.41 - 159.15)^2]^{1/2}$$

$$R_L = 162.23 \Omega \text{ (theoretical)}$$

$$R_L = 175 \Omega \text{ (practical)}$$

③ ~~Seco~~ Third Part.

Maximum output power was observed at $C_L = 100 \mu F$ and $R_L = 96 \Omega$.

At this point; $V_1 = 5.426 V$, $V_3 = 5.209 V$,
 $V_2 = 1.705 V$, $V_4 = 1.727 V$

Therefore at this point;
 $V_1 \approx V_3$ and $V_2 \approx V_4$ was observed.

Discussion: The values of the readings taken from LTSpice circuits and hence the inferred values of capacitance and resistance for maximum power transfer matched to a great extent with the values calculated theoretically. For obtaining sufficiently close values, more number of readings could have been taken around the theoretically calculated values. Theoretically in the first part the values V_2 and V_4 and in the third part the values V_2 and V_4 , and V_1 and V_3 are supposed to be equal.

Here they are not exactly the same but differ by around 2-4%. However such small gap is sufficient to verify the implications of the maximum power transfer theorem.

The inferences drawn from the readings recorded in the table match with the implications of the maximum power transfer theorem. Hence the experiment was successful in verifying the maximum power transfer theorem.

$$R_{AB} = 1\Omega \text{ and } R_{AC} = 1\Omega \text{ so}$$
$$V_{PAB} = 6V \quad V_{PAC} = 6V \quad \text{using } \Delta \text{ law}$$

$V_{FAB} = 6V \quad V_{FAC} = 6V$
So $V_{FAB} = V_{FAC}$. twice dint to check result

Result obtained is same as calculated with load connected across both terminals.

So maximum power transferred is stored in a capacitor connected between two terminals.

After disconnecting the load across terminals, the voltage across terminals will increase due to self-inductance of the coil.

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