INTRODUCTION TO ELECTRONICS LAB EC29003 EXPERIMENT O5

STUDY ON ANALOG CIRCUITS USING OP-AMPS

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EXPERIMENT O5

STUDY ON ANALOG CIRCUITS USING OP-AMP

AIM: To study various characteristics of analog circuits simulated using op-amps including frequency response, gain attenuation, voltage transfer characteristics and oscillations; and to theoretically verify the mathematical operations performed by op-amp circuits.

SIMULATION PLATFORMS USED:

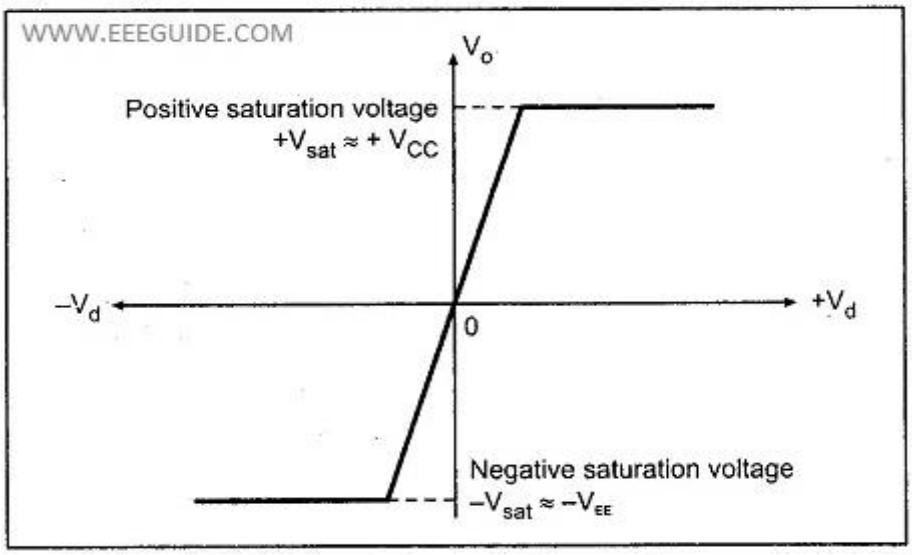
- Falstad
- LTSpice

THEORY:

An operational amplifier is a DC-coupled high-gain electronic voltage amplifier with a differential input and a single ended output. In the open loop configuration, an op-amp produces an output potential that is typically 100,000 times larger than the potential difference between the two input terminals.

OPEN LOOP CONFIGURATION

The magnitude of A_{OL} is typically very large and therefore even a small difference between the inverting and the non-inverting terminals can drive the amplifier output nearly to the supply voltage. This situation in which the output voltage becomes equal or nearly equal to the supply voltage and does not show any further increase in output voltage with increase in the differential input, is called saturation. Due to this, the voltage transfer characteristics of the opamp circuit in this configuration would look like the following.



IDEAL OP-AMP CHARCATERISTICS

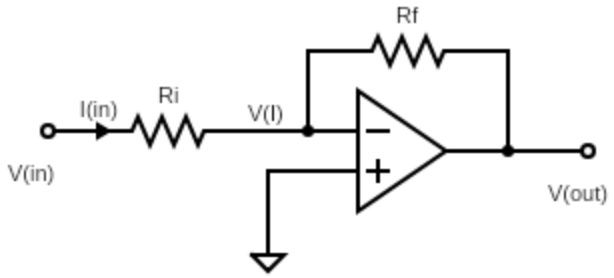
- Infinite open-loop gain
- Infinite input resistance and hence zero current entering the op-amp
- Zero input offset voltage
- Infinite output voltage range
- Infinite bandwidth with zero phase shift
- Infinite slew rate
- Zero output impedance
- Infinite common-mode rejection ratio (CMRR)

The two fundamental rules that come in very handy in solving the op-amp circuits analytically are-

- *VIRTUAL SHORTING: In a closed loop, the output attempts to do whatever is necessary to make the voltage difference between the two input terminals zero.*
- *INFINITE INPUT RESISTANCE: The input terminals draw zero current.*

INVERTING AMPLFIER

By forming a closed loop in an op-amp on providing a negative feedback can reduce the gain of the circuit. When negative feedback is used the circuit's overall gain and response becomes determined mostly by the feedback network, rather than by the op-amp's characteristics. The following circuit can be easily solved using the previously mentioned two rules.



$V_I = 0 \quad (by\ RULE\ O1)$

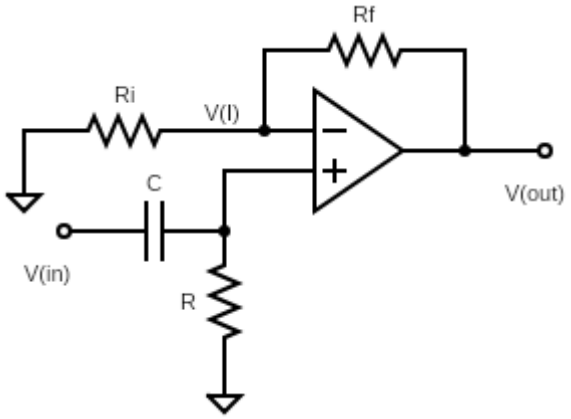
$I_{in} = \frac{V_{in} - V_I}{R_i} \quad (by\ Ohm's\ Law)$

$I_{in} = \frac{V_I - V_{out}}{R_f} \quad (by\ RULE\ O2)$

$\frac{V_I - V_{out}}{R_f} = \frac{V_{in} - V_I}{R_i} \xrightarrow{V_I=0} \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_i}$

Since the gain of an inverting amplifier is negative, it means that the output voltage is the negative of the input voltage scaled by an amplification factor, or in case of sinusoidal inputs, the output voltage is shifted by a phase of 180 degrees with respect to the input waveform.

NON-INVERTING AMPLFIER



$V_I = V_{in} \quad (by\ RULE\ O1)$

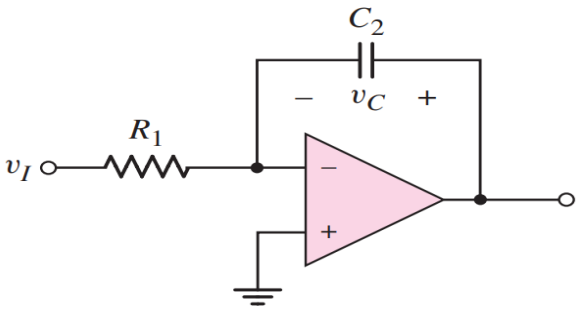
$I_{in} = \frac{0 - V_I}{R_i} \quad (by\ Ohm's\ Law)$

$I_{in} = \frac{V_I - V_{out}}{R_f} \quad (by\ RULE\ O2)$

$$\frac{V_I - V_{out}}{R_f} = \frac{0 - V_I}{R_i} \xrightarrow{V_I = V_{in}} \frac{V_{out}}{V_{in}} = 1 + \frac{R_f}{R_i}$$

Since the gain of a non-inverting amplifier is always positive, it means that the output voltage is always in the same phase as the input waveform. Besides, unlike for the inverting amplifier, the gain of a non-inverting amplifier is always greater than unity. This means that using this configuration, the input signal can only be strengthened, not weakened.

INTEGERATOR



from DONALD A. NEAMEN

Let the potential at the inverting terminal be v_{inv} and the potential at the output terminal of the op-amp be v_{out}. Also let the current flowing through the resistor be i_{in}.

$$v_{inv} = 0 \quad (by\ RULE\ O1)$$

$$i_{in} = \frac{v_I}{R_1} \quad (by\ Ohm's\ Law)$$

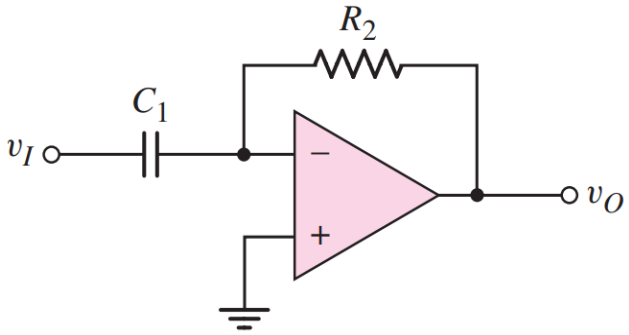
$$i_{in} = -C\frac{d}{dt}v_C \quad (by\ RULE\ O2)$$

$$v_C = v_{out} - v_{inv} = v_{out}$$

$$i_{in} = \frac{v_I}{R_1} = -C\frac{d}{dt}v_{out}$$

$$v_{out} = -\frac{1}{R_1 C}\int v_I(t)dt$$

DIFFERENTIATOR



from DONALD A. NEAMEN

Let the potential at the inverting terminal be v_{inv} and the current flowing through the capacitor be i_{in}.

$$v_{inv} = 0 \quad (by\ RULE\ O1)$$

$$i_{in} = C_1 \frac{d}{dt} v_C$$

$$i_{in} = \frac{v_{inv} - v_o}{R_2} = -\frac{v_o}{R_2}\ (by\ RULE\ O2)$$

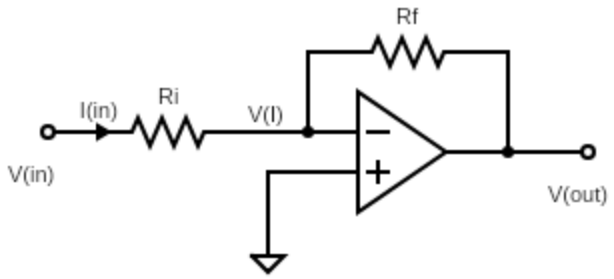
$$v_C = v_I - v_{inv} = v_I$$

$$i_{in} = -\frac{v_o}{R_2} = C_1 \frac{d}{dt} v_I$$

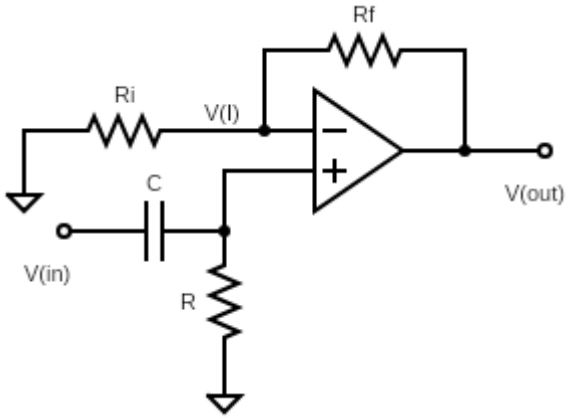
$$v_o = -R_2 C_1 \frac{d}{dt} v_I$$

The theoretical analysis and explanations related to all the other circuits simulated in this experiment are given in detail under the "OBSERVATIONS AND THEORY" section along with their experimental verifications.

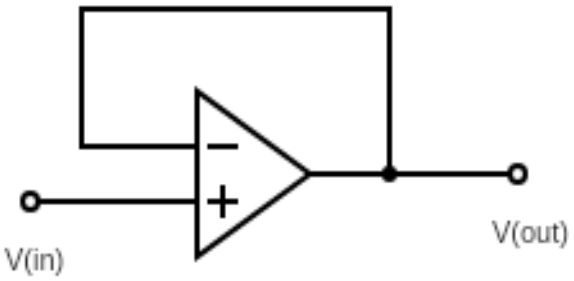
CIRCUIT DIAGRAMS:



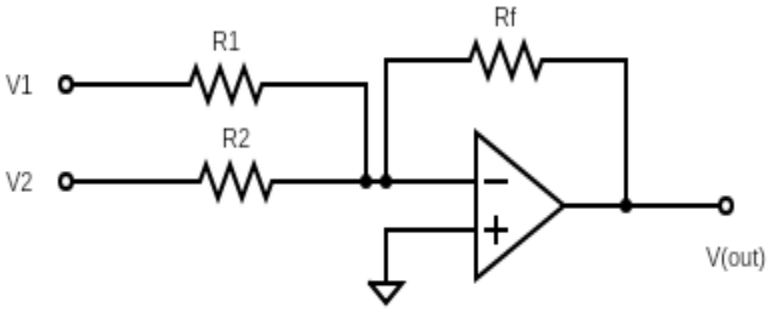
CIRCUIT O1



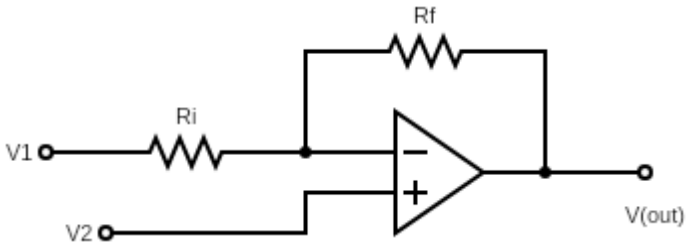
CIRCUIT O2



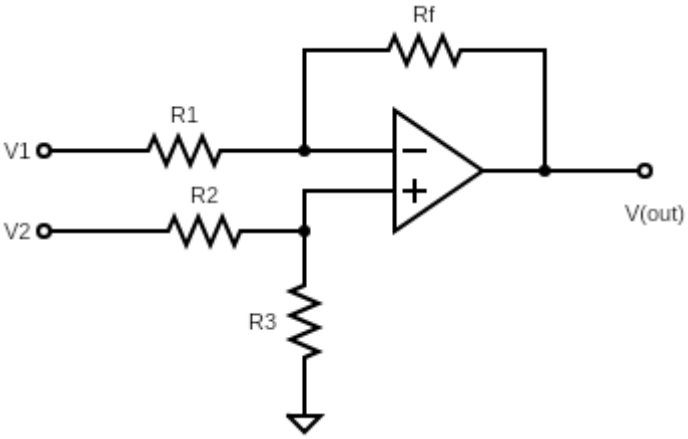
CIRCUIT O3



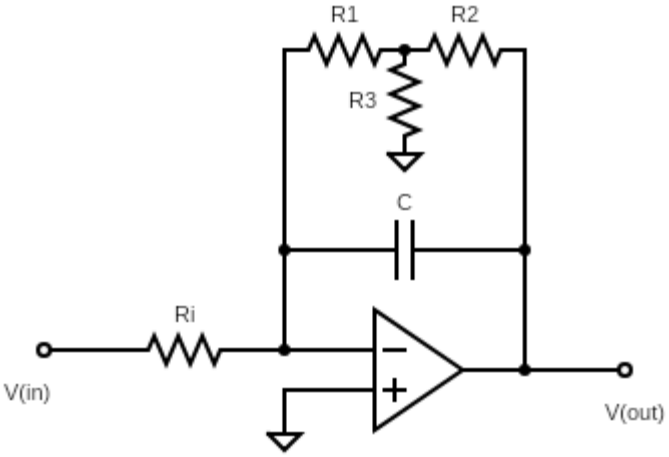
CIRCUIT O4



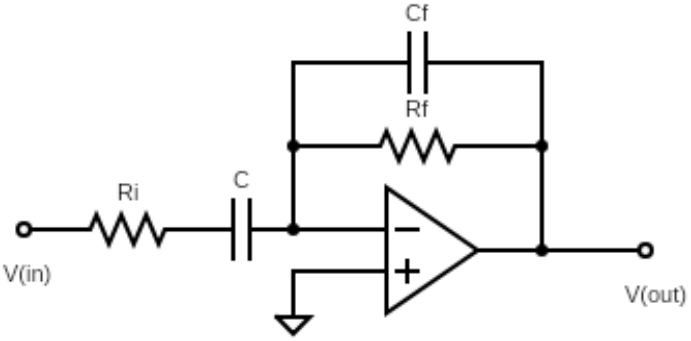
CIRCUIT O5



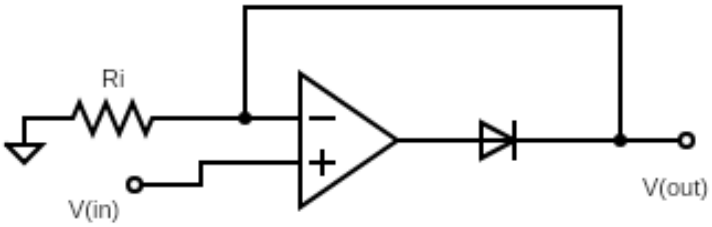
CIRCUIT O6



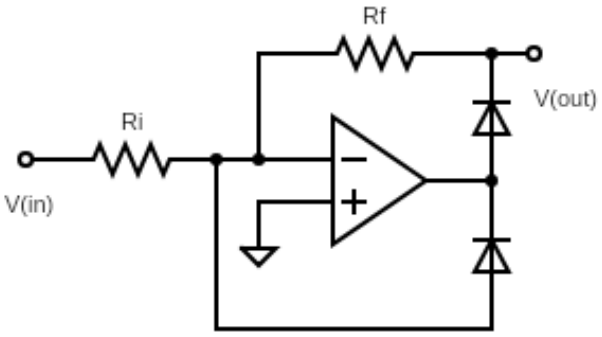
CIRCUIT O7



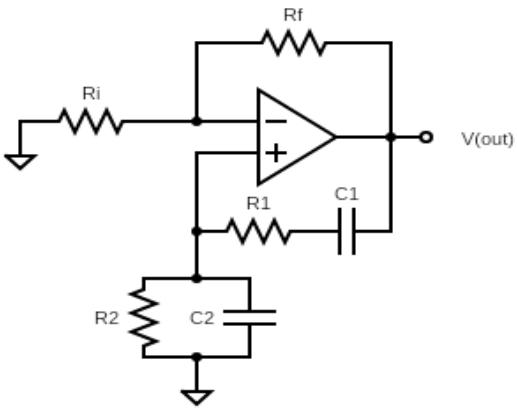
CIRCUIT O8



CIRCUIT O9



CIRCUIT O10



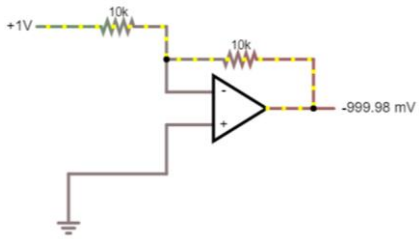
CIRCUIT O11

PROCEDURE:

SECTION A - DC GAIN

OPAMP IN NON-INVERTING CONFIGURATION

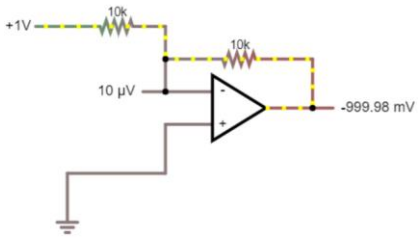
- On Falstad, the circuit as given in the first circuit diagram was drawn. The negative and positive supply voltages were set at 12 V and the resistances $R_i = 10\ k\Omega$ and $R_f = 10\ k\Omega$.
- The following Falstad circuit was simulated by setting V_{in} as 1 V DC.



- The output voltage was noted and the corresponding practical gain was calculated. It was compared with the theoretical value.
- The finite opamp gain considered in the experiment was compared with the theoretical value of gain in this configuration that is $-R_f/R_i$.

CHECKING VIRTUAL GROUND

- The same circuit as above was simulated after changing the feedback resistance to 100kΩ.
- The potential at the inverting terminal/pin was measured and the virtual ground condition was checked.



INPUT RESISTANCE

- The same circuit as in the first part of this section was simulated again. The current I_{in} was measured through the resistor R_i.
- The corresponding input resistance was calculated by the formula $R_{in} = V_{in}/I_{in}$. This value was compared with R_i.
- The above two steps were repeated for the feedback resistances 27kΩ, 47kΩ and 100kΩ.

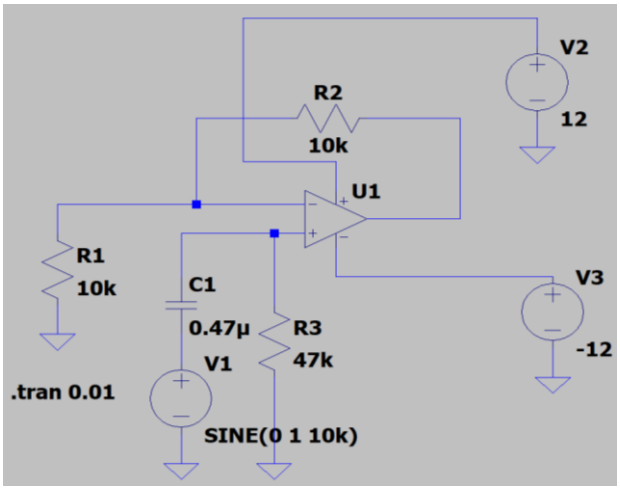
INPUT OUTPUT CHARACTERISTICS

- The circuit from the previous part was used. The feedback resistance was changed gradually from 1kΩ to 10MΩ and the values of potentials at the inverting terminal and the output terminal were noted.
- Finally, the output voltage was plotted as a function of voltage at inverting terminal. The saturation output voltage and the potential difference between the two input pins at which this saturation occurs are noted.

SECTION B – NON-INVERTING AMPLIFIER

GAIN MEASUREMENT

- On LTSpice, the circuit as given in the second circuit diagram was drawn. The input frequency was kept at 10kHz and the input AC amplitude at 1V.



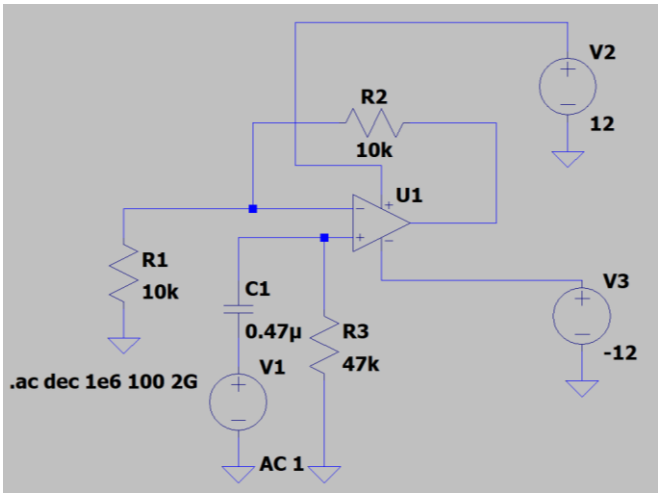
- The circuit was simulated with “transient” simulation command. The output waveform was viewed on the scope and corresponding gain was calculated for feedback resistances 10kΩ, 27kΩ, 47kΩ and 100kΩ.
- The gains were further compared with the theoretical values.

ATTENUATION OF GAIN AT LOW CAPACITANCES

- In the above circuit, the value of feedback resistance R_f was kept fixed at 10kΩ and the capacitance in the circuit was reduced to smaller values.
- The output waveform was observed on the scope and the attenuation of the gain (despite of keeping the values of R_f and R_i intact – on which the theoretical formula of gain in this configuration depends) was explained.

FREQUENCY RESPONSE

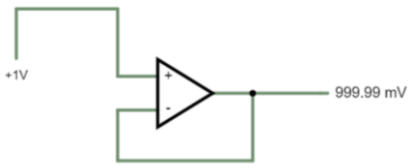
- The simulation command in the above circuit was changed to “AC Analysis” and the frequency response of the circuit was observed for input frequencies ranging from 100Hz to 2GHz.



- This was repeated for feedback resistances 10kΩ, 27kΩ, 47kΩ and 100kΩ while R_i was kept constant at 10kΩ.
- The Bode plots from the LTSpice were studied to determine the type of filter the opamp acts as, the cut-off frequency/bandwidth of the opamp, the gain-bandwidth product and the roll-off of the frequency response for each case.

SECTION C – VOLTAGE FOLLOWER

- The circuit as given in the third circuit diagram was drawn on Falstad and then simulated with 1V DC input. The magnitude and sign of the output voltage were noted and compared with the input voltage.

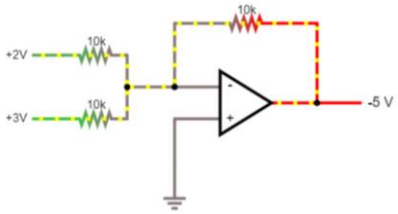


- The input voltage was varied over a range from -50 V to 50 V. The corresponding output voltages were noted.
- The input-output characteristics were plotted. The plot was studied to analyze the saturation of the output voltage and the slope in the linear region.

SECTION D – ADDER

SUMMING DC VOLTAGES

- The circuit as is given in the fourth circuit diagram was drawn on Falstad. The two input terminals were supplied with DC voltages 2V and 3V and the circuit was simulated.



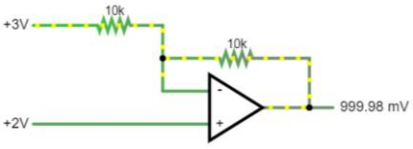
SUMMING AMPLIFIER

- The same circuit was used as in the above part. The two DC inputs were replaced by 1V AC input of 1kHz frequency at the first terminal and a DC input of 6.5V at the second terminal. The output voltage waveform was checked.
- The above step was repeated for the DC input voltage of -7.5V.

SECTION E – SUPERPOSITION

FOR DC VOLTAGES

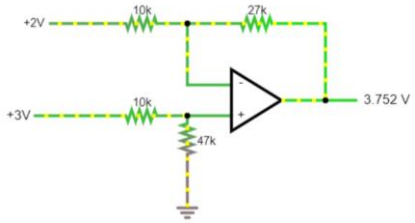
- The circuit as given in the fifth circuit diagram was drawn on Falstad. The input voltages were set to 3V DC and 2V DC as shown below.



- This was repeated for the feedback resistances of 47kΩ and 100kΩ. The output voltages were compared with the theoretical values. The saturation of the opamp was also checked simultaneously.

DIFFERENTIAL AMPLIFIER

- The circuit as given in the sixth circuit diagram was drawn on Falstad. The input voltages were set to 2V DC and 3V DC as shown below.

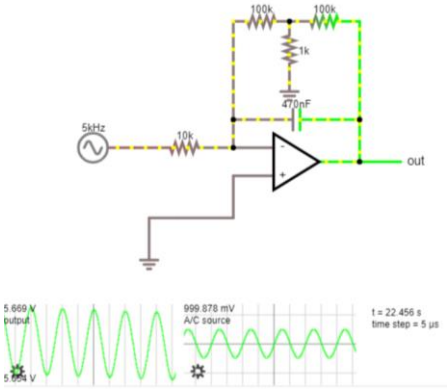


- This was repeated for the feedback resistance of 47kΩ. The output voltages were compared with the theoretical values. The saturation of the opamp was also checked simultaneously.

SECTION F – INTEGRATOR

SINUSOIDAL INPUT

- The circuit as given in the seventh circuit diagram was drawn on Falstad. The values of the components were set as shown below.



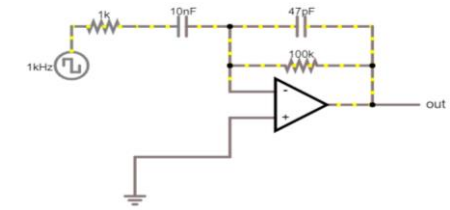
- On input, a 1V AC voltage was set at a frequency of 5kHz. The output waveform was observed and the phase difference between the two waveforms was noted.

SQUARE WAVE INPUT

- In the same circuit, the input voltage waveform was changed to square wave. The frequency was varied from 1kHz to 10kHz and the corresponding output waveforms were observed.

SECTION G – DIFFERENTIATOR

- The circuit as shown in the eighth circuit diagram was drawn on Falstad and values of the components were set as shown below.

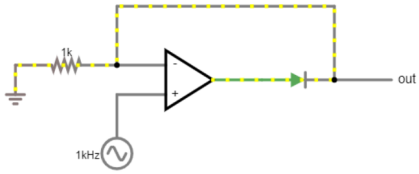


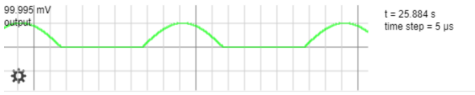
- On input square wave of 0.2V amplitude was set and the circuit was simulated for frequencies varying from 1kHz to 10kHz.
- The corresponding output waveforms were observed for each one of them.

SECTION H – ACTIVE RECTIFIER

CONFIGURATION O1

- The circuit as shown in the ninth circuit diagram was drawn on Falstad.

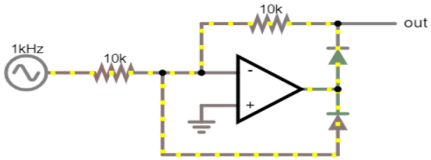


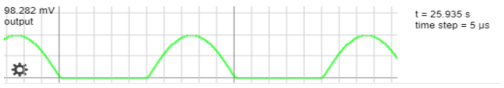


- Input voltage of 0.1V AC with 1kHz frequency was set and the circuit was simulated. The output voltage waveform was checked.

CONFIGURATION O2

- The circuit as shown in the tenth circuit diagram was drawn on Falstad.

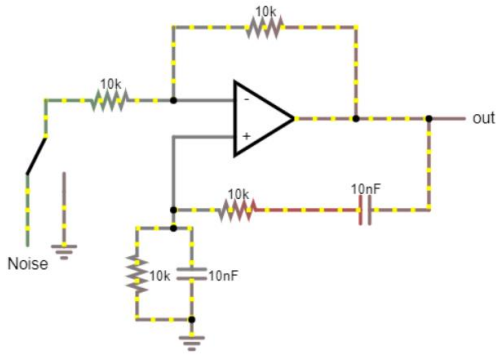




- Input voltage of 0.1V AC with 1kHz frequency was set and the circuit was simulated. The output voltage waveform was checked.

SECTION I – WEIN BRIDGE OSCILLATOR

- The circuit as shown in the eleventh circuit diagram was drawn on Falstad. Additionally, some arrangement was made to initialize the circuit with some noise using a noise input device and SPST switch as shown below.

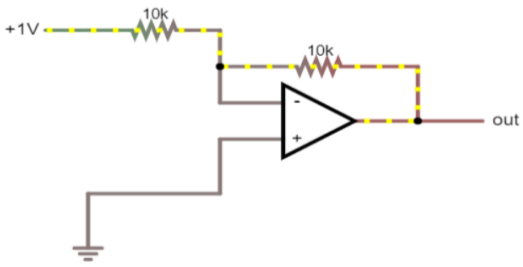


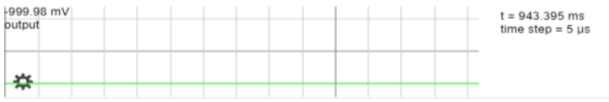
- After a few milli-seconds of exposure to noise, the switch is thrown to the grounded terminal. The resistance R_f is kept fixed at 10kΩ and the resistance R_i is varied to obtain the value at which a good sinusoidal oscillation is observed on the output. Fine tuning was done around significant changes. This value of R_i is noted as $R_{i\text{-}osc}$. The corresponding frequency of oscillation is noted along with the ratio of $R_{i\text{-}osc}/ R_f$ at this point. The former is compared with its theoretical value.
- The experiment was repeated for the feedback resistances of 27kΩ, (27||100) kΩ and 100kΩ.

OBSERVATIONS AND THEORY:

SECTION A - DC GAIN

OPAMP IN NON-INVERTING CONFIGURATION





For input DC voltage of 1V, output voltage came out to be -999.98mV.

$$V_{out-practical} = -999.98\, mV$$

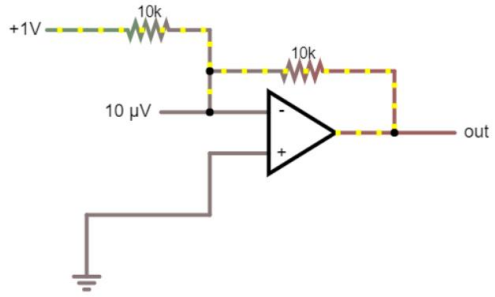
$$A_{V-practical} = \frac{V_{out-practical}}{V_{in}} = -\frac{-999.98}{1000} = -0.9998$$

Theoretically, closed loop gain for an op-amp in inverting configuration is

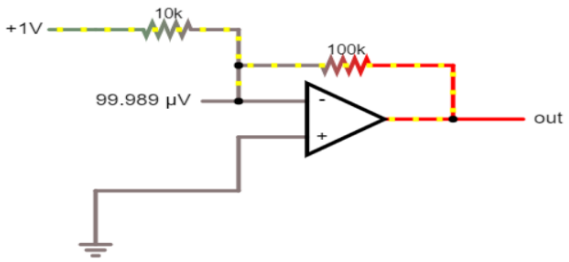
$$A_{V-theoretical} = -\frac{R_f}{R} = -\frac{10}{10} = -1$$

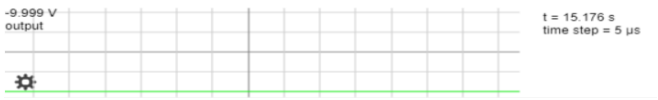
$$Therefore \quad V_{out-theoretical} = -1\, V$$

Therefore, $A_{V-practical}$ is little less than $A_{V-theoretical}$. This is because the theoretical formula used here was derived (check the "*THEORY*" section for derivation) considering the virtual ground condition, that is the open loop gain of the op-amp was assumed to be infinite. For practical purposes though, the open loop gain is large but finite. Through the following simulation, it can be experimentally verified that the inverting terminal is not exactly at ground potential and has some non-zero potential of 10µV. Due to this, the practical gain slightly deviates from the theoretical value of gain.



CHECKING VIRTUAL GROUND





$V_I = 99.989\ \mu V$

The potential V_I has a non-zero value and hence it cannot be exactly said to be at ground potential. Let A_{OL} be the open loop gain of the op-amp.

$V_{out} = A_{OL} * V_D$

$V_D = V_I$ ($because\ the\ other\ node\ is\ grounded$)

$V_I = \frac{V_{out}}{A_{OL}}$

If the op-amp is ideal and hence A_{OL} has infinite value, the potential V_I has to be zero provided the output voltage does not reach or exceed (in magnitude) the supply voltage. Here, the A_{OL} is very high but finite with a value of 10^5. Therefore, if the output voltage is not negligible, the potential at V_I will have some significant value and hence won't be at the ground potential. Here output voltage is around 1V and therefore the virtual ground condition is not satisfied practically.

INPUT RESISTANCE

$R_i = 10k\Omega\ and\ R_f = 10k\Omega$

$R_{in} = \frac{V_{in}}{I_{in}}$; $(V_{in} = 1V)$

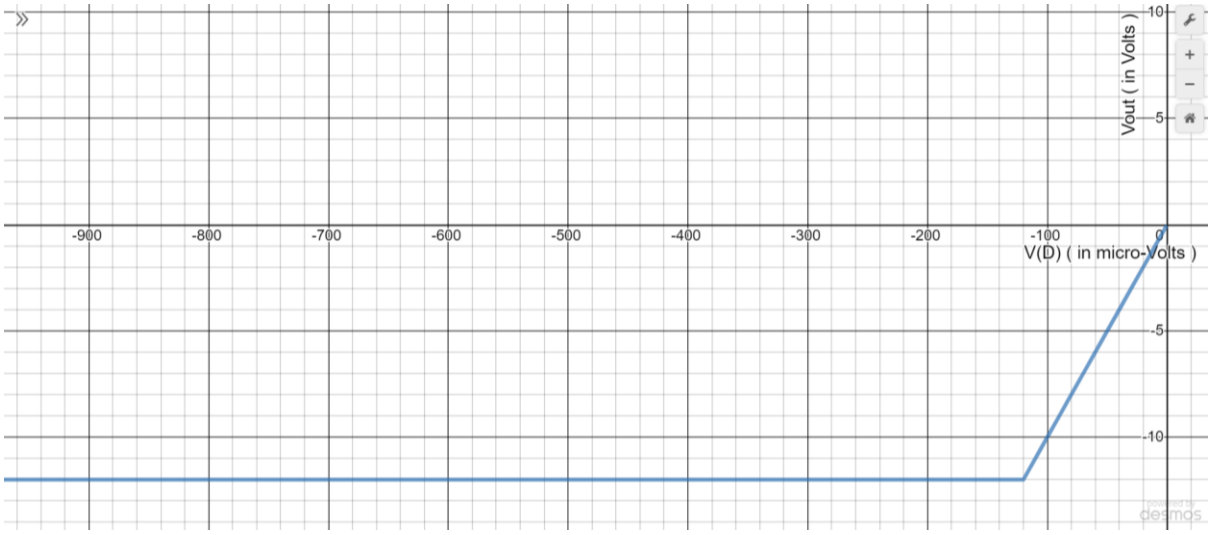
$R_i\ (in\ k\Omega)$	$R_f\ (in\ k\Omega)$	$I_{in}\ (in\ \mu A)$	$R_{in}\ (in\ k\Omega)$
10	10	99.999	10.0001
10	27	99.997	10.0003
10	47	99.995	10.0005
10	100	99.990	10.0010

For an ideal op-amp, the input terminals are virtually shorted for output voltages less than the supply voltage. In this scenario, the input resistance would simply be the resistance R_i that is 10kΩ. In a non-ideal case however, there is a potential drop between the inverting and non-inverting terminals because of a finite open-loop gain. Due to this, the input resistance becomes more than the resistance R_i. But since the potential drop across the terminals though non-zero remains very small, the input resistance here would be close to 10kΩ. This theoretical explanation is verified by the above observations. As the feedback resistance is increased, the potential difference between the two terminals also

increases and hence does the input resistance. However, the input resistance in all the cases is extremely close to R_i = 10kΩ.

INPUT OUTPUT CHARACTERISTICS

$R_f\ (in\ k\Omega)$	$V_I(in\ V)$	$V_{out}(in\ V)$	Gain
1	1.000µ	-0.100	10^5
5	5.000µ	-0.500	10^5
10	10.000µ	-1.000	10^5
20	19.999µ	-2.000	10^5
30	29.999µ	-3.000	10^5
40	39.998µ	-4.000	10^5
50	49.997µ	-5.000	10^5
60	59.996µ	-6.000	10^5
70	69.994µ	-6.999	10^5
80	79.993µ	-7.998	10^5
90	89.991µ	-8.999	10^5
100	99.989µ	-9.999	10^5
105	104.988µ	-10.499	10^5
110	109.987µ	-10.999	10^5
115	114.986µ	-11.499	10^5
120	119.984µ	-11.998	10^5
125	37.037m	-12.000	-
150	187.499m	-12.000	-
175	297.296m	-12.000	-
200	380.951m	-12.000	-
300	580.643m	-12.000	-
400	682.925m	-12.000	-
500	745.097m	-12.000	-
700	816.900m	-12.000	-
1M	871.286m	-12.000	-
2M	935.323m	-12.000	-
3M	956.810m	-12.000	-
5M	974.052m	-12.000	-
10M	987.013m	-12.000	-



The opamp is observed to give a saturated output voltage when the potential at the inverting terminal (while the non-inverting terminal is grounded) crosses a certain value. This saturated output voltage is -12V that is equal to the negative supply voltage. Besides, the saturation occurs at a very small value of V_I (around 0.2 mV) and it is the point where the characteristics cease to be linear. That is why, in the calculations if the magnitude of output voltage is less than the magnitude of supply voltage, we assume the two input terminals to be virtually shorted because of very small potential difference between them. Note that the potential difference between the input terminals V_D is actually $V_{NI} – V_I$. Here V_{NI} is zero and hence V_D is equal to $–V_I$.

SECTION B – NON-INVERTING AMPLIFIER

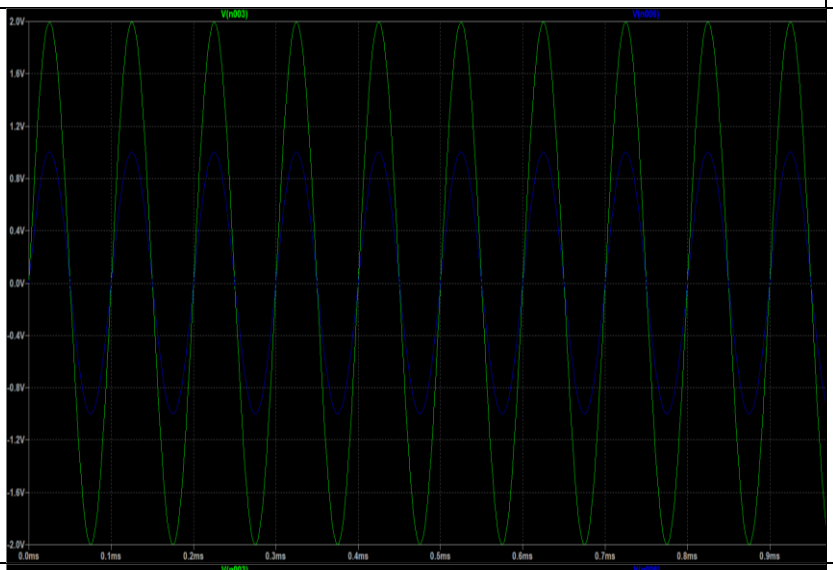
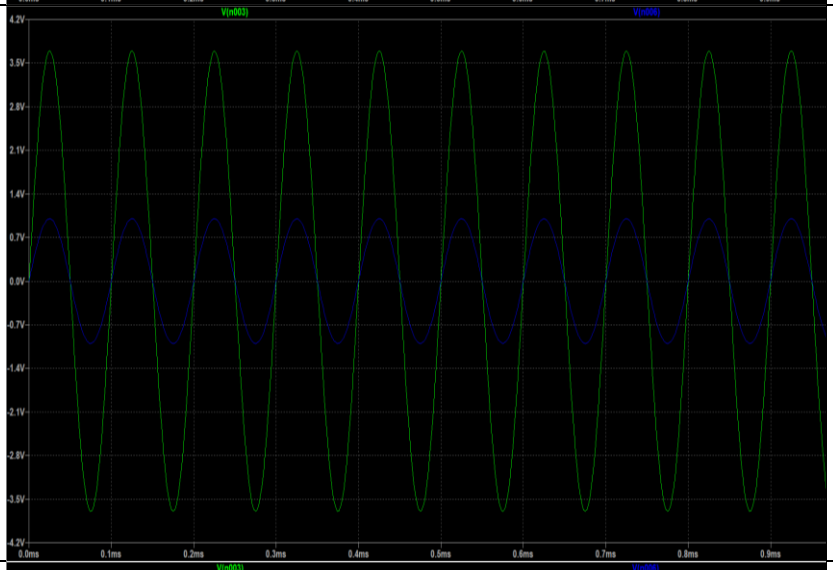
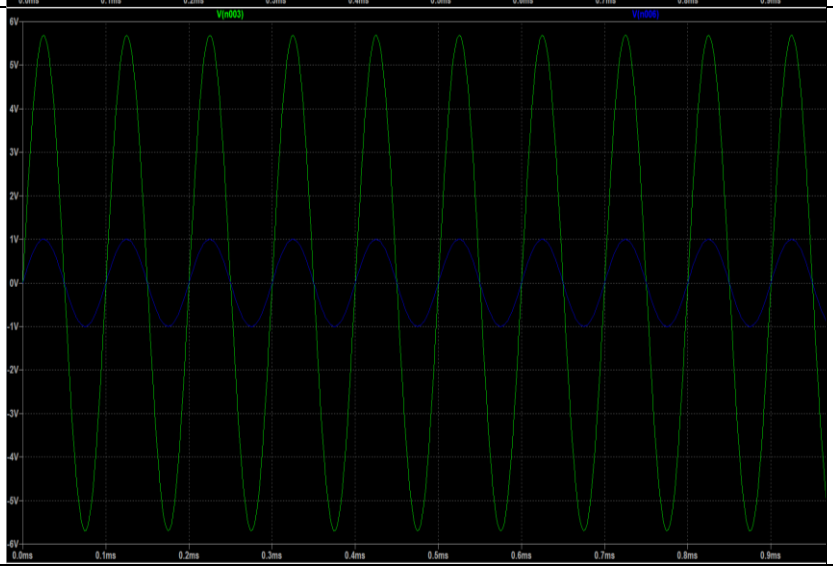
GAIN MEASUREMENT

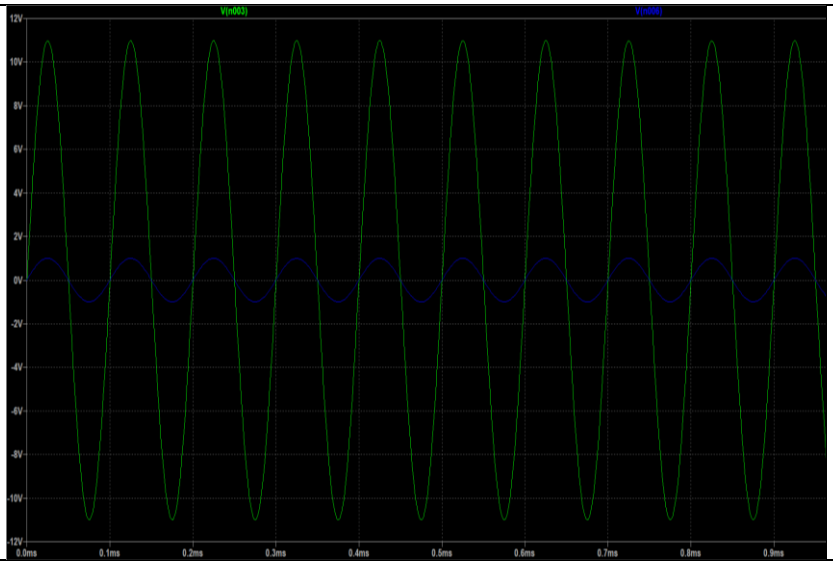
$$A_{V-theoretical} = 1 + \frac{R_f}{R_i}$$

$V_{in-amplitude} = 1V$

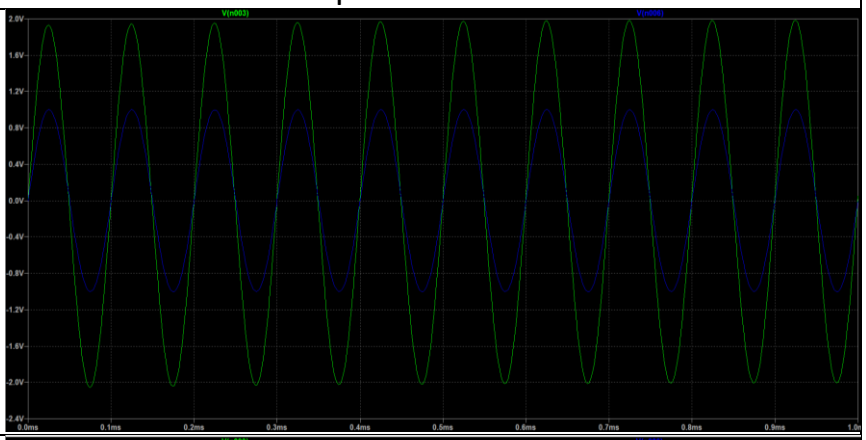
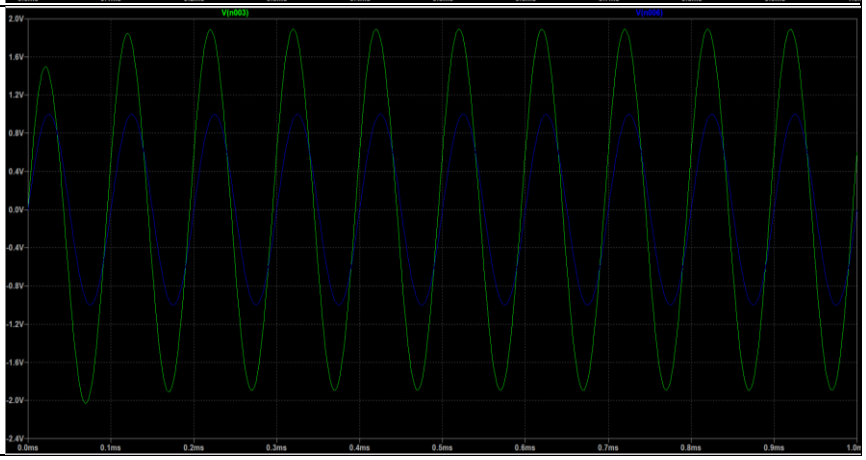
$R_i = 10\ k\Omega$

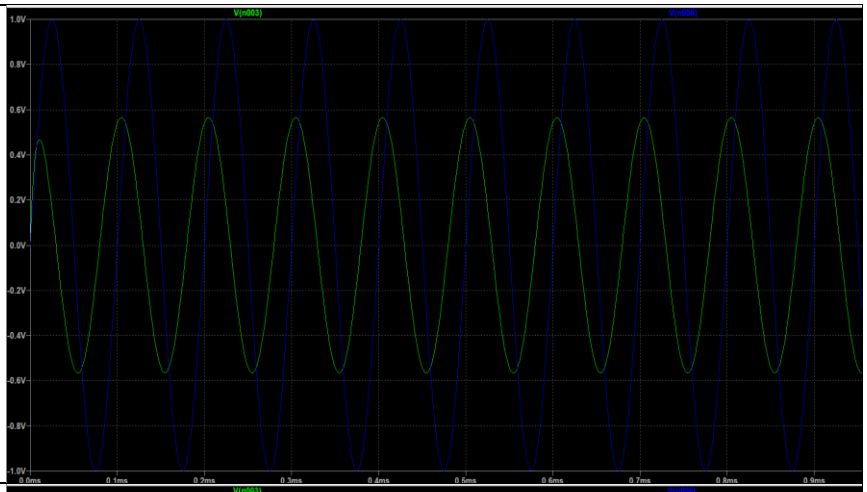
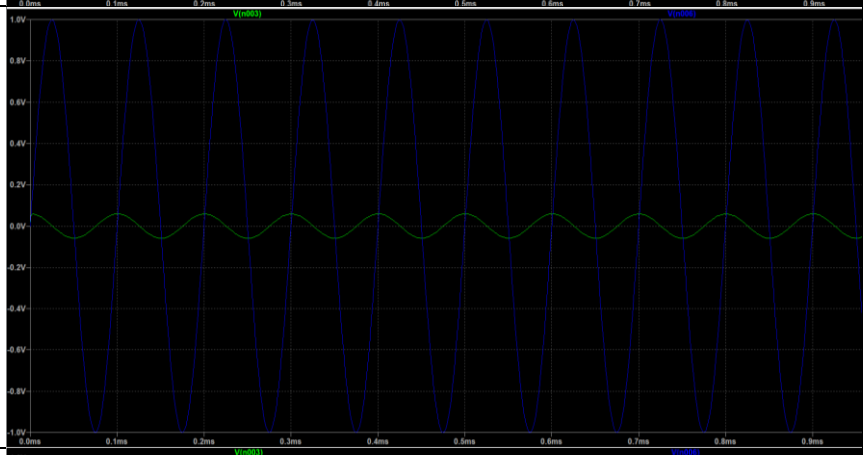
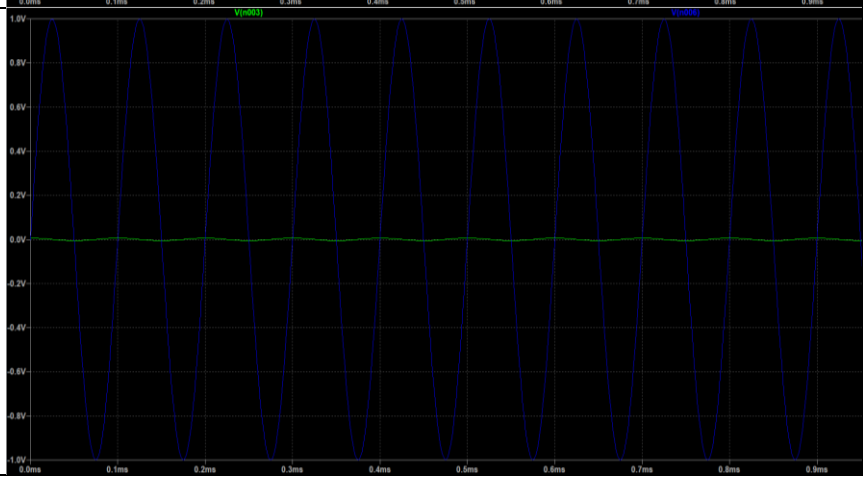
$Input\ Frequency\ of\ 10\ kHz$

R_f $(in\ k\Omega)$	Falstad Simulation	Practical gain	Theoretical gain
10		2.00	2.00
27		3.70	3.70
47		5.70	5.70

100		11.00	11.00

ATTENUATION AT LOW CAPACITANCES

C (in F)	LTSpice Simulation
10n	
1n	

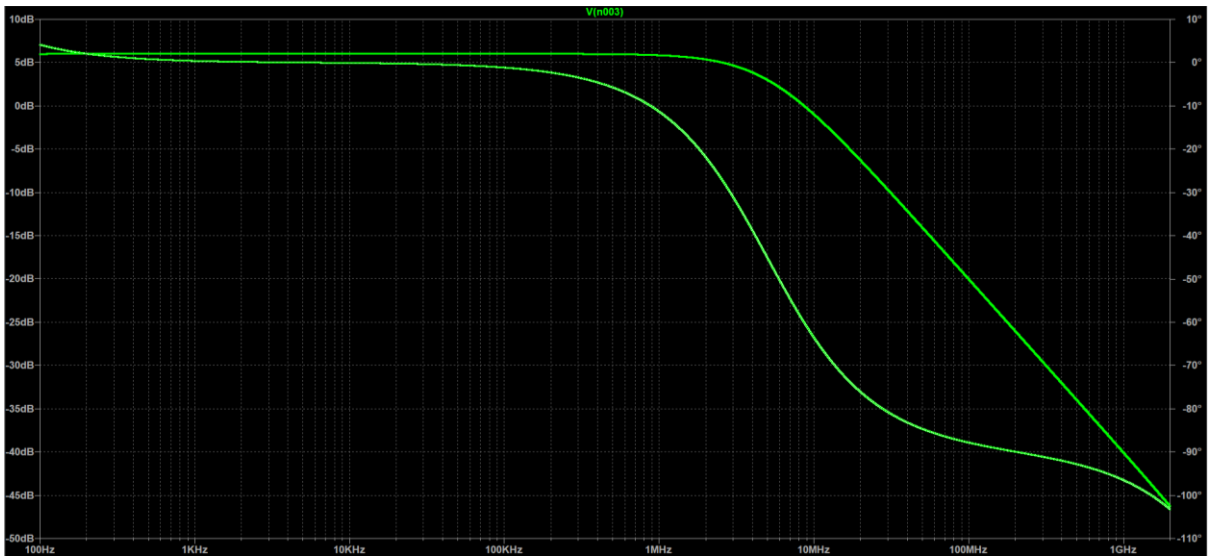
100p	
10p	
1p	

At very small values of capacitances, the gain of the circuit is observed to be highly attenuating. The theoretical formula of the closed loop gain in this configuration is independent of the value of the capacitance but still at low capacitances, the gain starts to reduce drastically below its theoretical value. This is because of the effect of parasitic capacitances. An opamp is generally made up of 20-30 transistors, all of which might have some junction capacitances, parasitic capacitances and winding capacitances. The value of these internal capacitances is very small (a few picofarads) and therefore can be

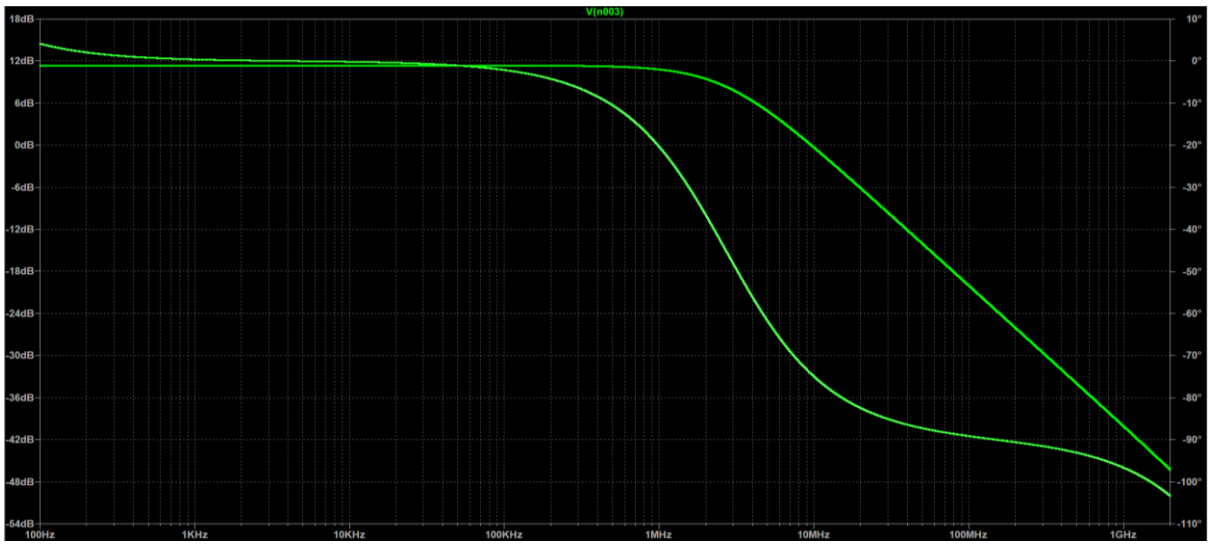
ignored when the external capacitance is high. But when the external capacitance itself is of the same order as these internal capacitances, there effect will become significant and cannot be ignored (as is done in the theoretical formulation). It is due to the intervention of the parasitic capacitances that the gain starts to attenuate heavily at very low capacitance values. In this experiment, the attenuation became visible first at around 1nF and kept on increasing drastically as the values were further reduced to 100pF, 10pF and 1pF.

FREQUENCY RESPONSE

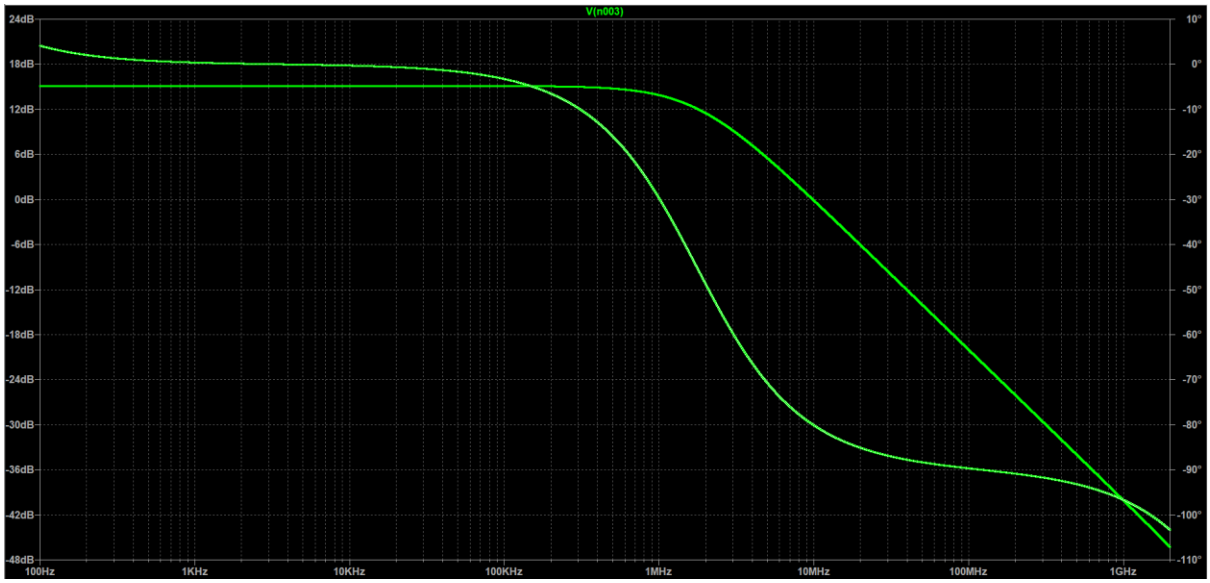
$R_f = 10\ k\Omega$



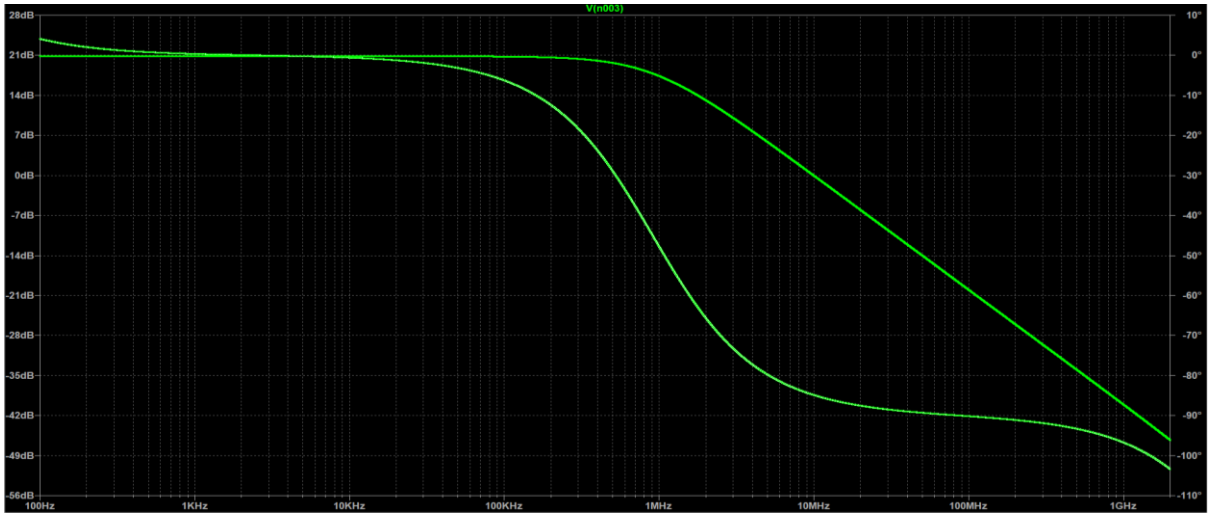
$R_f = 27\ k\Omega$



$R_f = 47\ k\Omega$



$R_f = 100\ k\Omega$



$R_f\ (in\ k\Omega)$	Maximum Gain (in dB)	Cut-Off Frequency / Bandwidth (in Hz)	GBP (in MHz)
10	5.996	5.01M	9.992
27	11.348	2.70M	9.972
47	15.117	1.75M	9.974
100	20.825	905.84K	9.961

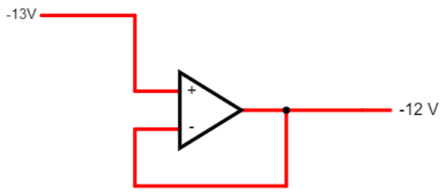
$R_f\ (in\ k\Omega)$	Gain at 100 MHz	Gain at 1 GHz	Roll-Off (in dB / decade)
10	-20.027	-40.077	-20.050
27	-20.020	-40.077	-20.057

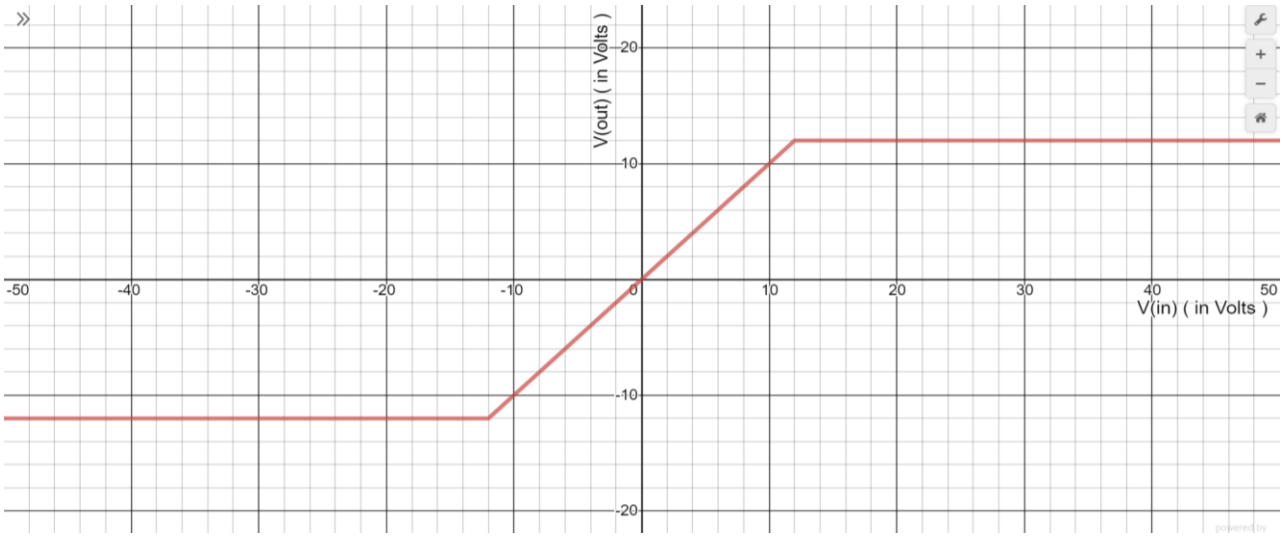
47	-20.018	-40.077	-20.059
100	-20.017	-40.077	-20.060

The bandwidth of the frequency response is observed to decrease with increase in the gain of the circuit. As a result of this, the GBP (gain bandwidth product) is observed to be almost constant. Besides, on increasing the gain of the circuit, the roll off is observed to slightly increase (in magnitude).

SECTION C – VOLTAGE FOLLOWER

$V_{in}(in\ V)$	$V_{out}(in\ V)$
-50	-12
-40	-12
-30	-12
-20	-12
-15	-12
-14	-12
-13	-12
-12	-12
-10	-10
-7	-7
-5	-5
-3	-3
0	0
3	3
5	5
7	7
10	10
12	12
13	12
14	12
15	12
20	12
30	12
40	12
50	12





$$V_{out-sat}^{+} = +12\,V = V_{supply}^{+}$$

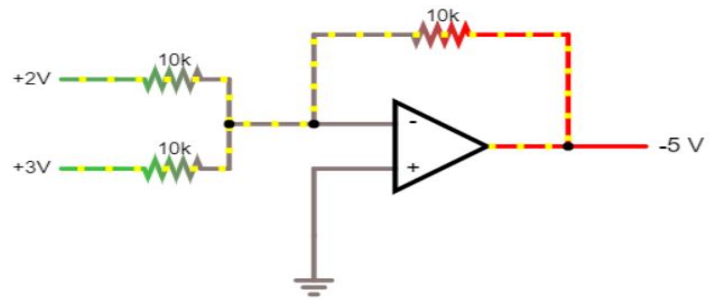
$$V_{out-sat}^{-} = -12\,V = V_{supply}^{-}$$

$$slope\ m = 1\ (for\ linear\ region)$$

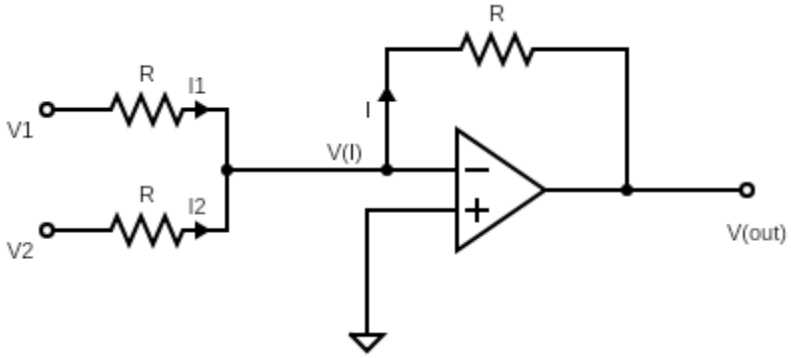
From the voltage transfer characteristics plotted above for the voltage follower circuit, it can be inferred that the input voltage and output voltage are same (both in magnitude and sign/phase) for the input voltage bounded by the negative and positive supply voltages. This result violates for the voltages lying outside this interval and the output gets saturated.

SECTION D – ADDER

SUMMING DC VOLTAGES



For solving the circuit theoretically, consider the virtual ground at the inverting input terminal.



$$V_I = 0\ V$$

$$I_I = \frac{V_1 - V_I}{R} = \frac{V_1}{R}$$

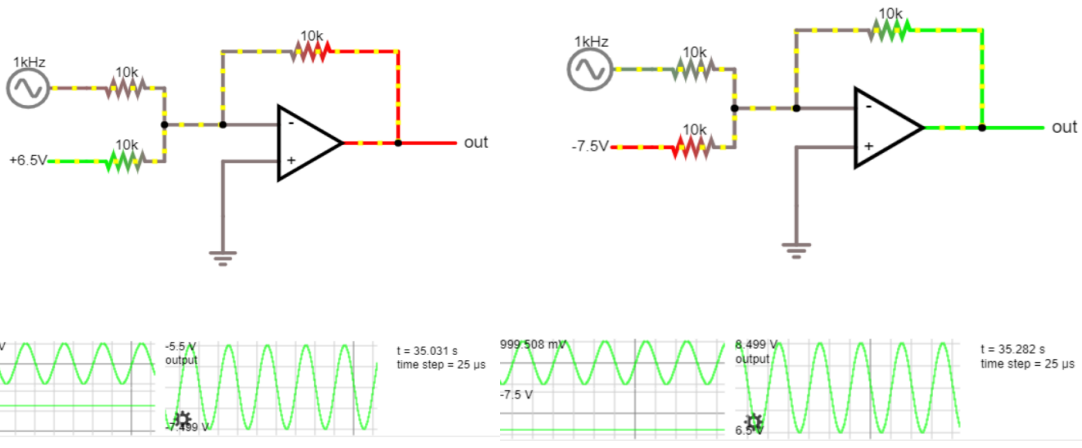
$$I_2 = \frac{V_2 - V_I}{R} = \frac{V_2}{R}$$

$$I = I_I + I_2 = \frac{V_1 + V_2}{R}$$

$$V_{out} = V_I - I * R = -(V_1 + V_2)$$

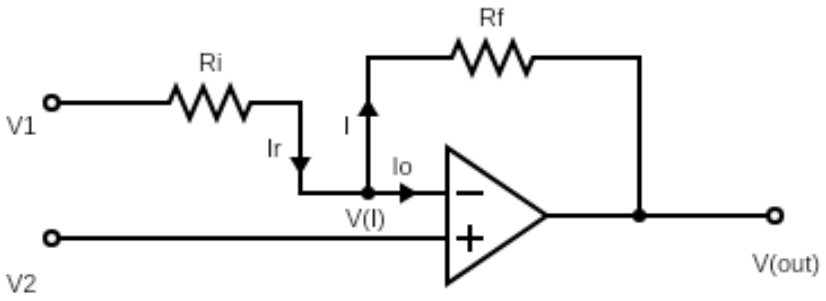
Hence, it is theoretically now established that the above circuit should give the negative of the sum of the two input voltages (provided the three resistances are the same). This can be further extended to any kind of input waveforms other than DC inputs. The following simulation uses the same circuit to superpose AC and a DC input. The theoretical explanation for this will be the same.

SUMMING AMPLIFIER



SECTION E – SUPERPOSITION

FOR DC VOLTAGES



For solving the circuit theoretically, consider the virtual ground at the inverting input terminal. (check "*THEORY*" section to see examples for solving op-amp circuits)

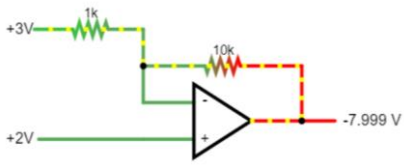
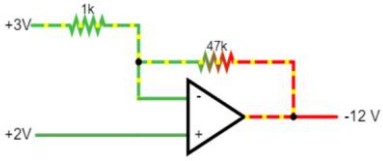
$V_I = V_2 \quad (virtual\ shorting)$

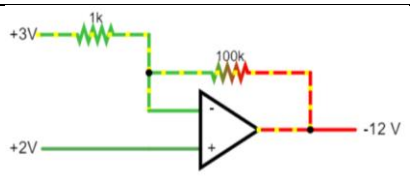
$$I_r = \frac{V_1 - V_I}{R_i} = \frac{V_1 - V_2}{R_i}$$

$I_O = 0 \quad (for\ an\ ideal\ op-amp\ the\ input\ resistance\ is\ infinite)$

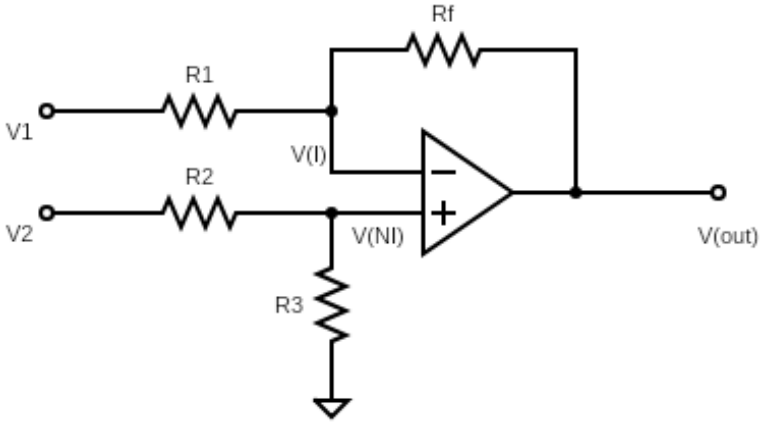
$$I = I_r - I_O = \frac{V_1 - V_2}{R_i}$$

$$V_{out} = V_I - I * R_f = V_2 - \frac{V_1 - V_2}{R_i} * R_f$$

$R_f\ (in\ k\Omega)$	Falstad Simulation	$V_{out}(in\ V)$	Theoretical $V_{out}(in\ V)$
10		-7.999	$2 - \frac{3-2}{1} * 10 = -8$
47		-12.000	$2 - \frac{3-2}{1} * 47 = -45$ The output voltage cannot be less than the negative supply voltage. This implies that the output is saturated at the $V_{supply}^{-} = -12V$

100		-12.000	$2 - \frac{3-2}{1} * 100 = -98$ The output voltage cannot be less than the negative supply voltage. This implies that the output is saturated at the $V_{supply}^{-} = -12V$

DIFFERENTIAL AMPLIFIER



$$V_{NI} = V_2 * \frac{R_3}{R_2 + R_3} \qquad (voltage\ division)$$

$$V_I = V_{NI} = V_2 * \frac{R_3}{R_2 + R_3} \qquad (virtual\ shorting)$$

$$\frac{V_1 - V_I}{R_1} = \frac{V_I - V_{out}}{R_f} \qquad (input\ resistance\ of\ an\ ideal\ op-amp\ is\ infinte)$$

$$V_{out} = V_I - R_f * \frac{V_1 - V_I}{R_1} = V_2 * \frac{R_3}{R_2 + R_3} - \frac{R_f}{R_1}\left(V_1 - V_2 * \frac{R_3}{R_2 + R_3}\right)$$

$$V_{out} = V_2 * \frac{R_3}{R_2 + R_3}\left(1 + \frac{R_f}{R_1}\right) - V_1 \frac{R_f}{R_1}$$

Special case when $R_1 = R_2$ *and* $R_3 = R_f$

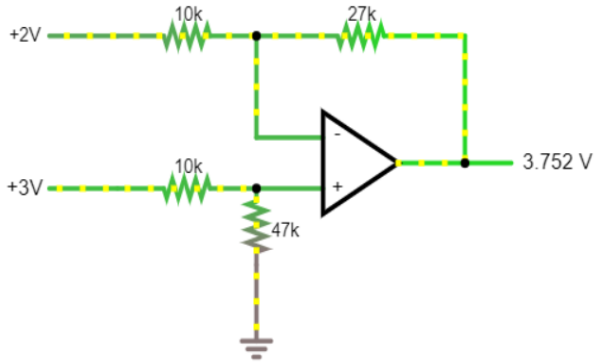
$$V_{out} = V_2 * \frac{R_f}{R_1 + R_f}\left(1 + \frac{R_f}{R_1}\right) - V_1 \frac{R_f}{R_1}$$

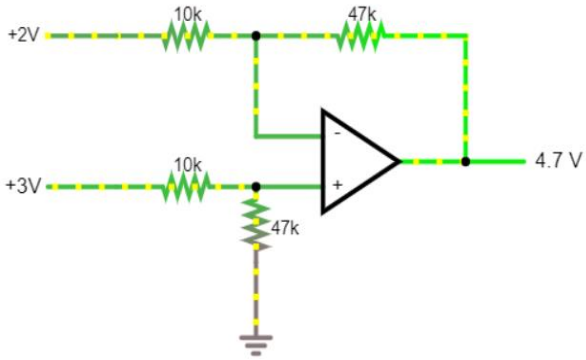
$$V_{out} = V_2 * \frac{R_f}{R_1} - V_1 \frac{R_f}{R_1}$$

$$V_{out} = (V_2 - V_1) * \frac{R_f}{R_1}$$

Therefore, for this particular case, the output voltage is proportional to the difference of the two input voltages. Hence, the above circuit can be used under this condition to work as a difference calculator of two input signals.

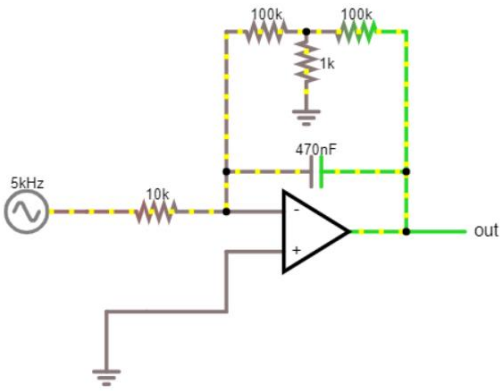
$V_1(V)$	$V_2(V)$	$R_1(k\Omega)$	$R_2(k\Omega)$	$R_3(k\Omega)$	$R_f(k\Omega)$	$V_{out-prac}(V)$	$V_{out-theor}(V)$
2	3	10	10	47	27	3.752	3.753
2	3	10	10	47	47	4.700	4.700

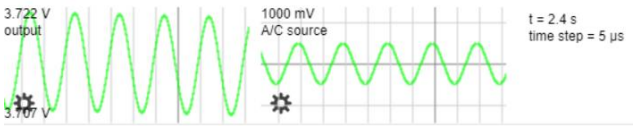




SECTION F – INTEGRATOR

SINUSOIDAL INPUT





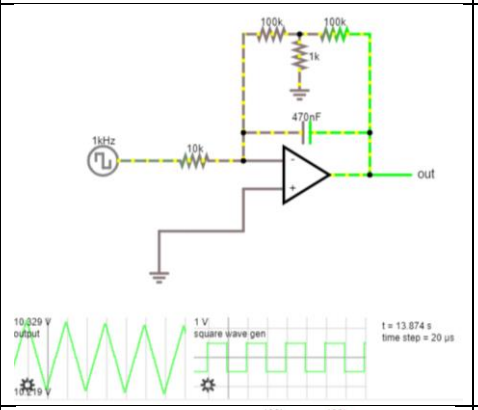
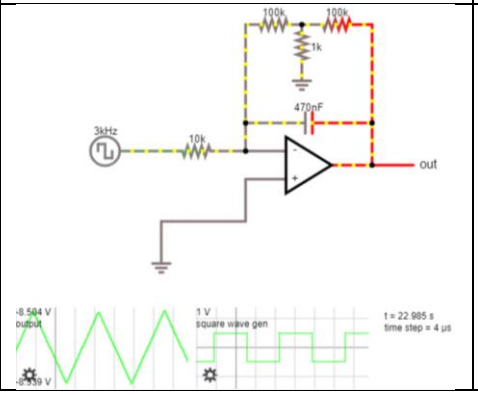
Between the input and the output AC waveforms, a phase difference of 90 degrees was observed. In fact, the output waveform *leads* the input waveform by 90 degrees. This can be explained as follows.

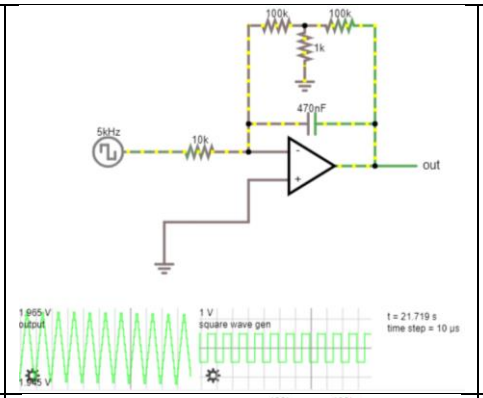
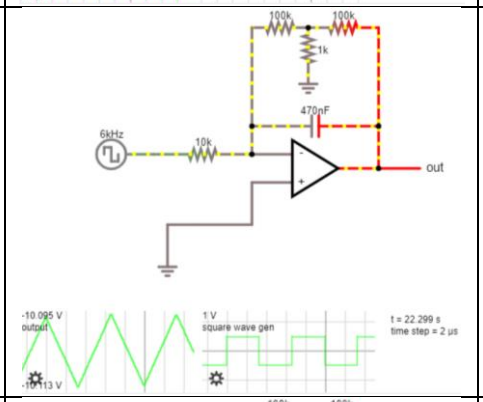
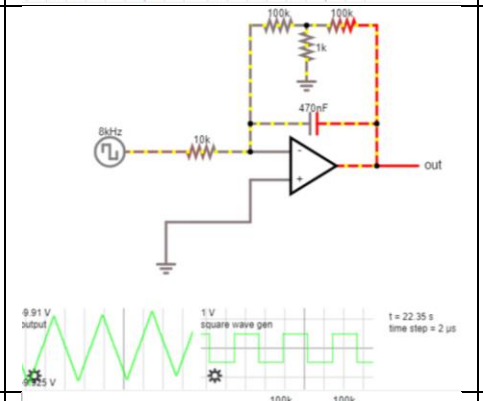
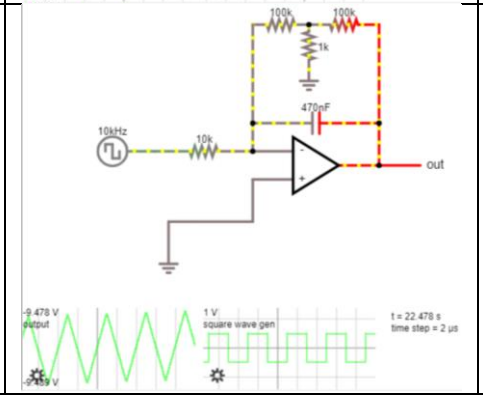
Consider the following input-output relation for the integrator circuit.

$$v_{out} = -\frac{1}{RC}\int v_{in}dt + c$$

v_{in} is a sinusoidal waveform. Its indefinite integral is negative of a co-sinusoid. Due to a negative sign outside the integral, the output waveform will be a cosine function (with some constant DC value). Co-sinusoidal function leads the sinusoidal function by 90 degrees. Therefore, the output waveform leads the input by 90 degrees.

SQUARE WAVE INPUT

Input Frequency (in kHz)	Falstad Simulation	Output Amplitude (in mV)
1		55.00
3		17.50

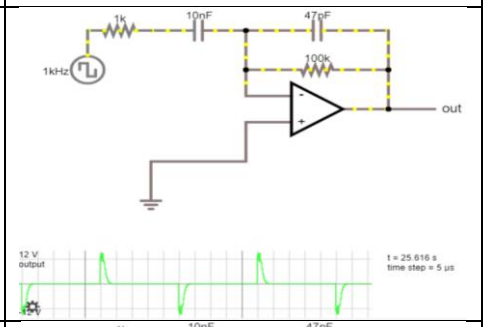
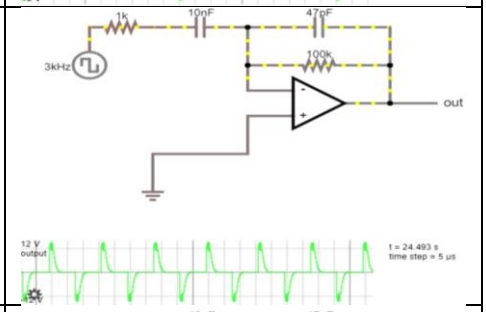
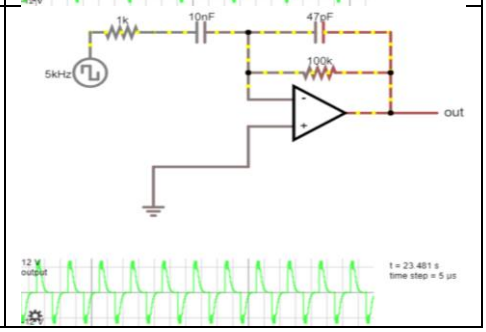
5		10.00
6		9.00
8		7.50
10		5.50

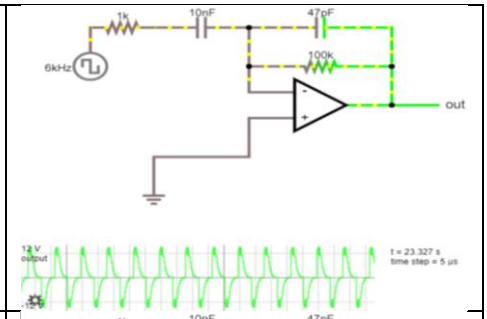
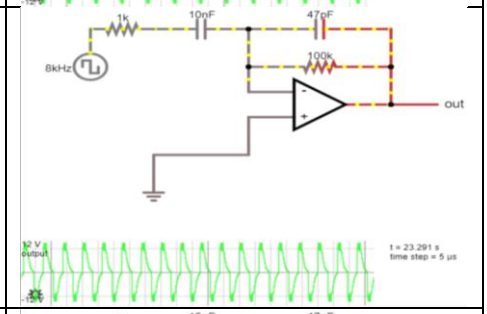
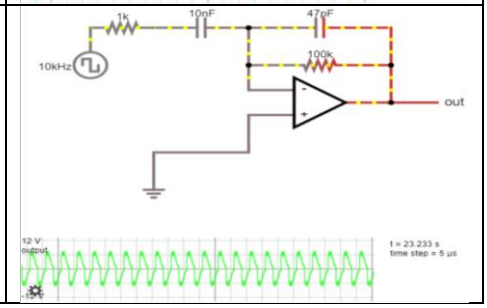
With increasing frequency, the amplitude of the output waveform was observed to decrease. This is in agreement with what is expected theoretically. By Fourier analysis, a square wave can be written as an infinite sum of sinusoids with frequencies as an odd harmonic of the input frequency.

$$\int \sin(wt)\, dt = -\frac{\cos(wt)}{w} + c$$

Consider the above indefinite integration of a sine function. The amplitude of its integral, which is also a sinusoid is inversely proportional to the frequency of the integrand. As a result of this, the amplitude corresponding to the integral of each term of the Fourier series will decrease on increasing the frequency, therefore decreasing the overall amplitude of the output waveform.

SECTION G – DIFFERENTIATOR

Input Frequency (in kHz)	Falstad Simulation
1	
3	
5	

6	
8	
10	

In all the simulations above, the maximum and minimum values on the output waveform were observed to be the same. This can be explained as below.

For an ideal square wave, the rise time and fall time are both zero and therefore, the derivative at the points of step jumps will be infinite. Since, the circuit in the above configuration acts as a differentiator, the output voltage should have been infinite at the time instants of step jumps. But the output voltage of an op-amp is limited by the values of negative and positive supply voltages. Therefore, irrespective of the frequency of the input waveform, the output waveform will remain bounded between the negative and positive supply voltages. For the simulation, the negative supply voltage was taken as -12V and positive as +12V.

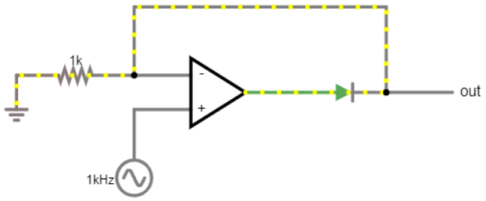
Therefore, $V_{out-max} = 12V$ and $V_{out-min} = -12V$, irrespective of the frequency of the square wave.

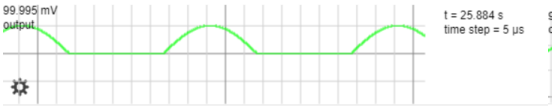
Secondly, the impulse train was observed to become more and more congested as the frequency was increased. That is, the impulses started to occur after lesser gap at high frequencies. This is because the derivative of a periodic signal

is also periodic with the same time period. As the frequency of the input is increased, the output frequency must therefore increase.

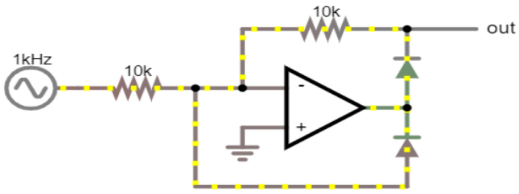
SECTION H – ACTIVE RECTIFIER

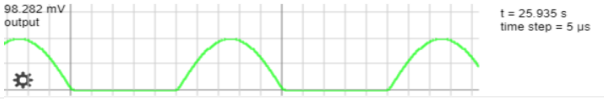
CONFIGURATION O1





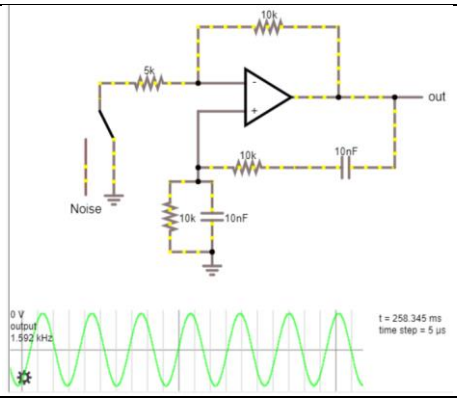
CONFIGURATION O2

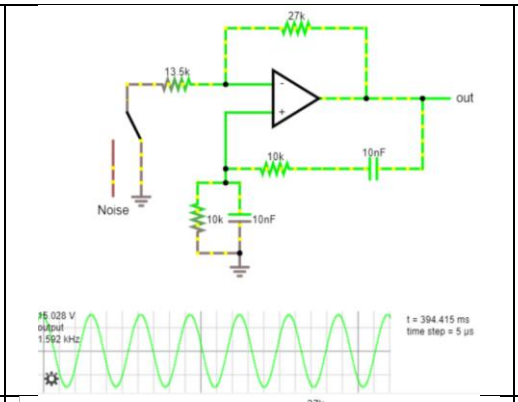
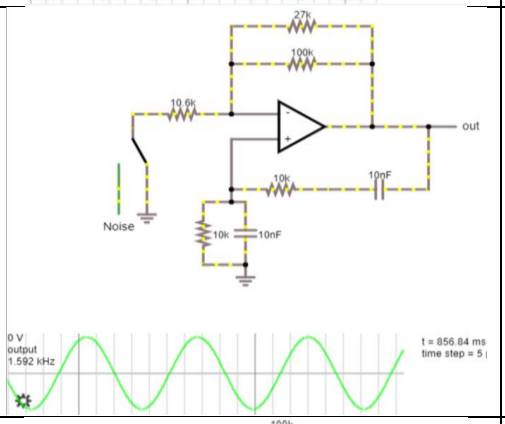
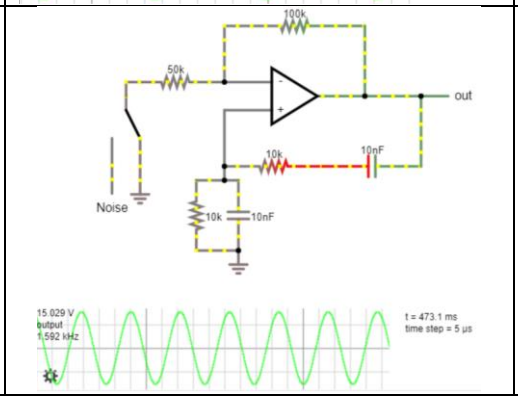




SECTION I – WEIN BRIDGE OSCILLATOR

$$f_{osc-theoretical} = \frac{1}{2\pi RC} = \frac{1}{2 * 3.141 * 10^4 * 10^{-8}} = 1.592\ kHz$$

$R_f(k\Omega)$	Falstad Simulation	$f_{osc-prac}$ (in kHz)	$R_{i-osc}(k\Omega)$	R_f/R_{i-osc}
10		1.592	5	2.00

27		1.592	13.5	2.00
27||100		1.592	10.6	2.01
100		1.592	50	2.00

The ratio R_f/R_i for which a good sinusoidal output waveform was observed is 2. Therefore, based on the observations, the resistance R_f should be twice the resistance R_i for the oscillations to occur. Moreover, the frequency of oscillations at the appropriate ratio is equal to the theoretical value of the frequency.