INTRODUCTION TO ELECTRONICS LAB EC29003 EXPERIMENT O4

STUDY ON SMALL SIGNAL CE AMPLIFIER

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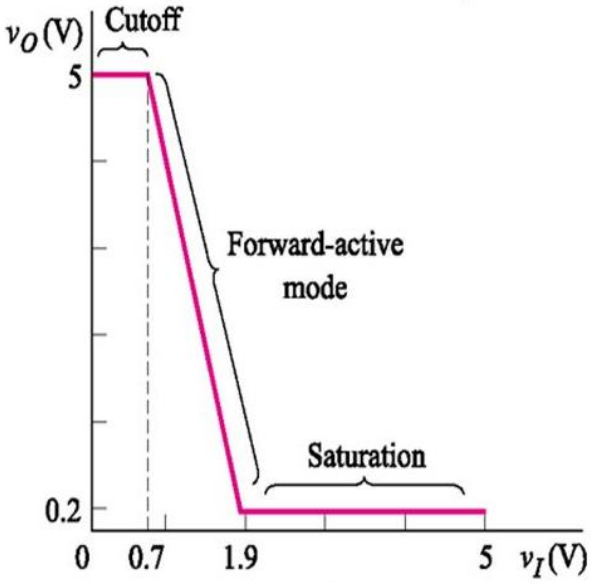
EXPERIMENT O4

STUDY ON SMALL SIGNAL CE AMPLIFIER

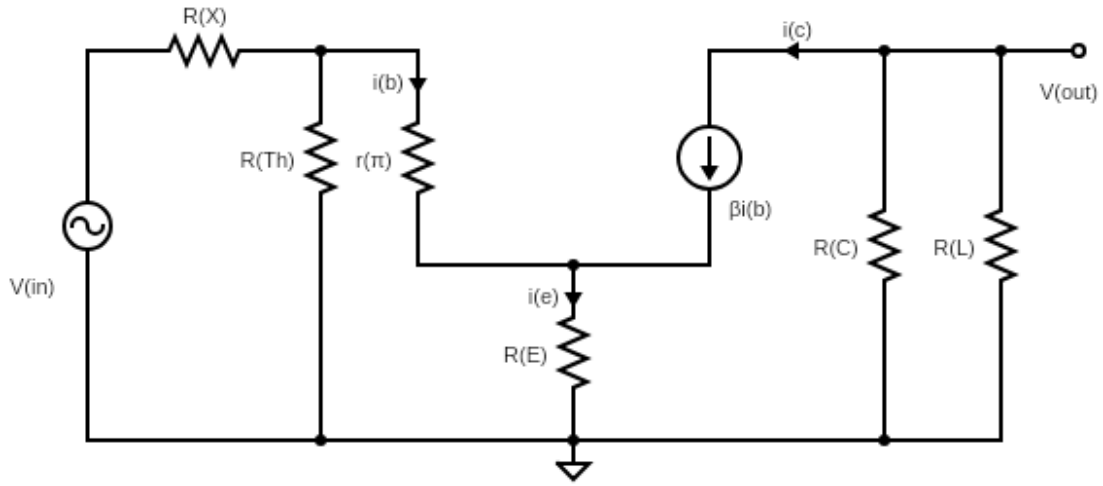
AIM: To study small signal common emitter amplifier and determine the frequency response of the amplifier under various conditions. To practically determine the values of input and output impedances of an amplifier in common emitter configuration.

THEORY:

The following are the voltage transfer characteristics of a bipolar junction transistor. For the transistor to serve as an amplifier, it must operate in the forward active region. From the voltage transfer characteristics, it is clear that the slope in the forward active mode is greater than one and hence the swing of the input sinusoidal signal will be amplified by the slope of this straight line. Also, since the slope of the voltage transfer characteristics in the forward active mode is negative, there is a 180-degree phase difference between the input and the output voltage waveform.



Refer to the "*CIRCUIT DIAGRAMS*" to have a look at the circuit of an amplifier in common emitter configuration. The following is the small signal hybrid pi model equivalent of the common emitter BJT amplifier.



Though transistor is a non-linear device, but for a small signal the I-V characteristics for the transistor can be very nicely approximated as linear characteristics. The hybrid pi model can be solved like any other electrical circuit containing linear elements. One very important thing to note is that there are a few parameters in the pi model that are not directly present in the amplifier circuit, for instance r_π known as *internal resistance*. Its value depends on the Q-point or the DC conditions of the amplifier.

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

Observe the constant current source supplying current βi_b. It is a dependent current source whose value can also be re-written as $g_m v_{be}$ where v_{be} is the voltage dropped across r_π and g_m is known as small signal transconductance.

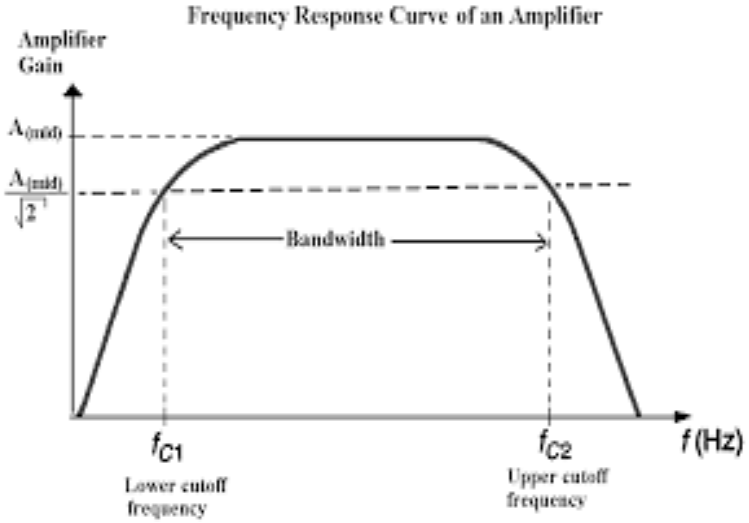
$$g_m = \frac{I_{CQ}}{V_T} = \frac{\beta}{r_\pi}$$

Output voltage is simply the potential drop across the load resistance (or in case load is disconnected take the potential drop across collector resistance). For a more general and practical case, a resistance r_o called small signal collector output resistance is connected in parallel to the load resistance in the pi model to account for the Early effect in the transistor. Refer to the "*OBSERVATIONS AND RELATED THEORY AND CALCULATIONS*" section for detailed analysis of small signal hybrid pi model.

Now, these formulations are only valid when the frequency is moderate, or more formally, when it lies in the mid frequency region. For an amplifier in a particular configuration, the mid frequency band is the range of frequency for which the voltage gain of the amplifier remains constant. Not only is this gain

constant but it is also the maximum attainable gain by the amplifier. The gain of the amplifier reduces outside this mid frequency region and therefore the frequency response of the amplifier looks like that of a band pass filter.

The frequency response of the amplifier is all because of the various capacitances present in the circuit. These capacitances include C_C (coupling capacitance), C_S (source capacitance), C_E (bypass capacitance), C_{CBJ} (base collector junction capacitance), C_{CEJ} (collector emitter junction capacitance), C_{CB} (Miller's capacitance) and C_{WO} (winding capacitance). The capacitances whose values are considerable (in microfarads) like C_S, C_E and C_C cause interreference at low frequencies and reduce the gain. Other capacitances like the internal or junction capacitances and stray wiring capacitances whose values are very small (in picofarads) show their effect at high frequencies.



The voltage and current gain along with input and output resistances for the amplifier can be calculated as follows.

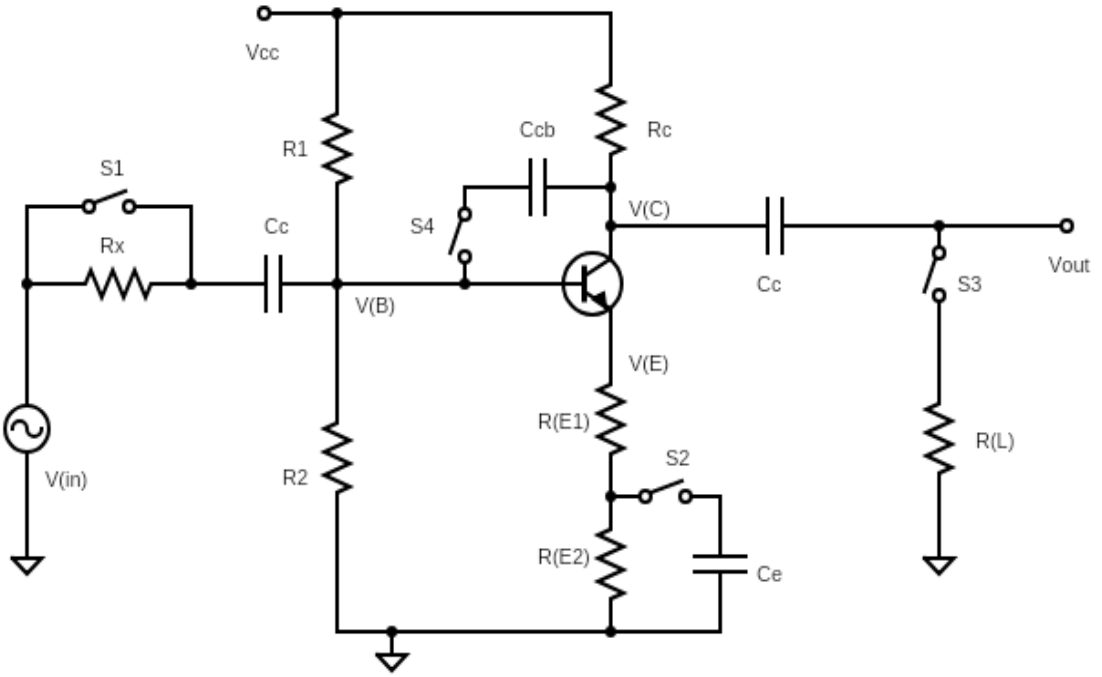
$$A_I = \frac{I_L}{I_{in}}$$

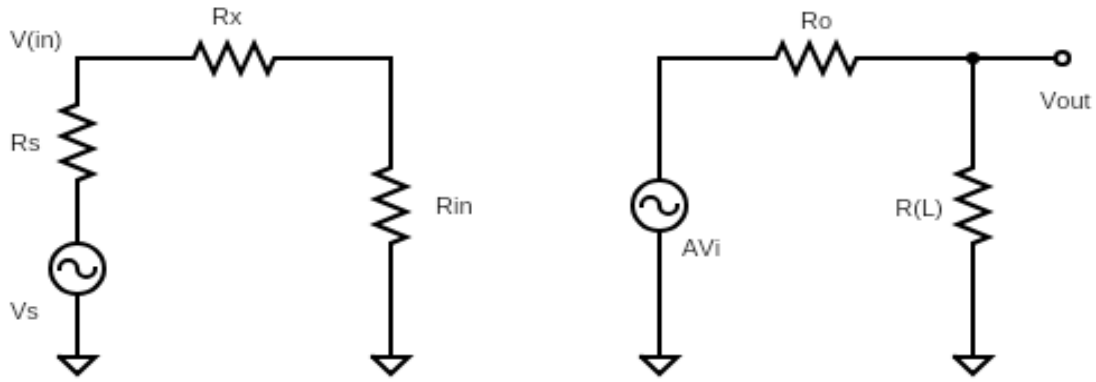
$$R_{input} = \frac{V_{in}}{I_{in}}$$

$$A_V = \frac{V_{out}}{V_{in}} = A_I \frac{R_L}{R_{input}}$$

$$R_{output} = \frac{V_{dc}}{I_{dc}}\Big|_{independent\ sources=0}$$

CIRCUIT DIAGRAMS:

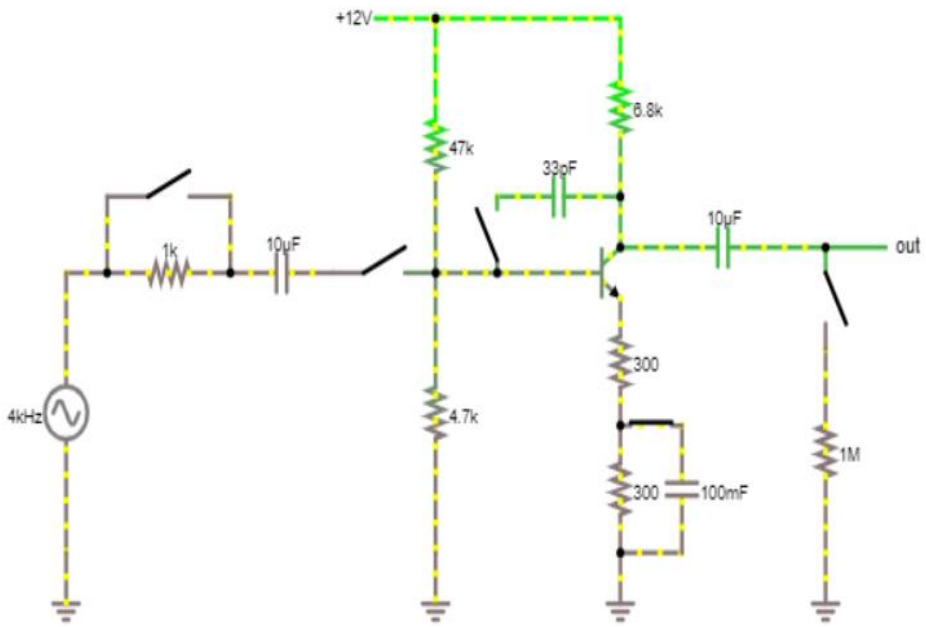




PROCEDURE:

PART I - MEASUREMENT OF DC CONDITIONS

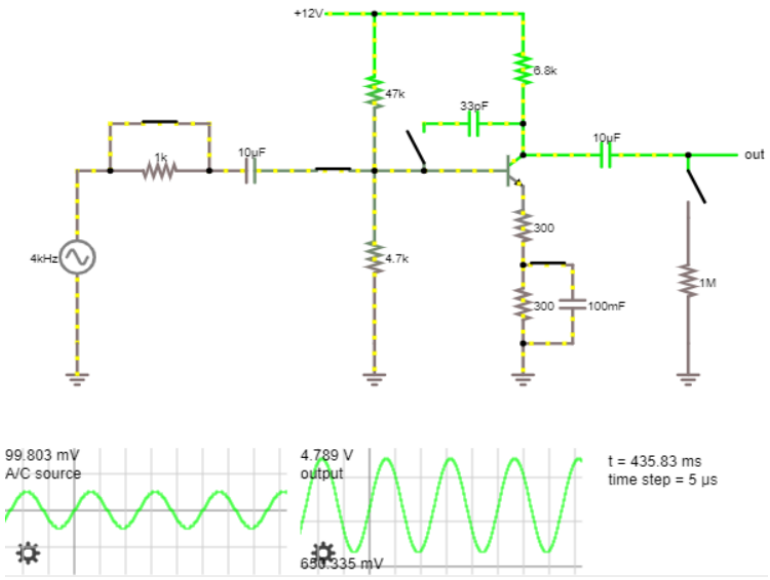
- The first circuit diagram was carefully observed and accordingly connections were made for a npn Bipolar Junction Transistor with β = 100. Suitable values of the components were chosen as shown below.



- For measuring the DC conditions, the AC source was disconnected from the circuit and the voltages V_B, V_C and V_E were measured; along with the base, collector and emitter currents I_B, I_C and I_E.
- Further, the voltages V_{BE}, V_{CE} and V_{BC} were measured. From these potential differences the operating region of the transistor was concluded and was made sure that it operates in the forward active mode.
- The circuit was solved theoretically to verify the practically measured values of currents and voltages.
- The theoretically obtained voltage-transfer characteristics were studied to conclude if the Q point is stably located, i.e., if the Q point lies at or close to the center of the active region in the voltage transfer characteristics.

PART II - MEASURE SIGNAL HANDLING CAPACITY WITHOUT LOAD

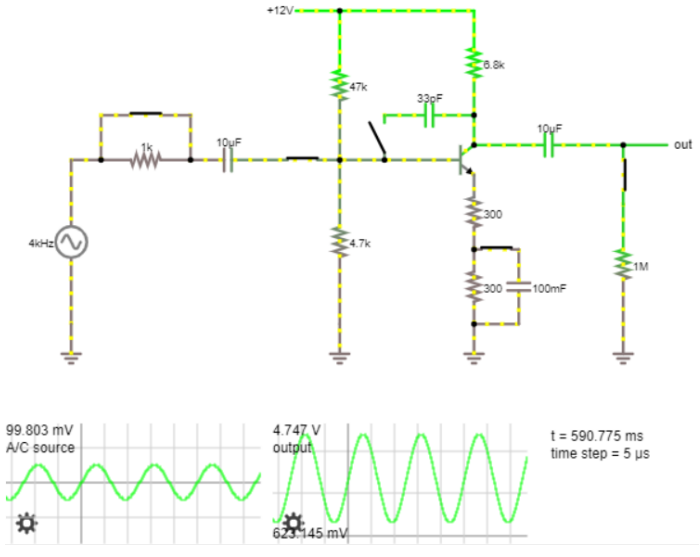
- The AC source was re-connected to the circuit used to measure the DC conditions as shown in the first circuit diagram. The values of the components were kept intact. Switch S_1 was closed to short the resistor R_X.



- Resistor R_{E2} was bypassed by connecting the capacitor C_E across its two terminals, in parallel, upon closing the switch S_2.
- A mid-band frequency of 4kHz sinusoidal voltage of 100mV amplitude was applied at V_{in} and the output waveform was observed and hence the gain was measured.
- The input voltage was increased in steps and the corresponding output voltage amplitude was recorded in a table.
- The maximum input voltage V_{SM} for which the gain remained constant was determined and noted as the signal handling capacity.

PART III - MEASUREMENT OF SIGNAL HANDLING CAPACITY WITH LOAD

- The same circuit was used as in the previous part keeping the values of all the components intact. The switch S_3 was closed to connect the load resistor R_L.



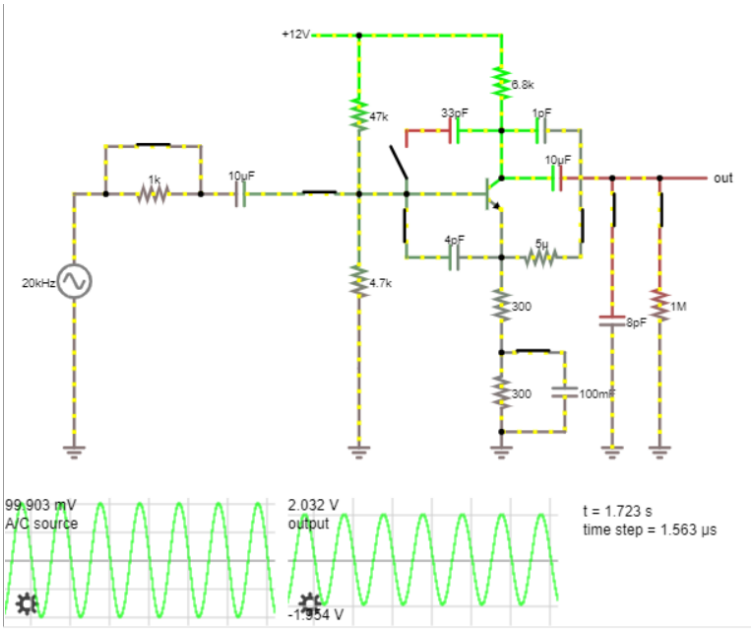
- The same steps were repeated as in the previous part and the signal handling capacity was compared with that obtained in the previous part.

PART IV - FREQUENCY RESPONSE

Note that the junction capacitances and the winding capacitance were connected explicitly because of absence of any of them modelled implicitly for the simulation platform that was used.

PART A – WITH LOAD CONNECTED

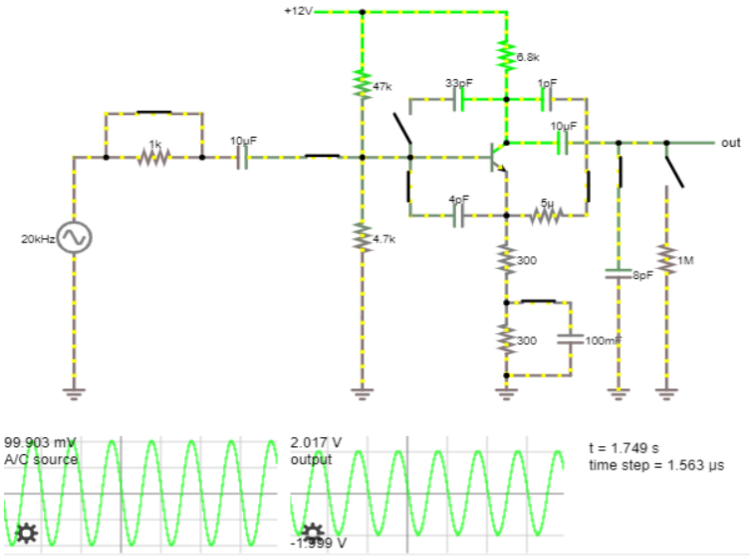
- The same circuit was simulated as in the part II except that the switches S_1, S_3 and S_2 were kept closed (refer to the first circuit diagram).



- A sinusoidal voltage of V_{in} = 100mV was chosen which is well below the value of V_{SM} inferred in the previous parts. The frequency of the AC source was varied over a long range of 100Hz to 20MHz.
- The output voltage V_{out} was measured at each frequency and hence the voltage gain V_{out}/ V_{in} was calculated and the observations were recorded in a table.
- The frequency response of the amplifier was plotted as a $20\log(V_{out}/ V_{in})$ vs frequency graph. From the graph, the lower and upper cut-off frequencies were determined.

PART B – WITH LOAD DISCONNECTED

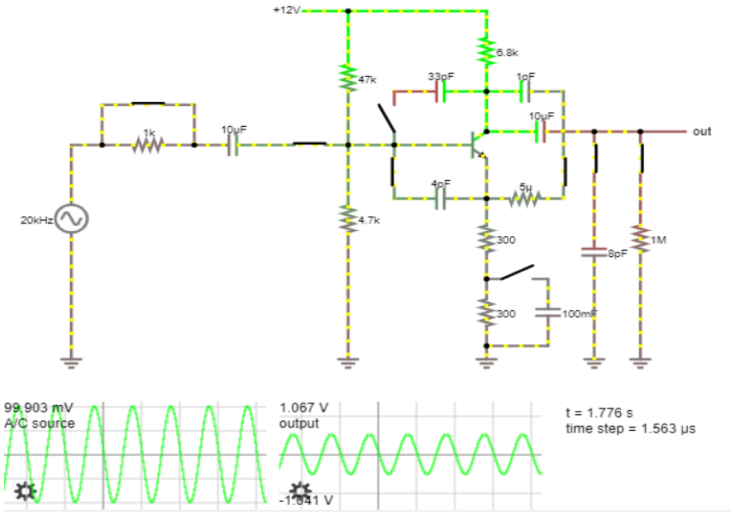
- The same circuit was simulated as in the part IV-A except that the switch S_3 was now opened to disconnect the load resistance R_L (refer to the first circuit diagram).



- The same steps were repeated and the frequency response of this circuit was plotted.
- The frequency response and the cut-off frequencies were compared for both PART A and PART B.

PART C – EFFECT OF C_E (SWITCH S_2 OPENED)

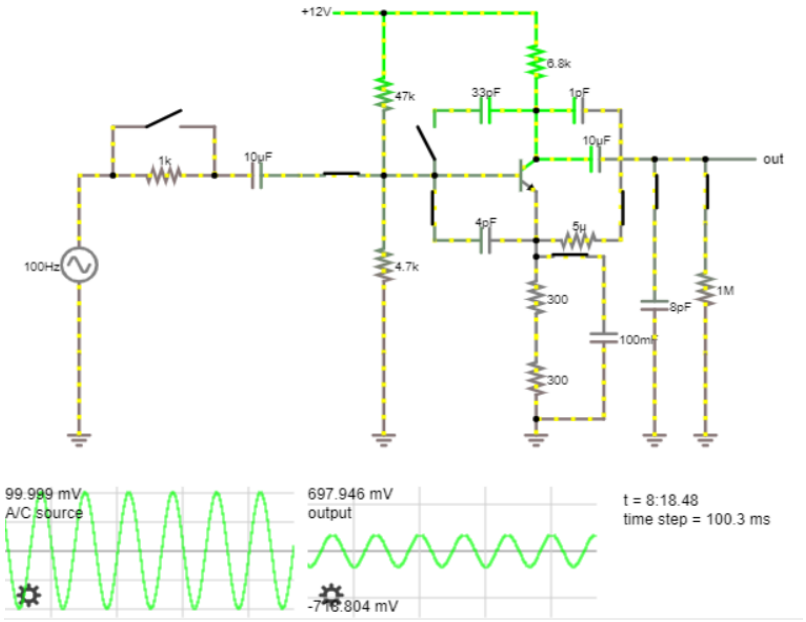
- The same circuit was simulated as in the part IV-A except that the switch S_2 was now opened to disconnect the capacitance C_E (refer to the first circuit diagram).



- The same steps were repeated and the frequency response of this circuit was plotted.
- The frequency response and the cut-off frequencies were compared for PART C with PART A.

PART D – EFFECT OF C_E (BYPASS BOTH R_{E1} AND R_{E2})

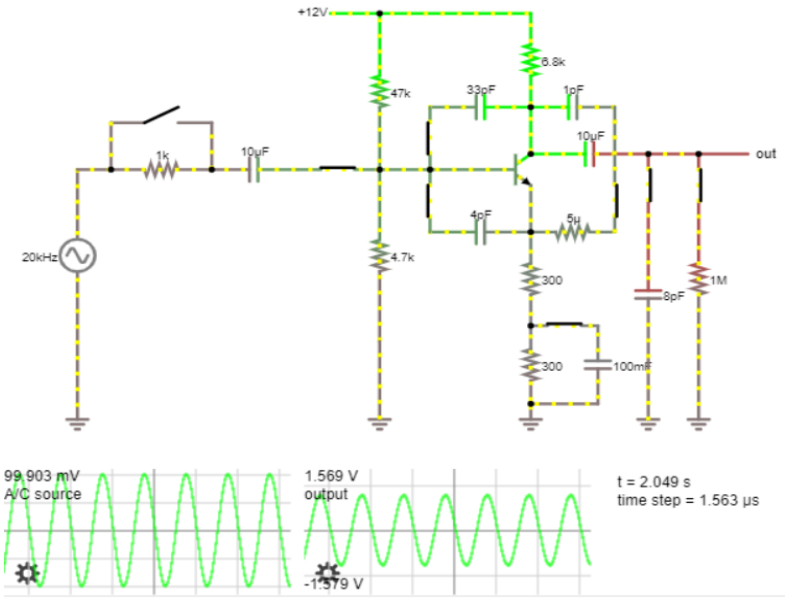
- The same circuit was simulated as in the part IV-A except that the capacitance C_E was now connected across both R_{E1} and R_{E2} (refer to the first circuit diagram). Therefore, now both the emitter resistances where bypassed.



- The same steps were repeated and the frequency response of this circuit was plotted.
- The frequency response and the cut-off frequencies were compared for PART D with PART A.

PART E – MILLER EFFECT OF C_{CB} (SWITCH S_4 CLOSED)

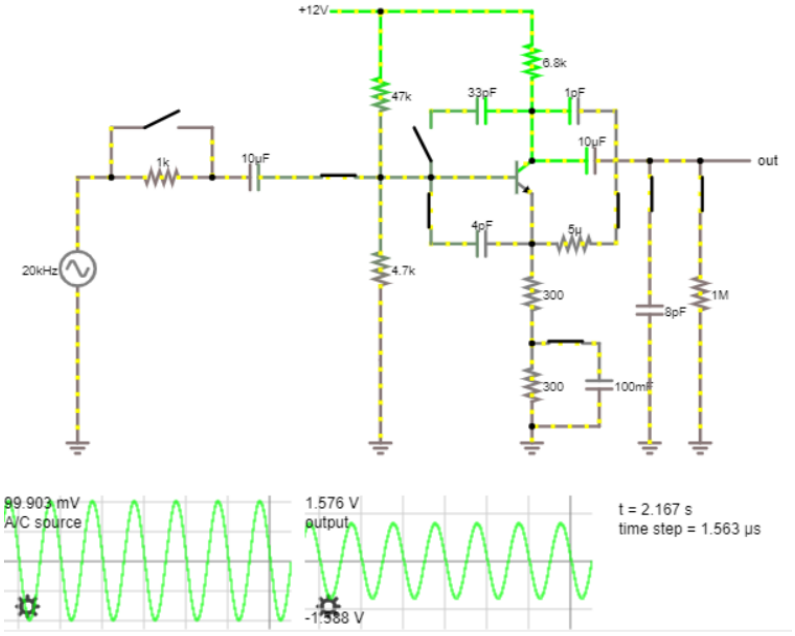
- The same circuit was simulated as in the part IV-A except that the switch S_1 was opened and switch S_4 was closed (refer to the first circuit diagram). Therefore, now the capacitor C_{CB} was connected.



- The same steps were repeated and the frequency response of this circuit was plotted.

PART F – MILLER EFFECT OF C_{CB} (SWITCH S_4 OPENED)

- The same circuit was simulated as in the part IV-E except that the switch S_4 was now opened (refer to the first circuit diagram). Therefore, now the capacitor C_{CB} was disconnected.



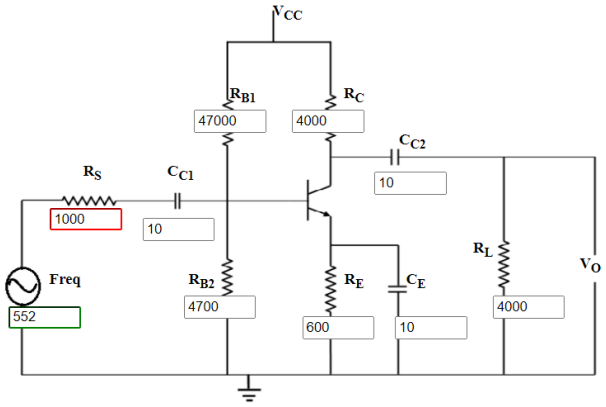
- The same steps were repeated and the frequency response of this circuit was plotted.

- The frequency response and the cut-off frequencies were compared for PART F with PART E.

PART V – SIMULATION ON VIRTUAL LABS

INSTRUCTION

CE Amplifier



CONTROLS

Source Resistance(R_S):	Ω
Collector Resistance(R_C) :	Ω
Emitter Resistance(R_E) :	Ω
Load Resistance(R_L) :	Ω
Base Resistance(R_{B1}) :	Ω
Base Resistance(R_{B2}) :	Ω
Coupling Capacitor(C_{C1}) :	µf
Coupling Capacitor(C_{C2}) :	µf
Bypass Capacitance(C_E) :	µf
Frequency(Freq) :	Hz

Add to Table | Plot | Clear

EXPERIMENTAL TABLE

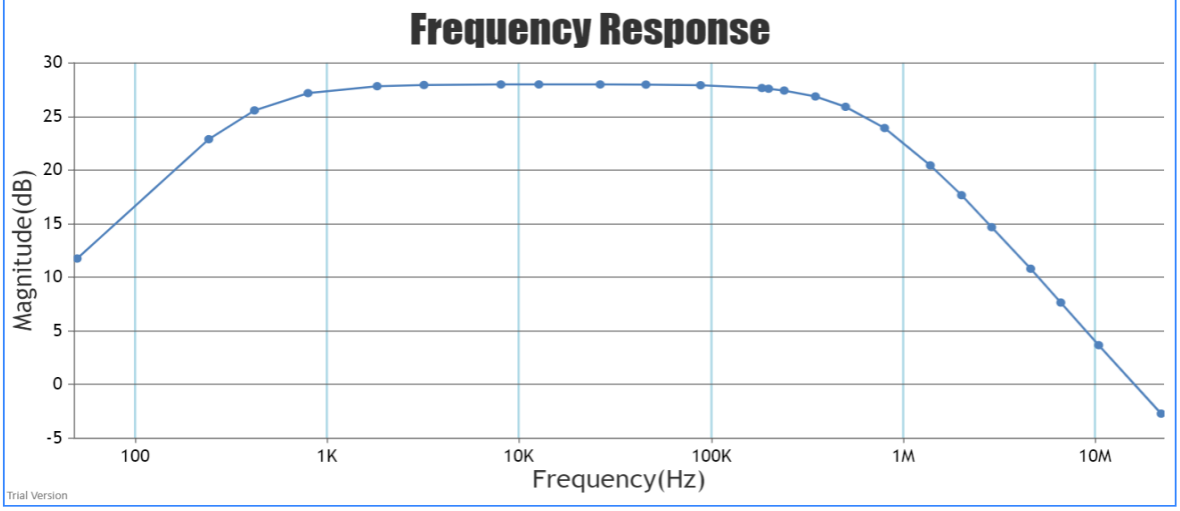
Serial No.	Frequency(Hz)	Magnitude(dB)
1	50	11.76372
2	241	22.8994
3	419	25.583999999999996
4	798	27.195999999999998
5	1827	27.845
6	3176	27.956599999999998
7	7977	28.0034

GRAPH PLOT

Midband gain= -25.1568

Low frequency cut-off = 2287.53817131 Hz

High frequency cut-off= 4.01933e+6 Hz



OBSERVATIONS AND RELATED THEORY AND CALCULATIONS:

MEASUREMENT OF DC CONDITIONS

The practically determined values of voltages and currents for the circuit simulated in the first part of the experiment are as follows. *(Refer to the Falstad circuit in the first part of the experiment and the first circuit diagram on the second page).*

$V_E = 468.917\ mV$

$V_B = 1.058\ V$

$V_C = 6.738\ V$

$V_{BE} = 588.93\ mV$

$V_{CB} = 5.680\ V$

$V_{CE} = 6.269\ V$

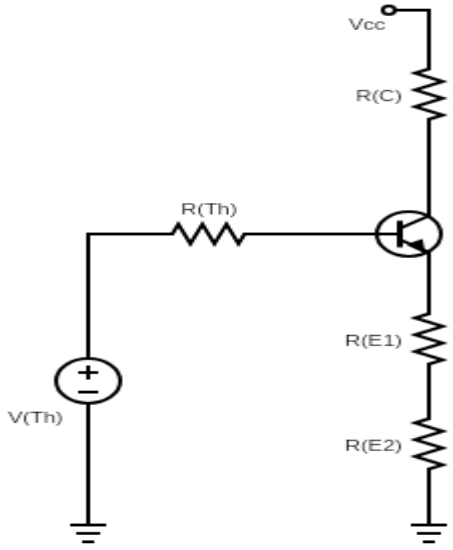
$I_E = 781.528\ \mu A$

$I_B = 7.738\ \mu A$

$I_C = 773.79\ \mu A$

The theoretical solution of the circuit simulated in the first part of the experiment is as follows.

Consider the following simplified model of the same circuit.



All the capacitors are removed from the simplified model because in steady state, a capacitor acts like an open circuit to DC input.

$$R_{Th} = \frac{R_1\, R_2}{R_1 + R_2} = \frac{47 * 4.7}{47 + 4.7} = 4.273\ k\Omega$$

$$V_{Th} = V_{CC}\frac{R_2}{R_1 + R_2} = 12 * \frac{4.7}{47 + 4.7} = 1.091\ V$$

Apply KVL on the loop containing base − emitter junction

$$V_{Th} = R_{Th}I_B + V_{BE} + I_E * (R_{E1} + R_{E2})$$

Assume that transistor is operating in the forward active region

$$Therefore \quad I_E = (1 + \beta)I_B$$

Put I_E in terms of I_B in the KVL equation

(take the knee voltage in forward bias as $V_{BE-on} = 0.6\ V$)

$$I_B = \frac{V_{Th} - V_{BE-on}}{R_{Th} + (1 + \beta) * (R_{E1} + R_{E2})} = \frac{1.091 - 0.6}{4.273 + \frac{(1 + 100)}{1000} * (300 + 300)}$$

$$= 7.568\ \mu A$$

$$I_E = (1 + 100) * 7.568 = 764.368\ \mu A$$

$$I_C = 7.568 * 100 = 756.800\ \mu A$$

$$V_{BE} = 600.00\ mV$$

$$V_C = V_{CC} - I_C R_C = 12 - 756.8 * 6.8 * 0.001 = 6.854\ V$$

$$V_E = I_E * (R_{E1} + R_{E2}) = 764.368 * 0.001 * (300 + 300) = 458.621\ mV$$

$$V_B = V_E + V_{BE} = 458.621 + 600 = 1.059\ V$$

$$V_{CB} = V_C - V_B = 6.854 - 1.059 = 5.795\ V$$

$$V_{CE} = V_C - V_E = 6.854 - 458.621 * 0.001 = 6.395\ V$$

Parameter	Practical Value	Theoretical Value
V_E	468.917 mV	458.621 mV
V_B	1.058 V	1.059 V
V_C	6.738 V	6.854 V
V_{BE}	588.93 mV	600.00 mV
V_{CB}	5.680 V	5.795 V
V_{CE}	6.269 V	6.395 V
I_E	781.528 μA	764.368 μA

I_B	$7.738\ \mu A$	$7.568\ \mu A$
I_C	$773.79\ \mu A$	$756.800\ \mu A$

For a npn transistor in common emitter configuration to operate in the forward active region, the potential differences V_{CB} and V_{BE} must be positive. That is, base emitter junction must be forward biased and base collector junction must be reverse biased. This condition is satisfied for the practical values determined for the circuit. Hence, *the circuit operates in forward active mode* for these values of components and can be used as an amplifier. Moreover, the theoretical calculations were done assuming the transistor operates in the active mode. Since, the conclusion drawn supports the assumption that was made, all the calculations are valid.

MEASUREMENT OF SIGNAL HANDLING CAPACITY WITHOUT LOAD

$V_{in}(mV)$	$V_{out}(V)$	$gain = V_{out}/V_{in}$
100	2.010	20.1
102	2.049	20.1
104	2.090	20.1
106	2.129	20.1
108	2.167	20.1
110	2.209	20.1
112	2.249	20.1
114	2.289	20.1
116	2.328	20.1
118	2.368	20.1
119	2.387	20.1
120	2.406	20.0

The gain remains almost constant as the amplitude of the input AC voltage is slowly increased from 100mV to 119mV. At 120mV a slight drop is observed. Therefore, the signal handling capacity of the circuit (without load) is

$$V_{SM} = 119mV$$

MEASUREMENT OF SIGNAL HANDLING CAPACITY WITH LOAD

The signal handling capacity of the amplifier reduces when the load is connected. Signal handling capacity is defined as the maximum amplitude of the input AC signal that can be passed through the amplifier without the BJT trespassing into saturation or the cut-off region, i.e., the output signal should remain undistorted / unclipped.

$V_{in}(mV)$	$V_{out}(V)$	$gain = V_{out}/V_{in}$
100	1.993	19.94
102	2.034	19.94
104	2.074	19.94
106	2.114	19.94
107	2.134	19.94
108	2.153	19.93

The gain remains almost constant as the amplitude of the input AC voltage is slowly increased from 100mV to 107mV. At 108mV a slight drop is observed. Therefore, the signal handling capacity of the circuit (without load) is

$$V_{SM} = 107mV$$

When the switch S_3 is closed (refer to the first circuit diagram) and the load is connected to the circuit, the value of V_{SM} is observed to decrease. Therefore, the signal handling capacity of the circuit reduces when the load is connected.

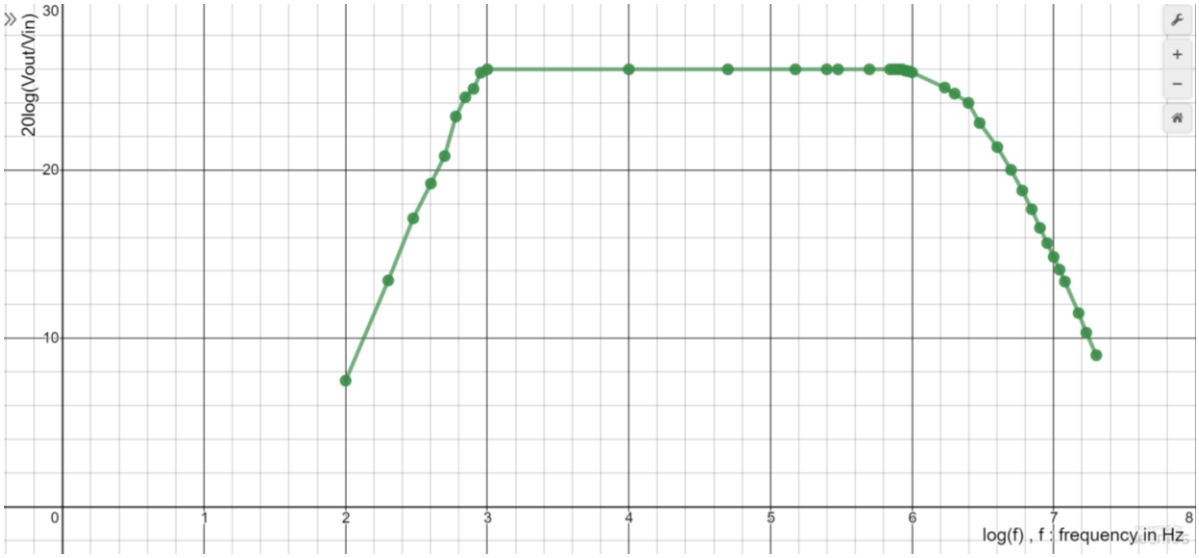
MEASUREMENT OF FREQUENCY RESPONSE

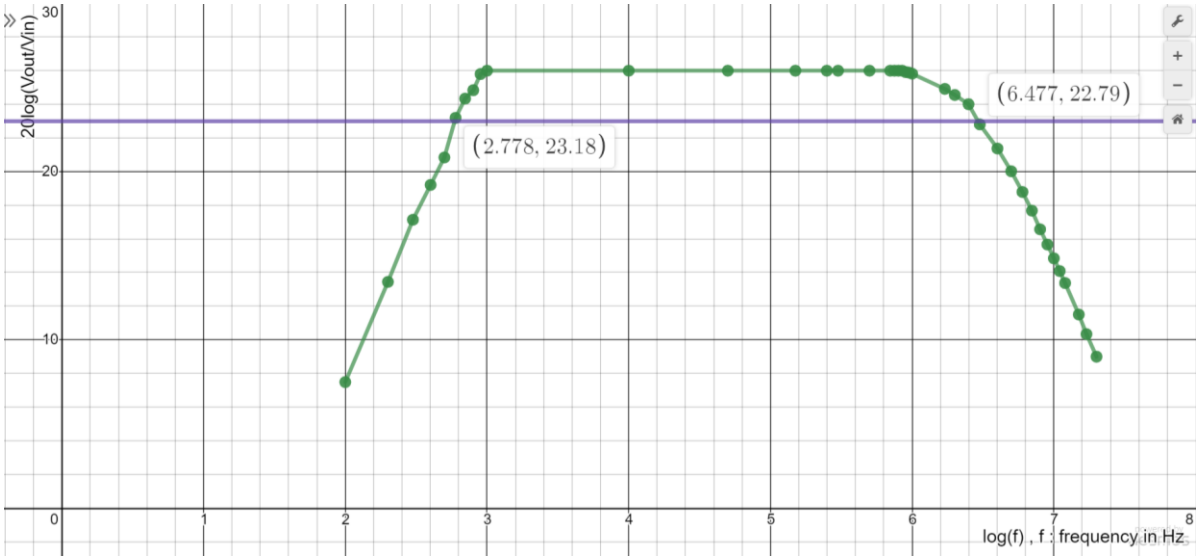
PART A – WITH LOAD CONNECTED

$V_{in} = 100\ mV$

$Frequency\ (Hz)$	$V_{out}(V)$	$gain = V_{out}/V_{in}$	$20 * \log(gain)$
100	0.237	2.37	7.49
200	0.470	4.70	13.44
300	0.719	7.19	17.13
400	0.912	9.12	19.20
500	1.101	11.01	20.83
600	1.443	14.43	23.18
700	1.645	16.45	24.32

800	1.741	17.41	24.82
900	1.946	19.46	25.78
1k	1.991	19.91	25.98
10k	1.991	19.91	25.98
50k	1.991	19.91	25.98
150k	1.991	19.91	25.98
250k	1.991	19.91	25.98
300k	1.991	19.91	25.98
500k	1.991	19.91	25.98
700k	1.991	19.91	25.98
750k	1.991	19.91	25.98
800k	1.991	19.91	25.98
850k	1.991	19.91	25.98
900k	1.972	19.72	25.90
950k	1.966	19.66	25.87
1.0M	1.950	19.50	25.80
1.7M	1.758	17.58	24.90
2.0M	1.686	16.86	24.54
2.5M	1.583	15.83	23.99
3.0M	1.379	13.79	22.79
4.0M	1.169	11.69	21.36
5.0M	1.001	10.01	20.01
6.0M	0.869	8.69	18.78
7.0M	0.765	7.65	17.67
8.0M	0.673	6.73	16.56
9.0M	0.607	6.07	15.66
10.0M	0.552	5.52	14.84
11.0M	0.506	5.06	14.08
12.0M	0.466	4.66	13.37
15.0M	0.376	3.76	11.50
17.0M	0.329	3.29	10.34
20.0M	0.282	2.82	9.00





Lower cut-off frequency f_L = 562.34 Hz (from the plot)

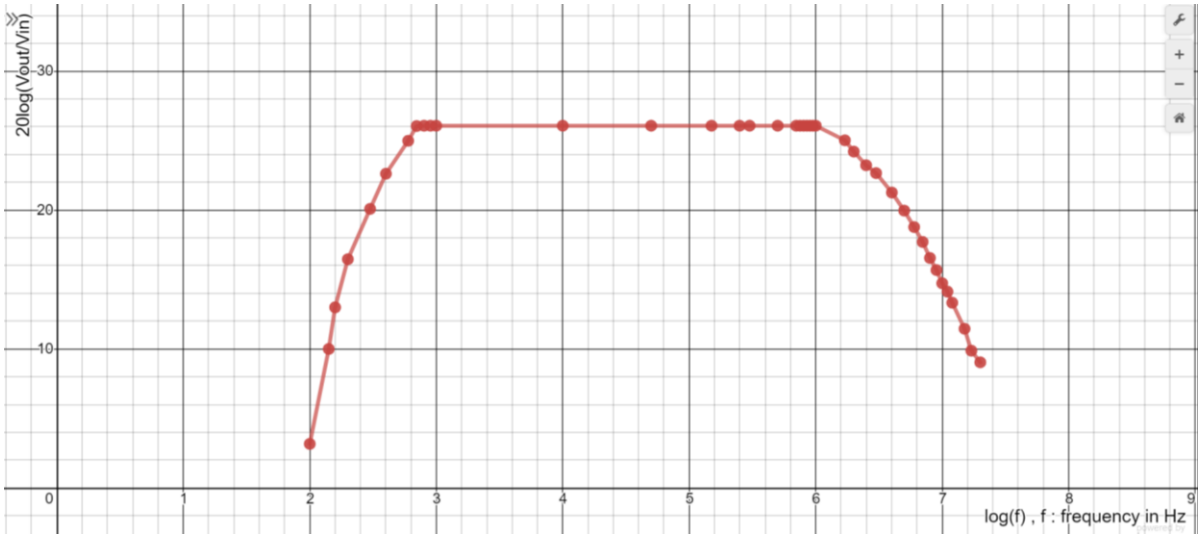
Higher cut-off frequency f_H = 2.67 MHz (from the plot)

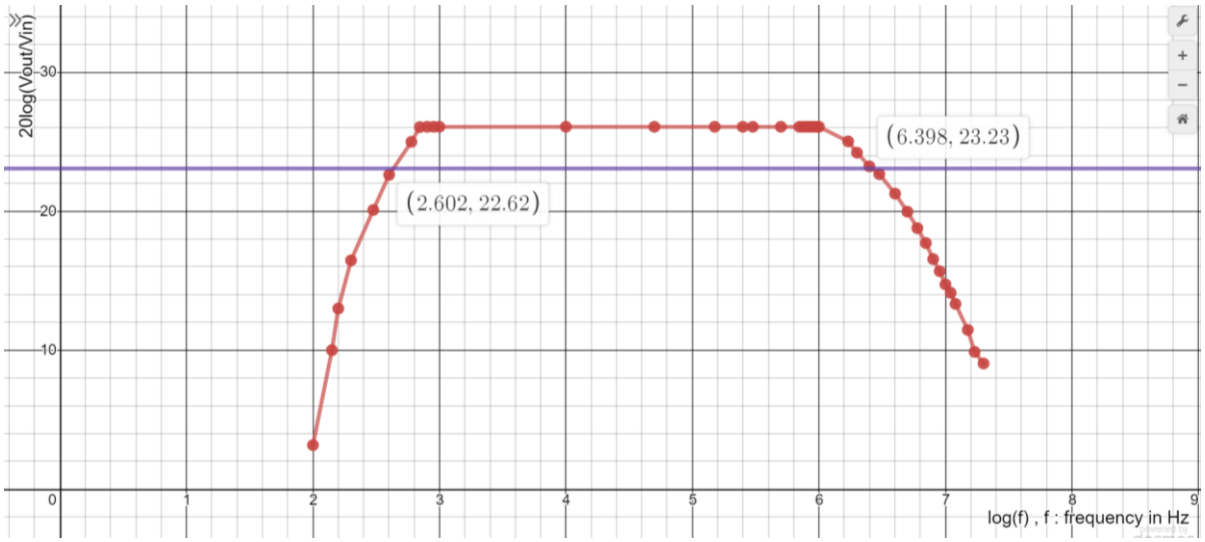
PART B – WITH LOAD DISCONNECTED

$V_{in} = 100\ mV$

$Frequency\ (Hz)$	$V_{out}(V)$	$gain = V_{out}/V_{in}$	$20 * (\log(gain)$
100	0.144	1.44	3.17
200	0.665	6.65	16.46
300	1.011	10.11	20.09
400	1.352	13.52	22.62
500	1.663	16.63	24.42

600	1.851	18.51	25.35
700	2.006	20.06	26.05
800	2.012	20.12	26.07
900	2.012	20.12	26.07
1k	2.012	20.12	26.07
10k	2.012	20.12	26.07
50k	2.012	20.12	26.07
150k	2.012	20.12	26.07
250k	2.012	20.12	26.07
300k	2.012	20.12	26.07
500k	2.012	20.12	26.07
700k	2.012	20.12	26.07
750k	2.012	20.12	26.07
800k	2.012	20.12	26.07
850k	2.012	20.12	26.07
900k	2.012	20.12	26.07
950k	2.012	20.12	26.07
1.0M	2.012	20.12	26.07
1.7M	1.782	17.82	25.02
2.0M	1.623	16.23	24.21
2.5M	1.450	14.50	23.23
3.0M	1.358	13.58	22.66
4.0M	1.156	11.56	21.26
5.0M	0.996	9.96	19.96
6.0M	0.869	8.69	18.78
7.0M	0.768	7.68	17.71
8.0M	0.672	6.72	16.55
9.0M	0.608	6.08	15.68
10.0M	0.545	5.45	14.73
11.0M	0.509	5.09	14.13
12.0M	0.464	4.64	13.33
15.0M	0.374	3.74	11.46
17.0M	0.312	3.12	9.88
20.0M	0.283	2.83	9.04



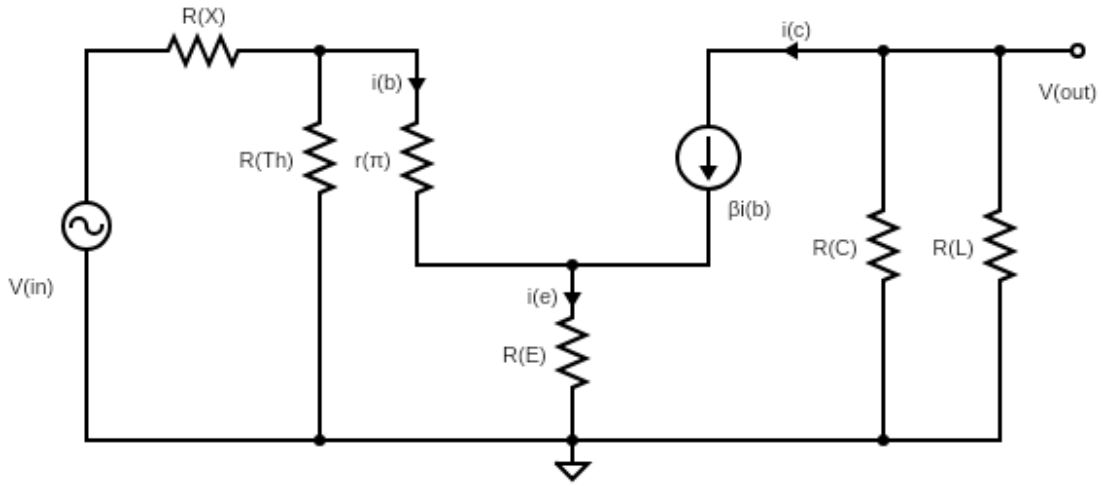


Lower cut-off frequency $f_L = 448.74$ Hz (from the plot)

Higher cut-off frequency $f_H = 2.48$ MHz (from the plot)

Comparison with Part A:

- The maximum gain of the amplifier (that is the gain in the mid-frequency region) increases when the load is disconnected. This is because the presence or absence of load does not affect the Q-point of the transistor and therefore the DC parameters will remain intact.



When the load was connected the current βi_b produced the output voltage V_{out} across $R_C||R_L$ (refer to the above small signal hybrid-pi model for CE amplifier). When the load is disconnected the output-voltage in this model is produced across R_C alone for the same current ($R_C||R_L < R_C$). Hence naturally, the output voltage (or the gain) will increase in the mid frequency region.

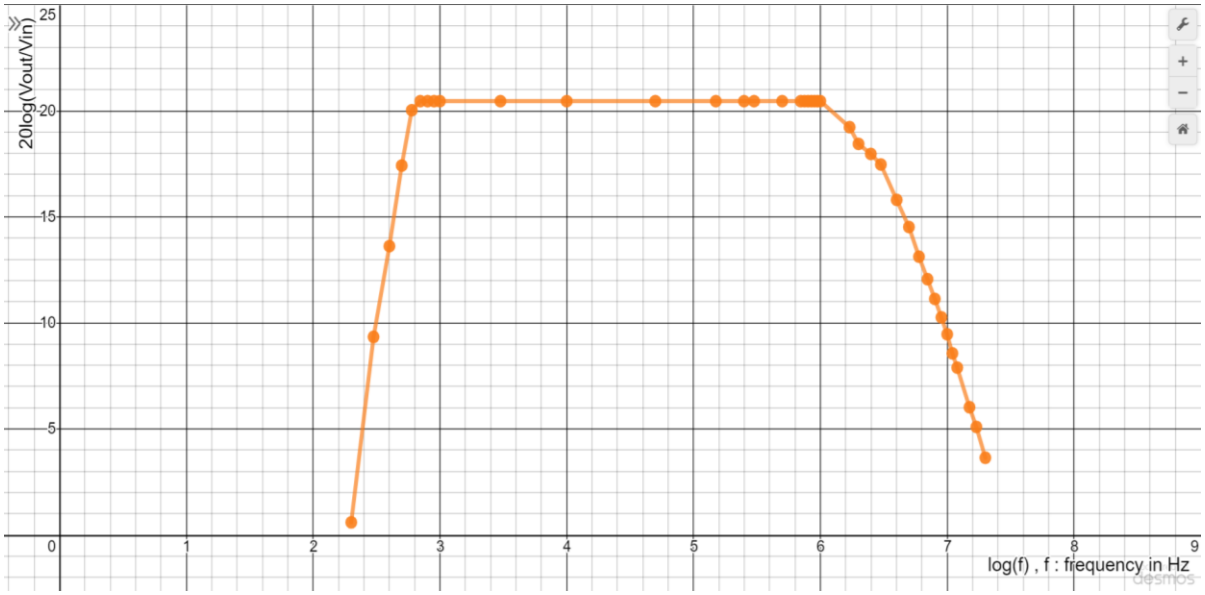
- The cut-off frequencies, both lower and upper, are observed to drop when the load is disconnected. In this particular case, the lower cut-off frequency reduces by 113.58 Hz and the upper cut-off frequency reduces by around 190 kHz.

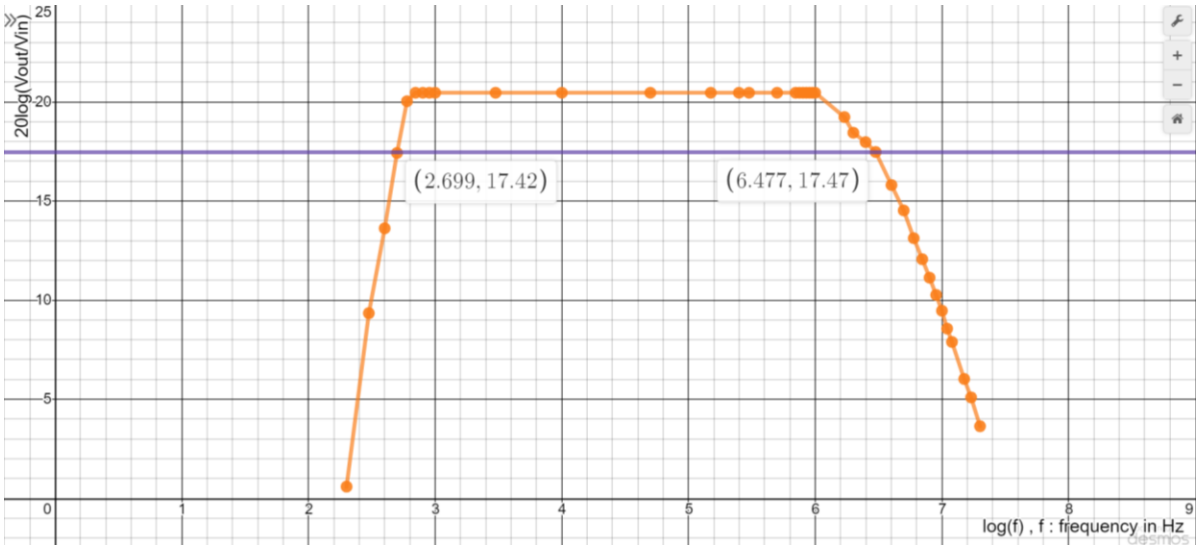
PART C – EFFECT OF C_E (SWITCH S_2 OPENED)

$V_{in} = 100\ mV$

$Frequency\ (Hz)$	$V_{out}(V)$	$gain = V_{out}/V_{in}$	$20 * (\log(gain)$
200	0.107	1.07	0.59
300	0.293	2.93	9.34
400	0.480	4.80	13.62
500	0.743	7.43	17.42
600	1.004	10.04	20.03
700	1.054	10.54	20.46
800	1.054	10.54	20.46
900	1.054	10.54	20.46
1k	1.054	10.54	20.46
10k	1.054	10.54	20.46
50k	1.054	10.54	20.46
150k	1.054	10.54	20.46

250k	1.054	10.54	20.46
300k	1.054	10.54	20.46
500k	1.054	10.54	20.46
700k	1.054	10.54	20.46
750k	1.054	10.54	20.46
800k	1.054	10.54	20.46
850k	1.054	10.54	20.46
900k	1.054	10.54	20.46
950k	1.054	10.54	20.46
1.0M	1.054	10.54	20.46
1.7M	0.915	9.15	19.23
2.0M	0.836	8.36	18.44
2.5M	0.792	7.92	17.97
3.0M	0.747	7.47	17.47
4.0M	0.617	6.17	15.80
5.0M	0.532	5.32	14.52
6.0M	0.453	4.53	13.12
7.0M	0.401	4.01	12.06
8.0M	0.360	3.60	11.13
9.0M	0.326	3.26	10.26
10.0M	0.297	2.97	9.46
11.0M	0.268	2.68	8.56
12.0M	0.248	2.48	7.89
15.0M	0.200	2.00	6.02
17.0M	0.179	1.79	5.09
20.0M	0.152	1.52	3.64



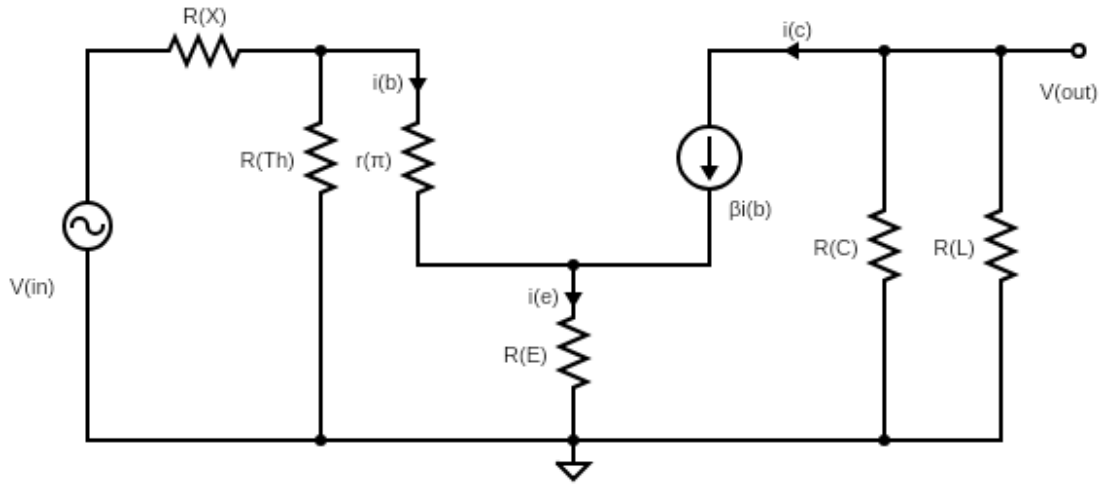


Lower cut-off frequency $f_L = 500.03$ Hz (from the plot)

Higher cut-off frequency $f_H = 3.00$ MHz (from the plot)

Comparison with Part A:

- The maximum gain of the amplifier (that is the gain in the mid-frequency region) reduces when the capacitor C_E is disconnected. *This can be explained as below.*



This is the *small signal hybrid π model* for an amplifier in common emitter configuration. All the capacitances have been shorted.

The Q-point of the circuit will remain intact irrespective of if the capacitor C_E is connected or disconnected (because capacitance acts as an open circuit for a DC input at steady state).

Therefore, the value of r_π will remain the same.

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

The value of R_E however depends on if C_E is connected or not.

$$R_E = R_{E1} + R_{E2} \ (\ if\ C_E\ is\ disconnected\ )$$

$$R_E = R_{E1} \ (\ if\ C_E\ is\ connected\ )$$

Using the approximate formula of small signal voltage gain for this model of amplifier, we get the following.

$$A_v = -\frac{R_C || R_L}{R_E}$$

Because the resistance R_E increases on disconnected the capacitor C_E, $|A_v|$ reduces (in the mid frequency region).

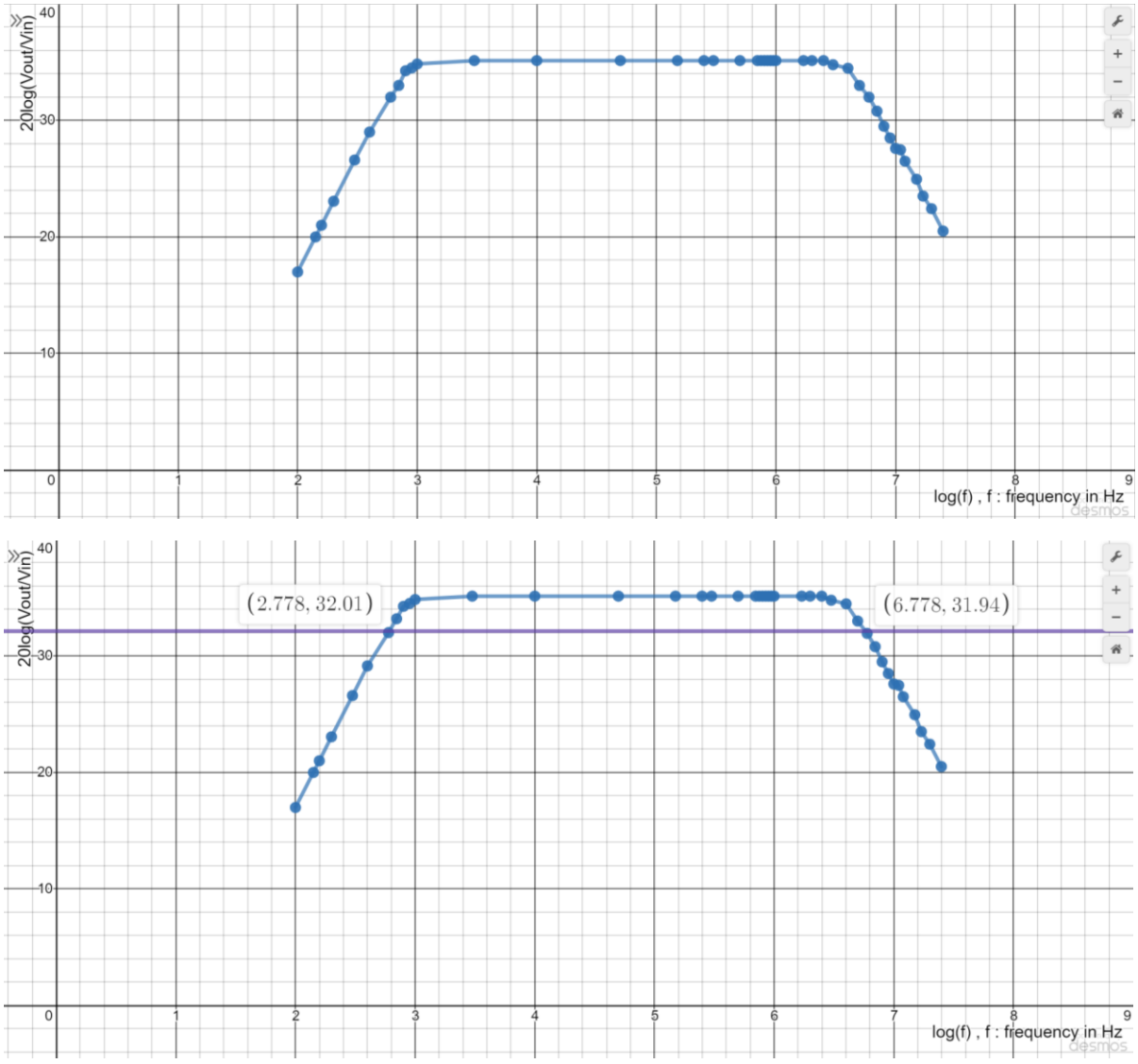
- The bandwidth of the frequency response increases when the capacitor C_E is disconnected. That is because the lower cut-off frequency reduces and the upper cut-off frequency increases. In this experiment, the former reduces by 62.31Hz and the latter increases by 330kHz and hence the bandwidth increases by around 330.06kHz.

PART D – EFFECT OF C_E (BYPASS BOTH R_{E1} AND R_{E2})

$V_{in} = 100\ mV$

$Frequency\ (Hz)$	$V_{out}(V)$	$gain = V_{out}/V_{in}$	$20 * (\log(gain)$
100	0.707	7.07	16.99
200	1.422	14.22	23.06
300	2.138	21.38	26.60
400	2.867	28.67	29.15
600	3.986	39.86	32.01
700	4.571	45.71	33.20
800	5.162	51.62	34.26
900	5.315	53.15	34.51
1k	5.528	55.28	34.85
3k	5.717	57.17	35.14
10k	5.717	57.17	35.14
50k	5.717	57.17	35.14
150k	5.717	57.17	35.14
250k	5.717	57.17	35.14
300k	5.717	57.17	35.14
500k	5.717	57.17	35.14
700k	5.717	57.17	35.14
750k	5.717	57.17	35.14
800k	5.717	57.17	35.14
850k	5.717	57.17	35.14
900k	5.717	57.17	35.14
950k	5.717	57.17	35.14
1.0M	5.717	57.17	35.14
1.7M	5.717	57.17	35.14
2.0M	5.717	57.17	35.14
2.5M	5.717	57.17	35.14
3.0M	5.489	54.89	34.79
4.0M	5.298	52.98	34.48
5.0M	4.467	44.67	33.00
6.0M	3.954	39.54	31.94
7.0M	3.469	34.69	30.80

8.0M	2.989	29.89	29.51
9.0M	2.682	26.82	28.57
10.0M	2.415	24.15	27.66
11.0M	2.366	23.66	27.48
12.0M	2.126	21.26	26.55
15.0M	1.768	17.68	24.95
17.0M	1.498	14.98	23.51
20.0M	1.322	13.22	22.42
25.0M	1.059	10.59	20.50



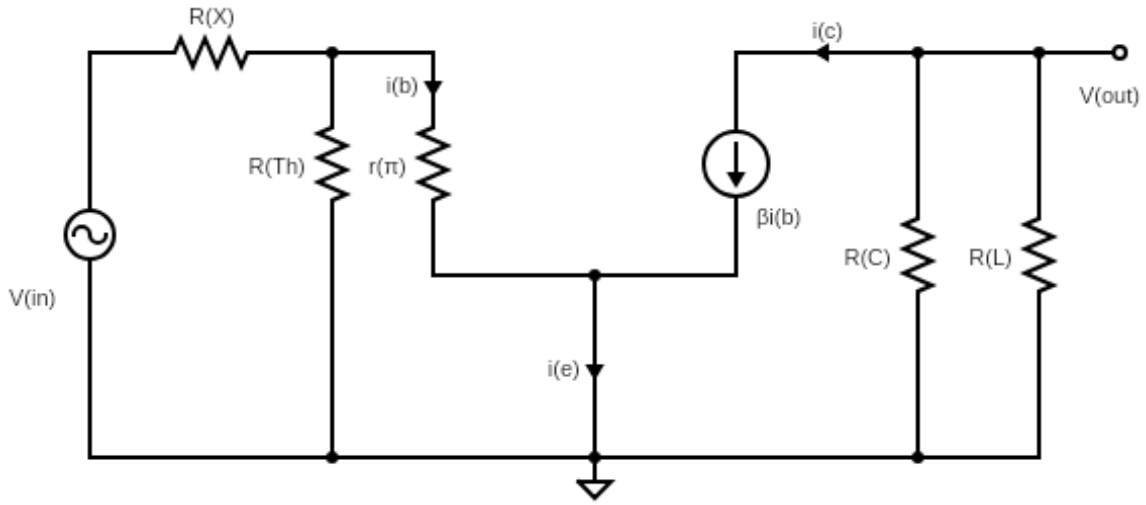
Lower cut-off frequency $f_L =$ 602.56 Hz (from the plot)

Higher cut-off frequency $f_H =$ 5.98 MHz (from the plot)

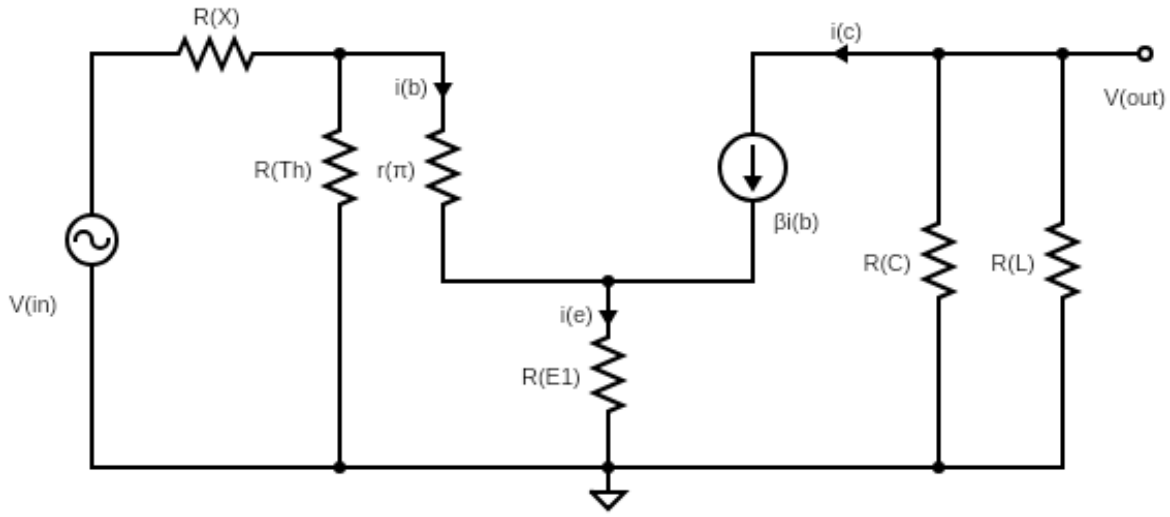
Comparison with Part A:

- The maximum gain of the amplifier (that is the gain in the mid-frequency region) increases considerably when the capacitor C_E bypasses both R_{E1} and R_{E2}. *This can be explained as below.*

This is the *small signal hybrid π model* for an amplifier in common emitter configuration when both the emitter resistances are bypassed. All the capacitances have been shorted.



This is the *small signal hybrid π model* for an amplifier in common emitter configuration when only R_{E2} is bypassed. All the capacitances have been shorted.



The Q-point of the circuit will remain intact irrespective of if the capacitor C_E bypasses any one or both of the emitter resistances (because capacitance acts as an open circuit for a DC input at steady state).

Therefore, the value of r_π will remain the same.

$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

Assume that R_X is much smaller compared to the parallel combination of R_{Th} and r_π, and hence to the parallel combination of R_{Th} and $(r_\pi + (1+\beta)R_E)$.

Therefore, by using the approximate formula of small signal voltage gain for the second model we get,

$$A_{v-2} = -\frac{R_C||R_L}{R_{E1}}$$

Also, for the first model, the following is valid.

$$i_b = \frac{V_{in}}{r_\pi}$$

$$V_{out} = \beta * i_b * (R_C||R_L)$$

$$A_{v-1} = -\beta \frac{R_C||R_L}{r_\pi}$$

$$Take\ the\ Q-values\ of\ the\ parameters\ from\ PART\ I$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = 100 * \frac{0.026}{0.774} = 3.36k\Omega$$

$$\frac{\beta}{r_\pi} = \frac{100}{3.36} = 29.77\ mA/V$$

$$\frac{1}{R_{E1}} = \frac{1}{300} = 3.33\ mA/V$$

Therefore, the value of $|A_{v-1}|$ is more than the value of $|A_{v-2}|$.

Hence the gain in the mid frequency region (or the maximum gain) increases when both the emitter resistances are bypassed.

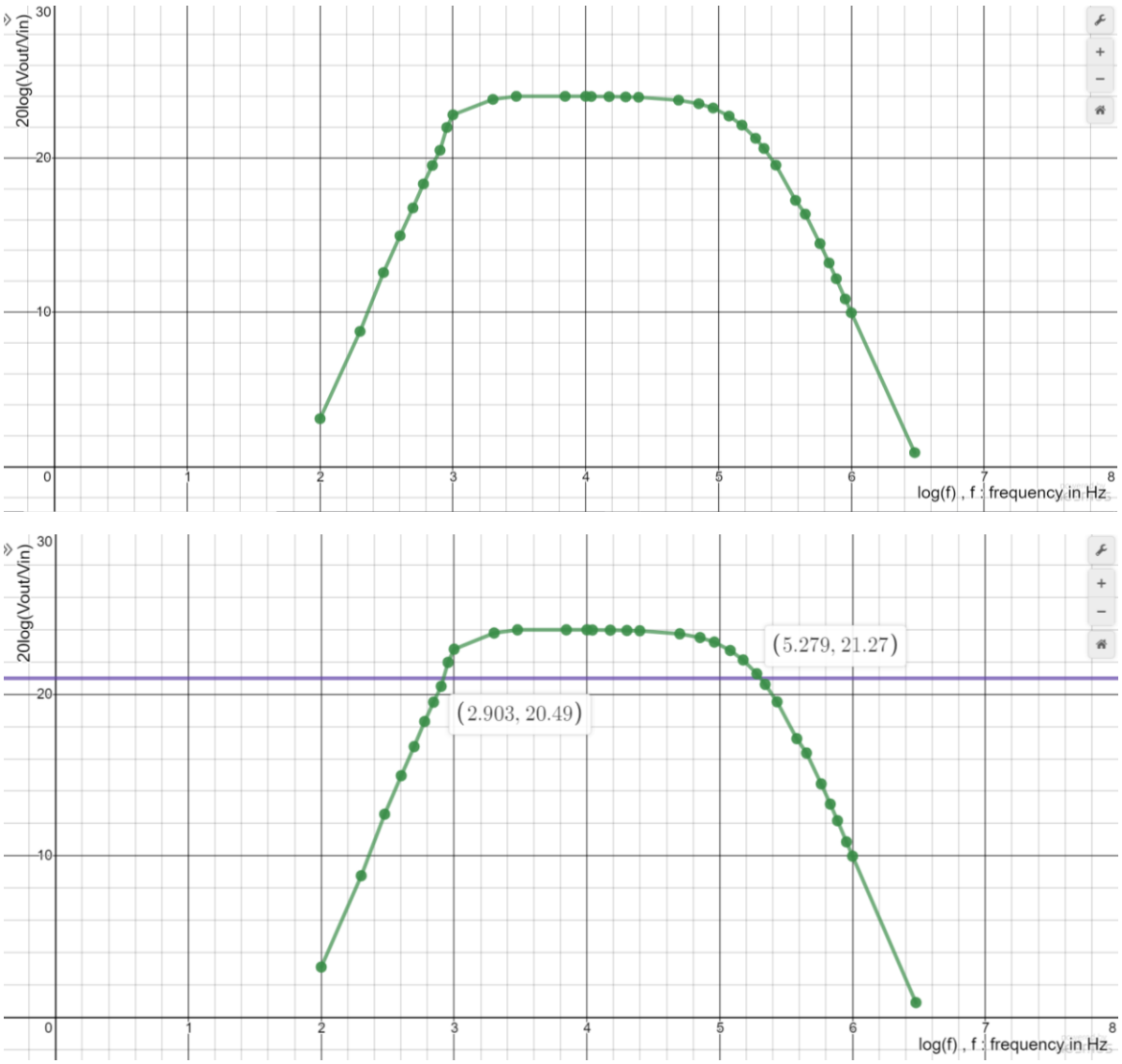
- Both the lower cut-off frequency and the upper cut-off frequency increase. In this experiment, the former increases by 40.22Hz and the latter increases by 3.31MHz. The latter increase is much more than the former increase. Therefore, the bandwidth of the frequency response increases by almost 3.31MHz.

PART E – MILLER EFFECT OF C_{CB} (SWITCH S_4 CLOSED)

$V_{in} = 100\ mV$

$Frequency\ (Hz)$	$V_{out}(V)$	$gain = V_{out}/V_{in}$	$20 * (\log(gain)$
100	0.143	1.43	3.11
200	0.274	2.74	8.76
300	0.425	4.25	12.57
400	0.560	5.60	14.96
500	0.689	6.89	16.76
600	0.823	8.23	18.31
700	0.945	9.45	19.51
800	1.058	10.58	20.49
900	1.254	12.54	21.97
1k	1.379	13.79	22.79
2k	1.547	15.47	23.79
3k	1.584	15.84	23.99
7k	1.584	15.84	23.99
10k	1.584	15.84	23.99
11k	1.582	15.82	23.98
15k	1.580	15.80	23.97
20k	1.576	15.76	23.95
25k	1.573	15.73	23.93
50k	1.538	15.38	23.74
71k	1.498	14.98	23.51
91k	1.450	14.50	23.23
120k	1.366	13.66	22.71
150k	1.276	12.76	22.12
190k	1.157	11.57	21.27
220k	1.073	10.73	20.61
270k	0.947	9.47	19.53
380k	0.728	7.28	17.25
450k	0.658	6.58	16.36
580k	0.528	5.28	14.45
680k	0.457	4.57	13.20
770k	0.406	4.06	12.17
900k	0.349	3.49	10.86
1.0M	0.315	3.15	9.97

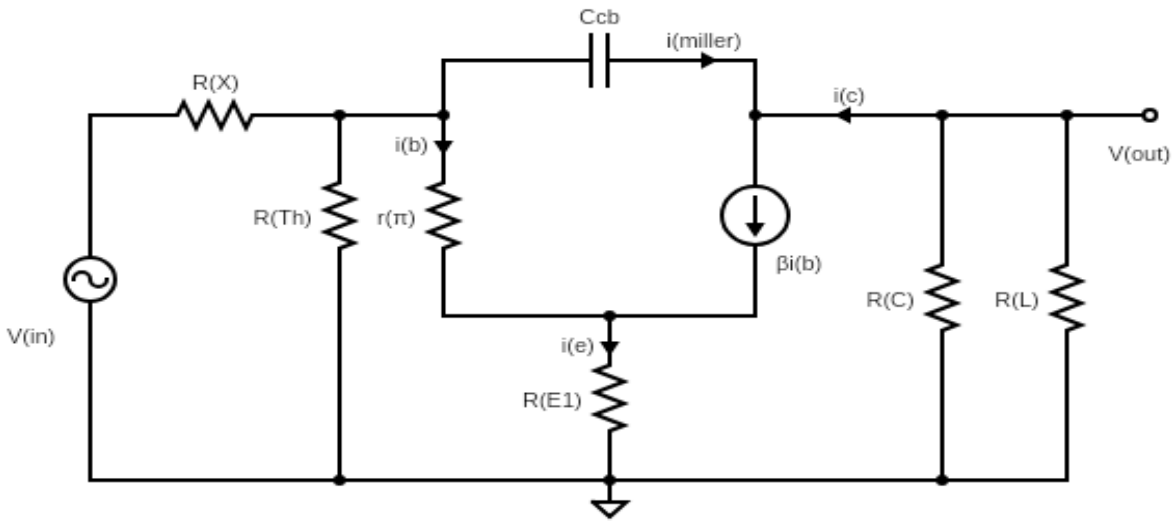
3.0M	0.111	1.11	0.91



Lower cut-off frequency f_L = 918.33 Hz (from the plot)

Higher cut-off frequency f_H = 191 kHz (from the plot)

The following is the modified hybrid pi model upon connecting the capacitance $C_{CB.}$

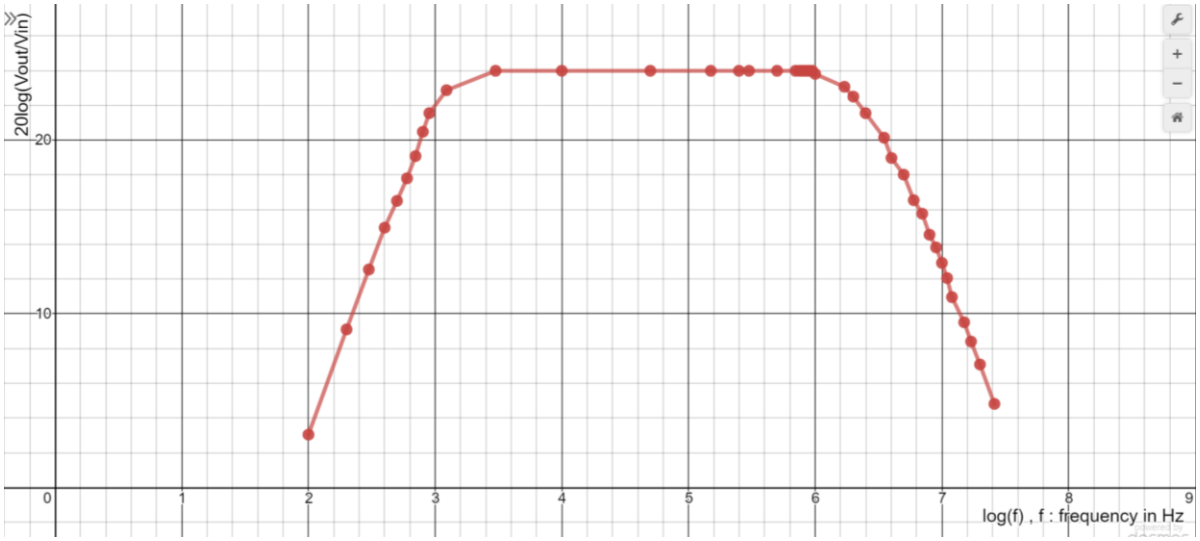


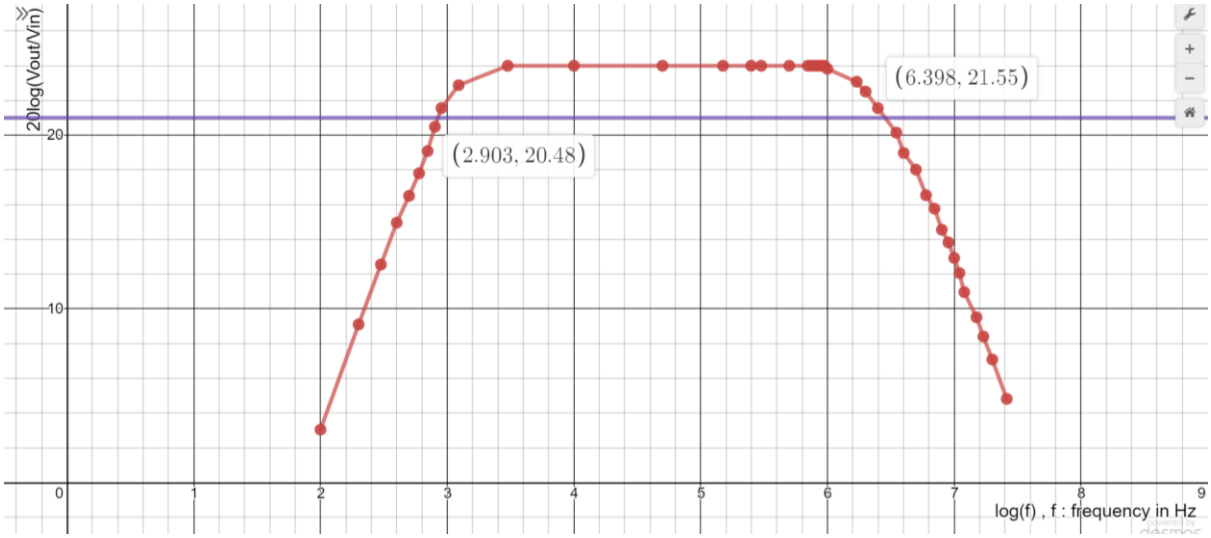
PART F – MILLER EFFECT OF C_{CB} (SWITCH S_4 OPENED)

$V_{in} = 100\ mV$

$Frequency\ (Hz)$	$V_{out}(V)$	$gain = V_{out}/V_{in}$	$20 * \log(gain)$
100	0.142	1.42	3.04
200	0.285	2.85	9.10
300	0.424	4.24	12.55
400	0.560	5.60	14.96
500	0.668	6.68	16.50
600	0.750	7.50	17.50
700	0.899	8.99	19.08
800	1.057	10.57	20.48
900	1.195	11.95	21.55
1k	1.392	13.92	22.87
10k	1.584	15.84	23.99
50k	1.584	15.84	23.99
150k	1.584	15.84	23.99
250k	1.584	15.84	23.99
300k	1.584	15.84	23.99
500k	1.584	15.84	23.99
700k	1.584	15.84	23.99
750k	1.584	15.84	23.99
800k	1.584	15.84	23.99
850k	1.584	15.84	23.99
900k	1.584	15.84	23.99

950k	1.584	15.84	23.99
1.0M	1.551	15.51	23.81
1.7M	1.424	14.24	23.07
2.0M	1.334	13.34	22.50
2.5M	1.195	11.95	21.55
3.5M	1.016	10.16	20.14
4.0M	0.888	8.88	18.97
5.0M	0.795	7.95	18.01
6.0M	0.671	6.71	16.54
7.0M	0.614	6.14	15.76
8.0M	0.534	5.34	14.55
9.0M	0.453	4.53	13.12
10.0M	0.443	4.43	12.93
11.0M	0.401	4.01	12.06
12.0M	0.353	3.53	10.96
15.0M	0.299	2.99	9.51
17.0M	0.263	2.63	8.40
20.0M	0.226	2.26	7.08
26.0M	0.174	1.74	4.81





Lower cut-off frequency f_L = 893.77 Hz (from the plot)

Higher cut-off frequency f_H = 2.80 MHz (from the plot)

Comparison between PART E and PART F:

- The maximum gain, that is the gain in the mid frequency region, in both the cases remains the same.
- The lower cut-off frequency reduces and the upper cut-off frequency increases when the capacitance C_{CB} is disconnected. The former decrease is very small, in this experiment it is 24.56Hz. Whereas the latter increase is comparatively much larger, in this experiment it is 2.61MHz.
- The bandwidth increases by almost 2.61MHz (in this experiment) when the capacitor C_{CB} is disconnected. Note that the bandwidth in PART E (190.08kHz) when the capacitor C_{CB} is connected is much lesser than that in PART A (2.67MHz).

INPUT RESISTANCE

$$V_{out}|_O = A * V_S * \frac{R_{in}}{R_{in} + R_S}$$

$$V_{out}|_{R_X} = A * V_S * \frac{R_{in}}{R_{in} + R_S + R_X}$$

$$R_{in} = R_X * \frac{V_{out}|_{R_X}}{V_{out}|_O - V_{out}|_{R_X}} - R_S$$

The circuit given in the fourth part of the experiment was simulated and the following measurements were done.

$V_{out}|_{R_X} = 1.581\ V$

$V_{out}|_{O} = 1.994\ V$

For this particular circuit, $R_X = 1k\Omega$ and $R_S = 0\Omega$ (assuming ideal voltage source)

$$R_{in} = 1 * \frac{1.581}{1.994 - 1.581} - 0 = 3.83\ k\Omega$$

For the same circuit. The switch S_1 was closed and the amplitude of the current flowing through the source and the potential difference across its terminals was measured.

$V_{in-amplitude} = 79.07\ mV$

$I_{in-amplitude} = 20.826\ \mu A$

$$R'_{in} = \frac{V_{in-amplitude}}{I_{in-amplitude}} = \frac{79.07}{20.826} = 3.79\ k\Omega$$

R'_{in} and R_{in} have almost the same value.

OUTPUT RESISTANCE

$$V_{out}|_{R_L} = A * V_{in} * \frac{R_L}{R_O + R_S}$$

$$V_{out}|_{\infty} = A * V_{in}$$

$$R_{out} = R_L * \frac{V_{out}|_{\infty} - V_{out}|_{R_L}}{V_{out}|_{R_L}}$$

The circuit given in the fourth part of the experiment was simulated and the following measurements were done.

$V_{out}|_{R_L} = 1.994\ V$

$V_{out}|_{\infty} = 2.008\ V$

For this particular circuit, $R_L = 1M\Omega$.

$$R_{out} = 1 * \frac{2.008 - 1.994}{1.994} = 7.02\ k\Omega$$