Elementary adders

You need to be alert to (usually minor) changes that may be made to the assignment statement or to the guidelines after the assignment is first put up. Refresh this frame and re-read the assignment carefully before you make your final submission.

Part 1 (Half adder)

- Design a half adder to add two bits to generate their sum and carry
- Test that it works by applying appropriate inputs and checking the outputs
- Label the terminals to reflect their roles
- Save it as a regular circuit (logic file), reopen and retest
- Save it as a component (cmp file), reopen and retest

Part 2 (Full adder)

- Using the half adder component and additional items, as needed, design a full adder to add two bits and an incoming carry bit to generate their sum and carry out
- Test that it works by applying appropriate inputs and checking the outputs
- Label the terminals to reflect their roles
- Save it as a regular circuit (logic file), reopen and retest
- Save it as a component (cmp file), reopen and retest

Part 3 (Ripple carry adder)

- Using the full adder component and additional items, as needed, design a ripple carry adder to add two bit vectors (of 4 bits) to generate their sum vector and the carry out
- Test that it works by applying appropriate inputs and checking the outputs
- Label the terminals to reflect their roles
- Save it as a regular circuit (logic file), reopen and retest
- Determine the delay of a ripple carry adder of n bits

Part 4 (Full adder/subtractor)

- Using the full adder component and additional items, as needed, design a full adder/subtractor to add/subtract two bits and to generate their sum/difference
- Test that it works by applying appropriate inputs and checking the outputs
- Label the terminals to reflect their roles
- Save it as a regular circuit (logic file), reopen and retest
- Save it as a component (cmp file), reopen and retest

Part 5 (Ripple carry adder/subtractor)

- Using the full adder/subtractor component and additional items, as needed, design a ripple carry adder to add/subtract two bit vectors (of 4 bits) to generate their sum/difference vector and the carry out
- Test that it works by applying appropriate inputs and checking the outputs
- Label the terminals to reflect their roles
- Save it as a regular circuit (logic file), reopen and retest
- Determine the delay of a ripple carry adder/subtractor of n bits

Marking guidelines

Assignment marking is to be done only **after** the deadline expires, as submissions gets blocked after the assignment is marked. Enter the breakup of marks while marking.

Half adder	
Correctly working circuit	**4**
Labels	**2**
Saving and component creation	**2+2**
Full adder	
Correctly working circuit	**4**
Labels	**2**
Saving and component creation	**2+2**
Ripple carry adder	
Correctly working circuit	**4**
Labels	**2**
Delay computation of RCA	**4**
Full adder/subtractor	
Correctly working circuit	**4**
Labels	**2**
Saving and component creation	**2+2**
Ripple carry adder/subtractor	
Correctly working circuit	**4**
Labels	**2**
Delay computation of RCA/S	**4**
Total Marks	***50***

Assignment submission

A PDF report, as appropriate, should be submitted. Submit all your files together.

Use electronic submission via the WBCM link

You should keep submitting your incomplete assignment from time to time after making some progress, as you can submit any number of times before the deadline expires. **You should submit all your files together**.