**Juan Arturo Garza**

**Seeking Hardware Design Internships, Available Summer or/and Fall 2024, US CITIZEN**

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**EDUCATION**

**Rice University,** Houston, TX

**Bachelor of Science**, Electrical and Computer Engineering, GPA**: 3.83** May 2024

**Masters,** Electrical and Computer Engineering,May2025

**WORK Experience**

Research Assistant - **SIMS Lab Rice University**, Houston TX January 2023 - Present

* Programed communication for data byte transfer between PC to FPGA and custom chip with Opal-Kelly XEM7310 requiring python library for Opal-Kelly board and system Verilog RTL on Vivado allowing other researchers to easily test custom ASIC chips easily, **reached ~100M Bits / second max transfer rate, 54% faster** than older solution
* Used Python socket libraries to communicate from PC to Pynq OS on Xilinx board to FPGA fabric with Scan Chain communication with AXI Lite interface and with DMA transfer for data byte transfer to allow researchers an additional method to test custom ASIC chips, **reached ~80M Bits / second**

CPU Implementation Physical Design Intern - **Apple**, Austin, TX May 2023 - August 2023

* Researched and created methodology for net switching power reduction in Place and Route flow through Non-Default Rule changes on critical nets resulting in **a 2% dynamic power improvement** across CPU design blocks increasing power efficiency for current and future route dominated designs going on Apple Products
* Customized Apple Physical Design flow with TCL interacting with industry leading tools for power, time reports, net and cell property querying and developed net profiling infrastructure for analysis across general design blocks

CPU Formal Verification Intern- **Arm Ltd**, Memory System Team**,** Austin, TX May 2022 - August 2022

* Tested, analyzed, and inserted Cadence formal verification software tool in Arm Formal verification flow with TCL and Ruby scripts which **decrease computation time by 5%** in generating formal verification proofs on Arm CPUs
* Implemented a Formal Triage Solution for CPU’s formal verification test results which will help future debug tracking using a Virtual Machine for a sever to track uploaded regression data resulting in easier debug experience
* **Awarded best collaborator Award** by Talent Acquisition for ability to work with peers in global office locations

Research Intern, **Human-Computer Interaction Institute, Carnegie Mellon**, Pittsburgh, PA June 2021 - August 2021

* Surveyed articles to research public opinion on autonomous delivery vehicles, including barriers to success and adoption strategies for cities for improvements on current designs, ended with presentation of progress.
* Built data scraper that gathered and sorted data with sentiment analysis library in Python with reddit API
* Presented results to department, finding the biggest barrier is trust from public in reliability if of delivery robots

**Capstones and Club Leadership**

**Masters ECE Capstone Project: Autonoma Processing,** Rice Houston TXAugust 2023 - Present

* Implementing custom architecture for accelerated pattern matching on Xilinx Artix-7 hardware for Rice SIMS Lab which could accelerate string pattern detection by over 10x compared to typical software-based solutions
* Created python scripts generating testbench and Verilog RTL describing Autonoma Processor logic based on graph representing string pattern criteria for customizable scalable design, utilizing UART for reading processed data
* Starting at 200Mhz for logic and pushing frequency of logic towards 400Mhz as optimizations of logic occur

**Undergrad ECE Capstone Project: Autonomous Parking,** Rice Houston TX August 2022 – May 2023

* Collaborated in team of eight to build **fully autonomous parking golf cart** utilizing jetson nano implementing a CNN machine learning Model controlling Arduino and beagle bone black for motor and steering of an electric golf cart
* Programed motor controller and sensor communication on Arduino in C++ and integrating in overall design of team
* **Earned three team awards** (4000$ total): 1st place Willy Revolution Awards for Outstanding Innovation, 2023 Rice Engineering Showcase People’s Choice Award, Rice ECE Bill Wilson Award for Senior Design

**Rice Society of Hispanic Professional Engineers,** Rice Houston TXAugust 2020-Present

* Voted into three leadership roles by 75+ SHPE Rice chapter—Staff Chair (2020-21), External Vice President (2021-23) **and Internal Vice President** (now) involving communications-related support at weekly Board meetings
* Created and planed general body meeting, created new initiatives such as mentorSHPE at Rice pairing 20+ underclassmen to upper classmen for navigating engineering at Rice, help student access opportunities at Rice
* Managed company sponsorships and relationship-building efforts with potential external partners where I raised over 20,000$ in 21-22 school year which helped fully fund our SHPE Rice members to go to National Conference

**SKILLS**

* Python, System Verilog, TCL script, C, C++, Cadence Innovus and Virtuoso, VLSI Magic, Perl, Ruby, LTSPICE, HPSICE, FPGA (Vitis HLS, Model Composer Simulink, MATLAB, Xilinx Vivado), Arduino, Prime Time PX, MSP430 programming, Linux, simple bash scripting, SPI I2C, TINA-TI, HyperLynx Spice

**Group Projects**

**VLSI Connect 3 board,** Rice Houston TX January - May 2022

* Collaborated with a team of four to design RTL of connect three board in Verilog and verified in Modelsim, then synthesized design to be routed into a physical design with Place and Route flow in Magic VLSI software.
* Created automated test bench scripts targeting edge and transition state cases using python to validate our design

**Pedometer Buildout, Team lead,** Rice Houston TX, April 2022 - May 2022

* Designed and prototyped a functional pedometer using an MSP430 microcontroller, communicating through Seral Peripheral Interface to a KX126 accelerometer and with SPI LCD Screen, using C to create drivers for communication
* Optimized for low power as only powered by two AA batteries lasting hours, implementing interrupts for computing
* Lead team of three and devised architecture of design, delegated tasks and ensured others focused on their strengths

**Technical Projects**

**Graduate IC Project: In Memory Computing,** Rice Houston TX October 2023 –Present

* Recreating paper results with Cadence Virtuoso “*C3SRAM: In-Memory-Computing*” where SRAM use Capacitive Coupling Computing for dot product multiplication accelerating CNN algorithms using 150 nm technology node
* Using Perl and python scripts to optimize sizing of PMOS and NMOS for timing, power, and verification of design

**Graduate Level High Performance Architecture Projects** Rice Houston TXJanuary 2023 - May 2023

* Created RTL Verilog of 32bit 5-stage pipelined processor handling simple assembly instructions on FPGA
* Programmed C simulation of Reorder Buffer and Tomasulo Out-of-Order Algorithm for processor and analyzed performance with differing implementations cache eviction and coherency policies such as MSI and MOSI

**32-bit Adder, Digital IC Course Competition,** Rice Houston TX April 2022 - May 2022

* Created, tested, and optimized 32-bit adder in Cadence Virtuoso and won course competition of fastest adder frequency. Tested for randomized input for edge cases of critical path using python to measure average delay
* Achieved 2.1 GHz (475 ps period) with Carry select Adder with optimized PMOS and NMOS sizing, compared separate adder architectures and adder configurations to settle on final fastest design with lowest EDP

**Graduate Level VLSI FPGA Projects,** Rice Houston TX September 2022 - December 2022

* Used Xilinx tools on Zed Board with Xilinx Model Composer, Vivado, and Vitis HLS in hardware acceleration projects: Systolic Matrix Multiplication, Cordic calculator, QR decomposition Matrix Equation Solver, refining my design skills
* Created RTL or behavioral logic for designs in tools and automated testbenches in MATLAB Simulink and C

**Leadership and Professional Development** **Experience**

**Course Assistant, Fundamentals of Electrical Engineering: ELEC 241,** Rice Houston TXAugust 2022-Present

* Assist 60+ student into EE course by grading course homework and hosting bi-weekly office hours going over homework’s and materials with average attendance of 8 to 15 students
* Mentor new ECE students into major, providing recourses for applying to internships, coursework navigation, and interview help to foster a collaborate and welcoming environment for students in ECE

**Management Leadership for Tomorrow | Career Prep Fellow**  February 2022–November 2023

* Selected among thousands of high achieving applicants to participate in this Career Preparation program focused on professional and leadership development.
* Complete business case studies and assignments to grow leadership and technical skills

**Thrive Scholars** May 2018-Present

* Selected as one of 100 students for six-year college access, college success and professional development program for high achieving, underrepresented first generation student leaders; Participated in comprehensive career development program including career coaching, case studies, and projects enhanced analytical, quantitative skills.

**Garza’s Auto Garage and Towing,** Manager, Durham, NCJanuary 2016 - May 2019

* Managed technical, operational, and customer-facing responsibilities for family auto repair business, including vehicle diagnostics, engine and transmission repair, tow truck operation, and delivery logistics
* Taught automotive repair skills to new workers and managed their work to match their skill set

**Additional:** TA Elec 327 (Spring) Implementation of Digital Systems covering embedded microcontroller C programming

**Interests**/**Hobbies**: Viola player, Alto Saxophone, Running 30-45 miles a week

**Relevant Coursework**: (Grad) High Performance Computer Architecture, (Grad) VLSI (Xilinx board FPGA), (Grad) Integrated Circuits (Cadence Virtuoso), Implementation of Digital Systems (Microcontroller Programming in C), Digital Logic Design, Embedded systems (Linux microcomputer), High Speed System Design (HyperLynx, TINA TI)