CHDL

```
int main() {

  bvec<5> c;
  c = Reg(c + Lit<5>(1));
 bvec<5> out = c;
 OUTPUT(out);

}
```

Verilog

```
module counter( input clk,
output [4:0] out)

reg[4:0] c;
assign out = c;
always@(posedge clk)
            c <= c + 5'b1;

endmodule
```