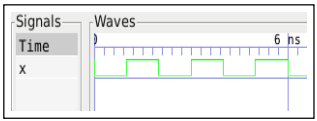
C++ Source

```
#include <fstream>
#include <chdl/chdl.h>
#include <chdl/techmap.h>

int main() {
  using namespace std;
  using namespace chdl;

  node x; x = Reg(!x); TAP(x);

  optimize();
  ofstream vcd("sample.vcd");
  run(vcd, 10);
  ofstream netl("sample.netl");
  techmap(netl);
  ofstream verilog("sample.v");
  print_verilog("top", verilog);
  return 0;
}
```

.vcd

```
$timescale 1 ns $end
$var reg 1 x x $end
$enddefinitions $end
#0
0x
#1
1x
#2
0x
#3
1x
```

Waveforms



Netlist

```
inputs
outputs
  x 1
design
  INV 1 0
  DFF 0 1
```

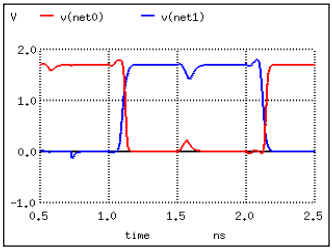
Verilog

```
module top(
  phi
);

  input phi;
  wire x;
  assign x = __x1;
  wire __x0;
  reg __x1;
  not __i0(__x0, __x1);
  initial
    begin
      __x1 <= 0;
    end
  always @ (posedge phi)
    begin
      __x1 <= __x0;
    end

endmodule
```

SPICE Netlist

```
X0 net1 net0 INV
X1 net0 net1 DFF
```

SPICE Simulation



FPGA