PROJECT 1:

Equivalence Checking with Formality

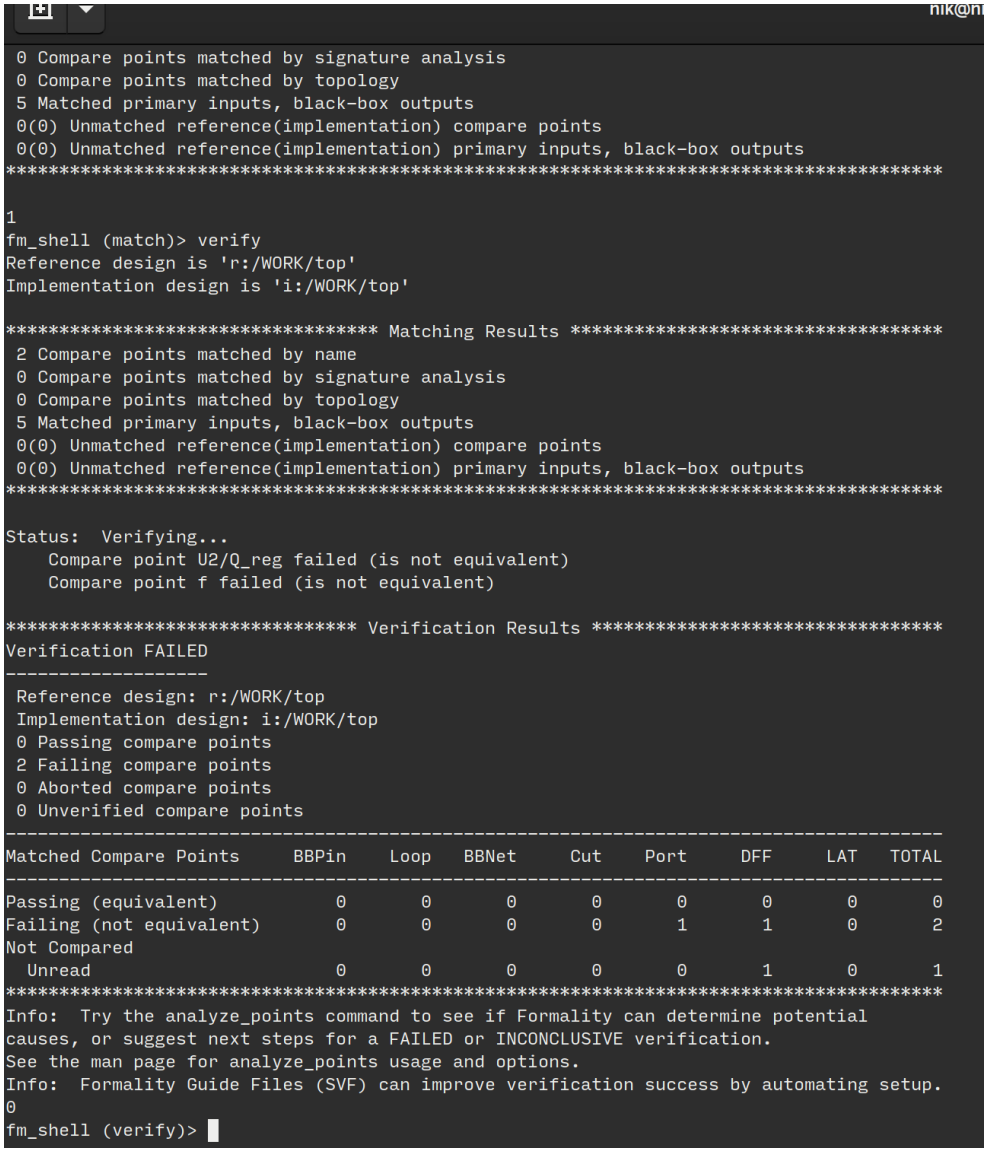
Nikolay Nikolov

Fig. 1: Task1, the combinational circuits match

Formality Results

```
fm_shell (setup)> match
Reference design is 'r:/WORK/project1_task1_1'
Implementation design is 'i:/WORK/project1_task1_1'
Status:  Checking designs...
Status:  Building verification models...
Status:  Matching...

********************************** Matching Results **********************************
 1 Compare points matched by name
 0 Compare points matched by signature analysis
 0 Compare points matched by topology
 4 Matched primary inputs, black-box outputs
 0(0) Unmatched reference(implementation) compare points
 0(0) Unmatched reference(implementation) primary inputs, black-box outputs
**************************************************************************************

1
verifyll (match)>
Reference design is 'r:/WORK/project1_task1_1'
Implementation design is 'i:/WORK/project1_task1_1'

********************************** Matching Results **********************************
 1 Compare points matched by name
 0 Compare points matched by signature analysis
 0 Compare points matched by topology
 4 Matched primary inputs, black-box outputs
 0(0) Unmatched reference(implementation) compare points
 0(0) Unmatched reference(implementation) primary inputs, black-box outputs
**************************************************************************************

Status:  Verifying...

******************************** Verification Results ********************************
Verification SUCCEEDED
----------------------
 Reference design: r:/WORK/project1_task1_1
 Implementation design: i:/WORK/project1_task1_1
 1 Passing compare points
--------------------------------------------------------------------------------------
Matched Compare Points     BBPin    Loop   BBNet     Cut    Port     DFF     LAT   TOTAL
--------------------------------------------------------------------------------------
Passing (equivalent)           0       0       0       0       1       0       0       1
Failing (not equivalent)       0       0       0       0       0       0       0       0
**************************************************************************************
1
_m_shell (verify)>
N-2017.09-SP2
fm_shell (verify)>
```

Fig. 2: Task 2, sequential circuits do not match



```
 0 Compare points matched by signature analysis
 0 Compare points matched by topology
 5 Matched primary inputs, black-box outputs
 0(0) Unmatched reference(implementation) compare points
 0(0) Unmatched reference(implementation) primary inputs, black-box outputs
****************************************************************************************

1
fm_shell (match)> verify
Reference design is 'r:/WORK/top'
Implementation design is 'i:/WORK/top'

********************************** Matching Results **********************************
 2 Compare points matched by name
 0 Compare points matched by signature analysis
 0 Compare points matched by topology
 5 Matched primary inputs, black-box outputs
 0(0) Unmatched reference(implementation) compare points
 0(0) Unmatched reference(implementation) primary inputs, black-box outputs
****************************************************************************************

Status:  Verifying...
    Compare point U2/Q_reg failed (is not equivalent)
    Compare point f failed (is not equivalent)

******************************** Verification Results ********************************
Verification FAILED
-------------------
 Reference design: r:/WORK/top
 Implementation design: i:/WORK/top
 0 Passing compare points
 2 Failing compare points
 0 Aborted compare points
 0 Unverified compare points
----------------------------------------------------------------------------------------
Matched Compare Points     BBPin    Loop   BBNet     Cut    Port     DFF     LAT   TOTAL
----------------------------------------------------------------------------------------
Passing (equivalent)           0       0       0       0       0       0       0       0
Failing (not equivalent)       0       0       0       0       1       1       0       2
Not Compared
  Unread                       0       0       0       0       0       1       0       1
****************************************************************************************
Info:  Try the analyze_points command to see if Formality can determine potential
causes, or suggest next steps for a FAILED or INCONCLUSIVE verification.
See the man page for analyze_points usage and options.
Info:  Formality Guide Files (SVF) can improve verification success by automating setup.
0
fm_shell (verify)>
```