Coverage and Run Reports

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Total Files: 7

File: Functional coverage report.txt

```
# Coverage Report by instance with details
# === Instance: /top_sv_unit
# === Design Unit: work.top_sv_unit
# ------
# Covergroup Coverage:
                            1
                                                81.25%
    Covergroups
                                    na
                                          na
       Coverpoints/Crosses
                            8
                                    na
                                           na
          Covergroup Bins 56
                                    52
                                            4
                                                92.85%
#
                                           Metric Goal Bins
# Covergroup
Status
#
# TYPE /top_sv_unit/alu_coverage/alu_cg
                                           81.25%
                                                     100
Uncovered
                                                      56
    covered/total bins:
                                              52
    missing/total bins:
                                                      56
                                               4
   % Hit:
                                           92.85%
                                                      100
    Coverpoint opcode_check
                                           100.00%
                                                      100
Covered
      covered/total bins:
       missing/total bins:
#
                                               0
                                                        2
                                                      100
       % Hit:
                                           100.00%
                                             2464
       bin r_type
                                                        1
Covered
                                             2544
       bin i_type
                                                        1
Covered
                                           100.00%
    Coverpoint alu_check
                                                      100
Covered
```

| # | covered/total bins: | 14 | 14 | - |
|-----------------------|------------------------|---------|-----|---|
| # | missing/total bins: | 0 | 14 | - |
| # | % Hit: | 100.00% | 100 | - |
| | bin add | 380 | 1 | - |
| | bin sub | 340 | 1 | - |
| | bin and_op | 353 | 1 | - |
| | bin or_op | 365 | 1 | - |
| Covered # Covered | bin xor_op | 385 | 1 | - |
| # | bin sll | 379 | 1 | - |
| Covered # | bin srl | 334 | 1 | - |
| Covered # | bin sra | 355 | 1 | - |
| | bin slt | 340 | 1 | - |
| | bin sltu | 350 | 1 | - |
| Covered # | bin eq | 325 | 1 | - |
| | bin neq | 365 | 1 | - |
| | bin ge | 364 | 1 | - |
| | bin geu | 373 | 1 | - |
| Covered # Cov Covered | rerpoint #coverpoint0# | 100.00% | 100 | - |
| | covered/total bins: | 2 | 2 | - |
| # | missing/total bins: | 0 | 2 | - |
| # | % Hit: | 100.00% | 100 | - |
| # Covered | bin reset_asserted | 282 | 1 | - |
| # Covered | bin reset_deasserted | 4726 | 1 | - |

| | verpoint #coverpoint1# | 50.00% | 100 | - |
|------------------|--------------------------------------|---------|-----|---|
| Uncovered | covered/total bins: | 1 | 2 | - |
| # | missing/total bins: | 1 | 2 | - |
| # | % Hit: | 50.00% | 100 | - |
| # ZERO | bin disabled | 0 | 1 | - |
| # Covered | bin enabled | 5008 | 1 | - |
| | verpoint #tr.rst_n2# | 100.00% | 100 | - |
| # | covered/total bins: | 2 | 2 | - |
| # | missing/total bins: | 0 | 2 | - |
| # | % Hit: | 100.00% | 100 | - |
| # Covered | bin auto[0] | 282 | 1 | - |
| # Covered | bin auto[1] | 4726 | 1 | - |
| # Co | verpoint #tr.i_ce3# | 50.00% | 100 | - |
| Uncovered | covered/total bins: | 1 | 2 | - |
| # | missing/total bins: | 1 | 2 | - |
| # | % Hit: | 50.00% | 100 | - |
| # ZERO | bin auto[0] | 0 | 1 | - |
| # | bin auto[1] | 5008 | 1 | _ |
| Covered # Cro | oss #cross0# | 100.00% | 100 | _ |
| Covered | | | | |
| # | covered/total bins: | 28 | 28 | - |
| # | missing/total bins: | 0 | 28 | - |
| # | % Hit: | 100.00% | 100 | - |
| # | Auto, Default and User Defined Bins: | | | |
| # | bin r_type_add | 194 | 1 | - |

| ~ 1 | | | | |
|--------------|-----------------|--------------|----------|---|
| Covered | | | | |
| # | bin r_type_sub | 163 | 1 | - |
| Covered | | 100 | _ | |
| # | bin r_type_and | 180 | 1 | - |
| Covered | | | | |
| # | bin r_type_or | 188 | 1 | - |
| Covered | | | | |
| # | bin r_type_xor | 181 | 1 | - |
| Covered | | | | |
| # | bin r_type_sll | 179 | 1 | - |
| Covered | | | | |
| # | bin r_type_srl | 169 | 1 | - |
| Covered | | | | |
| # | bin r_type_sra | 173 | 1 | - |
| Covered | | | | |
| # | bin r_type_slt | 167 | 1 | - |
| Covered | | | | |
| # | bin r_type_sltu | 170 | 1 | - |
| Covered | | | | |
| # | bin r_type_eq | 165 | 1 | - |
| Covered | | | | |
| # | bin r_type_neq | 177 | 1 | - |
| Covered | | | | |
| # | bin r_type_ge | 170 | 1 | - |
| Covered | | | | |
| # | bin r_type_geu | 188 | 1 | _ |
| Covered | | | | |
| # | bin i_type_add | 186 | 1 | - |
| Covered | | | | |
| # | bin i_type_sub | 177 | 1 | _ |
| Covered | | | | |
| # | bin i_type_and | 173 | 1 | _ |
| Covered | | | | |
| # | bin i_type_or | 177 | 1 | _ |
| Covered | | | | |
| # | bin i_type_xor | 204 | 1 | _ |
| Covered | _ 11 _ | | | |
| # | bin i_type_sll | 200 | 1 | _ |
| Covered | | | _ | |
| # | bin i_type_srl | 165 | 1 | _ |
| T Covered | / _F | _ • • | _ | |
| # | bin i_type_sra | 182 | 1 | _ |
| # Covered | 2111 1_C/PC_514 | - 0 4 | - | |
| # | bin i_type_slt | 173 | 1 | |
| | DIN I TONE PIC | ± 1 3 | T | - |
| Covered | hin i timo altu | 100 | 1 | |
| # | bin i_type_sltu | 180 | 1 | - |
| | | | | |

| Covere | ed | | | |
|-------------|--|---------|------|------|
| # | bin i_type_eq | 160 | 1 | _ |
| " Cover | | 200 | _ | |
| # | bin i_type_neq | 188 | 1 | _ |
| Covere | | | | |
| # | bin i_type_ge | 194 | 1 | _ |
| Cover | | | | |
| # | bin i_type_geu | 185 | 1 | _ |
| Covere | ed | | | |
| # | Cross #cross1# | 50.00% | 100 | _ |
| Uncove | ered | | | |
| # | covered/total bins: | 2 | 4 | |
| # | missing/total bins: | 2 | 4 | - |
| # | % Hit: | 50.00% | 100 | - |
| # | Auto, Default and User Defined Bins: | | | |
| # | bin <auto[1],auto[1]></auto[1],auto[1]> | 4726 | 1 | _ |
| Covere | | | | |
| # | <pre>bin <auto[0],auto[1]></auto[0],auto[1]></pre> | 282 | 1 | _ |
| Cover | | | | |
| # | bin <*,auto[0]> | 0 | 1 | 2 |
| ZERO | | | | |
| # | | | | |
| # COVI | ERGROUP COVERAGE: | | | |
| # | | | | |
| | | | | |
| | | | | |
| # Cove | ergroup | Metric | Goal | Bins |
| Status | s | | | |
| # | | | | |
| # | | | | |
| | | | | |
| | | | | |
| # TYI | PE /top_sv_unit/alu_coverage/alu_cg | 81.25% | 100 | _ |
| Uncove | ered | | | |
| # | covered/total bins: | 52 | 56 | - |
| # | missing/total bins: | 4 | 56 | - |
| # | % Hit: | 92.85% | 100 | - |
| # Covere | Coverpoint opcode_check | 100.00% | 100 | - |
| | | | | |

| # | covered/total bins: | 2 | 2 | - |
|--------------|---------------------|---------|-----|---|
| # | missing/total bins: | 0 | 2 | - |
| # | % Hit: | 100.00% | 100 | - |
| # Covered | bin r_type | 2464 | 1 | - |
| # Covered | bin i_type | 2544 | 1 | - |
| | verpoint alu_check | 100.00% | 100 | - |
| # | covered/total bins: | 14 | 14 | - |
| # | missing/total bins: | 0 | 14 | - |
| # | % Hit: | 100.00% | 100 | - |
| # Covered | bin add | 380 | 1 | - |
| # Covered | bin sub | 340 | 1 | - |
| # Covered | bin and_op | 353 | 1 | - |
| # | bin or_op | 365 | 1 | - |
| Covered # | bin xor_op | 385 | 1 | - |
| Covered # | bin sll | 379 | 1 | - |
| Covered # | bin srl | 334 | 1 | - |
| Covered # | bin sra | 355 | 1 | - |
| Covered # | bin slt | 340 | 1 | - |
| | bin sltu | 350 | 1 | - |
| Covered # | bin eq | 325 | 1 | - |
| Covered # | bin neq | 365 | 1 | - |
| Covered # | bin ge | 364 | 1 | - |
| Covered # | bin geu | 373 | 1 | - |
| Covered | | | | |

| # Cov | verpoint #coverpoint0# | 100.00% | 100 | - |
|--------------|------------------------|---------|-----|---|
| # | covered/total bins: | 2 | 2 | - |
| # | missing/total bins: | 0 | 2 | - |
| # | % Hit: | 100.00% | 100 | - |
| # Covered | bin reset_asserted | 282 | 1 | - |
| # Covered | bin reset_deasserted | 4726 | 1 | - |
| # Cov | verpoint #coverpoint1# | 50.00% | 100 | - |
| # | covered/total bins: | 1 | 2 | - |
| # | missing/total bins: | 1 | 2 | - |
| # | % Hit: | 50.00% | 100 | - |
| # ZERO | bin disabled | 0 | 1 | - |
| # Covered | bin enabled | 5008 | 1 | - |
| # Co | verpoint #tr.rst_n2# | 100.00% | 100 | - |
| Covered # | covered/total bins: | 2 | 2 | - |
| # | missing/total bins: | 0 | 2 | - |
| # | % Hit: | 100.00% | 100 | - |
| # Covered | bin auto[0] | 282 | 1 | - |
| # Covered | bin auto[1] | 4726 | 1 | - |
| | verpoint #tr.i_ce3# | 50.00% | 100 | - |
| # | covered/total bins: | 1 | 2 | - |
| # | missing/total bins: | 1 | 2 | - |
| # | % Hit: | 50.00% | 100 | - |
| # ZERO | bin auto[0] | 0 | 1 | - |

| # | bin auto[1] | 5008 | 1 | - |
|------------------|--------------------------------------|---------|-----|---|
| Covered | | | | |
| # Cro Covered | oss #cross0# | 100.00% | 100 | _ |
| # | covered/total bins: | 28 | 28 | - |
| # | missing/total bins: | 0 | 28 | - |
| # | % Hit: | 100.00% | 100 | - |
| # | Auto, Default and User Defined Bins: | | | |
| # | bin r_type_add | 194 | 1 | _ |
| Covered | | | | |
| # | bin r_type_sub | 163 | 1 | _ |
| Covered | | | | |
| # | bin r_type_and | 180 | 1 | _ |
| Covered | | | | |
| # | bin r_type_or | 188 | 1 | _ |
| Covered | | | | |
| # | bin r_type_xor | 181 | 1 | _ |
| Covered | | | | |
| # | bin r_type_sll | 179 | 1 | _ |
| Covered | _ <u></u> | | | |
| # | bin r_type_srl | 169 | 1 | _ |
| Covered | _ <u></u> | | | |
| # | bin r_type_sra | 173 | 1 | _ |
| " Covered | | | | |
| # | bin r_type_slt | 167 | 1 | _ |
| " Covered | 10-10 1121 00-1 | | _ | |
| # | bin r_type_sltu | 170 | 1 | _ |
| " Covered | 2111 1_0/pe_5104 | 170 | _ | |
| # | bin r_type_eq | 165 | 1 | _ |
| " Covered | 21m 1_0/pc_cq | 100 | _ | |
| # | bin r_type_neq | 177 | 1 | _ |
| " Covered | bin i_cype_ned | 1// | _ | |
| # | bin r_type_ge | 170 | 1 | _ |
| " Covered | DIN 1_type_ge | 170 | _ | |
| | hin u turna nau | 100 | 1 | |
| # | bin r_type_geu | 188 | 1 | _ |
| Covered | | 106 | - | |
| # | bin i_type_add | 186 | 1 | _ |
| Covered | | | | |
| # | bin i_type_sub | 177 | 1 | - |
| Covered | | | | |
| # | bin i_type_and | 173 | 1 | - |
| Covered | | | | |
| # | bin i_type_or | 177 | 1 | _ |

```
Covered
                                                          204
                                                                      1
             bin i_type_xor
Covered
             bin i_type_sll
                                                          200
                                                                       1
Covered
             bin i_type_srl
                                                          165
                                                                      1
Covered
             bin i_type_sra
                                                          182
                                                                       1
Covered
             bin i_type_slt
                                                          173
                                                                       1
Covered
             bin i_type_sltu
                                                          180
                                                                       1
Covered
             bin i_type_eq
                                                          160
                                                                       1
Covered
             bin i_type_neq
                                                          188
Covered
             bin i_type_ge
                                                          194
                                                                       1
Covered
             bin i_type_geu
                                                          185
                                                                       1
Covered
# Cross #cross__1#
                                                       50.00%
                                                                100
Uncovered
        covered/total bins:
                                                            2
                                                                      4
        missing/total bins:
                                                            2
                                                                       4
                                                       50.00%
#
        % Hit:
                                                                     100
        Auto, Default and User Defined Bins:
            bin <auto[1],auto[1]>
                                                         4726
                                                                       1
Covered
            bin <auto[0],auto[1]>
                                                          282
                                                                       1
Covered
            bin <*,auto[0]>
                                                            0
                                                                                  2
                                                                      1
ZERO
# TOTAL COVERGROUP COVERAGE: 81.25% COVERGROUP TYPES: 1
# Total Coverage By Instance (filtered view): 81.25%
#
#
```

File: UVM topology.txt

| # | | | | |
|---|-------------------|-----------------------------------|------|-------|
| # | Name | Type | Size | Value |
| # | | | | |
| # | uvm_test_top | alu_base_test | - | @472 |
| # | env | alu_env | - | @479 |
| # | agent | alu_agent | - | @486 |
| # | driver | alu_driver | - | @644 |
| # | rsp_port | uvm_analysis_port | - | @659 |
| # | seq_item_port | <pre>uvm_seq_item_pull_port</pre> | - | @651 |
| # | monitor | alu_monitor | - | @520 |
| # | mon2scb | uvm_analysis_port | - | @527 |
| # | sequencer | uvm_sequencer | - | @535 |
| # | rsp_export | uvm_analysis_export | - | @542 |
| # | seq_item_export | <pre>uvm_seq_item_pull_imp</pre> | - | @636 |
| # | arbitration_queue | array | 0 | - |
| # | lock_queue | array | 0 | - |
| # | num_last_reqs | integral | 32 | 'd1 |
| # | num_last_rsps | integral | 32 | 'd1 |
| # | coverage | alu_coverage | - | @500 |
| # | analysis_imp | uvm_analysis_imp | - | @507 |
| # | scoreboard | alu_scoreboard | - | @493 |
| # | scb_port | uvm_analysis_imp | - | @674 |
| # | | | | |
| # | | | | |
| | | | | |

File: code_coverage.txt

```
Coverage Report by DU with details
______
=== Design Unit: work.rv32i_alu
______
Branch Coverage:
                    Bins
  Enabled Coverage
                          Hits Misses Coverage
  _____
                    ____
                          ----
                               -----
                     43
  Branches
                           43
                                0 100.00%
Branch Coverage for Design Unit work.rv32i alu
  Line
         Item
                          Count Source
 File rv32i_alu.sv
5273 Count coming in to IF
  150
  150
                                     if (!i_rst_n) begin
           1
                           546
  154
            1
                           4727
                                    end else begin
Branch totals: 2 hits of 2 branches = 100.00%
4727 Count coming in to IF
  156
  156
                           4725
                                        if (i_ce && !stall_bit)
begin //update logicister only if this stage is enabled
                            2
                               All False Count
Branch totals: 2 hits of 2 branches = 100.00%
176
                           4727
                                Count coming in to IF
   179
                                4726
                                               end else if
(!stall_bit) begin //clock-enable will change only when not stalled
Branch totals: 1 hit of 1 branch = 100.00%
-----IF Branch-----
                           5008 Count coming in to IF
  196
  196
                             2463
                                        b = (opcode_rtype ||
             1
opcode_branch) ? i_rs2 : i_imm; // b can either be rs2 or imm
  196
             2
                             2545
                                        b = (opcode_rtype ||
opcode_branch) ? i_rs2 : i_imm; // b can either be rs2 or imm
```

Branch totals: 2 hits of 2 branches = 100.00%

```
-----IF Branch-----
  197
                              5009 Count coming in to IF
  197
             1
                               380
                                          if (alu\_add) y\_d = a + b;
                              4629 All False Count
Branch totals: 2 hits of 2 branches = 100.00%
-----IF Branch------
                              5009 Count coming in to IF
  198
  198
             1
                               340
                                          if (alu\_sub) y_d = a - b;
                              4669 All False Count
Branch totals: 2 hits of 2 branches = 100.00%
-----IF Branch------
                              5009 Count coming in to IF
  199
  199
                                 718
                                            if (alu_slt || alu_sltu)
begin
                              4291 All False Count
Branch totals: 2 hits of 2 branches = 100.00%
-----IF Branch-----
                               718 Count coming in to IF
  201
                                 353
   201
               1
                                                if (alu_slt) y_d =
(a[31] ^ b[31]) ? {31'b0, a[31]} : y_d;
                               365 All False Count
Branch totals: 2 hits of 2 branches = 100.00%
201
                               353 Count coming in to IF
   201
                                 169
                                                 if (alu_slt) y_d =
(a[31] ^ b[31]) ? {31'b0, a[31]} : y_d;
   201
                                 184
                                                if (alu_slt) y_d =
(a[31] ^ b[31]) ? {31'b0, a[31]} : y_d;
Branch totals: 2 hits of 2 branches = 100.00%
203
                              5009
                                    Count coming in to IF
  203
             1
                              385
                                          if (alu\_xor) y_d = a ^ b;
                              4624 All False Count
Branch totals: 2 hits of 2 branches = 100.00%
5009
  204
                                    Count coming in to IF
  204
             1
                               379
                                          if (alu_or) y_d = a \mid b;
                              4630
                                   All False Count
Branch totals: 2 hits of 2 branches = 100.00%
```

```
-----IF Branch-----
  205
                             5009 Count coming in to IF
                                        if (alu_and) y_d = a \& b;
  205
             1
                             334
                             4675 All False Count
Branch totals: 2 hits of 2 branches = 100.00%
-----IF Branch------
                             5009 Count coming in to IF
  206
  206
                                355
              1
                                          if (alu_sll) y_d = a <<
b[4:0];
                             4654 All False Count
Branch totals: 2 hits of 2 branches = 100.00%
207
                             5009 Count coming in to IF
  207
                               340
              1
                                           if (alu_srl) y_d = a >>
b[4:0];
                             4669 All False Count
Branch totals: 2 hits of 2 branches = 100.00%
-----IF Branch------
  208
                             5009
                                  Count coming in to IF
  208
                                  350
                                              if (alu_sra) y_d =
$signed(a) >>> b[4:0];
                             4659 All False Count
Branch totals: 2 hits of 2 branches = 100.00%
-----IF Branch------
  209
                             5009 Count coming in to IF
  209
              1
                               690
                                           if (alu_eq || alu_neq)
begin
                             4319 All False Count
Branch totals: 2 hits of 2 branches = 100.00%
211
                             690
                                  Count coming in to IF
                               365
  211
                                              if (alu_neq) y_d =
{31'b0, !y_d[0]};
                             325 All False Count
Branch totals: 2 hits of 2 branches = 100.00%
-----IF Branch------
                             5009 Count coming in to IF
  213
                                737
  213
              1
                                           if (alu_ge || alu_geu)
begin
```

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

215 737 Count coming in to IF

215 1 364 if $(alu_ge) y_d =$

 $(a[31] ^ b[31]) ? {31'b0, b[31]} : y_d;$

373 All False Count

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

215 364 Count coming in to IF

215 2 179 if (alu_ge) y_d =

 $(a[31] ^ b[31]) ? {31'b0, b[31]} : y_d;$

215 3 185 if (alu_ge) y_d =

 $(a[31] ^ b[31]) ? {31'b0, b[31]} : y_d;$

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

227 10015 Count coming in to IF

227 1 10013 if (!i_flush) begin

2 All False Count

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

228 10013 Count coming in to IF

228 1 10011 if (opcode_rtype ||

opcode_itype) rd_d = y_d;

2 All False Count

Branch totals: 2 hits of 2 branches = 100.00%

Condition Coverage:

Enabled Coverage
Bins Covered Misses Coverage
----Conditions
Bins Covered Misses Coverage
----12 12 0 100.00%

Condition Coverage for Design Unit work.rv32i_alu --

File rv32i_alu.sv

-----Focused Condition View-----

Line 199 Item 1 (alu_slt || alu_sltu)

Condition totals: 2 of 2 input terms covered = 100.00%

```
-----Focused Condition View (Bimodal)------
        201 Item 1 (a[31] ^ b[31])
Line
Condition totals: 2 of 2 input terms covered = 100.00%
-----Focused Condition View-----
        209 Item 1 (alu_eq | alu_neq)
Line
Condition totals: 2 of 2 input terms covered = 100.00%
-----Focused Condition View-----
        213 Item 1 (alu_ge | alu_geu)
Condition totals: 2 of 2 input terms covered = 100.00%
-----Focused Condition View (Bimodal)-----
        215 Item 1 (a[31] ^ b[31])
Condition totals: 2 of 2 input terms covered = 100.00%
-----Focused Condition View-----
        228 Item 1 (opcode_rtype | opcode_itype)
Condition totals: 2 of 2 input terms covered = 100.00%
Statement Coverage:
  Enabled Coverage
                        Bins
                                Hits Misses Coverage
   _____
                                 ----
                          ____
                                       _____
                                  47
                           47
                                          0 100.00%
  Statements
Statement Coverage for Design Unit work.rv32i_alu --
  Line
            Item
                                 Count
                                       Source
```

| | | |
|----------|------------|--------------------|
| File rv3 | 32i_alu.sv | |
| 31 | | module rv32i_alu (|
| 32 | | i_clk, |
| 33 | | i_rst_n, |
| 34 | | i_alu, |
| 35 | | i_rs1_addr, |
| 36 | | i_rs1, |
| 37 | | i_rs2, |
| 38 | | i_imm, |
| 39 | | i_funct3, |
| 40 | | i_opcode, |
| 41 | | i_exception, |
| 42 | | i_pc, |
| 43 | | i_rd_addr, |

```
44
                                                           i_ce,
    45
                                                           i_stall,
    46
                                                           i_force_stall,
    47
                                                           i_flush,
    48
                                                           o_rs1_addr,
    49
                                                           o_rs1,
    50
                                                           o_rs2,
    51
                                                           o_imm,
    52
                                                           o_funct3,
    53
                                                           o_opcode,
    54
                                                           o_exception,
    55
                                                           о_у,
    56
                                                           o_pc,
    57
                                                           o_next_pc,
    58
                                                           o_change_pc,
    59
                                                           o_wr_rd,
    60
                                                           o_rd_addr,
    61
                                                           o_rd,
    62
                                                           o_rd_valid,
    63
                                                           o_stall_from_alu,
    64
                                                           o_ce,
    65
                                                           o_stall,
    66
                                                           o_flush
    67
                                                       );
    68
                                                           input logic i_clk, i_rst_n;
    69
                                                               input logic [`ALU_WIDTH-1:0]
i alu;
        //alu operation type from previous stage
    70
                                                             input logic [4:0] i_rsl_addr;
//address for logicister source 1
    71
                                                              input logic [31:0] i_rs1; //
Source logicister 1 value
    72
                                                                 input logic [31:0] i_rs2;
//Source logicister 2 value
                                                                 input logic [31:0] i_imm;
//Immediate value from previous stage
    74
                                                               input logic [2:0] i_funct3;
//function type from previous stage
    75
                                                            input logic [`OPCODE_WIDTH-1:0]
i_opcode; //opcode type from previous stage
     76
                                                                                 input logic
[`EXCEPTION_WIDTH-1:0] i_exception; //exception from decoder stage
    77
                                                                  input logic [31:0] i_pc;
//Program Counter
    78
                                                              input logic [4:0] i_rd_addr;
//address for destination logicister (from previous stage)
    79
                                                            input logic i_ce; // input clk
```

```
enable for pipeline stalling of this stage
    80
                                                          // coverage off
    81
                                                           input logic i_stall; //informs
this stage to stall
    82
                                                               input logic i_force_stall;
//force this stage to stall
    83
                                                             input logic i_flush; //flush
this stage
    84
                                                          // coverage on
    85
                                                           output logic [4:0] o_rs1_addr;
//address for logicister source 1
    86
                                                              output logic [31:0] o_rs1;
//Source logicister 1 value
    87
                                                              output logic [31:0] o_rs2;
//Source logicister 2 value
    88
                                                              output logic [11:0] o_imm;
//Immediate value
    89
                                                             output logic [2:0] o_funct3;
// function type
     90
                                                                              output logic
[`OPCODE_WIDTH-1:0] o_opcode; //opcode type
                                                                              output logic
[`EXCEPTION_WIDTH-1:0] o_exception; //exception: illegal inst,ecall,ebreak,mret
    92
                                                                output logic [31:0] o_y;
//result of arithmetic operation
    93
                                                           output logic [31:0] o_pc; //pc
logicister in pipeline
    94
                                                           output logic [31:0] o_next_pc;
//new pc value
    95
                                                                output logic o_change_pc;
//high if PC needs to jump
    96
                                                            output logic o_wr_rd; //write
rd to the base logic if enabled
                                                            output logic [4:0] o_rd_addr;
//address for destination logicister
    98
                                                               output logic [31:0] o_rd;
//value to be written back to destination logicister
                                                                output logic o_rd_valid;
//high if o_rd is valid (not load nor csr instruction)
    100
                                                          // coverage off
                                                          output logic o_stall_from_alu
    101
                                                                ; //prepare to stall next
stage(memory-access stage) for load/store instruction
    103
                                                          // coverage on
    104
                                                             output logic o_ce; // output
clk enable for pipeline stalling of next stage
```

```
105
                                                            // coverage off
     106
                                                                      output logic o_stall;
//informs pipeline to stall
    107
                                                              output logic o_flush; //flush
previous stages
    108
                                                            // coverage on
    109
                                                            // Internal signals
    110
                                                            logic
                                                                          alu_add;
    111
                                                            logic
                                                                          alu_sub;
    112
                                                            logic
                                                                          alu_slt;
                                                                          alu_sltu;
    113
                                                            logic
                                                            logic
    114
                                                                          alu_xor;
                                                            logic
    115
                                                                          alu_or;
    116
                                                            logic
                                                                          alu_and;
    117
                                                            logic
                                                                          alu sll;
    118
                                                            logic
                                                                          alu_srl;
    119
                                                            logic
                                                                          alu sra;
    120
                                                            logic
                                                                          alu_eq;
    121
                                                            logic
                                                                          alu_neq;
    122
                                                            logic
                                                                          alu_ge;
    123
                                                            logic
                                                                          alu_geu;
    124
                                                            logic
                                                                          opcode_rtype;
    125
                                                            logic
                                                                          opcode_itype;
    126
                                                            // coverage off
    127
                                                            logic
                                                                          opcode_load;
    128
                                                            logic
                                                                          opcode_store;
    129
                                                            logic
                                                                          opcode_branch;
    130
                                                            logic
                                                                          opcode_jal;
    131
                                                            logic
                                                                          opcode_jalr;
    132
                                                            logic
                                                                          opcode_lui;
    133
                                                            logic
                                                                          opcode_auipc;
    134
                                                            logic
                                                                          opcode_system;
    135
                                                            logic
                                                                          opcode_fence;
    136
                                                            // coverage on
    137
                                                            logic [31:0] a; //operand A
                                                            logic [31:0] b; //operand B
    138
    139
                                                            logic [31:0] y_d; //ALU output
    140
                                                                  logic [31:0] rd_d; //next
value to be written back to destination logicister
    141
                                                              logic
                                                                            wr_rd_d;
                                                                                       //write
rd to baselogic if enabled
                                                                   logic
                                                                                 rd_valid_d;
//high if rd is valid (not load nor csr instruction)
    143
                                                            logic [31:0] a_pc;
    144
                                                            logic [31:0] sum;
    145
                                                            // coverage off
```

```
146
                                                             logic
                                                                          stall bit;
    147
                                                             // coverage on
                                                                   //logicister the output of
    148
i alu
    149
                       1
                                                   5273
                                                                  always_ff @(posedge i_clk,
negedge i_rst_n) begin
    150
                                                                 if (!i_rst_n) begin
    151
                                                546
                     1
                                                                     o_exception
                                                                                       <= 0;
    152
                     1
                                                546
                                                                     o_ce
                                                                                       <= 0;
    153
                     1
                                                546
                                                                     o_stall_from_alu <= 0;</pre>
    154
                                                                 end else begin
    155
                                                                      // coverage off -item c
1
    156
                                                                      if (i_ce && !stall_bit)
begin //update logicister only if this stage is enabled
    157
                                                     4725
                                                                                   o opcode <=
i opcode;
    158
                       1
                                                   4725
                                                                               o exception <=
i_exception;
    159
                     1
                                               4725
                                                                         o_y \ll y_d;
    160
                       1
                                                   4725
                                                                                o_rs1_addr <=
i_rs1_addr;
    161
                                               4725
                                                                         o_rs1 <= i_rs1;
                     1
                                               4725
    162
                                                                         o_rs2 <= i_rs2;
                     1
                                                    4725
    163
                       1
                                                                                  o_rd_addr <=
i_rd_addr;
     164
                        1
                                                       4725
                                                                                      o_imm <=
i_imm[11:0];
    165
                        1
                                                     4725
                                                                                   o_funct3 <=
i_funct3;
    166
                                               4725
                                                                         o rd <= rd d;
    167
                       1
                                                   4725
                                                                                o_rd_valid <=
rd valid d;
    168
                                               4725
                                                                         o_wr_rd <= wr_rd_d;</pre>
    169
                                                                         // coverage off
    170
                                                                          o_stall_from_alu <=
i_opcode[`STORE] || i_opcode[`LOAD]
                                                                               ; //stall next
stage(memory-access stage) when need to store/load
    172
                                                                         // coverage on
    173
                                                   4725
                                                                               o_pc <= i_pc;
//since accessing data memory always takes more than 1 cycle
    174
                                                                     end
                                                                     // coverage off
    175
    176
                                                                               if (i_flush &&
```

!stall_bit) begin //flush this stage so clock-enable of next stage is disabled at next

```
clock cycle
    177
                                                                         o_ce <= 0;
    178
                                                                         // coverage on
    179
                                                                                  end else if
(!stall_bit) begin //clock-enable will change only when not stalled
    180
                     1
                                              4726
                                                                        o_ce <= i_ce;
    181
                                                                         // coverage off
    182
                                                                      end else if (stall_bit
&& !i_stall)
    183
                                                                            o_ce <= 0; //if
this stage is stalled but next stage is not, disable
    184
                                                                    // coverage on
    185
                                                                      //clock enable of next
stage at next clock cycle (pipeline bubble)
    186
                                                                end
    187
                                                            end
    188
                                                                 // determine operation used
then compute for y output
    189
    190
                                              5009
                                                            always_comb begin
    191
                                              5009
                                                                y_d = 0;
    192
                                                                // coverage off
    193
                                                                            = (opcode_jal ||
opcode_auipc) ? i_pc : i_rs1; // a can either be pc or rs1
    194
                                                                // coverage on
    195
                                                                // coverage off -item c 1
    196
                                                  5009
                       1
                                                                          = (opcode_rtype | |
opcode_branch) ? i_rs2 : i_imm; // b can either be rs2 or imm
    197
                     1
                                               380
                                                                if (alu\_add) y\_d = a + b;
                                                                if (alu\_sub) y\_d = a - b;
    198
                     1
                                               340
    199
                                                                    if (alu_slt || alu_sltu)
begin
    200
                                               718
                                                                    y_d = {31'b0, (a < b)};
                                                                          if (alu slt) y d =
    201
                       1
                                                   353
(a[31] ^ b[31]) ? {31'b0, a[31]} : y_d;
    202
                                                                end
    203
                     1
                                               385
                                                                if (alu\_xor) y_d = a ^ b;
    204
                     1
                                               379
                                                                if (alu_or) y_d = a | b;
    205
                     1
                                               334
                                                                if (alu\_and) y\_d = a \& b;
    206
                      1
                                                   355
                                                                     if (alu_sll) y_d = a <<
b[4:0];
    207
                      1
                                                   340
                                                                     if (alu_srl) y_d = a >>
b[4:0];
     208
                                                       350
                        1
                                                                          if (alu_sra) y_d =
$signed(a) >>> b[4:0];
    209
                                                                      if (alu_eq || alu_neq)
```

```
begin
    210
                                                  690
                                                                        y_d = \{31'b0, (a ==
                      1
b)};
                                                                         if (alu_neq) y_d =
    211
                      1
                                                   365
{31'b0, !y_d[0]};
    212
                                                                end
    213
                                                                     if (alu_ge || alu_geu)
begin
    214
                      1
                                                  737
                                                                        y_d = {31'b0, (a >=
b)};
    215
                                                   364
                                                                           if (alu\_ge) y_d =
(a[31] ^ b[31]) ? {31'b0, b[31]} : y_d;
                                                                end
    217
                                                           end
    218
                                                            //determine o_rd to be saved to
baseg and next value of PC
    219
                                             10015
                                                           always_comb begin
    220
                      1
                                                10015
                                                                    o flush
                                                                             = i flush;
//flush this stage along with the previous stages
    221
                                             10015
                                                               rd d
                                                                            = 0;
    222
                                             10015
                                                               rd_valid_d = 0;
    223
                    1
                                             10015
                                                                o_{change_pc} = 0;
    224
                    1
                                             10015
                                                                o_next_pc = 0;
    225
                                             10015
                                                                wr_rd_d
                    1
                                                                           = 0;
    226
                    1
                                             10015
                                                                a_pc
                                                                            = i_pc;
    227
                                                                if (!i_flush) begin
    228
                      1
                                                10011
                                                                        if (opcode_rtype ||
opcode_itype) rd_d = y_d;
    229
                                                                    // coverage off
    230
                                                                        if (opcode_branch &&
y d[0]) begin
    231
                                                                           o_next_pc = sum;
//branch iff value of ALU is 1(true)
    232
                                                                        o change pc =
    233
                                                                             i_ce; //change
PC when ce of this stage is high (o_change_pc is valid)
    234
                                                                        o_flush = i_ce;
    235
                                                                    end
    236
                                                                           if (opcode_jal ||
opcode_jalr) begin
    237
                                                                            if (opcode_jalr)
a_pc = i_rs1;
    238
                                                                           o_next_pc = sum;
//jump to new PC
    239
                                                                        o_change_pc =
    240
                                                                             i_ce; //change
```

```
PC when ce of this stage is high (o_change_pc is valid)
    241
                                                                      o_flush = i_ce;
    242
                                                                        rd_d = i_pc + 4;
//logicister the next pc value to destination logicister
                                                                  end
    244
                                                                  // coverage on
    245
                                                              end
    246
                                                              // coverage off
    247
                                                                   if (opcode_lui) rd_d =
i_imm;
    248
                                                                 if (opcode_auipc) rd_d =
sum;
    249
                                                                     if (opcode_branch ||
opcode_store || (opcode_system && i_funct3 == 0) || opcode_fence)
    250
                                                                            wr_rd_d = 0;
//i_funct3==0 are the non-csr system instructions
                                                              else
    252
                                                                   wr_rd_d = 1; //always
write to the destination logic except when instruction is BRANCH or STORE or
SYSTEM(except CSR system instruction)
    253
                                                                       if (opcode_load ||
(opcode_system && i_funct3 != 0))
    254
                                                                 rd_valid_d =
    255
                                                                       0; //value of o_rd
for load and CSR write is not yet available at this stage
    256
                                                              else rd_valid_d = 1;
    257
                                                              // coverage on
    258
                                                                //stall logic (stall when
upper stages are stalled, when forced to stall, or when needs to flush previous stages
but are still stalled)
    259
                                                10015
                                                                    o_stall = (i_stall ||
i_force_stall) && !i_flush; //stall when alu needs wait time
    260
                                                          end
    261
    262
                                                          assign
                                                 10004
    263
                                                                     sum = a_pc + i_imm;
//share adder for all addition operation for less resource utilization
                     1
                                                  3
                                                            assign stall_bit = o_stall ||
    264
i_stall;
```

File: coverage_all_files_default.txt

| Coverage Report Summary Dat | a by file | | | | |
|---|--|---------------------|--------------------------|---|--------|
| ======================================= | ======== | :====== | :======= | ======= | ====== |
| === File: agent.sv | | | | | |
| | ======== | | :====== | :======= | ====== |
| Enabled Coverage | Bins | Hits | Misses | Coverage | |
| | | | | | |
| Branches | 12 | 5 | 7 | 41.66% | |
| Statements | 20 | 16 | 4 | 80.00% | |
| | | | | | |
| | ========= | | | ======= | ====== |
| === File: coverage.sv | | | | | |
| Enabled Coverage | Bins | | | Coverage | ====== |
| Enabled Coverage | BIIIS | | | | |
| Branches | 4 | 2 | | 50.00% | |
| Conditions | 2 | 0 | | 0.00% | |
| Statements | 9 | 6 | | 66.66% | |
| | | | | | |
| | | | | | |
| ======================================= | ======== | :====== | :====== | ======= | ====== |
| ==== File: driver.sv | ======== | ====== | ====== | ======= | ===== |
| | | | | | |
| === File: driver.sv | ======== | | | | |
| === File: driver.sv | ======== | | | ======= | |
| === File: driver.sv | ======= Bins | Hits | Misses | ======= | |
| === File: driver.sv ==================================== | ======= Bins | Hits | Misses | Coverage | |
| === File: driver.sv =================================== | ======== Bins 16 50 | Hits 6 31 | Misses 10 | Coverage 37.50% 62.00% | ===== |
| === File: driver.sv =================================== | ======== Bins 16 50 | Hits 6 31 | Misses 10 | Coverage 37.50% 62.00% | ===== |
| === File: driver.sv =================================== | ======= Bins 16 50 | Hits 6 31 | Misses 10 19 | Coverage 37.50% 62.00% | ===== |
| === File: driver.sv =================================== | ====================================== | Hits 6 31 | Misses 10 19 | Coverage 37.50% 62.00% | ===== |
| === File: driver.sv =================================== | ====================================== | Hits 6 31 | Misses 10 19 | Coverage 37.50% 62.00% | ===== |
| === File: driver.sv =================================== | Bins 16 50 =================================== | Hits 6 31 Hits | Misses 10 19 Misses | Coverage 37.50% 62.00% | ===== |
| === File: driver.sv =================================== | Bins 16 50 =================================== | Hits 6 31 Hits | Misses 10 19 Misses 1 | Coverage 37.50% 62.00% | ===== |
| === File: driver.sv =================================== | ### Bins | Hits 6 31 Hits 1 | Misses 10 19 Misses 1 | Coverage 37.50% 62.00% Coverage 50.00% | ===== |
| === File: driver.sv =================================== | Bins 16 50 Bins 2 15 | Hits 6 31 Hits 1 12 | Misses 10 19 Misses 13 | Coverage 37.50% 62.00% Coverage Coverage 50.00% | ====== |
| === File: driver.sv =================================== | Bins 16 50 Bins 2 15 | Hits 6 31 Hits 1 12 | Misses 10 19 Misses 13 | Coverage 37.50% 62.00% Coverage Coverage 50.00% | ====== |
| === File: driver.sv Enabled Coverage Branches Statements === File: environment.sv Enabled Coverage Enabled Coverage Branches Statements | Bins 16 50 Bins 2 15 | Hits 6 31 Hits 1 12 | Misses 10 19 Misses 13 3 | Coverage 37.50% 62.00% Coverage 50.00% 80.00% | ====== |
| === File: driver.sv =================================== | Bins 16 50 Bins 2 15 | Hits 6 31 Hits 1 12 | Misses 10 19 Misses 13 3 | Coverage 37.50% 62.00% Coverage Coverage 50.00% 80.00% | ====== |
| === File: driver.sv =================================== | Bins 16 50 Bins 2 15 | Hits 6 31 Hits 1 12 | Misses 10 19 Misses 13 3 | Coverage 37.50% 62.00% Coverage 50.00% 80.00% | ====== |

| === | ======================================= | | | ======= | ======= | :======== |
|-----|---|---------|---------|-----------|-----------|-----------|
| | Enabled Coverage | Bins | Hits | | Coverage | |
| | Branches | 16 | 6 | | 37.50% | |
| | Statements | 59 | 52 | 7 | 88.13% | |
| | | | | | | |
| === | ======================================= | | | :====== | ======= | ======== |
| === | File: rv32i_alu.sv | | | | | |
| === | | | | ======= | ======= | ======== |
| | Enabled Coverage | Bins | Hits | Misses | Coverage | |
| | | | | | | |
| | Branches | 43 | 42 | 1 | 97.67% | |
| | Conditions | 12 | 10 | 2 | 83.33% | |
| | Statements | 47 | 47 | 0 | 100.00% | |
| | | | | | | |
| === | | | | ======= | ======= | ======== |
| === | File: scoreboard.sv | | | | | |
| === | ======================================= | | | | | ========= |
| | Enabled Coverage | Bins | Hits | Misses | Coverage | |
| | | | | | | |
| | Branches | 139 | 74 | | 53.23% | |
| | Conditions | 29 | 10 | | 34.48% | |
| | Statements | 98 | 62 | 36 | 63.26% | |
| | | | | | | |
| | | ======= | | ======= | ======= | ======== |
| === | File: sequencer.sv | | | | | |
| === | | | | | | ======== |
| | Enabled Coverage | Bins | Hits | | Coverage | |
| | | | | | | |
| | Branches | 58 | 30 | | 51.72% | |
| | Conditions | 2 | 0 | | 0.00% | |
| | Statements | 798 | 776 | 22 | 97.24% | |
| | | | | | | |
| | | | | :====== | ======= | ======== |
| | File: test.sv | | | | | |
| === | | | | | | ======== |
| | Enabled Coverage | | Hits | | Coverage | |
| | | | | | | |
| | Branches | 6 | 2 | | 33.33% | |
| | Statements | 21 | 18 | 3 | 85.71% | |
| | | | | | . | |
| | | ======= | ======= | ====== | ======= | ======= |
| | File: top.sv | | | . | . | |
| _== | Enabled Coverage | | | | | ======= |
| | Enabled Coverage | Bins | Hits | MISSES | Coverage | |

=== File: transaction.sv

| Enal | bled Coverage | Bins | Hits | Misses | Coverage |
|------|---------------|------|------|--------|----------|
| | | | | | |
| Brai | nches | 45 | 0 | 45 | 0.00% |
| Cond | ditions | 9 | 0 | 9 | 0.00% |
| Sta | tements | 80 | 13 | 67 | 16.25% |

TOTAL COVERGROUP COVERAGE: 81.25% COVERGROUP TYPES: 1

TOTAL ASSERTION COVERAGE: 0.00% ASSERTIONS: 2

Total Coverage By File (code coverage only, filtered view): 57.66%

File: report.txt

Recursive Coverage Report Summary Data by DU

=== Design Unit: work.top_sv_unit

| Enabled Coverage | Bins | Hits | Misses | Coverage |
|---------------------|------|------|--------|----------|
| | | | | |
| Branches | 298 | 126 | 172 | 42.28% |
| Conditions | 42 | 10 | 32 | 23.80% |
| Covergroups | 1 | na | na | 81.25% |
| Coverpoints/Crosses | 8 | na | na | na |
| Covergroup Bins | 56 | 52 | 4 | 92.85% |
| Statements | 1150 | 986 | 164 | 85.73% |

=== Design Unit: work.alu_if

| ======================================= | ======= | ====== | ======= | ======================================= |
|---|---------|--------|---------|---|
| Enabled Coverage | Bins | Hits | Misses | Coverage |

| Assertions | 2 | 0 | 2 | 0.00% |
|------------|----|----|---|---------|
| Statements | 37 | 37 | 0 | 100.00% |

=== Design Unit: work.rv32i_alu

| Enabled Coverage | Bins | Hits | Misses | Coverage | |
|------------------|------|------|--------|----------|--|
| | | | | | |
| Branches | 43 | 42 | 1 | 97.67% | |
| Conditions | 12 | 10 | 2 | 83.33% | |
| Statements | 47 | 47 | 0 | 100.00% | |

=== Design Unit: work.top

| Enal | oled Coverage | Bins | Hits | Misses | Coverage |
|------|---------------|------|------|--------|----------|
| | | | | | |
| Asse | ertions | 2 | 0 | 2 | 0.00% |
| Brai | nches | 43 | 42 | 1 | 97.67% |
| Cond | ditions | 12 | 10 | 2 | 83.33% |
| Stat | tements | 91 | 90 | 1 | 98.90% |

File: report_1000.txt

| erage Repo | ort by DU with o | | | | |
|-----------------------|------------------|----------------|------------|---------|---|
| | nit: work.covera | | ====== | ====== | ========== |
| ======= nch Covera | aae: | ======== | ======= | ======= | ======================================= |
| Enabled (| | Bins | Hits | Misses | Coverage |
| | | | | | |
| Branches | | 145 | 75 | 70 | 51.72% |
| ======= | | ====Branch De | tails==== | ====== | |
| nch Covera | age for Design (| Unit work.cove | rage_sv_u | nit | |
| Line | Item | | Count | Source | 2 |
| | | | | | |
| ile transa | action.sv | | | | |
| | | CASE | Branch | | |
| 224 | | | 1025 | Count | coming in to CASE |
| 225 | 1 | | 68 | | |
| 227 | 1 | | 83 | | |
| 229 | 1 | | 74 | | |
| 231 | 1 | | 61 | | |
| 233 | 1 | | 79 | | |
| 235 | 1 | | 70 | | |
| 237 | 1 | | 79 | | |
| 239 | 1 | | 68 | | |
| 242 | 1 | | 84 | | |
| 244 | 1 | | 79 | | |
| 245 | 1 | | 82 | | |
| 246 | 1 | | 70 | | |
| 247 | 1 | | 70 | | |
| 249 | 1 | | 58 | | |
| 250 | 1 | | ***0*** | | |
| 250 | s: 14 hits of 15 | 5 branches = 9 | 3.33% | | |
| | | | | | |
| nch totals | | IF Br | anch | | |
| nch totals | | IF Br | anch 68 | | coming in to IF |
| nch totals | 1 | IF Br | | | |

-----IF Branch------

| 228 | | 83 | Count coming in to IF |
|--------------|----------------------------|---------------|-----------------------|
| 228 | 1 | 9 | |
| 228 | 2 | 74 | |
| Branch total | ls: 2 hits of 2 branc | hes = 100.00% | |
| | | | |
| | | IF Branch | |
| | | | |
| 230 | | 74 | Count coming in to IF |
| 230 | 1 | 7 | |
| 230 | 2 | 67 | |
| Branch total | ls: 2 hits of 2 branc | hes = 100.00% | |
| | | | |
| | | IF Branch | |
| 232 | | 61 | Count coming in to IF |
| 232 | 1 | 8 | |
| 232 | 2 | 53 | |
| | | | |
| Branch total | ls: 2 hits of 2 branc | mes = 100.00% | |
| | | | |
| | | IF Branch | |
| 234 | | 79 | Count coming in to IF |
| 234 | 1 | 9 | |
| 234 | 2 | 70 | |
| Branch total | ls: 2 hits of 2 branc | hes = 100.00% | |
| | | | |
| | | IF Branch | |
| 236 | | 70 | Count coming in to IF |
| 236 | 1 | 7 | |
| | | | |
| 236 | 2 | 63 | |
| Branch total | ls: 2 hits of 2 branc | hes = 100.00% | |
| | | | |
| | | IF Branch | |
| 238 | | 79 | Count coming in to IF |
| 238 | 1 | 7 | |
| 238 | 2 | 72 | |
| Branch total | ls: 2 hits of 2 branc | hes = 100.00% | |
| | | | |
| | | IF Branch | |
| 241 | | | |
| | - | 68 | Count coming in to IF |
| 241 | 1 | 4 | |
| 241 | 2 | 64 | |
| Branch total | ls: 2 hits of 2 branc | hes = 100.00% | |
| | | | |
| | | IF Branch | |
| 243 | | 84 | Count coming in to IF |
| 243 | 1 | 42 | |
| 243 | 2 | 42 | |
| | - ls: 2 hits of 2 branc | | |
| | | | |

| | | IF Branch | |
|----------------|------------------|-------------------|-------------------------|
| 244 | | 79 | Count coming in to IF |
| 244 | 2 | 42 | |
| 244 | 3 | 37 | |
| Branch totals: | 2 hits of 2 br | canches = 100.00% | |
| | | | |
| | | IF Branch | |
| 245 | | 82 | Count coming in to IF |
| 245 | 2 | 2 | |
| 245 | 3 | 80 | |
| Branch totals: | 2 hits of 2 br | canches = 100.00% | |
| | | | |
| | | IF Branch | |
| 246 | | 70 | Count coming in to IF |
| 246 | 2 | 70 | |
| 246 | 3 | * * * 0 * * * | |
| Branch totals: | 1 hit of 2 bra | anches = 50.00% | |
| | | | |
| | | IF Branch | |
| 248 | | 70 | Count coming in to IF |
| 248 | 1 | 31 | |
| 248 | 2 | 39 | |
| Branch totals: | 2 hits of 2 br | canches = 100.00% | |
| | | | |
| | | IF Branch | |
| 249 | | 58 | Count coming in to IF |
| 249 | 2 | 25 | |
| 249 | 3 | 33 | |
| Branch totals: | 2 hits of 2 br | ranches = 100.00% | |
| | | | |
| | | | |
| File coverag | | | |
| | | | |
| 69 | | 50001 | Count coming in to IF |
| 69 | 1 | 914 | |
| | | 49087 | All False Count |
| Branch totals: | : 2 hits of 2 br | canches = 100.00% | |
| | | | |
| | | | |
| File generat | | G2 G2 D 1 | |
| | | | Court coming in to CAGE |
| 131 | - | 1000 | Count coming in to CASE |
| 132 | 1 | 334 | |
| 136 | 1 | 333 | |
| 140 | 1 | 333 | |

Branch totals: 3 hits of 4 branches = 75.00%

-----IF Branch-----

149 1000 Count coming in to IF 149 1 *****

1000 All False Count

Branch totals: 1 hit of 2 branches = 50.00%

| | | CASE Branch | |
|-----|---|-------------|-------------------------|
| 372 | | 1025 | Count coming in to CASE |
| 373 | 1 | 68 | |
| 374 | 1 | 83 | |
| 375 | 1 | 74 | |
| 376 | 1 | 61 | |
| 377 | 1 | 79 | |
| 378 | 1 | 70 | |
| 379 | 1 | 79 | |
| 380 | 1 | 68 | |
| 381 | 1 | 84 | |
| 382 | 1 | 79 | |
| 383 | 1 | 82 | |
| 384 | 1 | 70 | |
| 385 | 1 | 70 | |
| 386 | 1 | 58 | |
| 387 | 1 | *** \ \ * * | |

Branch totals: 14 hits of 15 branches = 93.33%

| | | CASE Branch | |
|-----|---|-------------|-------------------------|
| 391 | | 1025 | Count coming in to CASE |
| 392 | 1 | 113 | |
| 393 | 1 | 91 | |
| 394 | 1 | 102 | |
| 395 | 1 | 91 | |
| 396 | 1 | 109 | |
| 397 | 1 | 88 | |
| 398 | 1 | 82 | |
| 399 | 1 | 76 | |
| 400 | 1 | 77 | |
| 401 | 1 | 105 | |
| 402 | 1 | 2 | |
| 403 | 1 | 89 | |

Branch totals: 12 hits of 12 branches = 100.00%

| | | TF Branch | |
|----------------|-------------|-----------------------------|-----------------------|
| 51 | | 50001 | |
| 51 | 1 | 914 | |
| | | 49087 | All False Count |
| Branch totals: | 2 hits of 2 | branches = 100.00% | |
| File scorebo | ard.sv | | |
| | | IF Branch | |
| 160 | | ***0*** | Count coming in to IF |
| 160 | 1 | ***0*** | |
| 162 | 1 | ***0*** | |
| Branch totals: | 0 hits of 2 | branches = 0.00% | |
| | | IF Branch | |
| 165 | | ***0*** | Count coming in to IF |
| 165 | 1 | ***0*** | |
| 165 | 2 | ***0*** | |
| Branch totals: | 0 hits of 2 | branches = 0.00% | |
| | | IF Branch | |
| 166 | | * * * 0 * * * | Count coming in to IF |
| 166 | 1 | ***0*** | |
| 166 | 2 | ***0*** | |
| Branch totals: | 0 hits of 2 | branches = 0.00% | |
| | | IF Branch | |
| 170 | | * * * 0 * * * | Count coming in to IF |
| 170 | 1 | * * * 0 * * * | |
| | | * * * 0 * * * | All False Count |
| Branch totals: | 0 hits of 2 | branches = 0.00% | |
| | | IF Branch | |
| 172 | | ***0*** | Count coming in to IF |
| 172 | 1 | ***0*** | |
| | | ***0*** | All False Count |
| Branch totals: | 0 hits of 2 | branches = 0.00% | |
| | | IF Branch | |
| 177 | | ***0*** | Count coming in to IF |
| 177 | 1 | * * * 0 * * * | |
| Branch totals: | 0 hits of 2 | ***0*** branches = 0.00% | All False Count |
| | | | |
| 187 | | ***0*** | Count coming in to IF |
| | | | - |

187 1 ***0***

0 All False Count

Branch totals: 0 hits of 2 branches = 0.00%

-----IF Branch-----

188 ***0*** Count coming in to IF

188 1 ***0***

0 All False Count

Branch totals: 0 hits of 2 branches = 0.00%

-----IF Branch-----

191 ***0*** Count coming in to IF

191 1 ***0***

0 All False Count

Branch totals: 0 hits of 2 branches = 0.00%

-----IF Branch------

201 ***0*** Count coming in to IF

201 1 ***0***

0 All False Count

Branch totals: 0 hits of 2 branches = 0.00%

-----IF Branch-----

206 ***0*** Count coming in to IF

206 1 ***0***

0 All False Count

Branch totals: 0 hits of 2 branches = 0.00%

-----IF Branch-----

215 ***0*** Count coming in to IF

215 1 ***0***

215 2 ***0***

Branch totals: 0 hits of 2 branches = 0.00%

-----IF Branch-----

218 ***0*** Count coming in to IF

218 2 ***0***

Branch totals: 0 hits of 2 branches = 0.00%

-----IF Branch------

221 ***0*** Count coming in to IF

0 All False Count

Branch totals: 0 hits of 2 branches = 0.00%

| 226 | _ | ***0*** | Count coming in to IF |
|--|----------------|---|-----------------------|
| 226 | 1 | ***0*** | |
| | | ***0*** | All False Count |
| nch totals: | 0 hits of 2 br | canches = 0.00% | |
| | | | |
| 227 | _ | ***0*** | Count coming in to IF |
| 227 | 1 | ***0*** | |
| | | ***0*** | All False Count |
| nch totals: | 0 hits of 2 br | canches = 0.00% | |
| | | | |
| 247 | | ***0*** | Count coming in to IF |
| 247 | 1 | * * * 0 * * * | |
| 249 | 1 | ***0*** | |
| 251 | 1 | ***0*** | |
| | | * * * 0 * * * | All False Count |
| nch totals: | 0 hits of 4 br | ranches = 0.00% | |
| | | IF Branch **0*** | |
| 257 | | | Count coming in to if |
| | 1 | ***0*** | Count coming in to IF |
| 257 257 | 1 | - | |
| 257 anch totals: | 0 hits of 2 br | ***0*** ***0*** ranches = 0.00% | All False Count |
| 257 anch totals: | 0 hits of 2 br | ***0*** ***0*** ranches = 0.00% | |
| 257 unch totals: | 0 hits of 2 br | ***0*** ***0*** ranches = 0.00% | All False Count |
| 257 anch totals: | 0 hits of 2 br | ***0*** ***0*** ranches = 0.00% CASE Branch ***0*** | All False Count |
| 257 anch totals: 305 308 | 0 hits of 2 br | ***0*** ***0*** ranches = 0.00% CASE Branch ***0*** ***0*** | All False Count |
| 257 anch totals: 305 308 309 | 0 hits of 2 br | ***0*** ***0*** ranches = 0.00% CASE Branch ***0*** ***0*** | All False Count |
| 257 anch totals: 305 308 309 310 | 0 hits of 2 br | ***0*** ***0*** ranches = 0.00% CASE Branch ***0*** **0*** **0*** | All False Count |
| 257 anch totals: 305 308 309 310 311 | 0 hits of 2 br | ***0*** ***0*** ranches = 0.00% CASE Branch ***0*** ***0*** ***0*** ***0*** | All False Count |
| 257 anch totals: 305 308 309 310 311 313 | 0 hits of 2 br | ***0*** ***0*** ranches = 0.00% CASE Branch ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** | All False Count |
| 257 anch totals: 305 308 309 310 311 313 314 | 0 hits of 2 br | ***0*** ***0*** ranches = 0.00% CASE Branch ***0*** **0*** **0*** **0*** **0*** **0*** **0*** | All False Count |
| 257 anch totals: 305 308 309 310 311 313 314 315 | 0 hits of 2 br | ***0*** ***0*** **anches = 0.00% CASE Branch ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** | All False Count |
| 257 anch totals: 305 308 309 310 311 313 314 315 316 | 0 hits of 2 br | ***0*** ***0*** **anches = 0.00% CASE Branch ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** | All False Count |
| 257 anch totals: 305 308 309 310 311 313 314 315 316 317 | 0 hits of 2 br | ***0*** ***0*** ranches = 0.00% CASE Branch ***0*** **0*** **0*** **0*** **0*** **0*** **0*** **0*** **0*** **0*** **0*** **0*** | All False Count |
| 257 anch totals: 305 308 309 310 311 313 314 315 316 317 318 | 0 hits of 2 br | ***0*** ***0*** **anches = 0.00% CASE Branch ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** | All False Count |
| 257 anch totals: 305 308 309 310 311 313 314 315 316 317 318 319 | 0 hits of 2 br | ***0*** ***0*** **anches = 0.00% CASE Branch ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** | All False Count |
| 257 anch totals: 305 308 309 310 311 313 314 315 316 317 318 319 320 | 0 hits of 2 br | ***0*** ***0*** **anches = 0.00% CASE Branch ***0*** **0*** | All False Count |

-----IF Branch-----

| | | 65 | 5 60 | 7.69% | |
|--------------------------------------|-------------|--------------------|----------|-------------|--------|
| | | | | | |
| Condition Coverage: Enabled Coverage | | Bins Cover | | | |
| | | | | | |
| | 0 hits of | 2 branches = 0.00% | | | |
| 322 | 3 | ***0* | * * | | |
| 322 | 2 | ***0* | | comming min | CO II |
| 322 | | | ** Count | | |
| | | IF Branch- | | | |
| Branch totals: | 0 hits of | 2 branches = 0.00% | | | |
| 321 | 3 | ***0* | * * | | |
| 321 | 2 | ***0* | * * | | |
| 321 | | ***0* | ** Count | coming in | to IF |
| | | IF Branch- | | | |
| Branch totals: | 0 hits of | 2 branches = 0.00% | | | |
| 320 | 3 | ***0* | * * | | |
| 320 | 2 | ***0* | * * | | |
| 320 | | ***0* | ** Count | coming in | to IF |
| | | IF Branch- | | | |
| Branch totals: | U hits of | 2 branches = 0.00% | | | |
| 319 | 3 | ***0* | * * | | |
| 319 | 2 | ***0* | | | |
| 319 | _ | | ** Count | coming in | to IF |
| | | IF Branch- | | | |
| | 2 111 00 01 | | | | |
| | | 2 branches = 0.00% | | | |
| 312 | 2 | ***0* | | | |
| 312 312 | 1 | ***()* | ** Count | coming in | CO TH. |
| | | IF Branch- | | | |
| | | | | | |
| Branch totals: | 0 hits of | 2 branches = 0.00% | | | |
| 310 | 3 | ***0* | * * | | |
| 310 | 2 | ***0* | * * | | |
| 310 | | ***0* | ** Count | coming in | to IF |

Condition Coverage for Design Unit work.coverage_sv_unit --

```
-----Focused Condition View-----
       243 Item 1 (rs1 < rs2)
Line
Condition totals: 1 of 1 input term covered = 100.00%
 Input Term Covered Reason for no coverage Hint
 (rs1 < rs2)
             Y
   Rows: Hits FEC Target
                         Non-masking condition(s)
______ ____
 Row 1: 1 (rs1 < rs2)_0
            1 (rs1 < rs2)_1
 Row 2:
-----Focused Condition View------
       244 Item 1 (rs1 < rs2)
Line
Condition totals: 1 of 1 input term covered = 100.00%
 Input Term Covered Reason for no coverage Hint
 (rs1 < rs2)
          Hits FEC Target
                            Non-masking condition(s)
   Rows:
______ ____
 Row 1:
            1 (rs1 < rs2)_0
 Row 2:
            1 (rs1 < rs2)_1
-----Focused Condition View------
Line
       245 Item 1 (rs1 == rs2)
Condition totals: 1 of 1 input term covered = 100.00%
  Input Term Covered Reason for no coverage Hint
  ______ _____
 (rs1 == rs2)
              Y
          Hits FEC Target
   Rows:
                            Non-masking condition(s)
_____ ____
            1 (rs1 == rs2)_0
 Row 1:
 Row 2: 1 (rs1 == rs2)_1
------Focused Condition View------
       246 Item 1 (rs1 != rs2)
Line
Condition totals: 0 of 1 input term covered = 0.00%
  Input Term Covered Reason for no coverage
  ______ ____
 (rs1 != rs2)
          N '_0' not hit
                                 Hit '_0'
```

```
Hits FEC Target
  Rows:
                          Non-masking condition(s)
______ _____
       ***0*** (rs1 != rs2)_0
 Row 1:
 Row 2: 1 (rs1 != rs2)_1 -
-----Focused Condition View-----
      248 Item 1 (rs1 >= rs2)
Condition totals: 1 of 1 input term covered = 100.00%
  Input Term Covered Reason for no coverage Hint
 ______
 (rs1 >= rs2) Y
  Rows: Hits FEC Target Non-masking condition(s)
______
 Row 1: 1 (rs1 >= rs2)_0
 Row 2:
           1 (rs1 >= rs2)_1 -
-----Focused Condition View-----
Line 249 \text{ Item} 1 \text{ (rs1 >= rs2)}
Condition totals: 1 of 1 input term covered = 100.00%
  Input Term Covered Reason for no coverage Hint
 _____
 (rs1 >= rs2)
             Y
  Rows: Hits FEC Target
                      Non-masking condition(s)
_____ ____
 Row 1:
          1 (rs1 >= rs2)_0
 Row 2:
           1 (rs1 >= rs2)_1
```

| Input Term | Covered | Reason for no coverage | Hint |
|------------------------|---------|------------------------|-------------------|
| | | | |
| (rst_n === 1'b0) | N | No hits | Hit '_0' and '_1' |
| (tx.o_exception !== 0) | N | No hits | Hit '_0' and '_1' |

```
(tx.o_ce !== 1'b0)
                              N No hits
 (tx.o_stall_from_alu !== 1'b0)
                               N No hits
                                                      Hit ' 0' and ' 1'
            Hits FEC Target
                                            Non-masking condition(s)
   Rows:
-----
                                             _____
 Row 1:
          ***0*** (rst_n === 1'b0)_0
 Row 2: ***0*** (rst_n === 1'b0)_1
                                                 ((tx.o_exception !== 0) &&
((tx.o_ce !== 1'b0) && (tx.o_stall_from_alu !== 1'b0)))
          ***0*** (tx.o_exception !== 0)_0
                                            (rst_n === 1'b0)
      4:
          ***0*** (tx.o_exception !== 0)_1
 Row
                                             ((rst_n === 1'b0) && ((tx.o_ce
!== 1'b0) && (tx.o_stall_from_alu !== 1'b0)))
            ***0*** (tx.o_ce !== 1'b0)_0
      5:
                                                     ((rst_n === 1'b0) \&\&
(tx.o_exception !== 0))
            ***0*** (tx.o_ce !== 1'b0)_1
      6:
                                                     ((rst_n === 1'b0) &&
(tx.o_exception !== 0) && (tx.o_stall_from_alu !== 1'b0))
               ***0***
                       (tx.o_stall_from_alu !== 1'b0)_0 ((rst_n === 1'b0) &&
(tx.o_exception !== 0) && (tx.o_ce !== 1'b0))
        8:
              ***0*** (tx.o_stall_from_alu !== 1'b0)_1 ((rst_n === 1'b0) &&
(tx.o_exception !== 0) && (tx.o_ce !== 1'b0))
-----Focused Condition View-----
        165 Item 1 (opcode[5] | opcode[8])
Line
Condition totals: 0 of 2 input terms covered = 0.00%
 Input Term Covered Reason for no coverage Hint
______
  opcode[5]
               N No hits
                                      Hit ' 0' and ' 1'
  opcode[8]
             N No hits
                                     Hit '\_0' and '\_1'
   Rows: Hits FEC Target
                                  Non-masking condition(s)
 ______ ____
 Row 1: ***0*** opcode[5]_0
                                  ~opcode[8]
      2:
         ***0*** opcode[5] 1
 Row
          ***0*** opcode[8]_0
 Row 3:
                                  ~opcode[5]
           ***0*** opcode[8]_1
 Row 4:
                                  ~opcode[5]
-----Focused Condition View-----
        166 Item 1 (opcode[0] | opcode[4])
Condition totals: 0 of 2 input terms covered = 0.00%
 Input Term Covered Reason for no coverage Hint
______
  opcode[0]
               N No hits
                                      Hit ' 0' and ' 1'
               N No hits
                                      Hit '_0' and '_1'
  opcode[4]
```

Rows: Hits FEC Target Non-masking condition(s)

Hit ' 0' and ' 1'

```
1: ***0*** opcode[0]_0
 Row
                                 ~opcode[4]
         ***0*** opcode[0]_1
 Row
     2:
         ***0*** opcode[4]_0
 Row 3:
                                 ~opcode[0]
 Row 4: ***0*** opcode[4] 1
                                 ~opcode[0]
------Focused Condition View-----
        172 Item 1 (opcode[0] | opcode[1])
Condition totals: 0 of 2 input terms covered = 0.00%
 Input Term Covered Reason for no coverage Hint
______ _____
              N No hits
                                     Hit '_0' and '_1'
  opcode[0]
  opcode[1]
              N No hits
                                    Hit '_0' and '_1'
          Hits FEC Target
                                 Non-masking condition(s)
   Rows:
 ______ ____
         ***0*** opcode[0]_0
     1:
 Row
                                  ~opcode[1]
 Row 2: ***0*** opcode[0]_1
         ***0*** opcode[1]_0
 Row
     3:
                                 ~opcode[0]
 Row 4: ***0*** opcode[1]_1
                                 ~opcode[0]
-----Focused Condition View-----
        177 Item 1 (opcode[4] && out && (((pc + imm) !== tx.o_next_pc) | (ce !==
Line
tx.o_change_pc) || (ce !== tx.o_flush)))
Condition totals: 0 of 1 input term covered = 0.00%
    Input Term Covered Reason for no coverage Hint
    ______ ____
 (opcode[4] && out && (((pc + imm) !== tx.o_next_pc) || (ce !== tx.o_change_pc) || (ce
              N No hits
!== tx.o_flush)))
                                        Hit '_0' and '_1'
   Rows: Hits FEC Target
                              Non-masking condition(s)
 -----
          ***0*** (opcode[4] && out && (((pc + imm) !== tx.o_next_pc) || (ce !==
 Row
***0*** (opcode[4] && out && (((pc + imm) !== tx.o_next_pc) || (ce !==
 Row
tx.o_change_pc) | | (ce !== tx.o_flush)))_1 -
------Focused Condition View------
        187 Item 1 (opcode[5] | opcode[6])
Condition totals: 0 of 2 input terms covered = 0.00%
```

```
Input Term Covered Reason for no coverage Hint
______ _____
             N No hits
                                  Hit '_0' and '_1'
  opcode[5]
  opcode[6] N No hits
                                  Hit '_0' and '_1'
         Hits FEC Target
   Rows:
                           Non-masking condition(s)
_____ ____
     1: ***0*** opcode[5]_0
 Row
                               ~opcode[6]
 Row 2:
         ***0*** opcode[5]_1
     3: ***0*** opcode[6]_0
 Row
                               ~opcode[5]
         ***0*** opcode[6]_1
 Row
     4:
                               ~opcode[5]
------Focused Condition View------
       188 Item 1 (opcode[6] === 1'b1)
Line
Condition totals: 0 of 1 input term covered = 0.00%
        Input Term Covered Reason for no coverage Hint
       ______ _____
 (opcode[6] === 1'b1)
                  N No hits
                                         Hit '_0' and '_1'
           Hits FEC Target
   Rows:
                                Non-masking condition(s)
_____
                                _____
     1: ***0*** (opcode[6] === 1'b1)_0 -
 Row
     2: ***0*** (opcode[6] === 1'b1)_1 -
 Row
-----Focused Condition View-----
Line
       tx.o_flush))
Condition totals: 0 of 3 input terms covered = 0.00%
          Input Term Covered Reason for no coverage Hint
          -----
  (sum !== tx.o_next_pc)
                      N No hits
                                           Hit ' 0' and ' 1'
 (ce !== tx.o_change_pc)
                       N No hits
                                           Hit '_0' and '_1'
   (ce !== tx.o_flush) N No hits
                                           Hit ' 0' and ' 1'
           Hits FEC Target
                                  Non-masking condition(s)
   Rows:
_____
                                  _____
 Row 1:
         ***0*** (sum !== tx.o_next_pc)_0 ~((ce !== tx.o_change_pc) || (ce !==
tx.o_flush))
     2:
         ***0*** (sum !== tx.o_next_pc)_1 -
 Row
 Row 3:
          ***0*** (ce !== tx.o_change_pc)_0 (~(sum !== tx.o_next_pc) && ~(ce !==
tx.o_flush))
    4:
          ***0*** (ce !== tx.o_change_pc)_1 ~(sum !== tx.o_next_pc)
 Row
 Row 5: ***0*** (ce !== tx.o_flush)_0 (~(sum !== tx.o_next_pc) && ~(ce !==
```

```
tx.o_change_pc))
 Row 6: ***0*** (ce !== tx.o_flush)_1 (~(sum !== tx.o_next_pc) && ~(ce !==
tx.o_change_pc))
-----Focused Condition View-----
         211 Item 1 (((opcode[4] | opcode[3]) | (opcode[9] && (funct3 == 0))) | |
Line
opcode[10])
Condition totals: 0 of 5 input terms covered = 0.00%
    Input Term Covered Reason for no coverage Hint
    opcode[4]
                   N No hits
                                           Hit '_0' and '_1'
                                           Hit '_0' and '_1'
    opcode[3]
                  N No hits
                  N No hits
    opcode[9]
                                          Hit '_0' and '_1'
 (funct3 == 0)
                  N No hits
                                          Hit '_0' and '_1'
    opcode[10]
                  N No hits
                                           Hit '_0' and '_1'
    Rows:
            Hits FEC Target
                                    Non-masking condition(s)
 ______ ____
           ***0*** opcode[4]_0
 Row 1:
                                      (~opcode[10] && ~(opcode[9] && (funct3 ==
0)) && ~opcode[3])
 Row 2:
          ***0*** opcode[4]_1
           ***0*** opcode[3]_0
 Row 3:
                                      (~opcode[10] && ~(opcode[9] && (funct3 ==
0)) && ~opcode[4])
          ***0*** opcode[3]_1
      4:
 Row
                                    ~opcode[4]
          ***0*** opcode[9]_0
      5:
                                    (~opcode[10] && ~(opcode[4] | opcode[3]))
 Row
           ***0*** opcode[9]_1
 Row 6:
                                       (~(opcode[4] | opcode[3]) && (funct3 ==
0))
           ***0*** (funct3 == 0)_0
 Row 7:
                                     (~opcode[10] && ~(opcode[4] || opcode[3])
&& opcode[9])
 Row 8: ***0*** (funct3 == 0) 1
                                    (~(opcode[4] | opcode[3]) && opcode[9])
 Row 9: ***0*** opcode[10]_0
                                     ~((opcode[4] || opcode[3]) || (opcode[9] &&
(funct3 == 0)))
Row 10: ***0*** opcode[10]_1 ~((opcode[4] || opcode[3]) || (opcode[9] &&
(funct3 == 0)))
-----Focused Condition View-----
         218 Item 1 (opcode[2] | (opcode[9] && (funct3 != 0)))
Condition totals: 0 of 3 input terms covered = 0.00%
    Input Term Covered Reason for no coverage Hint
   N No hits
                                           Hit ' 0' and ' 1'
    opcode[2]
                                          Hit '_0' and '_1'
    opcode[9]
                  N No hits
                  N No hits
                                          Hit '_0' and '_1'
 (funct3 != 0)
```

```
Rows:
           Hits FEC Target
                                     Non-masking condition(s)
          ***0*** opcode[2]_0
      1:
                                     ~(opcode[9] && (funct3 != 0))
 Row
          ***0*** opcode[2]_1
      2:
 Row
      3:
          ***0*** opcode[9]_0
                                     ~opcode[2]
 Row
          ***0*** opcode[9]_1
     4:
                                    (~opcode[2] && (funct3 != 0))
 Row
      5:
          ***0*** (funct3 != 0)_0
                                    (~opcode[2] && opcode[9])
 Row
          ***0*** (funct3 != 0)_1
 Row
      6:
                                    (~opcode[2] && opcode[9])
-----Focused Condition View-----
         221 Item 1 ((tx.o_stall !== (stall || force_stall)) && ~flush)
Condition totals: 0 of 2 input terms covered = 0.00%
                         Input Term Covered Reason for no coverage Hint
 (tx.o_stall !== (stall || force_stall)) N No hits
                                                                   Hit '_0'
and ' 1'
                               flush N No hits
                                                                  Hit '_0'
and '_1'
             Hits FEC Target
     Rows:
                                                                Non-masking
condition(s)
            _____
                      _____
_____
 Row 1: ***0*** (tx.o_stall !== (stall || force_stall))_0 -
 Row
      2: ***0*** (tx.o_stall !== (stall || force_stall))_1 ~flush
          ***0*** flush_0
 Row 3:
                                                       (tx.o_stall !== (stall
|| force_stall))
      4: ***0*** flush_1
                                                       (tx.o_stall !== (stall
| force_stall))
-----Focused Condition View-----
         226 Item 1 (~(tx.o_stall | stall) && (ce === 1'b1))
Condition totals: 0 of 3 input terms covered = 0.00%
    Input Term Covered Reason for no coverage Hint
   ______ _____
                  N No hits
    tx.o_stall
                                          Hit '_0' and '_1'
       stall
                  N No hits
                                          Hit '_0' and '_1'
                  N No hits
                                           Hit '_0' and '_1'
 (ce === 1'b1)
    Rows: Hits FEC Target
                                    Non-masking condition(s)
```

```
***0*** tx.o_stall_0
 Row
      1:
                                    ((ce === 1'b1) && ~stall)
          ***0*** tx.o_stall_1
      2:
 Row
          ***0*** stall_0
 Row
      3:
                                    ((ce === 1'b1) && ~tx.o_stall)
          ***0*** stall_1
     4:
 Row
                                    ~tx.o_stall
 Row
     5:
          ***0*** (ce === 1'b1)_0
                                    ~(tx.o_stall || stall)
          ***0*** (ce === 1'b1)_1
 Row 6:
                                    ~(tx.o_stall || stall)
-----Focused Condition View-----
Line 227 Item 1 ((opcode !== tx.o_opcode) || (exception !== tx.o_exception) ||
(out !== tx.o_y) || (rs1_addr !== tx.o_rs1_addr) || (rs1 !== tx.o_rs1) || (rs2 !==
tx.o_rs2) || (rd_addr !== tx.o_rd_addr) || (imm !== tx.o_imm) || (funct3 !==
tx.o_funct3) || (rd_d !== tx.o_rd) || (rd_valid !== tx.o_rd_valid) || (wr_rd_d !==
tx.o_wr_rd) || ((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc))
Condition totals: 0 of 14 input terms covered = 0.00%
                                   Input Term Covered Reason for no coverage
Hint
_____
                                                 N No hits
                      (opcode !== tx.o_opcode)
Hit '_0' and '_1'
                                                 N No hits
                 (exception !== tx.o_exception)
Hit '_0' and '_1'
                             (out !== tx.o_y)
                                                 N No hits
Hit '_0' and '_1'
                  (rs1_addr !== tx.o_rs1_addr)
                                                 N No hits
Hit '_0' and '_1'
                           (rs1 !== tx.o_rs1)
                                                 N No hits
Hit '_0' and '_1'
                           (rs2 !== tx.o_rs2)
                                                 N No hits
Hit ' 0' and ' 1'
                    (rd_addr !== tx.o_rd_addr)
                                                 N No hits
Hit ' 0' and ' 1'
                           (imm !== tx.o_imm) N No hits
Hit '_0' and '_1'
                      (funct3 !== tx.o_funct3)
                                                 N No hits
Hit '_0' and '_1'
                           Hit '_0' and '_1'
                  (rd_valid !== tx.o_rd_valid)
                                                 N No hits
Hit '_0' and '_1'
                      (wr_rd_d !== tx.o_wr_rd)
N No hits
Hit '_0' and '_1'
 Hit '\_0' and '\_1'
                             (pc !== tx.o_pc) N No hits
```

```
Rows:
            Hits FEC Target
                                                                          Non-masking
condition(s)
 Row 1: ***0*** (opcode !== tx.o_opcode)_0
                                                                         ~((exception
!== tx.o_exception) || ((out !== tx.o_y) || ((rs1_addr !== tx.o_rs1_addr) || ((rs1 !==
tx.o_rs1) || ((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !== tx.o_imm)
| ((funct3 !== tx.o_funct3) | ((rd_d !== tx.o_rd) | ((rd_valid !== tx.o_rd_valid) |
((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc
!== tx.o_pc)))))))))))
            ***0*** (opcode !== tx.o_opcode)_1
      2:
 Row
            ***0*** (exception !== tx.o_exception)_0
  Row
                                                                            (~(opcode
!== tx.o_opcode) && ~((out !== tx.o_y) || ((rs1_addr !== tx.o_rs1_addr) || ((rs1 !==
tx.o_rs1) || ((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !== tx.o_imm)
| ((funct3 !== tx.o_funct3) | ((rd_d !== tx.o_rd) | ((rd_valid !== tx.o_rd_valid) |
((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc
!== tx.o_pc))))))))))))
             ***0*** (exception !== tx.o_exception)_1
 Row 4:
                                                                         ~(opcode !==
tx.o_opcode)
            ***0*** (out !== tx.o_y)_0
        5:
 Row
                                                                            (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~((rs1_addr !== tx.o_rs1_addr) |
((rs1 !== tx.o_rs1) || ((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !==
tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !==
tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) ==
tx.o_stall_from_alu) | (pc !== tx.o_pc))))))))))
            ***0*** (out !== tx.o_y)_1
                                                                            (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception))
             ***0*** (rs1_addr !== tx.o_rs1_addr)_0
                                                                            (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~((rs1 !==
tx.o_rs1) || ((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !== tx.o_imm)
|| ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) ||
((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc
!== tx.o_pc)))))))))))
             ***0*** (rsl_addr !== tx.o_rsl_addr)_1
                                                                            (~(opcode
  Row
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y))
             ***0*** (rs1 !== tx.o_rs1)_0
                                                                            (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !==
tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !==
tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) ==
tx.o_stall_from_alu) | (pc !== tx.o_pc)))))))))
      10:
            ***0*** (rs1 !== tx.o_rs1)_1
                                                                            (~(opcode
```

!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr

```
!== tx.o_rs1_addr))
                          ***0*** (rs2 !== tx.o_rs2)_0
                                                                                                                                                  (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~((rd_addr !== tx.o_rd_addr) || ((imm !==
tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !==
tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) ==
tx.o_stall_from_alu) | (pc !== tx.o_pc))))))))
                        ***0*** (rs2 !== tx.o_rs2)_1
                                                                                                                                                  (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1))
                        ***0*** (rd_addr !== tx.o_rd_addr)_0
 Row
                                                                                                                                                  (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~((imm !== tx.o_imm)
| ((funct3 !== tx.o_funct3) | ((rd_d !== tx.o_rd) | ((rd_valid !== tx.o_rd_valid) |
((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc
!== tx.o_pc)))))))
                        ***0*** (rd_addr !== tx.o_rd_addr)_1
          14:
                                                                                                                                                  (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2))
                         ***0*** (imm !== tx.o_imm)_0
                                                                                                                                                  (~(opcode
 Row
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !==
tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) ==
tx.o_stall_from_alu) | (pc !== tx.o_pc))))))
                        ***0*** (imm !== tx.o_imm)_1
                                                                                                                                                  (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr))
 Row 17:
                        ***0*** (funct3 !== tx.o_funct3)_0
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~((rd_d !== tx.o_rd) || ((rd_valid !==
tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) ==
tx.o_stall_from_alu) || (pc !== tx.o_pc)))))
                        ***0*** (funct3 !== tx.o_funct3)_1
 Row
                                                                                                                                                  (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm))
 Row 19:
                        ***0*** (rd_d !== tx.o_rd)_0
                                                                                                                                                  (~(opcode
!== \  \, \text{tx.o\_opcode}) \  \, \&\& \  \, \sim (\text{exception}) \  \, \&\& \  \, \sim (\text{out } !== \  \, \text{tx.o\_y}) \  \, \&\& \  \, \sim (\text{rs1\_addr}) \  \, \& \  \, \& \  \, \sim (\text{rs1\_addr}) \  \,
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~((rd_valid !==
tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) ==
tx.o_stall_from_alu) | (pc !== tx.o_pc))))
 Row
          20:
                       ***0*** (rd_d !== tx.o_rd)_1
                                                                                                                                                  (~(opcode
```

```
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3))
              ***0*** (rd_valid !== tx.o_rd_valid)_0
                                                                             (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd)
&& ~((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) ||
(pc !== tx.o_pc))))
             ***0*** (rd_valid !== tx.o_rd_valid)_1
Row
     22:
                                                                             (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !==
tx.o_rd))
            ***0*** (wr_rd_d !== tx.o_wr_rd)_0
Row
                                                                             (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd)
&& \sim (rd_valid !== tx.o_rd_valid) \&\& \sim (((opcode[3] || opcode[2]) == tx.o_stall_from_alu))
|| (pc !== tx.o_pc)))
             ***0*** (wr_rd_d !== tx.o_wr_rd)_1
       24:
                                                                             (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd)
&& ~(rd_valid !== tx.o_rd_valid))
              ***0*** ((opcode[3] || opcode[2]) == tx.o_stall_from_alu)_0 (~(opcode
       25:
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd)
&& ~(rd_valid !== tx.o_rd_valid) && ~(wr_rd_d !== tx.o_wr_rd) && ~(pc !== tx.o_pc))
               ***0*** ((opcode[3] || opcode[2]) == tx.o_stall_from_alu)_1 (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd)
&& ~(rd_valid !== tx.o_rd_valid) && ~(wr_rd_d !== tx.o_wr_rd))
             ***0*** (pc !== tx.o_pc)_0
Row
     27:
                                                                             (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd)
&& ~(rd_valid !== tx.o_rd_valid) && ~(wr_rd_d !== tx.o_wr_rd) && ~((opcode[3] |
opcode[2]) == tx.o_stall_from_alu))
             ***0*** (pc !== tx.o_pc)_1
                                                                             (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd)
&& ~(rd_valid !== tx.o_rd_valid) && ~(wr_rd_d !== tx.o_wr_rd) && ~((opcode[3] |
```

```
opcode[2]) == tx.o_stall_from_alu))
-----Focused Condition View-----
        247 Item 1 (flush && ~(tx.o_stall | stall) && (tx.o_ce !== 1'b0))
Condition totals: 0 of 4 input terms covered = 0.00%
        Input Term Covered Reason for no coverage Hint
       N No hits
                                             Hit '_0' and '_1'
           flush
                     N No hits
                                             Hit '_0' and '_1'
        tx.o_stall
                     N No hits
                                             Hit '_0' and '_1'
           stall
                     N No hits
                                             Hit '_0' and '_1'
 (tx.o_ce !== 1'b0)
            Hits FEC Target
   Rows:
                                   Non-masking condition(s)
          ***0*** flush_0
 Row 1:
 Row 2: ***0*** flush_1
                                       (~(tx.o_stall || stall) && (tx.o_ce !==
1'b0))
          ***0*** tx.o_stall_0
 Row 3:
                                   (flush && (tx.o_ce !== 1'b0) && ~stall)
      4: ***0*** tx.o_stall_1
 Row
                                   flush
 Row 5:
             ***0*** stall_0
                                            (flush && (tx.o_ce !== 1'b0) &&
~tx.o_stall)
 Row 6: ***0*** stall_1
                                   (flush && ~tx.o_stall)
          ***0*** (tx.o_ce !== 1'b0)_0 (flush && ~(tx.o_stall || stall))
 Row 7:
 Row 8: ***0*** (tx.o_ce !== 1'b0)_1 (flush && ~(tx.o_stall || stall))
-----Focused Condition View-----
Line
        249 Item 1 (~(tx.o_stall | stall) && (tx.o_ce !== ce))
Condition totals: 0 of 3 input terms covered = 0.00%
      Input Term Covered Reason for no coverage Hint
     ______ ______
                    N No hits
                                           Hit ' 0' and ' 1'
      tx.o_stall
         stall
                    N No hits
                                           Hit ' 0' and ' 1'
 (tx.o_ce !== ce)
                    N No hits
                                           Hit '\_0' and '\_1'
   Rows:
            Hits FEC Target
                                   Non-masking condition(s)
 _____ ____
          ***0*** tx.o_stall_0
      1:
 Row
                                   ((tx.o_ce !== ce) && ~stall)
          ***0*** tx.o_stall_1
      2:
 Row
      3:
          ***0*** stall_0
                                   ((tx.o_ce !== ce) && ~tx.o_stall)
 Row
      4:
          ***0*** stall_1
 Row
                                   ~tx.o_stall
          ***0*** (tx.o_ce !== ce)_0
      5:
                                   ~(tx.o_stall | stall)
 Row
      6: ***0*** (tx.o_ce !== ce)_1 ~(tx.o_stall || stall)
 Row
```

------Focused Condition View------

```
Line 251 Item 1 (tx.o_stall && (tx.o_ce !== 1'b0))

Condition totals: 0 of 2 input terms covered = 0.00%

Input Term Covered Reason for no coverage Hin
```

```
Input Term Covered Reason for no coverage Hint
      ______ ____
                  N No hits
      tx.o_stall
                                     Hit '_0' and '_1'
 (tx.o_ce !== 1'b0) N No hits
                                     Hit '_0' and '_1'
   Rows: Hits FEC Target
                         Non-masking condition(s)
______ ____
 Row 1: ***0*** tx.o_stall_0
        ***0*** tx.o_stall_1
 Row 2:
                             (tx.o_ce !== 1'b0)
 Row 3: ***0*** (tx.o_ce !== 1'b0)_0 tx.o_stall
        ***0*** (tx.o_ce !== 1'b0)_1 tx.o_stall
 Row 4:
------Focused Condition View-----
      310 Item 1 (a < b)
Condition totals: 0 of 1 input term covered = 0.00%
 Input Term Covered Reason for no coverage Hint
_____
   (a < b)
            N No hits
                                Hit '_0' and '_1'
         Hits FEC Target
                             Non-masking condition(s)
   Rows:
______ _____
        ***0*** (a < b)_0
 Row 1:
 Row 2: ***0*** (a < b) 1
-----Focused Condition View-----
      312 Item 1 (a < b)
Condition totals: 0 of 1 input term covered = 0.00%
 Input Term Covered Reason for no coverage Hint
______ ____
   (a < b)
            N No hits
                                Hit '_0' and '_1'
   Rows:
          Hits FEC Target
                             Non-masking condition(s)
_____ ____
 Row 1:
        ***0*** (a < b)_0
 Row 2: ***0*** (a < b)_1
------Focused Condition View------
      319 Item 1 (a == b)
Line
```

Input Term Covered Reason for no coverage Hint

Condition totals: 0 of 1 input term covered = 0.00%

```
(a == b)
           N No hits
                               Hit ' 0' and ' 1'
          Hits FEC Target
   Rows:
                             Non-masking condition(s)
______ _____
        ***0*** (a == b)_0
 Row 1:
 Row 2: ***0*** (a == b)_1
------Focused Condition View------
      320 Item 1 (a != b)
Line
Condition totals: 0 of 1 input term covered = 0.00%
 Input Term Covered Reason for no coverage
                               Hit '_0' and '_1'
  (a != b) N No hits
   Rows: Hits FEC Target
                             Non-masking condition(s)
______
 Row 1: ***0*** (a != b)_0
 Row 2: ***0*** (a != b)_1
-----Focused Condition View-----
       321 Item 1 (a >= b)
Line
Condition totals: 0 of 1 input term covered = 0.00%
 Input Term Covered Reason for no coverage Hint
(a >= b) N No hits
                               Hit '_0' and '_1'
   Rows: Hits FEC Target
                         Non-masking condition(s)
______ ____
 Row 1: ***0*** (a >= b)_0
 Row 2: ***0*** (a >= b)_1
-----Focused Condition View-----
       322 Item 1 (a >= b)
Line
Condition totals: 0 of 1 input term covered = 0.00%
 Input Term Covered Reason for no coverage Hint
______ ____
           N No hits
                                Hit '_0' and '_1'
  (a >= b)
          Hits FEC Target
   Rows:
                            Non-masking condition(s)
_____ ____
        ***0*** (a >= b)_0
 Row 1:
 Row 2: ***0*** (a >= b)_1
```

| Covergroups | 1 | na | na | 34.8 | 48 | |
|--------------------------------|--------------|--------|------|------|------|-------------|
| Coverpoints/Crosses | 20 | na | na | | na | |
| Covergroup Bins | | 77 | 5238 | 1.4 | 4% | . – – – – - |
| | | | | | g 1 | ъ. |
| overgroup tatus | | | мет | ric | Goal | Bin |
| Lacus | | | | | | |
| | | | | | | . – – – – - |
| TYPE work.coverage_sv_unit::c | overage/alu_ | _cg | 34.8 | 34% | 100 | |
| covered/total bins: | | | | 77 | 5315 | - |
| missing/total bins: | | | 52 | 38 | 5315 | - |
| % Hit: | | | 1.4 | 4% | 100 | - |
| type_option.weight=1 | | | | | | |
| type_option.goal=100 | | | | | | |
| type_option.comment= | | | | | | |
| type_option.strobe=0 | | | | | | |
| type_option.merge_instances | s=auto(1) | | | | | |
| Coverpoint #coverpoint0# | | | 45. | 45% | 100 | |
| ncovered | | | | | | |
| covered/total bins: | | | | 5 | 11 | - |
| missing/total bins: | | | | 6 | 11 | - |
| % Hit: | | | 45.4 | 5% | 100 | - |
| type_option.weight=1 | | | | | | |
| type_option.goal=100 | | | | | | |
| type_option.comment= | | | | | | |
| <pre>bin opcode_types[0]</pre> | | | | 78 | 1 | |
| overed | | | | | | |
| <pre>bin opcode_types[1]</pre> | | | | 103 | 1 | |
| overed | | | | | | |
| <pre>bin opcode_types[2]</pre> | | | | 82 | 1 | |

bin opcode_types[3]

| ZERO |
|------|
|------|

| Q | bin opcode_types[4] | 90 | 1 | - |
|---------|------------------------|--------|-----|---|
| Covered | bin opcode_types[5] | 0 | 1 | - |
| ZERO | bin opcode_types[6] | 0 | 1 | - |
| ZERO | bin opcode_types[7] | 0 | 1 | - |
| ZERO | bin opcode_types[8] | 79 | 1 | - |
| Covered | bin opcode_types[9] | 0 | 1 | _ |
| ZERO | bin opcode_types[10] | 0 | 1 | _ |
| ZERO | verpoint #coverpoint1# | 28.57% | 100 | _ |
| Uncover | | 201071 | 200 | |
| | covered/total bins: | 4 | 14 | - |
| | missing/total bins: | 10 | 14 | - |
| | % Hit: | 28.57% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin alu_ops[0] | 0 | 1 | |
| ZERO | | | | |
| | bin alu_ops[1] | 60 | 1 | - |
| Covered | | | | |
| | bin alu_ops[2] | 71 | 1 | _ |
| Covered | | | | |
| 7.ED.O | bin alu_ops[3] | 0 | 1 | _ |
| ZERO | bin alu_ops[4] | 64 | 1 | |
| Covered | | 04 | Τ. | _ |
| COVETCA | bin alu_ops[5] | 0 | 1 | _ |
| ZERO | | | | |
| | bin alu_ops[6] | 0 | 1 | - |
| ZERO | | | | |
| | bin alu_ops[7] | 0 | 1 | - |
| ZERO | bin alu_ops[8] | 58 | 1 | |
| Covered | | 58 | 1 | - |
| COVELCA | bin alu_ops[9] | 0 | 1 | - |
| ZERO | | | | |

| | bin alu_ops[10] | 0 | 1 | - |
|---------|------------------------|---------|-----|---|
| ZERO | bin alu_ops[11] | 0 | 1 | _ |
| ZERO | DIN GIG_OPS[II] | v | _ | |
| | bin alu_ops[12] | 0 | 1 | - |
| ZERO | bin alu_ops[13] | 0 | 1 | _ |
| ZERO | DIN GIG_OPS[13] | v | _ | |
| Cov | verpoint #coverpoint2# | 100.00% | 100 | - |
| Covered | | | | |
| | covered/total bins: | 2 | 2 | - |
| | missing/total bins: | 0 | 2 | - |
| | % Hit: | 100.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 714 | 1 | - |
| Covered | | | | |
| | bin auto[1] | 200 | 1 | - |
| Covered | | | | |
| | verpoint #coverpoint3# | 100.00% | 100 | - |
| Covered | covered/total bins: | 1 | 1 | |
| | covered/total bins. | 1 | 1 | _ |
| | missing/total bins: | 0 | 1 | - |
| | % Hit: | 100.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin pc_values | 914 | 1 | - |
| Covered | | | | |
| | verpoint #coverpoint4# | 0.00% | 100 | _ |
| ZERO | covered/total bins: | 0 | 2 | - |
| | missing/total bins: | 2 | 2 | - |
| | % Hit: | 0.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | | | | |

| | type_option.comment= | | | |
|---------|------------------------|--------|-----|---|
| | bin auto[0] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[1] | 0 | 1 | _ |
| ZERO | | | | |
| | verpoint #coverpoint5# | 0.00% | 100 | _ |
| ZERO | | | | |
| | covered/total bins: | 0 | 2 | _ |
| | | | | |
| | missing/total bins: | 2 | 2 | _ |
| | - | | | |
| | % Hit: | 0.00% | 100 | _ |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[1] | 0 | 1 | _ |
| ZERO | | | | |
| | verpoint #coverpoint6# | 0.00% | 100 | _ |
| ZERO | <u> </u> | | | |
| | covered/total bins: | 0 | 1 | _ |
| | | | | |
| | missing/total bins: | 1 | 1 | _ |
| | 5 | | | |
| | % Hit: | 0.00% | 100 | _ |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin rd_addr | 0 | 1 | _ |
| ZERO | | | | |
| | verpoint #coverpoint7# | 50.00% | 100 | _ |
| Uncover | | | | |
| | covered/total bins: | 1 | 2 | _ |
| | | | | |
| | missing/total bins: | 1 | 2 | _ |
| | J, | | | |
| | % Hit: | 50.00% | 100 | _ |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 0 | 1 | _ |
| ZERO | 22.2 4400101 | O | Δ. | |

| | bin auto[1] | 914 | 1 | - |
|---------|-------------------------|--------|-----|---|
| Covered | I | | | |
| Cov | verpoint #coverpoint8# | 50.00% | 100 | - |
| Uncover | red | | | |
| | covered/total bins: | 1 | 2 | - |
| | missing/total bins: | 1 | 2 | - |
| | % Hit: | 50.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 914 | 1 | - |
| Covered | | | | |
| | bin auto[1] | 0 | 1 | - |
| ZERO | | | | |
| | verpoint #coverpoint9# | 50.00% | 100 | - |
| Uncover | | | | |
| | covered/total bins: | 1 | 2 | - |
| | missing/total bins: | 1 | 2 | - |
| | % Hit: | 50.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 914 | 1 | - |
| Covered | l | | | |
| | bin auto[1] | 0 | 1 | - |
| ZERO | | | | |
| Cov | verpoint #coverpoint10# | 50.00% | 100 | - |
| Uncover | red | | | |
| | covered/total bins: | 1 | 2 | - |
| | missing/total bins: | 1 | 2 | - |
| | % Hit: | 50.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| _ | bin auto[0] | 914 | 1 | - |
| Covered | l bin auto[1] | 0 | 1 | _ |
| | | | | |

| Cot | verpoint #coverpoint11# | 50.00% | 100 | _ |
|---------|-------------------------|----------|----------|---|
| Uncover | | 30.00% | T 0 0 | _ |
| oncover | covered/total bins: | 1 | 2 | _ |
| | covered, total bins. | 1 | 2 | |
| | missing/total bins: | 1 | 2 | _ |
| | midding, cocar bind | <u>-</u> | - | |
| | % Hit: | 50.00% | 100 | _ |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 914 | 1 | _ |
| Covered | | | | |
| | bin auto[1] | 0 | 1 | _ |
| ZERO | | | | |
| | verpoint #coverpoint12# | 50.00% | 100 | _ |
| Uncover | | | | |
| | covered/total bins: | 1 | 2 | _ |
| | | | | |
| | missing/total bins: | 1 | 2 | _ |
| | 5. | | | |
| | % Hit: | 50.00% | 100 | _ |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 914 | 1 | _ |
| Covered | | | | |
| | bin auto[1] | 0 | 1 | _ |
| ZERO | | | | |
| Cov | verpoint #coverpoint13# | 100.00% | 100 | _ |
| Covered | | | | |
| | covered/total bins: | 2 | 2 | _ |
| | | | | |
| | missing/total bins: | 0 | 2 | _ |
| | | | | |
| | % Hit: | 100.00% | 100 | _ |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 714 | 1 | _ |
| Covered | | | | |
| | bin auto[1] | 200 | 1 | _ |
| Covered | | 200 | <u> </u> | |
| 22121 | - | | | |

| | verpoint #coverpoint14# | 0.00% | 100 | - |
|----------------------------|---|----------------------------|-------------------------|---|
| ZERO | covered/total bins: | 0 | 4 | - |
| | missing/total bins: | 4 | 4 | - |
| | % Hit: | 0.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin exceptions[0] | 0 | 1 | _ |
| ZERO | | | | |
| | bin exceptions[1] | 0 | 1 | _ |
| ZERO | | | | |
| | bin exceptions[2] | 0 | 1 | - |
| ZERO | | | | |
| | bin exceptions[3] | 0 | 1 | - |
| ZERO | | | | |
| Cov | verpoint #vif.i_opcode15# | 10.93% | 100 | - |
| Uncover | | | | |
| | covered/total bins: | 7 | 64 | _ |
| | | | | |
| | missing/total bins: | 57 | 64 | - |
| | <pre>missing/total bins: % Hit:</pre> | 10.93% | 100 | - |
| | | | | - |
| | % Hit: | | | - |
| | % Hit: type_option.weight=1 | | | - |
| | <pre>% Hit: type_option.weight=1 type_option.goal=100</pre> | | | - |
| Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31]</pre> | 10.93% | 100 | - |
| Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31]</pre> | 10.93% | 100 | |
| Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63]</pre> | 10.93% | 100 | - |
| | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63]</pre> | 10.93% | 100 | |
| | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63] bin auto[64:95]</pre> | 10.93% 527 81 | 100 | |
| Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63] bin auto[64:95]</pre> | 10.93% 527 81 | 100 | - |
| Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63] bin auto[64:95]</pre> | 10.93% 527 81 73 | 100 | - |
| Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63] bin auto[64:95]</pre> | 10.93% 527 81 73 | 100 | - |
| Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63] bin auto[64:95] bin auto[64:95]</pre> | 10.93% 527 81 73 | 100 1 1 1 | - |
| Covered Covered ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63] bin auto[64:95] bin auto[64:95]</pre> | 10.93% 527 81 73 | 100 1 1 1 | - |
| Covered Covered ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63] bin auto[64:95] bin auto[64:95]</pre> bin auto[96:127] | 10.93% 527 81 73 0 70 | 100 1 1 1 1 | |
| Covered ZERO Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63] bin auto[64:95] bin auto[64:95]</pre> bin auto[96:127] | 10.93% 527 81 73 0 70 | 100 1 1 1 1 | |
| Covered ZERO Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63] bin auto[4:95] bin auto[96:127] bin auto[128:159] bin auto[160:191]</pre> | 10.93% 527 81 73 0 70 | 100 1 1 1 1 | |
| Covered ZERO Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63] bin auto[4:95] bin auto[96:127] bin auto[128:159] bin auto[160:191]</pre> | 10.93% 527 81 73 0 70 | 100 1 1 1 1 | |

| Covered | bin a | auto[256:287] | 67 | 1 | - |
|---------|-------|---------------|----|---|---|
| ZERO | bin a | auto[288:319] | 0 | 1 | - |
| ZERO | bin a | auto[320:351] | 0 | 1 | - |
| ZERO | bin a | auto[352:383] | 0 | 1 | - |
| ZERO | bin a | auto[384:415] | 0 | 1 | - |
| ZERO | bin a | auto[416:447] | 0 | 1 | - |
| ZERO | bin a | auto[448:479] | 0 | 1 | - |
| ZERO | bin a | auto[480:511] | 0 | 1 | - |
| Covered | bin a | auto[512:543] | 95 | 1 | - |
| ZERO | bin a | auto[544:575] | 0 | 1 | - |
| ZERO | bin a | auto[576:607] | 0 | 1 | _ |
| ZERO | bin a | auto[608:639] | 0 | 1 | _ |
| ZERO | bin a | auto[640:671] | 0 | 1 | _ |
| ZERO | bin a | auto[672:703] | 0 | 1 | - |
| ZERO | bin a | auto[704:735] | 0 | 1 | - |
| ZERO | bin a | auto[736:767] | 0 | 1 | - |
| ZERO | bin a | auto[768:799] | 0 | 1 | - |
| ZERO | bin a | auto[800:831] | 0 | 1 | - |
| ZERO | bin a | auto[832:863] | 0 | 1 | _ |
| ZERO | bin a | auto[864:895] | 0 | 1 | _ |
| ZERO | bin a | auto[896:927] | 0 | 1 | - |
| ZERO | bin a | auto[928:959] | 0 | 1 | - |
| ZERO | bin a | auto[960:991] | 0 | 1 | - |
| 2210 | | | | | |

| ZERO | bin auto[992:1023] | 0 | 1 | - |
|---------|---|---|---|---|
| Covered | bin auto[1024:1055] | 1 | 1 | - |
| ZERO | bin auto[1056:1087] | 0 | 1 | - |
| ZERO | bin auto[1088:1119] | 0 | 1 | - |
| ZERO | bin auto[1120:1151] | 0 | 1 | - |
| ZERO | bin auto[1152:1183] | 0 | 1 | - |
| ZERO | bin auto[1184:1215] | 0 | 1 | - |
| ZERO | bin auto[1216:1247] | 0 | 1 | - |
| ZERO | bin auto[1248:1279] | 0 | 1 | - |
| ZERO | bin auto[1280:1311] | 0 | 1 | _ |
| ZERO | bin auto[1312:1343] | 0 | 1 | - |
| ZERO | bin auto[1344:1375] | 0 | 1 | - |
| ZERO | bin auto[1376:1407] | 0 | 1 | - |
| ZERO | bin auto[1408:1439] | 0 | 1 | - |
| ZERO | bin auto[1440:1471] | 0 | 1 | - |
| ZERO | bin auto[1472:1503] | 0 | 1 | - |
| ZERO | bin auto[1504:1535] | 0 | 1 | - |
| ZERO | bin auto[1536:1567] | 0 | 1 | - |
| ZERO | bin auto[1568:1599] | 0 | 1 | - |
| ZERO | bin auto[1600:1631] | 0 | 1 | _ |
| ZERO | bin auto[1632:1663] | 0 | 1 | - |
| ZERO | bin auto[1664:1695] bin auto[1696:1727] | 0 | 1 | _ |
| ZERO | DIN auto[1070.1727] | J | _ | _ |

| ZEDO | bin auto[1728:1759] | 0 | 1 | - |
|----------------------|---|-------------|------------------------------|------------------|
| ZERO | bin auto[1760:1791] | 0 | 1 | - |
| ZERO | bin auto[1792:1823] | 0 | 1 | - |
| ZERO | bin auto[1824:1855] | 0 | 1 | - |
| ZERO | bin auto[1856:1887] | 0 | 1 | - |
| ZERO | bin auto[1888:1919] | 0 | 1 | - |
| ZERO | bin auto[1920:1951] | 0 | 1 | - |
| ZERO | bin auto[1952:1983] | 0 | 1 | _ |
| ZERO | bin auto[1984:2015] | 0 | 1 | _ |
| ZERO | bin auto[2016:2047] | 0 | 1 | _ |
| ZERO | verpoint #vif.i_exception16# | 0.00% | 100 | |
| ZERO | verpoint #vii.i_exception10# | 0.00% | 100 | _ |
| | covered/total bins: | 0 | 16 | _ |
| | | | | |
| | missing/total bins: | 16 | 16 | - |
| | missing/total bins: % Hit: | 16 0.00% | 16 | - |
| | | | | - |
| | % Hit: | | | - |
| | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment=</pre> | 0.00% | 100 | - |
| | <pre>% Hit: type_option.weight=1 type_option.goal=100</pre> | | | - |
| ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0]</pre> | 0.00% | 100 | - |
| | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment=</pre> | 0.00% | 100 | - |
| ZERO ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0]</pre> | 0.00% | 100 | - |
| ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0]</pre> | 0.00% | 100 | - |
| | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0]</pre> | 0.00% | 100 | - - - |
| ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] bin auto[1]</pre> | 0.00% | 100 | |
| ZERO ZERO ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] bin auto[1]</pre> | 0.00% | 100 | |
| ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] bin auto[1] bin auto[2]</pre> | 0.00% | 100 1 1 1 | - - - - |
| ZERO ZERO ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] bin auto[1] bin auto[2] bin auto[3] bin auto[4]</pre> | 0.00% | 100 1 1 1 1 1 | |
| ZERO ZERO ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] bin auto[1] bin auto[2] bin auto[3]</pre> | 0.00% | 100 1 1 1 1 | |

| ZERO | | | | |
|--------------------------------|--|---------------------------------|-----------------------|---|
| | bin auto[8] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[9] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[10] | 0 | 1 | _ |
| ZERO | zm ddoc[10] | Ç | _ | |
| ZHRO | bin auto[11] | 0 | 1 | _ |
| ZERO | DIN duco[11] | O | _ | |
| ZERO | bin auto[12] | 0 | 1 | |
| ZEDO | DIN Auto[12] | U | 1 | _ |
| ZERO | him | 0 | 1 | |
| | bin auto[13] | 0 | 1 | _ |
| ZERO | | _ | _ | |
| | bin auto[14] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[15] | 0 | 1 | _ |
| ZERO | | | | |
| Cov | verpoint #vif.i_alu17# | 10.93% | 100 | _ |
| Uncover | red | | | |
| | covered/total bins: | 7 | 64 | _ |
| | | | | |
| | missing/total bins: | 57 | 64 | _ |
| | | | | |
| | % Hit: | 10.93% | 100 | _ |
| | | | | |
| | | | | |
| | type_option.weight=1 | | | |
| | <pre>type_option.weight=1 type_option.goal=100</pre> | | | |
| | type_option.goal=100 | | | |
| | <pre>type_option.goal=100 type_option.comment=</pre> | | | _ |
| Covered | <pre>type_option.goal=100 type_option.comment= bin auto[0:255]</pre> | 520 | 1 | _ |
| Covered | <pre>type_option.goal=100 type_option.comment= bin auto[0:255]</pre> | 520 | 1 | - |
| | <pre>type_option.goal=100 type_option.comment= bin auto[0:255] d bin auto[256:511]</pre> | | | - |
| Covered | <pre>type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511]</pre> | 520 77 | 1 | - |
| Covered | <pre>type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767]</pre> | 520 | 1 | - |
| | <pre>type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767]</pre> | 520 77 73 | 1 1 1 | - |
| Covered | <pre>type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767]</pre> | 520 77 | 1 | - |
| Covered | <pre>type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023]</pre> | 520 77 73 | 1 1 1 | - |
| Covered | <pre>type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279]</pre> | 520 77 73 | 1 1 1 | - |
| Covered | <pre>type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279]</pre> | 520 77 73 0 70 | 1 1 1 1 | - |
| Covered ZERO Covered | <pre>type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279]</pre> | 520 77 73 | 1 1 1 | - |
| Covered | <pre>type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279] bin auto[1280:1535]</pre> | 520 77 73 0 70 | 1 1 1 1 | - |
| Covered ZERO Covered | <pre>type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279]</pre> | 520 77 73 0 70 | 1 1 1 1 | - |
| Covered ZERO Covered | <pre>type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279] bin auto[1280:1535]</pre> | 520 77 73 0 70 | 1 1 1 1 | - |
| Covered ZERO Covered | <pre>type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279] bin auto[1280:1535]</pre> | 520 77 73 0 70 | 1 1 1 1 | |
| Covered ZERO Covered | <pre>type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279] bin auto[1280:1535]</pre> | 520 77 73 0 70 0 | 1 1 1 1 1 | |
| Covered ZERO Covered ZERO ZERO | <pre>type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279] bin auto[1280:1535]</pre> | 520 77 73 0 70 0 | 1 1 1 1 1 | |
| Covered ZERO Covered ZERO ZERO | type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279] bin auto[1280:1535] bin auto[1536:1791] bin auto[1792:2047] bin auto[2048:2303] | 520 77 73 0 70 0 | 1 1 1 1 1 | |

| ZERO | bin auto[2304:2559] | 0 | 1 | - |
|---------|---------------------|----|---|---|
| ZERO | bin auto[2560:2815] | 0 | 1 | - |
| ZERO | bin auto[2816:3071] | 0 | 1 | - |
| ZERO | bin auto[3072:3327] | 0 | 1 | - |
| ZERO | bin auto[3328:3583] | 0 | 1 | - |
| ZERO | bin auto[3584:3839] | 0 | 1 | - |
| ZERO | bin auto[3840:4095] | 0 | 1 | - |
| Covered | bin auto[4096:4351] | 56 | 1 | - |
| ZERO | bin auto[4352:4607] | 0 | 1 | - |
| ZERO | bin auto[4608:4863] | 0 | 1 | - |
| ZERO | bin auto[4864:5119] | 0 | 1 | - |
| ZERO | bin auto[5120:5375] | 0 | 1 | - |
| ZERO | bin auto[5376:5631] | 0 | 1 | - |
| ZERO | bin auto[5632:5887] | 0 | 1 | - |
| ZERO | bin auto[5888:6143] | 0 | 1 | - |
| ZERO | bin auto[6144:6399] | 0 | 1 | - |
| ZERO | bin auto[6400:6655] | 0 | 1 | - |
| ZERO | bin auto[6656:6911] | 0 | 1 | - |
| ZERO | bin auto[6912:7167] | 0 | 1 | - |
| ZERO | bin auto[7168:7423] | 0 | 1 | - |
| ZERO | bin auto[7424:7679] | 0 | 1 | - |
| ZERO | bin auto[7680:7935] | 0 | 1 | - |
| ZERO | bin auto[7936:8191] | 0 | 1 | - |
| | | | | |

| Covered | bin auto[8192:8447] | 56 | 1 | - |
|---------|-----------------------|----|---|---|
| ZERO | bin auto[8448:8703] | 0 | 1 | - |
| ZERO | bin auto[8704:8959] | 0 | 1 | - |
| ZERO | bin auto[8960:9215] | 0 | 1 | - |
| ZERO | bin auto[9216:9471] | 0 | 1 | - |
| ZERO | bin auto[9472:9727] | 0 | 1 | - |
| ZERO | bin auto[9728:9983] | 0 | 1 | - |
| ZERO | bin auto[9984:10239] | 0 | 1 | - |
| ZERO | bin auto[10240:10495] | 0 | 1 | - |
| ZERO | bin auto[10496:10751] | 0 | 1 | - |
| ZERO | bin auto[10752:11007] | 0 | 1 | - |
| ZERO | bin auto[11008:11263] | 0 | 1 | - |
| ZERO | bin auto[11264:11519] | 0 | 1 | - |
| ZERO | bin auto[11520:11775] | 0 | 1 | - |
| ZERO | bin auto[11776:12031] | 0 | 1 | - |
| ZERO | bin auto[12032:12287] | 0 | 1 | - |
| ZERO | bin auto[12288:12543] | 0 | 1 | - |
| ZERO | bin auto[12544:12799] | 0 | 1 | - |
| ZERO | bin auto[12800:13055] | 0 | 1 | - |
| ZERO | bin auto[13056:13311] | 0 | 1 | - |
| ZERO | bin auto[13312:13567] | 0 | 1 | - |
| ZERO | bin auto[13568:13823] | 0 | 1 | - |
| ZERO | bin auto[13824:14079] | 0 | 1 | - |

| | bin auto[14080:14335] | 0 | 1 | - |
|---------------------------------|---|---|------------------|---|
| ZERO | bin auto[14336:14591] | 0 | 1 | - |
| ZERO | bin auto[14592:14847] | 0 | 1 | _ |
| ZERO | | · · | _ | |
| ZERO | bin auto[14848:15103] | 0 | 1 | - |
| ZERO | bin auto[15104:15359] | 0 | 1 | - |
| ZERO | bin auto[15360:15615] | 0 | 1 | - |
| ZERO | bin auto[15616:15871] | 0 | 1 | - |
| ZERO | bin auto[15872:16127] | 0 | 1 | _ |
| ZERO | Din auco[13072-10127] | Ü | 1 | |
| ZERO | bin auto[16128:16383] | 0 | 1 | - |
| Cro | oss #cross0# | 1.04% | 100 | _ |
| Uncover | red | | | |
| | covered/total bins: | 43 | 4096 | - |
| | missing/total bins: | 4053 | 4096 | - |
| | | | | |
| | % Hit: | 1.04% | 100 | _ |
| | <pre>% Hit: type_option.weight=1</pre> | 1.04% | 100 | - |
| | | 1.04% | 100 | - |
| | type_option.weight=1 | 1.04% | 100 | - |
| | <pre>type_option.weight=1 type_option.goal=100</pre> | 1.04% | 100 | - |
| | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[512:543],auto[8192:8447]></auto[512:543],auto[8192:8447]></pre> | 1.04% | 100 | - |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[512:543],auto[8192:8447]></auto[512:543],auto[8192:8447]></pre> | | | - |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[512:543],auto[8192:8447]> d bin <auto[256:287],auto[8192:8447]></auto[256:287],auto[8192:8447]></auto[512:543],auto[8192:8447]></pre> | 5 | 1 | - |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[512:543],auto[8192:8447]> d bin <auto[256:287],auto[8192:8447]> d bin <auto[128:159],auto[8192:8447]></auto[128:159],auto[8192:8447]></auto[256:287],auto[8192:8447]></auto[512:543],auto[8192:8447]></pre> | 5 | 1 | - |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[512:543],auto[8192:8447]> d bin <auto[256:287],auto[8192:8447]> d bin <auto[128:159],auto[8192:8447]> d bin <auto[64:95],auto[8192:8447]></auto[64:95],auto[8192:8447]></auto[128:159],auto[8192:8447]></auto[256:287],auto[8192:8447]></auto[512:543],auto[8192:8447]></pre> | 5 | 1 | - |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[512:543],auto[8192:8447]> d bin <auto[256:287],auto[8192:8447]> d bin <auto[128:159],auto[8192:8447]> d bin <auto[64:95],auto[8192:8447]></auto[64:95],auto[8192:8447]></auto[128:159],auto[8192:8447]></auto[256:287],auto[8192:8447]></auto[512:543],auto[8192:8447]></pre> | 5 3 3 | 1 1 1 | - |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[512:543],auto[8192:8447]> bin <auto[256:287],auto[8192:8447]> bin <auto[128:159],auto[8192:8447]> bin <auto[64:95],auto[8192:8447]> bin <auto[32:63],auto[8192:8447]> </auto[32:63],auto[8192:8447]></auto[64:95],auto[8192:8447]></auto[128:159],auto[8192:8447]></auto[256:287],auto[8192:8447]></auto[512:543],auto[8192:8447]></pre> | 5377 | 1 1 1 1 | - |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[512:543],auto[8192:8447]> bin <auto[256:287],auto[8192:8447]> bin <auto[128:159],auto[8192:8447]> bin <auto[64:95],auto[8192:8447]> bin <auto[32:63],auto[8192:8447]> bin <auto[0:31],auto[8192:8447]> </auto[0:31],auto[8192:8447]></auto[32:63],auto[8192:8447]></auto[64:95],auto[8192:8447]></auto[128:159],auto[8192:8447]></auto[256:287],auto[8192:8447]></auto[512:543],auto[8192:8447]></pre> | 5 3 3 | 1 1 1 | |
| Covered Covered Covered Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[512:543],auto[8192:8447]> bin <auto[256:287],auto[8192:8447]> bin <auto[128:159],auto[8192:8447]> bin <auto[64:95],auto[8192:8447]> bin <auto[32:63],auto[8192:8447]> bin <auto[0:31],auto[8192:8447]> bin <auto[0:31],auto[8192:8447]> bin <auto[512:543],auto[4096:4351]></auto[512:543],auto[4096:4351]></auto[0:31],auto[8192:8447]></auto[0:31],auto[8192:8447]></auto[32:63],auto[8192:8447]></auto[64:95],auto[8192:8447]></auto[128:159],auto[8192:8447]></auto[256:287],auto[8192:8447]></auto[512:543],auto[8192:8447]></pre> | 5377 | 1 1 1 1 | |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[512:543],auto[8192:8447]> bin <auto[256:287],auto[8192:8447]> bin <auto[128:159],auto[8192:8447]> bin <auto[64:95],auto[8192:8447]> bin <auto[32:63],auto[8192:8447]> bin <auto[0:31],auto[8192:8447]> bin <auto[512:543],auto[4096:4351]> bin <auto[512:543],auto[4096:4351]></auto[512:543],auto[4096:4351]></auto[512:543],auto[4096:4351]></auto[0:31],auto[8192:8447]></auto[32:63],auto[8192:8447]></auto[64:95],auto[8192:8447]></auto[128:159],auto[8192:8447]></auto[256:287],auto[8192:8447]></auto[512:543],auto[8192:8447]></pre> | 5 3 7 7 | 1 1 1 1 | |

| Covered | bin <auto[128:159],auto[4096:4351]></auto[128:159],auto[4096:4351]> | 3 | 1 | - |
|---------|---|----|---|---|
| Covered | bin <auto[64:95],auto[4096:4351]></auto[64:95],auto[4096:4351]> | 2 | 1 | - |
| Covered | bin <auto[32:63],auto[4096:4351]></auto[32:63],auto[4096:4351]> | 7 | 1 | - |
| Covered | bin <auto[0:31],auto[4096:4351]></auto[0:31],auto[4096:4351]> | 39 | 1 | - |
| Covered | bin <auto[512:543],auto[2048:2303]></auto[512:543],auto[2048:2303]> | 3 | 1 | - |
| Covered | bin <auto[256:287],auto[2048:2303]></auto[256:287],auto[2048:2303]> | 4 | 1 | - |
| Covered | bin <auto[128:159],auto[2048:2303]></auto[128:159],auto[2048:2303]> | 11 | 1 | - |
| Covered | bin <auto[64:95],auto[2048:2303]></auto[64:95],auto[2048:2303]> | 3 | 1 | - |
| Covered | bin <auto[32:63],auto[2048:2303]></auto[32:63],auto[2048:2303]> | 3 | 1 | - |
| Covered | bin <auto[0:31],auto[2048:2303]></auto[0:31],auto[2048:2303]> | 38 | 1 | - |
| Covered | bin <auto[512:543],auto[1024:1279]></auto[512:543],auto[1024:1279]> | 4 | 1 | - |
| Covered | bin <auto[256:287],auto[1024:1279]></auto[256:287],auto[1024:1279]> | 6 | 1 | - |
| Covered | bin <auto[128:159],auto[1024:1279]></auto[128:159],auto[1024:1279]> | 6 | 1 | - |
| Covered | bin <auto[64:95],auto[1024:1279]></auto[64:95],auto[1024:1279]> | 10 | 1 | - |
| Covered | bin <auto[32:63],auto[1024:1279]></auto[32:63],auto[1024:1279]> | 9 | 1 | - |
| Covered | bin <auto[0:31],auto[1024:1279]></auto[0:31],auto[1024:1279]> | 35 | 1 | - |
| Covered | bin <auto[512:543],auto[512:767]></auto[512:543],auto[512:767]> | 8 | 1 | - |
| Covered | bin <auto[256:287],auto[512:767]></auto[256:287],auto[512:767]> | 7 | 1 | - |
| Covered | bin <auto[128:159],auto[512:767]></auto[128:159],auto[512:767]> | 7 | 1 | - |
| Covered | bin <auto[64:95],auto[512:767]></auto[64:95],auto[512:767]> | 2 | 1 | - |
| Covered | bin <auto[32:63],auto[512:767]></auto[32:63],auto[512:767]> | 5 | 1 | - |
| Covered | bin <auto[0:31],auto[512:767]></auto[0:31],auto[512:767]> | 44 | 1 | - |
| Covered | bin <auto[512:543],auto[256:511]></auto[512:543],auto[256:511]> | 8 | 1 | - |

| Canada | bin <auto[256:287],auto[256:511]></auto[256:287],auto[256:511]> | 8 | 1 | - |
|---------|---|-----|---|----|
| Covered | bin <auto[128:159],auto[256:511]></auto[128:159],auto[256:511]> | 7 | 1 | - |
| Covered | bin <auto[64:95],auto[256:511]></auto[64:95],auto[256:511]> | 6 | 1 | - |
| Covered | bin <auto[32:63],auto[256:511]></auto[32:63],auto[256:511]> | 4 | 1 | - |
| Covered | bin <auto[0:31],auto[256:511]></auto[0:31],auto[256:511]> | 44 | 1 | _ |
| Covered | bin <auto[1024:1055],auto[0:255]></auto[1024:1055],auto[0:255]> | 1 | 1 | _ |
| Covered | | | | |
| Covered | bin <auto[512:543],auto[0:255]></auto[512:543],auto[0:255]> | 64 | 1 | _ |
| Covered | bin <auto[256:287],auto[0:255]></auto[256:287],auto[0:255]> | 37 | 1 | - |
| Covered | bin <auto[128:159],auto[0:255]></auto[128:159],auto[0:255]> | 33 | 1 | - |
| Covered | bin <auto[64:95],auto[0:255]></auto[64:95],auto[0:255]> | 43 | 1 | - |
| Covered | bin <auto[32:63],auto[0:255]></auto[32:63],auto[0:255]> | 46 | 1 | - |
| | bin <auto[0:31],auto[0:255]></auto[0:31],auto[0:255]> | 296 | 1 | - |
| Covered | bin <auto[2016:2047],*></auto[2016:2047],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1984:2015],*></auto[1984:2015],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1952:1983],*></auto[1952:1983],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1920:1951],*></auto[1920:1951],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1888:1919],*></auto[1888:1919],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1856:1887],*></auto[1856:1887],*> | 0 | 1 | 64 |
| ZERO | | | | |
| ZERO | bin <auto[1824:1855],*></auto[1824:1855],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1792:1823],*></auto[1792:1823],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1760:1791],*></auto[1760:1791],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1728:1759],*></auto[1728:1759],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1696:1727],*></auto[1696:1727],*> | 0 | 1 | 64 |
| ZEKO | | | | |

| ZERO | bin <auto[1664:1695],*></auto[1664:1695],*> | 0 | 1 | 64 |
|------|---|---|---|----|
| ZERO | bin <auto[1632:1663],*></auto[1632:1663],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1600:1631],*></auto[1600:1631],*> | 0 | 1 | 64 |
| | bin <auto[1568:1599],*></auto[1568:1599],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1536:1567],*></auto[1536:1567],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1504:1535],*></auto[1504:1535],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1472:1503],*></auto[1472:1503],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1440:1471],*></auto[1440:1471],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1408:1439],*></auto[1408:1439],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1376:1407],*></auto[1376:1407],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1344:1375],*></auto[1344:1375],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1312:1343],*></auto[1312:1343],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1280:1311],*></auto[1280:1311],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1248:1279],*></auto[1248:1279],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1216:1247],*></auto[1216:1247],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1184:1215],*></auto[1184:1215],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1152:1183],*></auto[1152:1183],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1120:1151],*></auto[1120:1151],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1088:1119],*></auto[1088:1119],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1056:1087],*></auto[1056:1087],*> | 0 | 1 | 64 |
| ZERO | bin <auto[992:1023],*></auto[992:1023],*> | 0 | 1 | 64 |
| ZERO | bin <auto[960:991],*></auto[960:991],*> | 0 | 1 | 64 |
| ZERO | bin <auto[928:959],*></auto[928:959],*> | 0 | 1 | 64 |
| ZERO | | | | |

| ZEDO | bin <auto[896:927],*></auto[896:927],*> | 0 | 1 | 64 |
|--------------|---|---|---|----|
| ZERO ZERO | bin <auto[864:895],*></auto[864:895],*> | 0 | 1 | 64 |
| ZERO | bin <auto[832:863],*></auto[832:863],*> | 0 | 1 | 64 |
| ZERO | bin <auto[800:831],*></auto[800:831],*> | 0 | 1 | 64 |
| ZERO | bin <auto[768:799],*></auto[768:799],*> | 0 | 1 | 64 |
| ZERO | bin <auto[736:767],*></auto[736:767],*> | 0 | 1 | 64 |
| ZERO | bin <auto[704:735],*></auto[704:735],*> | 0 | 1 | 64 |
| ZERO | bin <auto[672:703],*></auto[672:703],*> | 0 | 1 | 64 |
| ZERO | bin <auto[640:671],*></auto[640:671],*> | 0 | 1 | 64 |
| ZERO | bin <auto[608:639],*></auto[608:639],*> | 0 | 1 | 64 |
| ZERO | bin <auto[576:607],*></auto[576:607],*> | 0 | 1 | 64 |
| ZERO | bin <auto[544:575],*></auto[544:575],*> | 0 | 1 | 64 |
| ZERO | bin <auto[480:511],*></auto[480:511],*> | 0 | 1 | 64 |
| ZERO | bin <auto[448:479],*></auto[448:479],*> | 0 | 1 | 64 |
| ZERO | bin <auto[416:447],*></auto[416:447],*> | 0 | 1 | 64 |
| ZERO | bin <auto[384:415],*></auto[384:415],*> | 0 | 1 | 64 |
| ZERO | bin <auto[352:383],*></auto[352:383],*> | 0 | 1 | 64 |
| ZERO | bin <auto[320:351],*></auto[320:351],*> | 0 | 1 | 64 |
| ZERO | bin <auto[288:319],*></auto[288:319],*> | 0 | 1 | 64 |
| ZERO | bin <auto[224:255],*></auto[224:255],*> | 0 | 1 | 64 |
| ZERO | bin <auto[192:223],*></auto[192:223],*> | 0 | 1 | 64 |
| ZERO | bin <auto[160:191],*></auto[160:191],*> | 0 | 1 | 64 |
| ZERO | bin <auto[96:127],*></auto[96:127],*> | 0 | 1 | 64 |
| | | | | |

| ZEDO | bin <*,auto[16128:16383]> | 0 | 1 | 64 |
|--------------|---------------------------|---|---|----|
| ZERO ZERO | bin <*,auto[15872:16127]> | 0 | 1 | 64 |
| | bin <*,auto[15616:15871]> | 0 | 1 | 64 |
| ZERO ZERO | bin <*,auto[15360:15615]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[15104:15359]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[14848:15103]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[14592:14847]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[14336:14591]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[14080:14335]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[13824:14079]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[13568:13823]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[13312:13567]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[13056:13311]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[12800:13055]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[12544:12799]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[12288:12543]> | 0 | 1 | 64 |
| | bin <*,auto[12032:12287]> | 0 | 1 | 64 |
| ZERO ZERO | bin <*,auto[11776:12031]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[11520:11775]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[11264:11519]> | 0 | 1 | 64 |
| | bin <*,auto[11008:11263]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[10752:11007]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[10496:10751]> | 0 | 1 | 64 |
| ZERO | | | | |

| 700 | bin <*,auto[10240:10495]> | 0 | 1 | 64 |
|--------------|---------------------------|---|---|----|
| ZERO ZERO | bin <*,auto[9984:10239]> | 0 | 1 | 64 |
| | bin <*,auto[9728:9983]> | 0 | 1 | 64 |
| ZERO ZERO | bin <*,auto[9472:9727]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[9216:9471]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[8960:9215]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[8704:8959]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[8448:8703]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[7936:8191]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[7680:7935]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[7424:7679]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[7168:7423]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[6912:7167]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[6656:6911]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[6400:6655]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[6144:6399]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[5888:6143]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[5632:5887]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[5376:5631]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[5120:5375]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[4864:5119]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[4608:4863]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[4352:4607]> | 0 | 1 | 64 |
| ZEKU | | | | |

| | bin <*,auto[3840:4095]> | 0 | 1 | 64 |
|------|---|-------|------|----|
| ZERO | bin <*,auto[3584:3839]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[3328:3583]> | 0 | 1 | 64 |
| ZERO | hin (* auto[2072:2227] | 0 | 1 | 64 |
| ZERO | bin <*,auto[3072:3327]> | O | 1 | 04 |
| ZERO | bin <*,auto[2816:3071]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[2560:2815]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[2304:2559]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[1792:2047]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[1536:1791]> | 0 | 1 | 64 |
| ZERO | | | | |
| ZERO | bin <*,auto[1280:1535]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[768:1023]> | 0 | 1 | 64 |
| ZERO | bin <auto[1024:1055],auto[8192:8447]></auto[1024:1055],auto[8192:8447]> | 0 | 1 | 1 |
| ZEKO | bin <auto[1024:1055],auto[4096:4351]></auto[1024:1055],auto[4096:4351]> | 0 | 1 | 1 |
| ZERO | bin <auto[1024:1055],auto[2048:2303]></auto[1024:1055],auto[2048:2303]> | 0 | 1 | 1 |
| ZERO | bin <auto[1024:1055],auto[1024:1279]></auto[1024:1055],auto[1024:1279]> | 0 | 1 | 1 |
| ZERO | | | | |
| ZERO | bin <auto[1024:1055],auto[512:767]></auto[1024:1055],auto[512:767]> | 0 | 1 | 1 |
| ZERO | bin <auto[1024:1055],auto[256:511]></auto[1024:1055],auto[256:511]> | 0 | 1 | 1 |
| | oss #cross1# | 0.00% | 100 | _ |
| ZERO | covered/total bins: | 0 | 1024 | - |
| | missing/total bins: | 1024 | 1024 | - |
| | % Hit: | 0.00% | 100 | - |
| | | | | |

type_option.weight=1
type_option.goal=100

11 = 1 3

type_option.comment=

Auto, Default and User Defined Bins:

ZERO

Statement Coverage:

| Enabled Coverage | Bins | Hits | Misses | Coverage |
|------------------|------|------|--------|----------|
| | | | | |
| Statements | 391 | 298 | 93 | 76.21% |

Statement Coverage for Design Unit work.coverage_sv_unit --

| Line | Item | Count | Source |
|-------------|------|-------------|--------|
| | | | |
| File transa | | 5100 | |
| 143 | 1 | 51029 | |
| 144 | 1 | 51029 | |
| 145 | 1 | 51029 | |
| 146 | 1 | 51029 | |
| 147 | 1 | 51029 | |
| 148 | 1 | 51029 | |
| 149 | 1 | 51029 | |
| 152 | 1 | 51029 | |
| 153 | 1 | 51029 | |
| 154 | 1 | 51029 | |
| 155 | 1 | 51029 | |
| 156 | 1 | 51029 | |
| 157 | 1 | 51029 | |
| 158 | 1 | 51029 | |
| 159 | 1 | 51029 | |
| 160 | 1 | 51029 | |
| 161 | 1 | 51029 | |
| 164 | 1 | 51029 | |
| 165 | 1 | 51029 | |
| 166 | 1 | 51029 | |
| 167 | 1 | 51029 | |
| 168 | 1 | 51029 | |
| 169 | 1 | 51029 | |
| 170 | 1 | 51029 | |
| 171 | 1 | 51029 | |
| 172 | 1 | 51029 | |
| 173 | 1 | 51029 | |
| 174 | 1 | 51029 | |
| 175 | 1 | 51029 | |
| 176 | 1 | 51029 | |
| 177 | 1 | 51029 | |
| 178 | 1 | 51029 | |
| | | | |

| 179 | 1 | 51029 |
|-------------|--------|---------------|
| 180 | 1 | 51029 |
| 181 | 1 | 51029 |
| 182 | 1 | 51029 |
| 199 | 1 | 25 |
| 200 | 1 | 25 |
| 201 | 1 | 25 |
| 202 | 1 | 25 |
| 203 | 1 | 25 |
| 204 | 1 | 25 |
| 205 | 1 | 25 |
| 226 | 1 | 68 |
| 228 | 1 | 83 |
| 230 | 1 | 74 |
| 232 | 1 | 61 |
| 234 | 1 | 79 |
| 236 | 1 | 70 |
| 238 | 1 | 79 |
| 240 | 1 | 68 |
| 243 | 1 | 84 |
| 244 | 1 | 79 |
| 245 | 1 | 82 |
| 246 | 1 | 70 |
| 248 | 1 | 70 |
| 249 | 1 | 58 |
| 250 | 1 | ***0*** |
| 252 | 1 | 1025 |
| 264 | 1 | 1025 |
| 265 | 1 | 1025 |
| 266 | 1 | 1025 |
| 267 | 1 | 1025 |
| 268 | 1 | 1025 |
| 269 | 1 | 1025 |
| 270 | 1 | 1025 |
| 271 | 1 | 1025 |
| 272 | 1 | 1025 |
| File covera | age.sv | |
| 18 | 1 | 1 |
| 60 | 1 | 1 |
| 61 | 1 | 1 |
| 66 | 1 | 1 |
| 67 | 1 | 1 |
| 68 | 1 | 50002 |
| 70 | 1 | 914 |
| 73 | 1 | * * * 0 * * * |
| 78 | 1 | * * * 0 * * * |
| | | |

| 79 | 1 | * * * 0 * * * |
|--------|-------------|---------------|
| 80 | 1 | ***0*** |
| 81 | 1 | ***0*** |
| 82 | 1 | ***0*** |
| 87 | 1 | ***0*** |
| 88 | 1 | ***0*** |
| 89 | 1 | ***0*** |
| 90 | 1 | ***0*** |
| 91 | 1 | ***0*** |
| 92 | 1 | ***0*** |
| 93 | 1 | ***0*** |
| 98 | 1 | 1 |
| 99 | 1 | ***0*** |
| 100 | 1 | ***0*** |
| File d | river.sv | |
| 27 | 1 | 1 |
| 28 | 1 | 1 |
| 34 | 1 | 1 |
| 35 | 1 | 1026 |
| 36 | 1 | 1025 |
| 37 | 1 | 1025 |
| 46 | 1 | 1025 |
| 47 | 1 | 1025 |
| 48 | 1 | 1025 |
| 49 | 1 | 1025 |
| 50 | 1 | 1025 |
| 51 | 1 | 1025 |
| 52 | 1 | 1025 |
| 53 | 1 | 1025 |
| 54 | 1 | 1025 |
| 55 | 1 | 1025 |
| 56 | 1 | 1025 |
| 57 | 1 | 1025 |
| 58 | 1 | 1025 |
| 61 | 1 | 1025 |
| 63 | 1 | 1025 |
| 64 | 1 | 1025 |
| | enerator.sv | 1025 |
| 55 | 1 | 1 |
| 62 | 1 | 1 |
| 63 | 1 | 1 |
| 72 | 1 | 1 |
| 75 | 1 | 1 |
| 75 | 1 | 1 |
| 80 | 1 | 1 |
| 91 | 1 | 1 |
| シエ | 1 | 1 |

| 94 | 1 | 1 |
|-----|--------------|---------------|
| 97 | 1 | 1 |
| 100 | 1 | 1 |
| 103 | 1 | 1 |
| 106 | 1 | 1 |
| 109 | 1 | 1 |
| 112 | 1 | 1 |
| 115 | 1 | 1 |
| 125 | 1 | 1 |
| 125 | 2 | 1000 |
| 127 | 1 | 1000 |
| 128 | 1 | 1000 |
| 134 | 1 | 334 |
| 138 | 1 | 333 |
| 150 | 1 | * * * 0 * * * |
| 153 | 1 | 1000 |
| 156 | 1 | 1000 |
| 159 | 1 | 1000 |
| 169 | 1 | 1 |
| 171 | 1 | 1 |
| 172 | 1 | 1 |
| 175 | 1 | 1 |
| 177 | 1 | 1 |
| 178 | 1 | 1 |
| 181 | 1 | 1 |
| 183 | 1 | 1 |
| 184 | 1 | 1 |
| 187 | 1 | 1 |
| 189 | 1 | 1 |
| 190 | 1 | 1 |
| 199 | 1 | 1 |
| 201 | 1 | 1 |
| 202 | 1 | 1 |
| 205 | 1 | 1 |
| 207 | 1 | 1 |
| 208 | 1 | 1 |
| 211 | 1 | 1 |
| 213 | 1 | 1 |
| 214 | 1 | 1 |
| 223 | 1 | 1 |
| 225 | 1 | 1 |
| 226 | 1 | 1 |
| 229 | 1 | 1 |
| 231 | 1 | 1 |
| 232 | 1 | 1 |
| 235 | 1 | 1 |
| | - | ± |

| 237 | 1 | 1 |
|-----|---|---|
| 238 | 1 | 1 |
| 247 | 1 | 1 |
| 249 | 1 | 1 |
| 250 | 1 | 1 |
| 253 | 1 | 1 |
| 255 | 1 | 1 |
| 256 | 1 | 1 |
| 259 | 1 | 1 |
| 261 | 1 | 1 |
| 262 | 1 | 1 |
| 265 | 1 | 1 |
| 267 | 1 | 1 |
| 268 | 1 | 1 |
| 277 | 1 | 1 |
| 278 | 1 | 1 |
| 279 | 1 | 1 |
| 282 | 1 | 1 |
| 283 | 1 | 1 |
| 284 | 1 | 1 |
| 293 | 1 | 1 |
| 295 | 1 | 1 |
| 296 | 1 | 1 |
| 299 | 1 | 1 |
| 301 | 1 | 1 |
| 302 | 1 | 1 |
| 311 | 1 | 1 |
| 312 | 1 | 1 |
| 313 | 1 | 1 |
| 316 | 1 | 1 |
| 317 | 1 | 1 |
| 318 | 1 | 1 |
| 327 | 1 | 1 |
| 328 | 1 | 1 |
| 329 | 1 | 1 |
| 332 | 1 | 1 |
| 333 | 1 | 1 |
| 334 | 1 | 1 |
| 343 | 1 | 1 |
| 344 | 1 | 1 |
| 345 | 1 | 1 |
| 348 | 1 | 1 |
| 349 | 1 | 1 |
| 350 | 1 | 1 |
| 356 | 1 | 1 |
| 357 | 1 | 1 |
| | | |

| 358 | 1 | 1 |
|-----------------|---|---------|
| 373 | 1 | 68 |
| 374 | 1 | 83 |
| 375 | 1 | 74 |
| 376 | 1 | 61 |
| 377 | 1 | 79 |
| 378 | 1 | 70 |
| 379 | 1 | 79 |
| 380 | 1 | 68 |
| 381 | 1 | 84 |
| 382 | 1 | 79 |
| 383 | 1 | 82 |
| 384 | 1 | 70 |
| 385 | 1 | 70 |
| 386 | 1 | 58 |
| 387 | 1 | ***0*** |
| 392 | 1 | 113 |
| 393 | 1 | 91 |
| 394 | 1 | 102 |
| 395 | 1 | 91 |
| 396 | 1 | 109 |
| 397 | 1 | 88 |
| 398 | 1 | 82 |
| 399 | 1 | 76 |
| 400 | 1 | 77 |
| 401 | 1 | 105 |
| 402 | 1 | 2 |
| 403 | 1 | 89 |
| 408 | 1 | 1025 |
| 409 | 1 | 1025 |
| 410 | 1 | 1025 |
| 411 | 1 | 1025 |
| 412 | 1 | 1025 |
| 413 | 1 | 1025 |
| 414 | 1 | 1025 |
| 415 | 1 | 1025 |
| 416 | 1 | 1025 |
| 417 | 1 | 1025 |
| 420 | 1 | 1025 |
| File monitor.sv | | |
| 18 | 1 | 1 |
| 31 | 1 | 1 |
| 32 | 1 | 1 |
| 44 | 1 | 1 |
| 45 | 1 | 1 |
| 47 | 1 | 50002 |
| | | |

| 49 | 1 | 50002 |
|-----|---|---------------|
| 52 | 1 | 914 |
| 53 | 1 | 914 |
| 54 | 1 | 914 |
| 55 | 1 | 914 |
| 56 | 1 | 914 |
| 57 | 1 | 914 |
| 58 | 1 | 914 |
| 59 | 1 | 914 |
| 60 | 1 | 914 |
| 61 | 1 | 914 |
| 62 | 1 | 914 |
| 63 | 1 | 914 |
| 64 | 1 | 914 |
| 65 | 1 | 914 |
| 66 | 1 | 914 |
| 67 | 1 | 914 |
| 70 | 1 | 914 |
| 73 | 1 | ***0*** |
| 88 | 1 | 1 |
| 92 | 1 | 1 |
| 105 | 1 | 1 |
| 106 | 1 | 1 |
| 119 | 1 | 1 |
| 120 | 1 | 1 |
| 122 | 1 | 1 |
| 124 | 1 | 1 |
| 126 | 1 | 1 |
| 129 | 1 | ***0*** |
| 130 | 1 | ***0*** |
| 131 | 1 | ***0*** |
| 132 | 1 | * * * 0 * * * |
| 133 | 1 | * * * 0 * * * |
| 134 | 1 | * * * 0 * * * |
| 135 | 1 | * * * 0 * * * |
| 136 | 1 | ***0*** |
| 137 | 1 | ***0*** |
| 138 | 1 | * * * 0 * * * |
| 139 | 1 | ***0*** |
| 140 | 1 | ***0*** |
| 141 | 1 | ***0*** |
| 142 | 1 | ***0*** |
| 143 | 1 | * * * 0 * * * |
| 144 | 1 | ***0*** |
| 145 | 1 | ***0*** |
| 146 | 1 | ***0*** |
| | | |

| 147 | 1 | ***0*** |
|------------|----------|---------------|
| 150 | 1 | * * * 0 * * * |
| 152 | 1 | * * * 0 * * * |
| 154 | 1 | ***0*** |
| File score | board.sv | |
| 16 | 1 | 1 |
| 17 | 1 | 1 |
| 43 | 1 | 1 |
| 44 | 1 | 1 |
| 51 | 1 | 1 |
| 52 | 1 | 1 |
| 61 | 1 | 1 |
| 62 | 1 | 1 |
| 73 | 1 | 1 |
| 74 | 1 | 915 |
| 75 | 1 | 915 |
| 76 | 1 | 914 |
| 77 | 1 | 914 |
| 80 | 1 | 914 |
| 81 | 1 | 914 |
| 82 | 1 | 914 |
| 83 | 1 | 914 |
| 84 | 1 | 914 |
| 85 | 1 | |
| | | 914 |
| 86 | 1 | 914 |
| 87 | 1 | 914 |
| 88 | 1 | 914 |
| 89 | 1 | 914 |
| 90 | 1 | 914 |
| 91 | 1 | 914 |
| 92 | 1 | 914 |
| 93 | 1 | 914 |
| 94 | 1 | 914 |
| 95 | 1 | 914 |
| 131 | 1 | 1 |
| 132 | 1 | 1 |
| 133 | 1 | ***0*** |
| 134 | 1 | ***0*** |
| 135 | 1 | ***0*** |
| 136 | 1 | ***0*** |
| 137 | 1 | ***0*** |
| 140 | 1 | ***0*** |
| 141 | 1 | ***0*** |
| 142 | 1 | ***0*** |
| 143 | 1 | ***0*** |
| 144 | 1 | ***0*** |
| | | |

| 145 | 1 | ***0*** |
|-----|---|---------------|
| 146 | 1 | ***0*** |
| 147 | 1 | ***0*** |
| 148 | 1 | ***0*** |
| 149 | 1 | ***0*** |
| 150 | 1 | ***0*** |
| 151 | 1 | ***0*** |
| 152 | 1 | ***0*** |
| 153 | 1 | ***0*** |
| 154 | 1 | ***0*** |
| 161 | 1 | ***0*** |
| 164 | 1 | ***0*** |
| 173 | 1 | ***0*** |
| 183 | 1 | ***0*** |
| 189 | 1 | ***0*** |
| 192 | 1 | ***0*** |
| 196 | 1 | ***0*** |
| 202 | 1 | ***0*** |
| 207 | 1 | ***0*** |
| 211 | 1 | ***0*** |
| 218 | 1 | ***0*** |
| 222 | 1 | ***0*** |
| 242 | 1 | ***0*** |
| 248 | 1 | ***0*** |
| 250 | 1 | ***0*** |
| 252 | 1 | ***0*** |
| 258 | 1 | ***0*** |
| 308 | 1 | ***0*** |
| 309 | 1 | ***0*** |
| 310 | 1 | ***0*** |
| 312 | 1 | ***0*** |
| 313 | 1 | ***0*** |
| 314 | 1 | * * * 0 * * * |
| 315 | 1 | ***0*** |
| 316 | 1 | ***0*** |
| 317 | 1 | ***0*** |
| 318 | 1 | ***0*** |
| 319 | 1 | * * * 0 * * * |
| 320 | 1 | * * * 0 * * * |
| 321 | 1 | * * * 0 * * * |
| 322 | 1 | * * * 0 * * * |
| 323 | 1 | ***0*** |
| | | |

=== Design Unit: work.rv32i_alu

Branch Coverage:

| Enabled Coverage | Bins | Hits | Misses | Coverage |
|------------------|------|------|--------|----------|
| | | | | |
| Branches | 62 | 55 | 7 | 88.70% |

Branch Coverage for Design Unit work.rv32i_alu

| Branch Coverag | ge for Design Ur | iit work.rv321_alu | |
|----------------|------------------|--------------------|-----------------------|
| Line | Item | Count | Source |
| | | | |
| File rv32i_a | alu.sv | | |
| | | IF Branch | |
| 174 | | 1026 | Count coming in to IF |
| 174 | 1 | 1026 | |
| 178 | 1 | * * * 0 * * * | |
| Branch totals | : 1 hit of 2 bra | anches = 50.00% | |
| | | | |
| | | IF Branch | |
| 179 | | * * * 0 * * * | Count coming in to IF |
| 179 | 1 | * * * 0 * * * | |
| | | * * * 0 * * * | All False Count |
| Branch totals | : 0 hits of 2 br | canches = 0.00% | |
| | | | |
| | | IF Branch | |
| 198 | | * * * 0 * * * | Count coming in to IF |
| 198 | 1 | * * * 0 * * * | |
| 201 | 1 | * * * 0 * * * | |
| 204 | 1 | * * * 0 * * * | |
| | | * * * 0 * * * | All False Count |
| Branch totals | : 0 hits of 4 br | ranches = 0.00% | |
| | | | |
| | | IF Branch | |
| 218 | | 1025 | Count coming in to IF |
| 218 | 1 | 165 | |
| 218 | 2 | 860 | |
| Branch totals | : 2 hits of 2 br | canches = 100.00% | |

220 1025 Count coming in to IF
220 1 222
220 2 803

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

223 1 68

958 All False Count

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

224 1026 Count coming in to IF

224 1 83

943 All False Count

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

225 1026 Count coming in to IF

225 1 135

891 All False Count

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

227 135 Count coming in to IF

227 1 74

61 All False Count

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

227 74 Count coming in to IF

227 2 40

227 3 34

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

229 1026 Count coming in to IF

229 1 79

947 All False Count

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

230 1026 Count coming in to IF

230 1 70

956 All False Count

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

231 1026 Count coming in to IF

231 1 79

947 All False Count

Branch totals: 2 hits of 2 branches = 100.00%

| | | IF Branch | |
|---|--|---|--|
| 232 | | 1026 | |
| 232 | 1 | 68 | |
| 232 | 1 | | All Ealgo Count |
| - 1 1 . | 0.14. | | All False Count |
| Branch totals: | 2 hits of 2 | 2 branches = 100.00% | |
| | | | |
| | | IF Branch | |
| 233 | | 1026 | Count coming in to IF |
| 233 | 1 | 84 | |
| | | 942 | All False Count |
| Branch totals: | 2 hits of | 2 branches = 100.00% | |
| | | | |
| | | IF Branch | |
| 234 | | 1026 | |
| 234 | 1 | 79 | |
| 234 | 1 | | All Dalas Count |
| P 1 | 0.1.1. | | All False Count |
| Branch totals: | 2 hits of 2 | 2 branches = 100.00% | |
| | | | |
| | | IF Branch | |
| 235 | | 1026 | Count coming in to IF |
| 235 | 1 | 152 | |
| | | 874 | All False Count |
| Branch totals: | 2 hits of | 2 branches = 100.00% | |
| | | | |
| | | | |
| | | IF Branch | |
| | | | Count coming in to IF |
| 237 | | 152 | Count coming in to IF |
| | 1 | 152 70 | Count coming in to IF |
| 237 237 | 1 | 152 70 82 | |
| 237 237 | 1 | 152 70 | Count coming in to IF |
| 237 237 Branch totals: | 1 2 hits of : | 152 70 82 2 branches = 100.00% | Count coming in to IF All False Count |
| 237 237 Branch totals: | 1 2 hits of : | 152 70 82 2 branches = 100.00% | Count coming in to IF |
| 237 237 Branch totals: | 1 2 hits of : | 152 70 82 2 branches = 100.00% | Count coming in to IF All False Count |
| 237 237 Branch totals: | 1 2 hits of : | 152 70 82 2 branches = 100.00% | Count coming in to IF All False Count |
| 237 237 Branch totals: | 1 2 hits of : | 152 70 82 2 branches = 100.00% IF Branch 1026 128 | Count coming in to IF All False Count |
| 237 237 Branch totals:239 239 | 1 2 hits of : | 152 70 82 2 branches = 100.00% IF Branch 1026 128 | Count coming in to IF All False Count Count coming in to IF |
| 237 237 Branch totals:239 239 | 1 2 hits of : | 152 70 82 2 branches = 100.00% IF Branch 1026 128 898 | Count coming in to IF All False Count Count coming in to IF |
| 237 237 Branch totals:239 239 Branch totals: | 1 2 hits of : 1 2 hits of : | 152 70 82 2 branches = 100.00% IF Branch 1026 128 898 2 branches = 100.00% | Count coming in to IF All False Count Count coming in to IF All False Count |
| 237 237 Branch totals: 239 239 Branch totals: | 1 2 hits of : 1 2 hits of : | 152 70 82 2 branches = 100.00% IF Branch | Count coming in to IF All False Count Count coming in to IF All False Count |
| 237 237 Branch totals: 239 239 Branch totals: | 1 2 hits of 2 | 152 70 82 2 branches = 100.00% | Count coming in to IF All False Count Count coming in to IF All False Count |
| 237 237 Branch totals: 239 239 Branch totals: | 1 2 hits of : 1 2 hits of : | 152 70 82 2 branches = 100.00% | Count coming in to IF All False Count Count coming in to IF All False Count Count coming in to IF |
| 237 237 Branch totals: | 1 2 hits of 2 1 2 hits of 2 | 152 70 82 2 branches = 100.00% IF Branch | Count coming in to IF All False Count Count coming in to IF All False Count Count coming in to IF |
| 237 237 Branch totals: | 1 2 hits of 2 1 2 hits of 2 | 152 70 82 2 branches = 100.00% | Count coming in to IF All False Count Count coming in to IF All False Count Count coming in to IF |
| 237 237 Branch totals: | 1 2 hits of : 1 2 hits of : 1 2 hits of : 2 hits of : | 152 70 82 2 branches = 100.00% IF Branch 1026 128 898 2 branches = 100.00% IF Branch 128 70 58 2 branches = 100.00% | Count coming in to IF All False Count Count coming in to IF All False Count Count coming in to IF All False Count |
| 237 237 Branch totals: | 1 2 hits of : 1 2 hits of : 1 2 hits of : 2 hits of : | 152 70 82 2 branches = 100.00% IF Branch 1026 128 898 2 branches = 100.00% IF Branch 128 70 58 2 branches = 100.00% | Count coming in to IF All False Count Count coming in to IF All False Count Count coming in to IF |
| 237 237 Branch totals: | 1 2 hits of : 1 2 hits of : 1 2 hits of : 2 hits of : | 152 70 82 2 branches = 100.00% IF Branch 1026 128 898 2 branches = 100.00% IF Branch 128 70 58 2 branches = 100.00% | Count coming in to IF All False Count Count coming in to IF All False Count Count coming in to IF All False Count |
| 237 237 Branch totals: 239 239 Branch totals: 241 241 Branch totals: | 1 2 hits of : 1 2 hits of : 1 2 hits of : 2 hits of : | 152 70 82 2 branches = 100.00% IF Branch 1026 128 898 2 branches = 100.00% IF Branch 128 70 58 2 branches = 100.00% | Count coming in to IF All False Count Count coming in to IF All False Count Count coming in to IF All False Count |
| 237 237 Branch totals: | 1 2 hits of 3 1 2 hits of 3 | 152 70 82 2 branches = 100.00% | Count coming in to IF All False Count Count coming in to IF All False Count Count coming in to IF All False Count |

| Branch | totals: | 2 | hits | \circ f | 2 | branches | = | 100 | 00% |
|--------|---------|---|------|-----------|---|----------|---|-----|-----|
| | | | | | | | | | |

| | | IF Branch | |
|---------------|-----------------|--------------------|-----------------------|
| 257 | | 1193 | Count coming in to IF |
| 257 | 1 | 1191 | |
| | | 2 | All False Count |
| Branch totals | : 2 hits of 2 k | oranches = 100.00% | |
| | | | |
| | | IF Branch | |
| 258 | | 1191 | Count coming in to IF |
| 258 | 1 | 232 | |
| | | 959 | All False Count |
| Branch totals | : 2 hits of 2 k | oranches = 100.00% | |
| | | | |
| | | IF Branch | |
| 259 | | 1191 | Count coming in to IF |
| 259 | 1 | 55 | |
| | | 1136 | All False Count |
| Branch totals | : 2 hits of 2 k | oranches = 100.00% | |
| | | | |
| | | IF Branch | |
| 266 | | 1191 | Count coming in to IF |
| 266 | 1 | 255 | |
| | | 936 | All False Count |
| Branch totals | : 2 hits of 2 k | oranches = 100.00% | |
| | | | |
| | | IF Branch | |
| 267 | | 255 | Count coming in to IF |
| 267 | 1 | 161 | |
| | | 94 | All False Count |
| Branch totals | : 2 hits of 2 k | oranches = 100.00% | |
| | | | |
| | | IF Branch | |
| 277 | | 1193 | Count coming in to IF |
| 277 | 1 | 81 | |
| | | 1112 | All False Count |
| Branch totals | : 2 hits of 2 k | oranches = 100.00% | |
| | | | |
| | | IF Branch | |
| 278 | | 1193 | Count coming in to IF |
| 278 | 1 | 83 | |
| | | 1110 | All False Count |
| Branch totals | : 2 hits of 2 k | oranches = 100.00% | |
| | | | |
| | | IF Branch | |
| 280 | | 1193 | Count coming in to IF |
| | | | |

280 1 335 283 1 858

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

287 1193 Count coming in to IF

287 1 109

290 1 1084

Branch totals: 2 hits of 2 branches = 100.00%

Condition Coverage:

| Enabled Coverage | Bins | Covered | Misses | Coverage |
|------------------|------|---------|--------|----------|
| | | | | |
| Conditions | 34 | 25 | 9 | 73.52% |

Condition Coverage for Design Unit work.rv32i_alu --

File rv32i_alu.sv

-----Focused Condition View-----

Line 179 Item 1 (i_ce && ~stall_bit)

Condition totals: 0 of 2 input terms covered = 0.00%

Input Term Covered Reason for no coverage Hint

i_ce N No hits Hit '_0' and '_1'

stall_bit N No hits Hit '_0' and '_1'

Rows: Hits FEC Target Non-masking condition(s)

Row 1: ***0*** i_ce_0 -

Row 2: ***0*** i_ce_1 ~stall_bit

Row 3: ***0*** stall_bit_0 i_ce

Row 4: ***0*** stall_bit_1 i_ce

-----Focused Condition View-----

Line 198 Item 1 (i_flush && ~stall_bit)

Condition totals: 0 of 2 input terms covered = 0.00%

Input Term Covered Reason for no coverage Hint

i_flush N No hits Hit '_0' and '_1'

stall_bit N No hits Hit '_0' and '_1'

```
Rows:
         Hits FEC Target
                                Non-masking condition(s)
 Row 1: ***0*** i_flush_0
         ***0*** i_flush_1
 Row 2:
                                ~stall_bit
 Row 3: ***0*** stall_bit_0
                                i_flush
         ***0*** stall_bit_1
 Row 4:
                                i_flush
------Focused Condition View------
Line 204 Item 1 (stall_bit && ~i_stall)
Condition totals: 0 of 2 input terms covered = 0.00%
 Input Term Covered Reason for no coverage Hint
______
  stall_bit
              N No hits
                                   Hit '_0' and '_1'
             N No hits
                                   Hit '_0' and '_1'
   i_stall
   Rows: Hits FEC Target
                                Non-masking condition(s)
 -----
 Row 1: ***0*** stall_bit_0
         ***0*** stall_bit_1
 Row 2:
                                ~i_stall
 Row 3: ***0*** i_stall_0
                                stall_bit
         ***0*** i_stall_1
 Row 4:
                                stall_bit
-----Focused Condition View-----
        218 Item 1 (opcode_jal || opcode_auipc)
Condition totals: 2 of 2 input terms covered = 100.00%
  Input Term Covered Reason for no coverage Hint
  opcode_jal
                Y
 opcode_auipc
   Rows: Hits FEC Target
                                Non-masking condition(s)
 ______ ____
 Row 1:
             1 opcode_jal_0
                                ~opcode_auipc
 Row 2:
             1 opcode_jal_1
 Row 3:
             1 opcode_auipc_0
                                ~opcode_jal
           1 opcode_auipc_1
 Row
    4:
                               ~opcode_jal
------Focused Condition View------
        220 Item 1 (opcode_rtype || opcode_branch)
Line
Condition totals: 2 of 2 input terms covered = 100.00%
   Input Term Covered Reason for no coverage Hint
  opcode_rtype
```

| | | | FEC Target | | | condition(s) |
|--------|---------|------------|---------------|----------------|---------------|--------------------------|
| | | | | | | 1. |
| Row | | | | | ~opcode_brar | icn |
| | | | opcode_rtype | | | |
| Row | | | | | ~opcode_rtyp | |
| Row | 4: | 1 | opcode_bran | cn_1 | ~opcode_rtyp | De . |
| | | Focused | d Condition ' | View | | - |
| Line | 22 | 25 Item | 1 (alu_slt | alu_sl | tu) | |
| Condit | ion tot | tals: 2 of | 2 input term | ms covered | 1 = 100.00% | |
| | | | Reason for | | ge Hint | |
| a. | lu_slt | Y | | | | |
| alı | u_sltu | Y | | | | |
| | | | | | | |
| | | | | | Non-masking | |
| | | | alu_slt_0 | | | |
| | | | alu_slt_1 | | _ | |
| | | | alu_sltu_0 | | ~alu_slt | |
| | | | alu_sltu_1 | | - ~alu_slt | |
| | | | | | | |
| | Fc | cused Cond | dition View | (Bimodal)- | | - |
| Line | 22 | 27 Item | 1 (a[31] ^ | b[31]) | | |
| Condit | ion tot | cals: 2 of | 2 input term | ms covered | = 100.00% | |
| Input | t Term | Covered | Reason for | no covera | ge | Hint |
| | | | | | | |
| | a[31] | | | | | |
| | b[31] | Y | | | | |
| Ro | ws: I | Hits(->0) | Hits(->1) | FEC Targe | et | Non-masking condition(s) |
| | | | | | | |
| Row | 1: | 1 | 0 | a[31]_0 | | - |
| Row | 2: | 0 | 1 | a[31]_1 | | - |
| Row | 3: | 1 | 1 | b[31]_0 | | - |
| Row | 4: | 0 | 1 | b[31]_1 | | - |
| - | | | | - - | | |

------Focused Condition View------

235 Item 1 (alu_eq | alu_neq) Line

Condition totals: 2 of 2 input terms covered = 100.00%

Input Term Covered Reason for no coverage Hint

______ ____

Y alu_eq alu_neq Y

Hits FEC Target Non-masking condition(s)

______ ____

Row 1: $1 alu_eq_0$ ~alu_neq

Row 2: 1 alu_eq_1

Row 3: 1 alu_neq_0 ~alu_eq

1 alu_neq_1 Row 4: ~alu_eq

-----Focused Condition View-----

239 Item 1 (alu_ge || alu_geu) Line

Y

Condition totals: 2 of 2 input terms covered = 100.00%

Input Term Covered Reason for no coverage Hint

alu_ge Y

alu_geu

Rows: Hits FEC Target Non-masking condition(s)

_____ ____

Row 1: 1 alu_ge_0 ~alu_geu

Row 2: 1 alu_ge_1

Row 3: 1 alu_geu_0 ~alu_ge

1 alu_geu_1 Row 4: ~alu_ge

-----Focused Condition View (Bimodal)-----

241 Item 1 (a[31] ^ b[31]) Line

Condition totals: 2 of 2 input terms covered = 100.00%

Input Term Covered Reason for no coverage Hint

a[31] Y b[31] Y

Rows: Hits(->0) Hits(->1) FEC Target Non-masking condition(s)

```
Row 1:
       0
                  1 a[31]_0
Row 2:
              1
                      1 a[31] 1
Row 3:
                      1 b[31]_0
              0
Row 4:
                      0 b[31]_1
              1
------Focused Condition View------
       258 Item 1 (opcode_rtype || opcode_itype)
Condition totals: 2 of 2 input terms covered = 100.00%
  Input Term Covered Reason for no coverage Hint
 opcode rtype
 opcode_itype
               Y
   Rows: Hits FEC Target
                               Non-masking condition(s)
______
 Row 1:
             1 opcode_rtype_0
                              ~opcode_itype
 Row 2:
             1 opcode_rtype_1
 Row 3:
             1 opcode_itype_0
                              ~opcode_rtype
            1 opcode_itype_1
 Row
    4:
                             ~opcode_rtype
------Focused Condition View------
       259 Item 1 (opcode_branch && y_d[0])
Condition totals: 2 of 2 input terms covered = 100.00%
   Input Term Covered Reason for no coverage Hint
   ______ _____
 opcode_branch
               Y
      y_d[0]
               Y
   Rows: Hits FEC Target
                              Non-masking condition(s)
______
             1 opcode_branch_0
 Row 1:
             1 opcode_branch_1
 Row 2:
                             y_d[0]
             1 y_d[0]_0
 Row 3:
                               opcode_branch
    4: 1 y_d[0]_1
                               opcode_branch
 Row
------Focused Condition View------
       266 Item 1 (opcode_jal || opcode_jalr)
Line
```

Condition totals: 2 of 2 input terms covered = 100.00%

```
Input Term Covered Reason for no coverage Hint
  opcode_jal
                 Υ
 opcode_jalr
                Υ
   Rows: Hits FEC Target
                              Non-masking condition(s)
         _____
      1:
                1 opcode_jal_0
 Row
                                   ~opcode_jalr
               1 opcode_jal_1
 Row 2:
               1 opcode_jalr_0
 Row
      3:
                                   ~opcode_jal
               1 opcode_jalr_1
 Row
      4:
                                    ~opcode_jal
-------Focused Condition View------
           280 Item 1 (((opcode_branch || opcode_store) || (opcode_system &&
Line
(i_funct3 == 0))) || opcode_fence)
Condition totals: 4 of 5 input terms covered = 80.00%
     Input Term Covered Reason for no coverage Hint
                   Y
   opcode_branch
   opcode_store
                    Y
   opcode_system
                    Y
 (i_funct3 == 0)
                    N '_0' not hit
                                    Hit '_0'
    opcode_fence
                    Y
                             Non-masking condition(s)
    Rows: Hits FEC Target
 ______ _____
                   1 opcode_branch_0 (~opcode_fence && ~(opcode_system &&
(i_funct3 == 0)) && ~opcode_store)
               1 opcode branch 1
                   1 opcode_store_0 (~opcode_fence && ~(opcode_system &&
(i_funct3 == 0)) && ~opcode_branch)
 Row
               1 opcode_store_1 ~opcode_branch
  Row 5:
                   1 opcode_system_0
                                         (~opcode_fence && ~(opcode_branch | |
opcode_store))
                  1 opcode_system_1
  Row 6:
                                         (~(opcode_branch | opcode_store) &&
(i funct3 == 0))
       7:
             ***0*** (i_funct3 == 0)_0
                                         (~opcode_fence && ~(opcode_branch | |
opcode_store) && opcode_system)
  Row 8:
                                         (~(opcode_branch || opcode_store) &&
                   1 (i_funct3 == 0)_1
opcode_system)
                                          ~((opcode_branch | opcode_store) |
  Row
      9:
                   1 opcode_fence_0
(opcode_system && (i_funct3 == 0)))
                                         ~((opcode_branch || opcode_store) ||
 Row
      10:
                   1 opcode_fence_1
(opcode_system && (i_funct3 == 0)))
```

```
------ View-----Focused Condition View-----
Line
       287 Item 1 (opcode_load | | (opcode_system && (i_funct3 != 0)))
Condition totals: 1 of 3 input terms covered = 33.33%
     Input Term Covered Reason for no coverage Hint
    ______ _____
                 Y
    opcode_load
                 N '_1' not hit
  opcode_system
                                     Hit '_1'
                 N '_1' not hit
 (i_funct3 != 0)
                                     Hit '_1'
          Hits FEC Target
   Rows:
                               Non-masking condition(s)
______ ____
 Row
     1:
              1 opcode_load_0
                                ~(opcode_system && (i_funct3 != 0))
             1 opcode_load_1
 Row
     2:
 Row
     3:
             1 opcode_system_0
                               ~opcode_load
 Row 4: ***0*** opcode_system_1
                               (~opcode_load && (i_funct3 != 0))
 Row
     5:
          1 (i_funct3 != 0)_0
                               (~opcode_load && opcode_system)
     6: ***0*** (i_funct3 != 0)_1 (~opcode_load && opcode_system)
 Row
Expression Coverage:
  Enabled Coverage
                     Bins Covered Misses Coverage
   _____
                               ____
                        ----
                                     _____
                         7 0
                                     7 0.00%
  Expressions
Expression Coverage for Design Unit work.rv32i_alu --
 File rv32i_alu.sv
-----Focused Expression View------
       193 Item 1 (i_opcode[3] | i_opcode[2])
Expression totals: 0 of 2 input terms covered = 0.00%
  Input Term Covered Reason for no coverage Hint
 i_opcode[3]
              N No hits
                                   Hit '_0' and '_1'
 i_opcode[2]
              N No hits
                                   Hit '_0' and '_1'
          Hits FEC Target
   Rows:
                               Non-masking condition(s)
_____
                               ______
         ***0*** i_opcode[3]_0
     1:
 Row
                                ~i opcode[2]
     2: ***0*** i_opcode[3]_1
 Row
         ***0*** i_opcode[2]_0
     3:
 Row
                               ~i_opcode[3]
     4: ***0*** i_opcode[2]_1
 Row
                              ~i_opcode[3]
```

```
Line
       Expression totals: 0 of 3 input terms covered = 0.00%
   Input Term Covered Reason for no coverage Hint
  ______
               N '_1' not hit
     i_stall
                                 Hit '_1'
 i_force_stall
              N '_1' not hit
                                 Hit '_1'
     i_flush
              N No hits
                                 Hit '_0' and '_1'
   Rows: Hits FEC Target
                             Non-masking condition(s)
______
 Row
     1:
             1 i_stall_0
                             ~i_force_stall
     2: ***0*** i_stall_1
                             ~i_flush
 Row
 Row
           1 i_force_stall_0
                             ~i_stall
 Row 4: ***0*** i_force_stall_1
                             (~i_flush && ~i_stall)
 Row
     5:
        ***0*** i_flush_0
                             (i_stall || i_force_stall)
 Row 6: ***0*** i_flush_1
                             (i_stall || i_force_stall)
-----Focused Expression View-----
      299 Item 1 (o_stall | i_stall)
Expression totals: 0 of 2 input terms covered = 0.00%
 Input Term Covered Reason for no coverage Hint
______
   o stall
         N '_1' not hit
                               Hit ' 1'
   i_stall N '_1' not hit
                               Hit '_1'
   Rows: Hits FEC Target
                         Non-masking condition(s)
______ ____
 Row 1:
         1 o_stall_0
                             ~i_stall
 Row 2:
        ***0*** o_stall_1
 Row 3:
         1 i_stall_0
                             ~o stall
 Row 4: ***0*** i_stall_1
                             ~o_stall
Statement Coverage:
                     Bins
                            Hits Misses Coverage
  Enabled Coverage
  _____
                      ----
                            ----
                       65
                             48
                                    17 73.84%
  Statements
```

-----Focused Expression View------

| Line | Item | Count | Source |
|-------------|---------|---------------|--------|
| | | | |
| File rv32i_ | _alu.sv | | |
| 173 | 1 | 1026 | |
| 175 | 1 | 1026 | |
| 176 | 1 | 1026 | |
| 177 | 1 | 1026 | |
| 181 | 1 | * * * 0 * * * | |
| 182 | 1 | * * * 0 * * * | |
| 183 | 1 | * * * 0 * * * | |
| 184 | 1 | * * * 0 * * * | |
| 185 | 1 | * * * 0 * * * | |
| 186 | 1 | * * * 0 * * * | |
| 187 | 1 | * * * 0 * * * | |
| 188 | 1 | * * * 0 * * * | |
| 189 | 1 | * * * 0 * * * | |
| 190 | 1 | * * * 0 * * * | |
| 191 | 1 | * * * 0 * * * | |
| 192 | 1 | * * * 0 * * * | |
| 193 | 1 | * * * 0 * * * | |
| 195 | 1 | * * * 0 * * * | |
| 200 | 1 | * * * 0 * * * | |
| 203 | 1 | * * * 0 * * * | |
| 205 | 1 | * * * 0 * * * | |
| 215 | 1 | 1026 | |
| 216 | 1 | 1026 | |
| 218 | 1 | 1026 | |
| 220 | 1 | 1026 | |
| 223 | 1 | 68 | |
| 224 | 1 | 83 | |
| 226 | 1 | 135 | |
| 227 | 1 | 74 | |
| 229 | 1 | 79 | |
| 230 | 1 | 70 | |
| 231 | 1 | 79 | |
| 232 | 1 | 68 | |
| 233 | 1 | 84 | |
| 234 | 1 | 79 | |
| 236 | 1 | 152 | |
| 237 | 1 | 70 | |
| 240 | 1 | 128 | |
| 241 | 1 | 70 | |
| 248 | 1 | 1193 | |
| 249 | 1 | 1193 | |
| 251 | 1 | 1193 | |
| 252 | 1 | 1193 | |
| | | | |

| 253 | 1 | 1193 |
|-----|---|------|
| 254 | 1 | 1193 |
| 255 | 1 | 1193 |
| 256 | 1 | 1193 |
| 258 | 1 | 232 |
| 260 | 1 | 55 |
| 262 | 1 | 55 |
| 264 | 1 | 55 |
| 267 | 1 | 161 |
| 268 | 1 | 255 |
| 270 | 1 | 255 |
| 272 | 1 | 255 |
| 273 | 1 | 255 |
| 277 | 1 | 81 |
| 278 | 1 | 83 |
| 281 | 1 | 335 |
| 284 | 1 | 858 |
| 288 | 1 | 109 |
| 290 | 1 | 1084 |
| 294 | 1 | 1193 |
| 298 | 1 | 1166 |
| 299 | 1 | 3 |
| | | |

=== Design Unit: work.rv32i_alu_tb

Statement Coverage:

| Enabled Coverage | Bins | Hits | Misses | Coverage |
|------------------|------|------|--------|----------|
| | | | | |
| Statements | 41 | 39 | 2 | 95.12% |

Statement Coverage for Design Unit work.rv32i_alu_tb --

| | Line | Item | Coun | nt Source |
|---|---------------|--------|-------|-----------|
| | | | | |
| F | ile rv32i_alu | ı_tb.s | v | |
| | 98 | 1 | | 1 |
| | 99 | 1 | | 1 |
| | 100 | 1 | | 1 |
| | 152 | 1 | | 1 |
| | 153 | 1 | | 1 |
| | 154 | 1 | 10000 | 12 |
| | 155 | 1 | 10000 | 1 |
| | 161 | 1 | | 1 |
| | | | | |

| TYPE work.cov | erage_sv_unit::cc | overage/alu_cg | 34.84% | 100 | - |
|----------------------|-------------------|----------------|--------|------|------|
| | | | | | |
| | | | | | |
| Scacus | | | | | |
| Covergroup Status | | | Metric | Goal | Bins |
| Covergueur | | | Mahaai | Coo. | D1~- |
| | | | | | |
| COVERGROUP COV | ERAGE: | | | | |
| 249 | 1 | ***0*** | | | |
| 248 | 1 | ***0*** | | | |
| 247 | 1 | 1 | | | |
| 242 | 2 | 1 | | | |
| 242 | 1 | 1 | | | |
| 200 | 1 | 1 | | | |
| 197 | 1 | 1 | | | |
| 196 | 1 | 1 | | | |
| 195 | 1 | 1 | | | |
| 194 | 1 | 1 | | | |
| 193 | 1 | 1 | | | |
| 192 | 1 | 1 | | | |
| 186 | 1 | 1 | | | |
| 185 | 1 | 1 | | | |
| 184 | 1 | 1 | | | |
| 183 | 1 | 1 | | | |
| 182 | 1 | 1 | | | |
| 181 | 1 | 1 | | | |
| 176 | 1 | 1 | | | |
| 175 | 1 | 1 | | | |
| 174 | 1 | 1 | | | |
| 173 | 1 | 1 | | | |
| 172 | 1 | 1 | | | |
| 171 | 1 | 1 | | | |
| 170 | 1 | 1 | | | |
| 169 | 1 | 1 | | | |
| 168 | 1 | 1 | | | |
| 167 | 1 | 1 | | | |
| 166 | 1 | 1 | | | |
| 165 | 1 | 1 | | | |
| 164 | 1 | 1 | | | |
| 163 | 1 | 1 | | | |
| 162 | 1 | 1 | | | |
| | | | | | |

77

5315

Uncovered

covered/total bins:

| mis | sing/total bins: | 5238 | 5315 | - |
|--------------|----------------------------------|--------|------|---|
| % H: | it: | 1.44% | 100 | - |
| type | e_option.weight=1 | | | |
| | e_option.goal=100 | | | |
| | e_option.comment= | | | |
| | e_option.strobe=0 | | | |
| | e_option.merge_instances=auto(1) | | | |
| | erpoint #coverpoint0# | 45.45% | 100 | _ |
| Uncovere | | 10,100 | 200 | |
| 01100 (01 | covered/total bins: | 5 | 11 | - |
| | missing/total bins: | 6 | 11 | - |
| | % Hit: | 45.45% | 100 | _ |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | <pre>bin opcode_types[0]</pre> | 78 | 1 | - |
| Covered | | | | |
| | bin opcode_types[1] | 103 | 1 | - |
| Covered | | | | |
| _ | bin opcode_types[2] | 82 | 1 | _ |
| Covered | | _ | | |
| | <pre>bin opcode_types[3]</pre> | 0 | 1 | _ |
| ZERO | | | | |
| | bin opcode_types[4] | 90 | 1 | _ |
| Covered | 1 | 2 | 1 | |
| 7700 | bin opcode_types[5] | 0 | 1 | _ |
| ZERO | | 2 | 1 | |
| ZED O | <pre>bin opcode_types[6]</pre> | 0 | 1 | _ |
| ZERO | hin anada tamas[7] | 0 | 1 | |
| ZED O | bin opcode_types[7] | 0 | 1 | _ |
| ZERO | bin opcode_types[8] | 79 | 1 | |
| Covered | DIN Opcode_types[0] | 19 | 1 | _ |
| covered | bin opcode_types[9] | 0 | 1 | _ |
| ZERO | pri obcode_cybes[3] | U | 1 | _ |
| ZERU | bin opcode_types[10] | 0 | 1 | _ |
| ZERO | pri obcode_clbes[10] | U | Τ. | _ |
| | erpoint #coverpoint1# | 28.57% | 100 | _ |
| Uncover | | 20.376 | 100 | |
| 01100 4 61 6 | covered/total bins: | 4 | 14 | _ |
| | | - | | |

| | missing/total bins: | 10 | 14 | - |
|---------|---|---------|-----|---|
| | % Hit: | 28.57% | 100 | _ |
| | <pre>type_option.weight=1 type_option.goal=100 type_option.comment=</pre> | | | |
| | bin alu_ops[0] | 0 | 1 | - |
| ZERO | bin alu_ops[1] | 60 | 1 | - |
| Covered | bin alu_ops[2] | 71 | 1 | - |
| ZERO | bin alu_ops[3] | 0 | 1 | - |
| Covered | bin alu_ops[4] | 64 | 1 | - |
| ZERO | bin alu_ops[5] | 0 | 1 | - |
| ZERO | bin alu_ops[6] | 0 | 1 | - |
| ZERO | bin alu_ops[7] | 0 | 1 | - |
| Covered | bin alu_ops[8] | 58 | 1 | - |
| ZERO | bin alu_ops[9] | 0 | 1 | - |
| ZERO | bin alu_ops[10] | 0 | 1 | - |
| ZERO | bin alu_ops[11] | 0 | 1 | - |
| ZERO | bin alu_ops[12] | 0 | 1 | - |
| ZERO | bin alu_ops[13] | 0 | 1 | - |
| | erpoint #coverpoint2# | 100.00% | 100 | - |
| COVCIEU | covered/total bins: | 2 | 2 | - |
| | missing/total bins: | 0 | 2 | _ |
| | % Hit: | 100.00% | 100 | _ |
| | <pre>type_option.weight=1</pre> | | | |

type_option.goal=100

| | type_option.comment= | | | |
|--------|------------------------|---------|-----|---|
| | bin auto[0] | 714 | 1 | - |
| Covere | d | | | |
| | bin auto[1] | 200 | 1 | - |
| Covere | d | | | |
| Со | verpoint #coverpoint3# | 100.00% | 100 | _ |
| Covere | | | | |
| | covered/total bins: | 1 | 1 | _ |
| | 2010200, 00002 22122 | _ | _ | |
| | missing/total bins: | 0 | 1 | _ |
| | missing/total bins: | U | 1 | |
| | % Hit: | 100.00% | 100 | |
| | 6 HIL. | 100.00% | 100 | _ |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin pc_values | 914 | 1 | - |
| Covere | d | | | |
| Со | verpoint #coverpoint4# | 0.00% | 100 | - |
| ZERO | | | | |
| | covered/total bins: | 0 | 2 | _ |
| | | | | |
| | missing/total bins: | 2 | 2 | _ |
| | _ | | | |
| | % Hit: | 0.00% | 100 | _ |
| | | 0.000 | 100 | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[1] | 0 | 1 | - |
| ZERO | | | | |
| Со | verpoint #coverpoint5# | 0.00% | 100 | - |
| ZERO | | | | |
| | covered/total bins: | 0 | 2 | _ |
| | | | | |
| | missing/total bins: | 2 | 2 | _ |
| | 3. | | | |
| | % Hit: | 0.00% | 100 | _ |
| | . 1116. | 0.000 | 100 | |
| | type_option.weight=1 | | | |
| | | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 0 | 1 | - |
| ZERO | | | | |

| | bin auto[1] | 0 | 1 | - |
|---------|--|--------|-----|--------------|
| ZERO | | | | |
| | erpoint #coverpoint6# | 0.00% | 100 | _ |
| ZERO | 10 | 0 | 1 | |
| | covered/total bins: | 0 | 1 | _ |
| | missing/total bins: | 1 | 1 | _ |
| | | | | |
| | % Hit: | 0.00% | 100 | _ |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin rd_addr | 0 | 1 | _ |
| ZERO | | | | |
| | rerpoint #coverpoint7# | 50.00% | 100 | _ |
| Uncover | | | _ | |
| | covered/total bins: | 1 | 2 | _ |
| | missing/total bins: | 1 | 2 | _ |
| | missing/total bins. | 1 | ۷ | |
| | % Hit: | 50.00% | 100 | - |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 0 | 1 | - |
| ZERO | | | | |
| | bin auto[1] | 914 | 1 | - |
| Covered | | | | |
| Cov | rerpoint #coverpoint8# | 50.00% | 100 | - |
| Uncover | ed | | | |
| | covered/total bins: | 1 | 2 | - |
| | missing/total bins: | 1 | 2 | _ |
| | 2 | | | |
| | % Hit: | 50.00% | 100 | - |
| | type_option.weight=1 | | | |
| | | | | |
| | <pre>type_option.goal=100 type_option.comment=</pre> | | | |
| | bin auto[0] | 914 | 1 | |
| Covered | | 914 | 1 | - |
| covered | bin auto[1] | 0 | 1 | _ |
| ZERO | 211 4460[1] | O | 1 | |
| | rerpoint #coverpoint9# | 50.00% | 100 | _ |
| COV | <u>στροτιίο</u> πουνοτροτιίο <u></u> νπ | 30.00% | 100 | |

| 01100 1 01 | | | | |
|------------|-------------------------|--------|-----|---|
| | covered/total bins: | 1 | 2 | - |
| | missing/total bins: | 1 | 2 | - |
| | % Hit: | 50.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 914 | 1 | _ |
| Covered | | | | |
| | bin auto[1] | 0 | 1 | _ |
| ZERO | | | | |
| | verpoint #coverpoint10# | 50.00% | 100 | _ |
| Uncover | | | | |
| | covered/total bins: | 1 | 2 | _ |
| | | | | |
| | missing/total bins: | 1 | 2 | _ |
| | 5. | | | |
| | % Hit: | 50.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 914 | 1 | - |
| Covered | i | | | |
| | bin auto[1] | 0 | 1 | - |
| ZERO | | | | |
| Cor | verpoint #coverpoint11# | 50.00% | 100 | - |
| Uncover | red | | | |
| | covered/total bins: | 1 | 2 | - |
| | | | | |
| | missing/total bins: | 1 | 2 | - |
| | | | | |
| | % Hit: | 50.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 914 | 1 | _ |
| Covered | i | | | |
| | bin auto[1] | 0 | 1 | - |
| ZERO | | | | |
| Cor | verpoint #coverpoint12# | 50.00% | 100 | - |
| Uncover | red | | | |
| | | | | |

| | covered/total bins: | 1 | 2 | - |
|---------|-------------------------|---------|-----|---|
| | missing/total bins: | 1 | 2 | - |
| | % Hit: | 50.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 914 | 1 | _ |
| Covered | | | | |
| | bin auto[1] | 0 | 1 | - |
| ZERO | | | | |
| Cov | rerpoint #coverpoint13# | 100.00% | 100 | |
| Covered | | | | |
| | covered/total bins: | 2 | 2 | - |
| | | | | |
| | missing/total bins: | 0 | 2 | - |
| | % Hit: | 100.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 714 | 1 | _ |
| Covered | | | | |
| | bin auto[1] | 200 | 1 | - |
| Covered | | | | |
| Cov | erpoint #coverpoint14# | 0.00% | 100 | _ |
| ZERO | | | | |
| | covered/total bins: | 0 | 4 | _ |
| | missing/total bins: | 4 | 4 | - |
| | % Hit: | 0.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin exceptions[0] | 0 | 1 | - |
| ZERO | | | | |
| | bin exceptions[1] | 0 | 1 | - |
| ZERO | | | | |
| | bin exceptions[2] | 0 | 1 | _ |
| ZERO | | | | |
| | bin exceptions[3] | 0 | 1 | - |

| ZERO | | | |
|-----------------------------|--------|-----|---|
| Coverpoint #vif.i_opcode15# | 10.93% | 100 | - |
| Uncovered | | | |
| covered/total bins: | 7 | 64 | - |
| | | | |
| missing/total bins: | 57 | 64 | - |
| | | | |
| % Hit: | 10.93% | 100 | _ |
| | | | |
| type_option.weight=1 | | | |
| type_option.goal=100 | | | |
| type_option.comment= | | | |
| | 527 | 1 | |
| bin auto[0:31] | 547 | 1 | _ |
| Covered | | _ | |
| bin auto[32:63] | 81 | 1 | _ |
| Covered | | | |
| bin auto[64:95] | 73 | 1 | _ |
| Covered | | | |
| bin auto[96:127] | 0 | 1 | _ |
| ZERO | | | |
| bin auto[128:159] | 70 | 1 | _ |
| Covered | | | |
| bin auto[160:191] | 0 | 1 | _ |
| ZERO | | | |
| bin auto[192:223] | 0 | 1 | _ |
| ZERO | | | |
| bin auto[224:255] | 0 | 1 | _ |
| ZERO | · · | _ | |
| bin auto[256:287] | 67 | 1 | |
| Covered | 07 | 1 | _ |
| | • | - | |
| bin auto[288:319] | 0 | 1 | _ |
| ZERO | | | |
| bin auto[320:351] | 0 | 1 | _ |
| ZERO | | | |
| bin auto[352:383] | 0 | 1 | - |
| ZERO | | | |
| bin auto[384:415] | 0 | 1 | _ |
| ZERO | | | |
| bin auto[416:447] | 0 | 1 | _ |
| ZERO | | | |
| bin auto[448:479] | 0 | 1 | _ |
| ZERO | | | |
| bin auto[480:511] | 0 | 1 | _ |
| ZERO ZERO | Ŭ | _ | |
| bin auto[512:543] | 95 | 1 | |
| | 90 | 1 | _ |
| Covered | | | |

| ZERO | bin auto[544:575] | 0 | 1 | - |
|---------|---------------------|---|---|---|
| ZERO | bin auto[576:607] | 0 | 1 | - |
| ZERO | bin auto[608:639] | 0 | 1 | - |
| ZERO | bin auto[640:671] | 0 | 1 | - |
| ZERO | bin auto[672:703] | 0 | 1 | - |
| ZERO | bin auto[704:735] | 0 | 1 | - |
| ZERO | bin auto[736:767] | 0 | 1 | - |
| ZERO | bin auto[768:799] | 0 | 1 | - |
| ZERO | bin auto[800:831] | 0 | 1 | - |
| ZERO | bin auto[832:863] | 0 | 1 | - |
| ZERO | bin auto[864:895] | 0 | 1 | - |
| ZERO | bin auto[896:927] | 0 | 1 | - |
| | bin auto[928:959] | 0 | 1 | - |
| ZERO | bin auto[960:991] | 0 | 1 | - |
| ZERO | bin auto[992:1023] | 0 | 1 | - |
| ZERO | bin auto[1024:1055] | 1 | 1 | - |
| Covered | bin auto[1056:1087] | 0 | 1 | - |
| ZERO | bin auto[1088:1119] | 0 | 1 | - |
| ZERO | bin auto[1120:1151] | 0 | 1 | _ |
| ZERO | bin auto[1152:1183] | 0 | 1 | _ |
| ZERO | bin auto[1184:1215] | 0 | 1 | - |
| ZERO | bin auto[1216:1247] | 0 | 1 | _ |
| ZERO | bin auto[1248:1279] | 0 | 1 | - |
| ZERO | | | | |

| ZERO | bin auto[1280:1311] | 0 | 1 | - |
|------|---------------------|---|---|---|
| ZERO | bin auto[1312:1343] | 0 | 1 | - |
| | bin auto[1344:1375] | 0 | 1 | - |
| ZERO | bin auto[1376:1407] | 0 | 1 | - |
| ZERO | bin auto[1408:1439] | 0 | 1 | - |
| ZERO | bin auto[1440:1471] | 0 | 1 | - |
| ZERO | bin auto[1472:1503] | 0 | 1 | - |
| ZERO | bin auto[1504:1535] | 0 | 1 | - |
| ZERO | bin auto[1536:1567] | 0 | 1 | - |
| ZERO | bin auto[1568:1599] | 0 | 1 | - |
| ZERO | bin auto[1600:1631] | 0 | 1 | - |
| ZERO | bin auto[1632:1663] | 0 | 1 | _ |
| ZERO | bin auto[1664:1695] | 0 | 1 | - |
| ZERO | bin auto[1696:1727] | 0 | 1 | - |
| ZERO | bin auto[1728:1759] | 0 | 1 | - |
| ZERO | bin auto[1760:1791] | 0 | 1 | _ |
| ZERO | bin auto[1792:1823] | 0 | 1 | _ |
| ZERO | bin auto[1824:1855] | 0 | 1 | - |
| ZERO | bin auto[1856:1887] | 0 | 1 | _ |
| ZERO | bin auto[1888:1919] | 0 | 1 | _ |
| ZERO | bin auto[1920:1951] | 0 | 1 | _ |
| ZERO | bin auto[1952:1983] | 0 | 1 | _ |
| ZERO | bin auto[1984:2015] | 0 | 1 | _ |
| ZERO | | | | |

| 77D0 | bin auto[2016:2047] | 0 | 1 | - |
|------------|------------------------------|--------|-----|---|
| ZERO Co | verpoint #vif.i_exception16# | 0.00% | 100 | _ |
| ZERO | <u> </u> | | | |
| | covered/total bins: | 0 | 16 | - |
| | missing/total bins: | 16 | 16 | _ |
| | % Hit: | 0.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[1] | 0 | 1 | |
| ZERO | | | | |
| | bin auto[2] | 0 | 1 | _ |
| ZERO | | - | _ | |
| 2210 | bin auto[3] | 0 | 1 | _ |
| ZERO | Sin duco[5] | · · | _ | |
| ZEKO | bin auto[4] | 0 | 1 | |
| ZED O | DIN auto[4] | U | Т | _ |
| ZERO | | | - | |
| | bin auto[5] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[6] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[7] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[8] | 0 | 1 | - |
| ZERO | | | | |
| | bin auto[9] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[10] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[11] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[12] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[13] | 0 | 1 | _ |
| ZERO | 211 0000(10) | Č | _ | |
| ZLICO | bin auto[14] | 0 | 1 | _ |
| ZERO | Din auco[if] | U | T | _ |
| LEKU | bin auto[15] | 0 | 1 | |
| ZED C | Din auco[13] | U | 1 | _ |
| ZERO | rownsint Herif i al. 170 | 10 000 | 100 | |
| Co | verpoint #vif.i_alu17# | 10.93% | 100 | _ |

| | covered/total bins: | 7 | 64 | - |
|-----------------|---|-----------|-----|---|
| | missing/total bins: | 57 | 64 | - |
| | % Hit: | 10.93% | 100 | - |
| | <pre>type_option.weight=1 type_option.goal=100 type_option.comment=</pre> | | | |
| Covered | <pre>bin auto[0:255] bin auto[256:511]</pre> | 520 77 | 1 | _ |
| Covered | | 73 | 1 | - |
| Covered | bin auto[768:1023] | 0 | 1 | - |
| ZERO Covered | bin auto[1024:1279] | 70 | 1 | - |
| ZERO | bin auto[1280:1535] | 0 | 1 | - |
| ZERO | <pre>bin auto[1536:1791] bin auto[1792:2047]</pre> | 0 | 1 | _ |
| ZERO | bin auto[2048:2303] | 62 | 1 | - |
| Covered | bin auto[2304:2559] | 0 | 1 | - |
| ZERO ZERO | bin auto[2560:2815] | 0 | 1 | - |
| ZERO | bin auto[2816:3071] | 0 | 1 | - |
| ZERO | <pre>bin auto[3072:3327] bin auto[3328:3583]</pre> | 0 | 1 | - |
| ZERO | bin auto[3584:3839] | 0 | 1 | - |
| ZERO | bin auto[3840:4095] | 0 | 1 | - |
| ZERO Covered | bin auto[4096:4351] | 56 | 1 | - |
| ZERO | bin auto[4352:4607] | 0 | 1 | - |

| ZERO | bin auto[4608:4863] | 0 | 1 | - |
|---------|-----------------------|----|---|---|
| ZERO | bin auto[4864:5119] | 0 | 1 | - |
| | bin auto[5120:5375] | 0 | 1 | - |
| ZERO | bin auto[5376:5631] | 0 | 1 | - |
| ZERO | bin auto[5632:5887] | 0 | 1 | - |
| ZERO | bin auto[5888:6143] | 0 | 1 | - |
| ZERO | bin auto[6144:6399] | 0 | 1 | - |
| ZERO | bin auto[6400:6655] | 0 | 1 | - |
| ZERO | bin auto[6656:6911] | 0 | 1 | _ |
| ZERO | bin auto[6912:7167] | 0 | 1 | - |
| ZERO | bin auto[7168:7423] | 0 | 1 | - |
| ZERO | bin auto[7424:7679] | 0 | 1 | - |
| ZERO | bin auto[7680:7935] | 0 | 1 | - |
| ZERO | bin auto[7936:8191] | 0 | 1 | - |
| ZERO | bin auto[8192:8447] | 56 | 1 | _ |
| Covered | bin auto[8448:8703] | 0 | 1 | - |
| ZERO | bin auto[8704:8959] | 0 | 1 | _ |
| ZERO | bin auto[8960:9215] | 0 | 1 | _ |
| ZERO | bin auto[9216:9471] | 0 | 1 | _ |
| ZERO | bin auto[9472:9727] | 0 | 1 | _ |
| ZERO | bin auto[9728:9983] | 0 | 1 | _ |
| ZERO | bin auto[9984:10239] | 0 | 1 | _ |
| ZERO | bin auto[10240:10495] | 0 | 1 | _ |
| ZERO | | - | | |

| ZERO | bin auto[10496:10751] | 0 | 1 | - |
|------|-----------------------|---|---|---|
| ZERO | bin auto[10752:11007] | 0 | 1 | - |
| ZERO | bin auto[11008:11263] | 0 | 1 | - |
| ZERO | bin auto[11264:11519] | 0 | 1 | - |
| ZERO | bin auto[11520:11775] | 0 | 1 | - |
| ZERO | bin auto[11776:12031] | 0 | 1 | - |
| ZERO | bin auto[12032:12287] | 0 | 1 | - |
| ZERO | bin auto[12288:12543] | 0 | 1 | - |
| ZERO | bin auto[12544:12799] | 0 | 1 | - |
| ZERO | bin auto[12800:13055] | 0 | 1 | - |
| ZERO | bin auto[13056:13311] | 0 | 1 | - |
| ZERO | bin auto[13312:13567] | 0 | 1 | - |
| ZERO | bin auto[13568:13823] | 0 | 1 | - |
| ZERO | bin auto[13824:14079] | 0 | 1 | - |
| ZERO | bin auto[14080:14335] | 0 | 1 | - |
| ZERO | bin auto[14336:14591] | 0 | 1 | - |
| ZERO | bin auto[14592:14847] | 0 | 1 | - |
| ZERO | bin auto[14848:15103] | 0 | 1 | - |
| ZERO | bin auto[15104:15359] | 0 | 1 | - |
| ZERO | bin auto[15360:15615] | 0 | 1 | - |
| ZERO | bin auto[15616:15871] | 0 | 1 | - |
| ZERO | bin auto[15872:16127] | 0 | 1 | - |
| ZERO | bin auto[16128:16383] | 0 | 1 | - |
| | | | | |

| Cross #cross0# | 1.04% | 100 | - |
|--|-------|------|---|
| Uncovered covered/total bins: | 43 | 4096 | _ |
| missing/total bins: | 4053 | 4096 | - |
| % Hit: | 1.04% | 100 | - |
| <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[512:543],auto[8192:8447]> Covered bin <auto[256:287],auto[8192:8447]></auto[256:287],auto[8192:8447]></auto[512:543],auto[8192:8447]></pre> | 5 | 1 | - |
| Covered bin <auto[128:159],auto[8192:8447]> Covered</auto[128:159],auto[8192:8447]> | 3 | 1 | - |
| bin <auto[64:95],auto[8192:8447]> Covered</auto[64:95],auto[8192:8447]> | 7 | 1 | - |
| <pre>bin <auto[32:63],auto[8192:8447]> Covered</auto[32:63],auto[8192:8447]></pre> | 7 | 1 | - |
| <pre>bin <auto[0:31],auto[8192:8447]> Covered</auto[0:31],auto[8192:8447]></pre> | 31 | 1 | - |
| <pre>bin <auto[512:543],auto[4096:4351]> Covered</auto[512:543],auto[4096:4351]></pre> | 3 | 1 | - |
| bin <auto[256:287],auto[4096:4351]> Covered</auto[256:287],auto[4096:4351]> | 2 | 1 | - |
| <pre>bin <auto[128:159],auto[4096:4351]> Covered bin <auto[64:95],auto[4096:4351]></auto[64:95],auto[4096:4351]></auto[128:159],auto[4096:4351]></pre> | 3 | 1 | - |
| Covered bin <auto[32:63],auto[4096:4351]></auto[32:63],auto[4096:4351]> | 7 | 1 | _ |
| Covered bin <auto[0:31],auto[4096:4351]></auto[0:31],auto[4096:4351]> | 39 | 1 | _ |
| Covered bin <auto[512:543],auto[2048:2303]></auto[512:543],auto[2048:2303]> | 3 | 1 | _ |
| Covered bin <auto[256:287],auto[2048:2303]></auto[256:287],auto[2048:2303]> | 4 | 1 | - |
| Covered bin <auto[128:159],auto[2048:2303]></auto[128:159],auto[2048:2303]> | 11 | 1 | - |
| Covered bin <auto[64:95],auto[2048:2303]></auto[64:95],auto[2048:2303]> | 3 | 1 | - |
| Covered bin <auto[32:63],auto[2048:2303]> Covered</auto[32:63],auto[2048:2303]> | 3 | 1 | - |

| Covered | bin <auto[0:31],auto[2048:2303]></auto[0:31],auto[2048:2303]> | 38 | 1 | - |
|---------|--|----|---|---|
| Covered | bin <auto[512:543],auto[1024:1279]></auto[512:543],auto[1024:1279]> | 4 | 1 | - |
| Covered | bin <auto[256:287],auto[1024:1279]></auto[256:287],auto[1024:1279]> | 6 | 1 | - |
| Covered | bin <auto[128:159],auto[1024:1279]></auto[128:159],auto[1024:1279]> | 6 | 1 | - |
| Covered | bin <auto[64:95],auto[1024:1279]></auto[64:95],auto[1024:1279]> | 10 | 1 | - |
| Covered | bin <auto[32:63],auto[1024:1279]></auto[32:63],auto[1024:1279]> | 9 | 1 | - |
| Covered | bin <auto[0:31],auto[1024:1279]></auto[0:31],auto[1024:1279]> | 35 | 1 | - |
| Covered | bin <auto[512:543],auto[512:767]></auto[512:543],auto[512:767]> | 8 | 1 | - |
| Covered | bin <auto[256:287],auto[512:767]></auto[256:287],auto[512:767]> | 7 | 1 | - |
| Covered | bin <auto[128:159],auto[512:767]></auto[128:159],auto[512:767]> | 7 | 1 | - |
| Covered | bin <auto[64:95],auto[512:767]></auto[64:95],auto[512:767]> | 2 | 1 | - |
| Covered | bin <auto[32:63],auto[512:767]></auto[32:63],auto[512:767]> | 5 | 1 | - |
| Covered | bin <auto[0:31],auto[512:767]></auto[0:31],auto[512:767]> | 44 | 1 | - |
| Covered | bin <auto[512:543],auto[256:511]></auto[512:543],auto[256:511]> | 8 | 1 | - |
| Covered | bin <auto[256:287],auto[256:511]></auto[256:287],auto[256:511]> | 8 | 1 | - |
| Covered | bin <auto[128:159],auto[256:511]></auto[128:159],auto[256:511]> | 7 | 1 | - |
| Covered | bin <auto[64:95],auto[256:511]></auto[64:95],auto[256:511]> | 6 | 1 | - |
| Covered | bin <auto[32:63],auto[256:511]></auto[32:63],auto[256:511]> | 4 | 1 | - |
| Covered | <pre>bin <auto[0:31],auto[256:511]></auto[0:31],auto[256:511]></pre> | 44 | 1 | - |
| Covered | bin <auto[1024:1055],auto[0:255]></auto[1024:1055],auto[0:255]> | 1 | 1 | - |
| Covered | bin <auto[512:543],auto[0:255]></auto[512:543],auto[0:255]> | 64 | 1 | - |
| Covered | bin <auto[256:287],auto[0:255]></auto[256:287],auto[0:255]> | 37 | 1 | - |
| Covered | bin <auto[128:159],auto[0:255]></auto[128:159],auto[0:255]> | 33 | 1 | - |

| Covered | bin <auto[64:95],auto[0:255]></auto[64:95],auto[0:255]> | 43 | 1 | - |
|---------|---|-----|---|----|
| Covered | bin <auto[32:63],auto[0:255]></auto[32:63],auto[0:255]> | 46 | 1 | - |
| Covered | bin <auto[0:31],auto[0:255]></auto[0:31],auto[0:255]> | 296 | 1 | - |
| ZERO | bin <auto[2016:2047],*></auto[2016:2047],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1984:2015],*></auto[1984:2015],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1952:1983],*></auto[1952:1983],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1920:1951],*></auto[1920:1951],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1888:1919],*></auto[1888:1919],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1856:1887],*></auto[1856:1887],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1824:1855],*></auto[1824:1855],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1792:1823],*></auto[1792:1823],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1760:1791],*></auto[1760:1791],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1728:1759],*></auto[1728:1759],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1696:1727],*></auto[1696:1727],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1664:1695],*></auto[1664:1695],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1632:1663],*></auto[1632:1663],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1600:1631],*></auto[1600:1631],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1568:1599],*></auto[1568:1599],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1536:1567],*></auto[1536:1567],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1504:1535],*></auto[1504:1535],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1472:1503],*></auto[1472:1503],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1440:1471],*></auto[1440:1471],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1408:1439],*></auto[1408:1439],*> | 0 | 1 | 64 |
| | | | | |

| ZERO | bin <auto[1376:1407],*></auto[1376:1407],*> | 0 | 1 | 64 |
|------|---|---|---|----|
| ZERO | bin <auto[1344:1375],*></auto[1344:1375],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1312:1343],*></auto[1312:1343],*> | 0 | 1 | 64 |
| | bin <auto[1280:1311],*></auto[1280:1311],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1248:1279],*></auto[1248:1279],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1216:1247],*></auto[1216:1247],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1184:1215],*></auto[1184:1215],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1152:1183],*></auto[1152:1183],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1120:1151],*></auto[1120:1151],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1088:1119],*></auto[1088:1119],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1056:1087],*></auto[1056:1087],*> | 0 | 1 | 64 |
| ZERO | bin <auto[992:1023],*></auto[992:1023],*> | 0 | 1 | 64 |
| ZERO | bin <auto[960:991],*></auto[960:991],*> | 0 | 1 | 64 |
| ZERO | bin <auto[928:959],*></auto[928:959],*> | 0 | 1 | 64 |
| ZERO | bin <auto[896:927],*></auto[896:927],*> | 0 | 1 | 64 |
| ZERO | bin <auto[864:895],*></auto[864:895],*> | 0 | 1 | 64 |
| ZERO | bin <auto[832:863],*></auto[832:863],*> | 0 | 1 | 64 |
| ZERO | bin <auto[800:831],*></auto[800:831],*> | 0 | 1 | 64 |
| ZERO | bin <auto[768:799],*></auto[768:799],*> | 0 | 1 | 64 |
| ZERO | bin <auto[736:767],*></auto[736:767],*> | 0 | 1 | 64 |
| ZERO | bin <auto[704:735],*></auto[704:735],*> | 0 | 1 | 64 |
| ZERO | bin <auto[672:703],*></auto[672:703],*> | 0 | 1 | 64 |
| ZERO | bin <auto[640:671],*></auto[640:671],*> | 0 | 1 | 64 |
| ZERO | | | | |

| ZERO | bin <auto[608:639],*></auto[608:639],*> | 0 | 1 | 64 |
|------|---|---|---|----|
| ZERO | bin <auto[576:607],*></auto[576:607],*> | 0 | 1 | 64 |
| ZERO | bin <auto[544:575],*></auto[544:575],*> | 0 | 1 | 64 |
| | bin <auto[480:511],*></auto[480:511],*> | 0 | 1 | 64 |
| ZERO | bin <auto[448:479],*></auto[448:479],*> | 0 | 1 | 64 |
| ZERO | bin <auto[416:447],*></auto[416:447],*> | 0 | 1 | 64 |
| ZERO | bin <auto[384:415],*></auto[384:415],*> | 0 | 1 | 64 |
| ZERO | bin <auto[352:383],*></auto[352:383],*> | 0 | 1 | 64 |
| ZERO | bin <auto[320:351],*></auto[320:351],*> | 0 | 1 | 64 |
| ZERO | bin <auto[288:319],*></auto[288:319],*> | 0 | 1 | 64 |
| ZERO | bin <auto[224:255],*></auto[224:255],*> | 0 | 1 | 64 |
| ZERO | bin <auto[192:223],*></auto[192:223],*> | 0 | 1 | 64 |
| ZERO | bin <auto[160:191],*></auto[160:191],*> | 0 | 1 | 64 |
| ZERO | bin <auto[96:127],*></auto[96:127],*> | 0 | 1 | 64 |
| ZERO | bin <*,auto[16128:16383]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[15872:16127]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[15616:15871]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[15360:15615]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[15104:15359]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[14848:15103]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[14592:14847]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[14336:14591]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[14080:14335]> | 0 | 1 | 64 |
| ZERO | | | | |

| ZIDO | bin <*,auto[13824:14079]> | 0 | 1 | 64 |
|--------------|---------------------------|---|---|----|
| ZERO ZERO | bin <*,auto[13568:13823]> | 0 | 1 | 64 |
| | bin <*,auto[13312:13567]> | 0 | 1 | 64 |
| ZERO ZERO | bin <*,auto[13056:13311]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[12800:13055]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[12544:12799]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[12288:12543]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[12032:12287]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[11776:12031]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[11520:11775]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[11264:11519]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[11008:11263]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[10752:11007]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[10496:10751]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[10240:10495]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[9984:10239]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[9728:9983]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[9472:9727]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[9216:9471]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[8960:9215]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[8704:8959]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[8448:8703]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[7936:8191]> | 0 | 1 | 64 |
| ZERO | | | | |

| ZEDO | bin <*,auto[7680:7935]> | 0 | 1 | 64 |
|--------------|-------------------------|---|---|----|
| ZERO ZERO | bin <*,auto[7424:7679]> | 0 | 1 | 64 |
| | bin <*,auto[7168:7423]> | 0 | 1 | 64 |
| ZERO ZERO | bin <*,auto[6912:7167]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[6656:6911]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[6400:6655]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[6144:6399]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[5888:6143]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[5632:5887]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[5376:5631]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[5120:5375]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[4864:5119]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[4608:4863]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[4352:4607]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[3840:4095]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[3584:3839]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[3328:3583]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[3072:3327]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[2816:3071]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[2560:2815]> | 0 | 1 | 64 |
| | bin <*,auto[2304:2559]> | 0 | 1 | 64 |
| ZERO ZERO | bin <*,auto[1792:2047]> | 0 | 1 | 64 |
| | bin <*,auto[1536:1791]> | 0 | 1 | 64 |
| ZERO | | | | |

| | bin <*,auto[1280:1535]> | 0 | 1 | 64 |
|------|---|-------|------|------|
| ZERO | | | | |
| | bin <*,auto[768:1023]> | 0 | 1 | 64 |
| ZERO | | | | _ |
| ZEDO | bin <auto[1024:1055],auto[8192:8447]></auto[1024:1055],auto[8192:8447]> | 0 | 1 | 1 |
| ZERO | bin <auto[1024:1055],auto[4096:4351]></auto[1024:1055],auto[4096:4351]> | 0 | 1 | 1 |
| ZERO | | | | |
| | bin <auto[1024:1055],auto[2048:2303]></auto[1024:1055],auto[2048:2303]> | 0 | 1 | 1 |
| ZERO | | | | |
| | bin <auto[1024:1055],auto[1024:1279]></auto[1024:1055],auto[1024:1279]> | 0 | 1 | 1 |
| ZERO | bin <auto[1024:1055],auto[512:767]></auto[1024:1055],auto[512:767]> | 0 | 1 | 1 |
| ZERO | DIN (auto[1024.1035],auto[512.707]> | O | 1 | Τ. |
| | bin <auto[1024:1055],auto[256:511]></auto[1024:1055],auto[256:511]> | 0 | 1 | 1 |
| ZERO | | | | |
| Cros | ss #cross1# | 0.00% | 100 | - |
| ZERO | | | | |
| | covered/total bins: | 0 | 1024 | _ |
| | missing/total bins: | 1024 | 1024 | _ |
| | | | | |
| | % Hit: | 0.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | Auto, Default and User Defined Bins: | | | |
| | bin <*,*> | 0 | 1 | 1024 |

ZERO

TOTAL COVERGROUP COVERAGE: 34.84% COVERGROUP TYPES: 1

Total Coverage By Design Unit (filtered view): 41.08%

File: report_50.txt

| | =========== | :========= | | ======= | ======================================= |
|----------------|-------------------|-------------------|---------|---------|---|
| == Design U | nit: work.covera | | | | |
| anch Cover | ========= age: | :======== | ===== | ====== | ========== |
| Enabled | | Bins | | | |
| Branches | | 145 | | | |
| -====== | | ====Branch Detai | ils==== | ====== | |
| ranch Cover | age for Design (| Jnit work.coverag | ge_sv_u | nit | |
| Line | Item | C | Count | Source | |
| File trans | | - | | | |
| | | CASE Bra | anch | | |
| 224 | | 0.152 520 | | | coming in to CASE |
| 225 | 1 | | 12 | | |
| 227 | 1 | | 6 | | |
| 229 | 1 | | 2 | | |
| 231 | 1 | | 3 | | |
| 233 | 1 | | 6 | | |
| 235 | 1 | | 9 | | |
| 237 | 1 | | 4 | | |
| 239 | 1 | | 5 | | |
| 242 | 1 | | 9 | | |
| 244 | 1 | | 6 | | |
| 245 | 1 | | 5 | | |
| 246 | 1 | | 2 | | |
| 247 | 1 | | 3 | | |
| 249 | 1 | | 3 | | |
| 250 | 1 | * * * | *0*** | | |
| anch total | s: 14 hits of 15 | branches = 93.3 | 33% | | |
| | | IF Branc | ch | | |
| 226 | | | 12 | Count | coming in to IF |
| | 1 | | 3 | | |
| 226 | 1 | | 3 | | |

-----IF Branch------

| 228 | 6 Count coming in to IF |
|---|-------------------------|
| 228 1 | 2 |
| 228 2 | 4 |
| Branch totals: 2 hits of 2 branches = 100.00% | |
| | |
| | |
| IF Branch | |
| 230 | 2 Count coming in to IF |
| 230 1 | 1 |
| 230 2 | 1 |
| Branch totals: 2 hits of 2 branches = 100.00% | |
| | |
| | |
| IF Branch- | |
| 232 | 3 Count coming in to IF |
| 232 1 | 1 |
| 232 2 | 2 |
| Branch totals: 2 hits of 2 branches = 100.00% | |
| | |
| | |
| IF Branch- | |
| 234 | 6 Count coming in to IF |
| 234 1 | 2 |
| 234 2 | 4 |
| Branch totals: 2 hits of 2 branches = 100.00% | |
| | |
| TD D | |
| IF Branch- | |
| 236 | 9 Count coming in to IF |
| 236 1 | 2 |
| 236 2 | 7 |
| Branch totals: 2 hits of 2 branches = 100.00% | |
| | |
| IF Branch- | |
| | |
| 238 | 4 Count coming in to IF |
| 238 1 | 1 |
| 238 2 | 3 |
| Branch totals: 2 hits of 2 branches = 100.00% | |
| | |
| IF Branch- | |
| | |
| 241 | 5 Count coming in to IF |
| 241 1 | 2 |
| 241 2 | 3 |
| Branch totals: 2 hits of 2 branches = 100.00% | |
| | |
| IF Branch- | |
| | |
| 243 | 9 Count coming in to IF |
| 243 1 | 4 |
| 243 2 | 5 |
| Branch totals: 2 hits of 2 branches = 100.00% | |
| Branch Cotars. 2 mics of 2 branches - 100.00% | |

| | | IF Branch | |
|---------------|-------------------|------------------|-------------------------|
| 244 | | 6 | Count coming in to IF |
| 244 | 2 | 1 | |
| 244 | 3 | 5 | |
| Branch totals | s: 2 hits of 2 br | anches = 100.00% | |
| | | | |
| | | IF Branch | |
| 245 | | 5 | Count coming in to IF |
| 245 | 2 | 2 | |
| 245 | 3 | 3 | |
| Branch totals | s: 2 hits of 2 br | anches = 100.00% | |
| | | | |
| | | IF Branch | |
| 246 | | 2 | Count coming in to IF |
| 246 | 2 | 2 | |
| 246 | 3 | ***0*** | |
| Branch totals | s: 1 hit of 2 bra | nches = 50.00% | |
| | | | |
| | | | |
| 248 | | 3 | Count coming in to IF |
| 248 | 1 | 2 | |
| 248 | 2 | 1 | |
| Branch totals | s: 2 hits of 2 br | anches = 100.00% | |
| | | | |
| | | | |
| 249 | | 3 | Count coming in to IF |
| 249 | 2 | 2 | |
| 249 | 3 | 1 | |
| Branch totals | s: 2 hits of 2 br | anches = 100.00% | |
| | | | |
| File covera | 200 07 | | |
| | | TF Branch | |
| 69 | | 501 | Count coming in to IF |
| 69 | 1 | 65 | count coming in co ir |
| 0,7 | <u> </u> | 436 | All False Count |
| Branch totals | s: 2 hits of 2 br | | THE FALSE COUNTY |
| | | 100.000 | |
| | | | |
| File genera | ator.sv | | |
| | | CASE Branch | |
| 131 | | 50 | Count coming in to CASE |
| 132 | 1 | 17 | - |
| 136 | 1 | 17 | |
| 140 | 1 | 16 | |
| - | | | |

Branch totals: 3 hits of 4 branches = 75.00%

-----IF Branch-----

50 Count coming in to IF 149

0 149 1

50 All False Count

Branch totals: 1 hit of 2 branches = 50.00%

| | | CASE Branch | |
|-----|---|-------------|-------------------------|
| 372 | | 75 | Count coming in to CASE |
| 373 | 1 | 12 | |
| 374 | 1 | 6 | |
| 375 | 1 | 2 | |
| 376 | 1 | 3 | |
| 377 | 1 | 6 | |
| 378 | 1 | 9 | |
| 379 | 1 | 4 | |
| 380 | 1 | 5 | |
| 381 | 1 | 9 | |
| 382 | 1 | 6 | |
| 383 | 1 | 5 | |
| 384 | 1 | 2 | |
| 385 | 1 | 3 | |
| 386 | 1 | 3 | |
| 387 | 1 | ***0*** | |

Branch totals: 14 hits of 15 branches = 93.33%

| | CASE Branch | | |
|-------------------|-------------|---|-----|
| coming in to CASE | 75 Cour | | 391 |
| | 21 | 1 | 392 |
| | 4 | 1 | 393 |
| | 6 | 1 | 394 |
| | 7 | 1 | 395 |
| | 7 | 1 | 396 |
| | 4 | 1 | 397 |
| | 4 | 1 | 398 |
| | 3 | 1 | 399 |
| | 7 | 1 | 400 |
| | 6 | 1 | 401 |
| | 2 | 1 | 402 |
| | 4 | 1 | 403 |

Branch totals: 12 hits of 12 branches = 100.00%

| | | | | IF Branch | |
|----------|-----------|--------|------|----------------------|-------------------------|
| 51 | | | | 501 | Count coming in to IF |
| 51 | | 1 | | 65 | |
| | | | | 436 | All False Count |
| Branch | totals: 2 | hits | of 2 | branches = 100.00% | |
| | | | | | |
| | scoreboar | | | TE Door ah | |
| 160 | | | | ***()*** | Count coming in to IF |
| 160 | | 1 | | ***()*** | count coming in to ir |
| 162 | | 1 | | ***()*** | |
| | | | of 2 | branches = 0.00% | |
| or and i | cocars. o | 111 05 | OL Z | Dianches - 0.000 | |
| | | | | | |
| 165 | | | | | Count coming in to IF |
| 165 | | 1 | | ***0*** | |
| 165 | | 2 | | ***0*** | |
| Branch | totals: 0 | hits | of 2 | branches = 0.00% | |
| | | | | IF Branch | |
| 166 | | | | ***0*** | Count coming in to IF |
| 166 | | 1 | | ***0*** | |
| 166 | | 2 | | ***0*** | |
| Branch | totals: 0 | hits | of 2 | branches = 0.00% | |
| | | | | IF Branch | |
| 170 | | | | ***0*** | Count coming in to IF |
| 170 | | 1 | | ***0*** | |
| | | | | ***0*** | All False Count |
| Branch | totals: 0 | hits | of 2 | branches = 0.00% | |
| | | | | IF Branch | |
| 172 | | | | ***0*** | |
| 172 | | 1 | | ***0*** | J |
| | | | | ***0*** | All False Count |
| Branch | totals: 0 | hits | of 2 | branches = 0.00% | |
| | | | | TE Dwee-ah | |
| 177 | | | | ***0*** | |
| 177 | | 1 | | ***0*** | Count Country III to IF |
| ± / / | | 1 | | Ÿ | All False Count |
| Branch | totals: 0 | hits | of 2 | branches = 0.00% | AII PAISE COUIL |
| | | | | _ | |
| 187 | | | | IF Branch ***0*** | Count coming in to IF |
| _0 / | | | | ŭ | |

187 1 ***0***

0 All False Count

Branch totals: 0 hits of 2 branches = 0.00%

-----IF Branch-----

188 ***0*** Count coming in to IF

188 1 ***0***

0 All False Count

Branch totals: 0 hits of 2 branches = 0.00%

-----IF Branch-----

191 ***0*** Count coming in to IF

191 1 ***0***

0 All False Count

Branch totals: 0 hits of 2 branches = 0.00%

-----IF Branch------

201 ***0*** Count coming in to IF

201 1 ***0***

0 All False Count

Branch totals: 0 hits of 2 branches = 0.00%

-----IF Branch-----

206 ***0*** Count coming in to IF

206 1 ***0***

0 All False Count

Branch totals: 0 hits of 2 branches = 0.00%

-----IF Branch-----

215 ***0*** Count coming in to IF

215 1 ***0***

215 2 ***0***

Branch totals: 0 hits of 2 branches = 0.00%

-----IF Branch-----

218 ***0*** Count coming in to IF

218 2 ***0***

Branch totals: 0 hits of 2 branches = 0.00%

-----IF Branch------

221 ***0*** Count coming in to IF

0 All False Count

Branch totals: 0 hits of 2 branches = 0.00%

| 226 | _ | ***0*** | Count coming in to IF |
|--|----------------|--|--|
| 226 | 1 | ***0*** | |
| | | ***0*** | All False Count |
| nch totals: | 0 hits of 2 br | anches = 0.00% | |
| | | | |
| 227 | | ***0*** | Count coming in to IF |
| 227 | 1 | ***0*** | |
| | | ***0*** | All False Count |
| nch totals: | 0 hits of 2 br | anches = 0.00% | |
| | | | |
| 247 | | * * * 0 * * * | Count coming in to IF |
| 247 | 1 | ***0*** | |
| 249 | 1 | * * * 0 * * * | |
| 251 | 1 | ***0*** | |
| | | ***0*** | All False Count |
| nch totals: | 0 hits of 4 br | anches = 0.00% | |
| | | IF Branch | |
| | | ***0** | |
| 257 | 1 | ***0*** | |
| | 1 | ***0*** ***0*** | Count coming in to IF |
| 257 257 anch totals: | 0 hits of 2 br | ***0*** ***0*** *anches = 0.00% | Count coming in to IF All False Count |
| 257 257 anch totals: | 0 hits of 2 br | ***0*** ***0*** *anches = 0.00% | Count coming in to IF |
| 257 257 nch totals: | 0 hits of 2 br | ***0*** ***0*** anches = 0.00% | Count coming in to IF All False Count |
| 257 257 nch totals: | 0 hits of 2 br | ***0*** ***0*** anches = 0.00% CASE Branch ***0*** | Count coming in to IF All False Count |
| 257 257 anch totals: 305 308 | 0 hits of 2 br | ***0*** ***0*** *anches = 0.00% CASE Branch ***0*** | Count coming in to IF All False Count |
| 257 257 anch totals: 305 308 309 | 0 hits of 2 br | ***0*** ***0*** *anches = 0.00% CASE Branch ***0*** ***0*** | Count coming in to IF All False Count |
| 257 257 anch totals: 305 308 309 310 | 0 hits of 2 br | ***0*** ***0*** *anches = 0.00% CASE Branch ***0*** ***0*** ***0*** | Count coming in to IF All False Count |
| 257 257 anch totals: 305 308 309 310 311 | 0 hits of 2 br | ***0*** ***0*** *anches = 0.00% CASE Branch ***0*** ***0*** ***0*** ***0*** ***0*** | Count coming in to IF All False Count |
| 257 257 anch totals: 305 308 309 310 311 313 | 0 hits of 2 br | ***0*** ***0*** *anches = 0.00% CASE Branch ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** | Count coming in to IF All False Count |
| 257 257 anch totals: 305 308 309 310 311 313 314 | 0 hits of 2 br | ***0*** ***0*** *anches = 0.00% CASE Branch ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** | Count coming in to IF All False Count |
| 257 257 anch totals: 305 308 309 310 311 313 314 315 | 0 hits of 2 br | ***0*** ***0*** *anches = 0.00% CASE Branch ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** | Count coming in to IF All False Count |
| 257 257 anch totals: 305 308 309 310 311 313 314 315 316 | 0 hits of 2 br | ***0*** ***0*** *anches = 0.00% CASE Branch ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** | Count coming in to IF All False Count |
| 257 257 anch totals: 305 308 309 310 311 313 314 315 316 317 318 | 0 hits of 2 br | ***0*** ***0*** *anches = 0.00% CASE Branch ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** | Count coming in to IF All False Count |
| 257 257 anch totals: 305 308 309 310 311 313 314 315 316 317 318 319 | 0 hits of 2 br | ***0*** ***0*** **anches = 0.00% CASE Branch ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** | Count coming in to IF All False Count |
| 257 257 anch totals: 305 308 309 310 311 313 314 315 316 317 318 319 320 | 0 hits of 2 br | ***0*** ***0*** **anches = 0.00% CASE Branch ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** | Count coming in to IF All False Count |
| 257 257 anch totals: 305 308 309 310 311 313 314 315 316 317 318 319 | 0 hits of 2 br | ***0*** ***0*** **anches = 0.00% CASE Branch ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** ***0*** | Count coming in to IF All False Count |

-----IF Branch-----

| ========== | | =====Condition De | | | | |
|-----------------|--------------|-------------------|---------|--------|---------------|-------|
| Conditions | 3 | 65 | | | 7.69% | |
| Condition Cove | overage | Bins Cov | | | | |
| | | | | | | |
| | 0 hits of 2 | branches = 0.00% | | | | |
| 322 | 3 | *** | 0*** | | | |
| 322 | 2 | | 0*** | Courre | | OO II |
| 322 | | | | | coming in | |
| | | IF Branc | h | | | |
| Branch totals: | 0 hits of 2 | branches = 0.00% | | | | |
| 321 | 3 | * * * | 0 * * * | | | |
| 321 | 2 | * * * | 0 * * * | | | |
| 321 | | *** | 0*** | Count | coming in | to IF |
| | | IF Branc | h | | | |
| Branch totals: | 0 hits of 2 | branches = 0.00% | | | | |
| 320 | 3 | * * * | 0 * * * | | | |
| 320 | 2 | * * * | 0*** | | | |
| 320 | | * * * | 0 * * * | Count | coming in | to IF |
| | | IF Branc | h | | . – – – – – – | |
| Branch totals: | 0 hits of 2 | branches = 0.00% | | | | |
| 319 | 3 | | 0 * * * | | | |
| 319 | 2 | | 0 * * * | | | |
| 319 | | *** | 0*** | | coming in | |
| | | IF Branc | h | | | |
| Branch totals: | 0 hits of 2 | branches = 0.00% | | | | |
| 312 | 2 | | 0 * * * | | | |
| 312 | 1 | | 0 * * * | | | |
| 312 | | | | Count | coming in | to IF |
| | | IF Branc | h | | | |
| Braileir cocars | 0 11100 01 1 | | | | | |
| | | branches = 0.00% | O . | | | |
| 310 310 | 2 | | 0*** | | | |
| 310 | 0 | | 0*** | Count | coming in | to IF |
| 0.1.0 | | | | | | |

Condition Coverage for Design Unit work.coverage_sv_unit --

```
-----Focused Condition View------
       243 Item 1 (rs1 < rs2)
Line
Condition totals: 1 of 1 input term covered = 100.00%
 Input Term Covered Reason for no coverage Hint
 (rs1 < rs2)
             Y
   Rows: Hits FEC Target
                         Non-masking condition(s)
______ ____
 Row 1: 1 (rs1 < rs2)_0
            1 (rs1 < rs2)_1
 Row 2:
-----Focused Condition View------
       244 Item 1 (rs1 < rs2)
Line
Condition totals: 1 of 1 input term covered = 100.00%
 Input Term Covered Reason for no coverage Hint
 (rs1 < rs2)
          Hits FEC Target
                            Non-masking condition(s)
   Rows:
______ ____
 Row 1:
            1 (rs1 < rs2)_0
 Row 2:
            1 (rs1 < rs2)_1
-----Focused Condition View-----
Line
       245 Item 1 (rs1 == rs2)
Condition totals: 1 of 1 input term covered = 100.00%
  Input Term Covered Reason for no coverage Hint
  ______ _____
 (rs1 == rs2)
              Y
          Hits FEC Target
   Rows:
                            Non-masking condition(s)
_____ ____
            1 (rs1 == rs2)_0
 Row 1:
 Row 2: 1 (rs1 == rs2)_1
------Focused Condition View------
       246 Item 1 (rs1 != rs2)
Line
Condition totals: 0 of 1 input term covered = 0.00%
  Input Term Covered Reason for no coverage
  ______ ____
 (rs1 != rs2)
          N '_0' not hit
                                 Hit '_0'
```

```
Hits FEC Target
  Rows:
                          Non-masking condition(s)
______ _____
       ***0*** (rs1 != rs2)_0
 Row 1:
 Row 2: 1 (rs1 != rs2)_1 -
-----Focused Condition View-----
      248 Item 1 (rs1 >= rs2)
Condition totals: 1 of 1 input term covered = 100.00%
  Input Term Covered Reason for no coverage Hint
 ______
 (rs1 >= rs2) Y
  Rows: Hits FEC Target Non-masking condition(s)
______
 Row 1: 1 (rs1 >= rs2)_0
 Row 2:
           1 (rs1 >= rs2)_1 -
-----Focused Condition View-----
Line 249 \text{ Item} 1 \text{ (rs1 >= rs2)}
Condition totals: 1 of 1 input term covered = 100.00%
  Input Term Covered Reason for no coverage Hint
 ______
 (rs1 >= rs2)
             Y
  Rows: Hits FEC Target
                      Non-masking condition(s)
______ ____
 Row 1:
           1 (rs1 >= rs2)_0
 Row 2:
           1 (rs1 >= rs2)_1
```

| Input Term | Covered | Reason for no coverage | Hint |
|------------------------|---------|------------------------|-------------------|
| | | | |
| (rst_n === 1'b0) | N | No hits | Hit '_0' and '_1' |
| (tx.o_exception !== 0) | N | No hits | Hit '_0' and '_1' |

```
(tx.o_ce !== 1'b0)
                              N No hits
 (tx.o_stall_from_alu !== 1'b0)
                               N No hits
                                                      Hit ' 0' and ' 1'
            Hits FEC Target
                                            Non-masking condition(s)
   Rows:
-----
                                             _____
 Row 1:
          ***0*** (rst_n === 1'b0)_0
 Row 2: ***0*** (rst_n === 1'b0)_1
                                                 ((tx.o_exception !== 0) &&
((tx.o_ce !== 1'b0) && (tx.o_stall_from_alu !== 1'b0)))
          ***0*** (tx.o_exception !== 0)_0
                                            (rst_n === 1'b0)
      4:
          ***0*** (tx.o_exception !== 0)_1
 Row
                                             ((rst_n === 1'b0) && ((tx.o_ce
!== 1'b0) && (tx.o_stall_from_alu !== 1'b0)))
            ***0*** (tx.o_ce !== 1'b0)_0
      5:
                                                     ((rst_n === 1'b0) \&\&
(tx.o_exception !== 0))
            ***0*** (tx.o_ce !== 1'b0)_1
      6:
                                                     ((rst_n === 1'b0) &&
(tx.o_exception !== 0) && (tx.o_stall_from_alu !== 1'b0))
               ***0***
                       (tx.o_stall_from_alu !== 1'b0)_0 ((rst_n === 1'b0) &&
(tx.o_exception !== 0) && (tx.o_ce !== 1'b0))
        8:
              ***0*** (tx.o_stall_from_alu !== 1'b0)_1 ((rst_n === 1'b0) &&
(tx.o_exception !== 0) && (tx.o_ce !== 1'b0))
-----Focused Condition View-----
        165 Item 1 (opcode[5] | opcode[8])
Line
Condition totals: 0 of 2 input terms covered = 0.00%
 Input Term Covered Reason for no coverage Hint
______
  opcode[5]
               N No hits
                                      Hit ' 0' and ' 1'
  opcode[8]
             N No hits
                                     Hit '\_0' and '\_1'
   Rows: Hits FEC Target
                                  Non-masking condition(s)
 ______ ____
 Row 1: ***0*** opcode[5]_0
                                  ~opcode[8]
      2:
         ***0*** opcode[5] 1
 Row
          ***0*** opcode[8]_0
 Row 3:
                                  ~opcode[5]
           ***0*** opcode[8]_1
 Row 4:
                                  ~opcode[5]
-----Focused Condition View------
        166 Item 1 (opcode[0] | opcode[4])
Condition totals: 0 of 2 input terms covered = 0.00%
 Input Term Covered Reason for no coverage Hint
______
  opcode[0]
               N No hits
                                      Hit ' 0' and ' 1'
               N No hits
                                      Hit '_0' and '_1'
  opcode[4]
```

Rows: Hits FEC Target Non-masking condition(s)

Hit ' 0' and ' 1'

```
1: ***0*** opcode[0]_0
 Row
                                 ~opcode[4]
         ***0*** opcode[0]_1
 Row
     2:
         ***0*** opcode[4]_0
 Row 3:
                                 ~opcode[0]
 Row 4: ***0*** opcode[4] 1
                                 ~opcode[0]
------Focused Condition View-----
        172 Item 1 (opcode[0] | opcode[1])
Condition totals: 0 of 2 input terms covered = 0.00%
 Input Term Covered Reason for no coverage Hint
______ _____
              N No hits
                                    Hit '_0' and '_1'
  opcode[0]
  opcode[1]
              N No hits
                                    Hit '_0' and '_1'
          Hits FEC Target
                                 Non-masking condition(s)
   Rows:
 ______ ____
         ***0*** opcode[0]_0
     1:
 Row
                                  ~opcode[1]
 Row 2: ***0*** opcode[0]_1
         ***0*** opcode[1]_0
 Row
     3:
                                 ~opcode[0]
 Row 4: ***0*** opcode[1]_1
                                 ~opcode[0]
-----Focused Condition View-----
        177 Item 1 (opcode[4] && out && (((pc + imm) !== tx.o_next_pc) | (ce !==
Line
tx.o_change_pc) || (ce !== tx.o_flush)))
Condition totals: 0 of 1 input term covered = 0.00%
    Input Term Covered Reason for no coverage Hint
    ______ ____
 (opcode[4] && out && (((pc + imm) !== tx.o_next_pc) || (ce !== tx.o_change_pc) || (ce
              N No hits
!== tx.o_flush)))
                                        Hit '_0' and '_1'
   Rows: Hits FEC Target
                              Non-masking condition(s)
 -----
          ***0*** (opcode[4] && out && (((pc + imm) !== tx.o_next_pc) || (ce !==
 Row
***0*** (opcode[4] && out && (((pc + imm) !== tx.o_next_pc) || (ce !==
 Row
tx.o_change_pc) | | (ce !== tx.o_flush)))_1 -
------Focused Condition View-----
        187 Item 1 (opcode[5] | opcode[6])
Condition totals: 0 of 2 input terms covered = 0.00%
```

```
Input Term Covered Reason for no coverage Hint
______ _____
             N No hits
                                  Hit '_0' and '_1'
  opcode[5]
  opcode[6] N No hits
                                  Hit '_0' and '_1'
         Hits FEC Target
   Rows:
                           Non-masking condition(s)
_____ ____
     1: ***0*** opcode[5]_0
 Row
                               ~opcode[6]
 Row 2:
         ***0*** opcode[5]_1
     3: ***0*** opcode[6]_0
 Row
                               ~opcode[5]
         ***0*** opcode[6]_1
 Row
     4:
                               ~opcode[5]
------Focused Condition View------
       188 Item 1 (opcode[6] === 1'b1)
Line
Condition totals: 0 of 1 input term covered = 0.00%
        Input Term Covered Reason for no coverage Hint
        ______ _____
 (opcode[6] === 1'b1)
                  N No hits
                                         Hit '_0' and '_1'
           Hits FEC Target
   Rows:
                                Non-masking condition(s)
_____
                                _____
     1: ***0*** (opcode[6] === 1'b1)_0 -
 Row
     2: ***0*** (opcode[6] === 1'b1)_1 -
 Row
-----Focused Condition View------
Line
       tx.o_flush))
Condition totals: 0 of 3 input terms covered = 0.00%
          Input Term Covered Reason for no coverage Hint
          -----
  (sum !== tx.o_next_pc)
                      N No hits
                                           Hit ' 0' and ' 1'
 (ce !== tx.o_change_pc)
                       N No hits
                                           Hit '_0' and '_1'
    (ce !== tx.o_flush) N No hits
                                           Hit ' 0' and ' 1'
           Hits FEC Target
                                  Non-masking condition(s)
   Rows:
_____
                                  _____
 Row 1:
         ***0*** (sum !== tx.o_next_pc)_0 ~((ce !== tx.o_change_pc) || (ce !==
tx.o_flush))
     2:
         ***0*** (sum !== tx.o_next_pc)_1 -
 Row
 Row 3:
          ***0*** (ce !== tx.o_change_pc)_0 (~(sum !== tx.o_next_pc) && ~(ce !==
tx.o_flush))
    4:
          ***0*** (ce !== tx.o_change_pc)_1 ~(sum !== tx.o_next_pc)
 Row
 Row 5: ***0*** (ce !== tx.o_flush)_0 (~(sum !== tx.o_next_pc) && ~(ce !==
```

```
tx.o_change_pc))
 Row 6: ***0*** (ce !== tx.o_flush)_1 (~(sum !== tx.o_next_pc) && ~(ce !==
tx.o_change_pc))
-----Focused Condition View-----
         211 Item 1 (((opcode[4] | opcode[3]) | (opcode[9] && (funct3 == 0))) | |
Line
opcode[10])
Condition totals: 0 of 5 input terms covered = 0.00%
    Input Term Covered Reason for no coverage Hint
    opcode[4]
                   N No hits
                                           Hit '_0' and '_1'
                                           Hit '_0' and '_1'
    opcode[3]
                  N No hits
                  N No hits
    opcode[9]
                                          Hit '_0' and '_1'
 (funct3 == 0)
                  N No hits
                                          Hit '_0' and '_1'
    opcode[10]
                  N No hits
                                           Hit '_0' and '_1'
    Rows:
            Hits FEC Target
                                    Non-masking condition(s)
 ______ ____
           ***0*** opcode[4]_0
 Row 1:
                                      (~opcode[10] && ~(opcode[9] && (funct3 ==
0)) && ~opcode[3])
 Row 2:
          ***0*** opcode[4]_1
           ***0*** opcode[3]_0
 Row 3:
                                      (~opcode[10] && ~(opcode[9] && (funct3 ==
0)) && ~opcode[4])
          ***0*** opcode[3]_1
      4:
 Row
                                    ~opcode[4]
          ***0*** opcode[9]_0
      5:
                                    (~opcode[10] && ~(opcode[4] | opcode[3]))
 Row
           ***0*** opcode[9]_1
 Row 6:
                                       (~(opcode[4] | opcode[3]) && (funct3 ==
0))
           ***0*** (funct3 == 0)_0
 Row 7:
                                     (~opcode[10] && ~(opcode[4] || opcode[3])
&& opcode[9])
 Row 8: ***0*** (funct3 == 0) 1
                                    (~(opcode[4] | opcode[3]) && opcode[9])
 Row 9: ***0*** opcode[10]_0
                                     ~((opcode[4] || opcode[3]) || (opcode[9] &&
(funct3 == 0)))
Row 10: ***0*** opcode[10]_1 ~((opcode[4] || opcode[3]) || (opcode[9] &&
(funct3 == 0)))
-----Focused Condition View------
         218 Item 1 (opcode[2] | (opcode[9] && (funct3 != 0)))
Condition totals: 0 of 3 input terms covered = 0.00%
    Input Term Covered Reason for no coverage Hint
   N No hits
                                           Hit ' 0' and ' 1'
    opcode[2]
                                          Hit '_0' and '_1'
    opcode[9]
                  N No hits
                  N No hits
                                          Hit '_0' and '_1'
 (funct3 != 0)
```

```
Rows:
           Hits FEC Target
                                     Non-masking condition(s)
          ***0*** opcode[2]_0
      1:
                                     ~(opcode[9] && (funct3 != 0))
 Row
          ***0*** opcode[2]_1
      2:
 Row
      3:
          ***0*** opcode[9]_0
                                     ~opcode[2]
 Row
          ***0*** opcode[9]_1
     4:
                                    (~opcode[2] && (funct3 != 0))
 Row
      5:
          ***0*** (funct3 != 0)_0
                                    (~opcode[2] && opcode[9])
 Row
          ***0*** (funct3 != 0)_1
 Row
      6:
                                    (~opcode[2] && opcode[9])
-----Focused Condition View-----
         221 Item 1 ((tx.o_stall !== (stall || force_stall)) && ~flush)
Condition totals: 0 of 2 input terms covered = 0.00%
                         Input Term Covered Reason for no coverage Hint
 (tx.o_stall !== (stall || force_stall)) N No hits
                                                                   Hit '_0'
and ' 1'
                               flush N No hits
                                                                  Hit '_0'
and '_1'
             Hits FEC Target
     Rows:
                                                                Non-masking
condition(s)
            _____
                      _____
_____
 Row 1: ***0*** (tx.o_stall !== (stall || force_stall))_0 -
 Row
      2: ***0*** (tx.o_stall !== (stall || force_stall))_1 ~flush
          ***0*** flush_0
 Row 3:
                                                       (tx.o_stall !== (stall
|| force_stall))
      4: ***0*** flush_1
                                                       (tx.o_stall !== (stall
| force_stall))
-----Focused Condition View-----
         226 Item 1 (~(tx.o_stall | stall) && (ce === 1'b1))
Condition totals: 0 of 3 input terms covered = 0.00%
    Input Term Covered Reason for no coverage Hint
   ______ _____
                  N No hits
    tx.o_stall
                                          Hit '_0' and '_1'
       stall
                  N No hits
                                          Hit '_0' and '_1'
                  N No hits
                                           Hit '_0' and '_1'
 (ce === 1'b1)
    Rows: Hits FEC Target
                                    Non-masking condition(s)
```

```
***0*** tx.o_stall_0
 Row
      1:
                                    ((ce === 1'b1) && ~stall)
          ***0*** tx.o_stall_1
      2:
 Row
          ***0*** stall_0
 Row
      3:
                                    ((ce === 1'b1) && ~tx.o_stall)
          ***0*** stall_1
     4:
 Row
                                    ~tx.o_stall
 Row
     5:
          ***0*** (ce === 1'b1)_0
                                    ~(tx.o_stall || stall)
          ***0*** (ce === 1'b1)_1
 Row 6:
                                    ~(tx.o_stall || stall)
-----Focused Condition View-----
Line 227 Item 1 ((opcode !== tx.o_opcode) || (exception !== tx.o_exception) ||
(out !== tx.o_y) || (rs1_addr !== tx.o_rs1_addr) || (rs1 !== tx.o_rs1) || (rs2 !==
tx.o_rs2) || (rd_addr !== tx.o_rd_addr) || (imm !== tx.o_imm) || (funct3 !==
tx.o_funct3) || (rd_d !== tx.o_rd) || (rd_valid !== tx.o_rd_valid) || (wr_rd_d !==
tx.o_wr_rd) || ((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc))
Condition totals: 0 of 14 input terms covered = 0.00%
                                   Input Term Covered Reason for no coverage
Hint
_____
                                                 N No hits
                      (opcode !== tx.o_opcode)
Hit '_0' and '_1'
                                                 N No hits
                 (exception !== tx.o_exception)
Hit '_0' and '_1'
                             (out !== tx.o_y)
                                                 N No hits
Hit '_0' and '_1'
                  (rs1_addr !== tx.o_rs1_addr)
                                                 N No hits
Hit '_0' and '_1'
                           (rs1 !== tx.o_rs1)
                                                 N No hits
Hit '_0' and '_1'
                           (rs2 !== tx.o_rs2)
                                                 N No hits
Hit ' 0' and ' 1'
                    (rd_addr !== tx.o_rd_addr)
                                                 N No hits
Hit ' 0' and ' 1'
                           (imm !== tx.o_imm) N No hits
Hit '_0' and '_1'
                      (funct3 !== tx.o_funct3)
                                                 N No hits
Hit '_0' and '_1'
                           Hit '_0' and '_1'
                  (rd_valid !== tx.o_rd_valid)
                                                 N No hits
Hit '_0' and '_1'
                      (wr_rd_d !== tx.o_wr_rd)
N No hits
Hit '_0' and '_1'
 Hit '\_0' and '\_1'
                             (pc !== tx.o_pc) N No hits
```

```
Rows:
            Hits FEC Target
                                                                          Non-masking
condition(s)
 Row 1: ***0*** (opcode !== tx.o_opcode)_0
                                                                         ~((exception
!== tx.o_exception) || ((out !== tx.o_y) || ((rs1_addr !== tx.o_rs1_addr) || ((rs1 !==
tx.o_rs1) || ((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !== tx.o_imm)
| ((funct3 !== tx.o_funct3) | ((rd_d !== tx.o_rd) | ((rd_valid !== tx.o_rd_valid) |
((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc
!== tx.o_pc)))))))))))
            ***0*** (opcode !== tx.o_opcode)_1
      2:
 Row
            ***0*** (exception !== tx.o_exception)_0
  Row
                                                                            (~(opcode
!== tx.o_opcode) && ~((out !== tx.o_y) || ((rs1_addr !== tx.o_rs1_addr) || ((rs1 !==
tx.o_rs1) || ((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !== tx.o_imm)
| ((funct3 !== tx.o_funct3) | ((rd_d !== tx.o_rd) | ((rd_valid !== tx.o_rd_valid) |
((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc
!== tx.o_pc))))))))))))
             ***0*** (exception !== tx.o_exception)_1
 Row 4:
                                                                         ~(opcode !==
tx.o_opcode)
            ***0*** (out !== tx.o_y)_0
        5:
 Row
                                                                            (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~((rs1_addr !== tx.o_rs1_addr) |
((rs1 !== tx.o_rs1) || ((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !==
tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !==
tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) ==
tx.o_stall_from_alu) | (pc !== tx.o_pc))))))))))
            ***0*** (out !== tx.o_y)_1
                                                                            (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception))
             ***0*** (rs1_addr !== tx.o_rs1_addr)_0
                                                                            (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~((rs1 !==
tx.o_rs1) || ((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !== tx.o_imm)
|| ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) ||
((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc
!== tx.o_pc)))))))))))
             ***0*** (rsl_addr !== tx.o_rsl_addr)_1
                                                                            (~(opcode
  Row
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y))
             ***0*** (rs1 !== tx.o_rs1)_0
                                                                            (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !==
tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !==
tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) ==
tx.o_stall_from_alu) | (pc !== tx.o_pc)))))))))
      10:
            ***0*** (rs1 !== tx.o_rs1)_1
                                                                            (~(opcode
```

!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr

```
!== tx.o_rs1_addr))
                          ***0*** (rs2 !== tx.o_rs2)_0
                                                                                                                                                  (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~((rd_addr !== tx.o_rd_addr) || ((imm !==
tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !==
tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) ==
tx.o_stall_from_alu) | (pc !== tx.o_pc))))))))
                        ***0*** (rs2 !== tx.o_rs2)_1
                                                                                                                                                  (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1))
                        ***0*** (rd_addr !== tx.o_rd_addr)_0
 Row
                                                                                                                                                  (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~((imm !== tx.o_imm)
| ((funct3 !== tx.o_funct3) | ((rd_d !== tx.o_rd) | ((rd_valid !== tx.o_rd_valid) |
((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc
!== tx.o_pc)))))))
                        ***0*** (rd_addr !== tx.o_rd_addr)_1
          14:
                                                                                                                                                  (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2))
                         ***0*** (imm !== tx.o_imm)_0
                                                                                                                                                  (~(opcode
 Row
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !==
tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) ==
tx.o_stall_from_alu) | (pc !== tx.o_pc))))))
                        ***0*** (imm !== tx.o_imm)_1
                                                                                                                                                  (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr))
 Row 17:
                        ***0*** (funct3 !== tx.o_funct3)_0
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~((rd_d !== tx.o_rd) || ((rd_valid !==
tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) ==
tx.o_stall_from_alu) || (pc !== tx.o_pc)))))
                        ***0*** (funct3 !== tx.o_funct3)_1
 Row
                                                                                                                                                  (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm))
 Row 19:
                        ***0*** (rd_d !== tx.o_rd)_0
                                                                                                                                                  (~(opcode
!== \  \, \text{tx.o\_opcode}) \  \, \&\& \  \, \sim (\text{exception}) \  \, \&\& \  \, \sim (\text{out } !== \  \, \text{tx.o\_y}) \  \, \&\& \  \, \sim (\text{rs1\_addr}) \  \, \& 
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~((rd_valid !==
tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) ==
tx.o_stall_from_alu) | (pc !== tx.o_pc))))
 Row
          20:
                       ***0*** (rd_d !== tx.o_rd)_1
                                                                                                                                                  (~(opcode
```

```
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3))
              ***0*** (rd_valid !== tx.o_rd_valid)_0
                                                                             (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd)
&& ~((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) ||
(pc !== tx.o_pc))))
             ***0*** (rd_valid !== tx.o_rd_valid)_1
Row
     22:
                                                                             (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !==
tx.o_rd))
            ***0*** (wr_rd_d !== tx.o_wr_rd)_0
Row
                                                                             (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd)
&& \sim (rd_valid !== tx.o_rd_valid) \&\& \sim (((opcode[3] || opcode[2]) == tx.o_stall_from_alu))
|| (pc !== tx.o_pc)))
             ***0*** (wr_rd_d !== tx.o_wr_rd)_1
       24:
                                                                             (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd)
&& ~(rd_valid !== tx.o_rd_valid))
              ***0*** ((opcode[3] || opcode[2]) == tx.o_stall_from_alu)_0 (~(opcode
       25:
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd)
&& ~(rd_valid !== tx.o_rd_valid) && ~(wr_rd_d !== tx.o_wr_rd) && ~(pc !== tx.o_pc))
               ***0*** ((opcode[3] || opcode[2]) == tx.o_stall_from_alu)_1 (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd)
&& ~(rd_valid !== tx.o_rd_valid) && ~(wr_rd_d !== tx.o_wr_rd))
             ***0*** (pc !== tx.o_pc)_0
Row
     27:
                                                                             (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd)
&& ~(rd_valid !== tx.o_rd_valid) && ~(wr_rd_d !== tx.o_wr_rd) && ~((opcode[3] |
opcode[2]) == tx.o_stall_from_alu))
             ***0*** (pc !== tx.o_pc)_1
                                                                             (~(opcode
!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rsl_addr
!== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !==
tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd)
&& ~(rd_valid !== tx.o_rd_valid) && ~(wr_rd_d !== tx.o_wr_rd) && ~((opcode[3] |
```

```
opcode[2]) == tx.o_stall_from_alu))
-----Focused Condition View-----
        247 Item 1 (flush && ~(tx.o_stall | stall) && (tx.o_ce !== 1'b0))
Condition totals: 0 of 4 input terms covered = 0.00%
        Input Term Covered Reason for no coverage Hint
       N No hits
                                             Hit '_0' and '_1'
           flush
                     N No hits
                                             Hit '_0' and '_1'
        tx.o_stall
                     N No hits
                                             Hit '_0' and '_1'
           stall
                     N No hits
                                             Hit '_0' and '_1'
 (tx.o_ce !== 1'b0)
            Hits FEC Target
   Rows:
                                   Non-masking condition(s)
          ***0*** flush_0
 Row 1:
 Row 2: ***0*** flush_1
                                       (~(tx.o_stall || stall) && (tx.o_ce !==
1'b0))
          ***0*** tx.o_stall_0
 Row 3:
                                   (flush && (tx.o_ce !== 1'b0) && ~stall)
      4: ***0*** tx.o_stall_1
 Row
                                   flush
 Row 5:
             ***0*** stall_0
                                            (flush && (tx.o_ce !== 1'b0) &&
~tx.o_stall)
 Row 6: ***0*** stall_1
                                   (flush && ~tx.o_stall)
          ***0*** (tx.o_ce !== 1'b0)_0 (flush && ~(tx.o_stall || stall))
 Row 7:
 Row 8: ***0*** (tx.o_ce !== 1'b0)_1 (flush && ~(tx.o_stall || stall))
-----Focused Condition View------
Line
        249 Item 1 (~(tx.o_stall | stall) && (tx.o_ce !== ce))
Condition totals: 0 of 3 input terms covered = 0.00%
      Input Term Covered Reason for no coverage Hint
     ______ ______
                    N No hits
                                           Hit ' 0' and ' 1'
      tx.o_stall
         stall
                    N No hits
                                           Hit ' 0' and ' 1'
 (tx.o_ce !== ce)
                    N No hits
                                           Hit '\_0' and '\_1'
   Rows:
            Hits FEC Target
                                   Non-masking condition(s)
 _____ ____
          ***0*** tx.o_stall_0
      1:
 Row
                                   ((tx.o_ce !== ce) && ~stall)
          ***0*** tx.o_stall_1
      2:
 Row
      3:
          ***0*** stall_0
                                   ((tx.o_ce !== ce) && ~tx.o_stall)
 Row
      4:
          ***0*** stall_1
 Row
                                   ~tx.o_stall
          ***0*** (tx.o_ce !== ce)_0
      5:
                                   ~(tx.o_stall | stall)
 Row
      6: ***0*** (tx.o_ce !== ce)_1 ~(tx.o_stall || stall)
 Row
```

------Focused Condition View------

```
Line 251 Item 1 (tx.o_stall && (tx.o_ce !== 1'b0))

Condition totals: 0 of 2 input terms covered = 0.00%

Input Term Covered Reason for no coverage Hin
```

```
Input Term Covered Reason for no coverage Hint
      ______ ____
                  N No hits
      tx.o_stall
                                     Hit '_0' and '_1'
 (tx.o_ce !== 1'b0) N No hits
                                     Hit '_0' and '_1'
   Rows: Hits FEC Target
                         Non-masking condition(s)
______ ____
 Row 1: ***0*** tx.o_stall_0
        ***0*** tx.o_stall_1
 Row 2:
                             (tx.o_ce !== 1'b0)
 Row 3: ***0*** (tx.o_ce !== 1'b0)_0 tx.o_stall
        ***0*** (tx.o_ce !== 1'b0)_1 tx.o_stall
 Row 4:
------Focused Condition View-----
      310 Item 1 (a < b)
Condition totals: 0 of 1 input term covered = 0.00%
 Input Term Covered Reason for no coverage Hint
_____
   (a < b)
            N No hits
                                Hit '_0' and '_1'
         Hits FEC Target
                            Non-masking condition(s)
   Rows:
______ _____
        ***0*** (a < b)_0
 Row 1:
 Row 2: ***0*** (a < b) 1
-----Focused Condition View-----
      312 Item 1 (a < b)
Condition totals: 0 of 1 input term covered = 0.00%
 Input Term Covered Reason for no coverage Hint
______ ____
   (a < b)
            N No hits
                               Hit '_0' and '_1'
   Rows:
          Hits FEC Target
                            Non-masking condition(s)
______
 Row 1:
        ***0*** (a < b)_0
 Row 2: ***0*** (a < b)_1
------Focused Condition View-----
      319 Item 1 (a == b)
Line
```

Input Term Covered Reason for no coverage Hint

Condition totals: 0 of 1 input term covered = 0.00%

```
(a == b)
           N No hits
                               Hit ' 0' and ' 1'
          Hits FEC Target
   Rows:
                             Non-masking condition(s)
______ _____
        ***0*** (a == b)_0
 Row 1:
 Row 2: ***0*** (a == b)_1
------Focused Condition View------
      320 Item 1 (a != b)
Line
Condition totals: 0 of 1 input term covered = 0.00%
 Input Term Covered Reason for no coverage
                               Hit '_0' and '_1'
  (a != b) N No hits
   Rows: Hits FEC Target
                             Non-masking condition(s)
______
 Row 1: ***0*** (a != b)_0
 Row 2: ***0*** (a != b)_1
-----Focused Condition View-----
       321 Item 1 (a >= b)
Line
Condition totals: 0 of 1 input term covered = 0.00%
 Input Term Covered Reason for no coverage Hint
(a >= b) N No hits
                               Hit '_0' and '_1'
   Rows: Hits FEC Target
                         Non-masking condition(s)
______ ____
 Row 1: ***0*** (a >= b)_0
 Row 2: ***0*** (a >= b)_1
-----Focused Condition View-----
       322 Item 1 (a >= b)
Line
Condition totals: 0 of 1 input term covered = 0.00%
 Input Term Covered Reason for no coverage Hint
______ ____
           N No hits
                                Hit '_0' and '_1'
  (a >= b)
          Hits FEC Target
   Rows:
                            Non-masking condition(s)
_____ ____
        ***0*** (a >= b)_0
 Row 1:
 Row 2: ***0*** (a >= b)_1
```

| Covergroup Coverage: | | | | | | |
|--------------------------------|--------------|-----|------|------|------|------|
| Covergroups | 1 | na | na | 34.8 | 1% | |
| Coverpoints/Crosses | 20 | na | na | | na | |
| Covergroup Bins | | 51 | 5264 | 0.9 | 5% | |
| | | | | | | |
| Covergroup | | | Met | ric | Goal | Bins |
| Status | | | | | | |
| | | | | | | |
| | | | | | | |
| TYPE work.coverage_sv_unit::co | overage/alu_ | .cg | 34.8 | 31% | 100 | - |
| Uncovered | | | | | | |
| covered/total bins: | | | | 51 | 5315 | - |
| missing/total bins: | | | 52 | 64 | 5315 | - |
| % Hit: | | | 0.9 | 5% | 100 | - |
| type_option.weight=1 | | | | | | |
| type_option.goal=100 | | | | | | |
| type_option.comment= | | | | | | |
| type_option.strobe=0 | | | | | | |
| type_option.merge_instances | s=auto(1) | | | | | |
| Coverpoint #coverpoint0# | | | 45. | 45% | 100 | _ |
| Uncovered | | | | | | |
| covered/total bins: | | | | 5 | 11 | - |
| missing/total bins: | | | | 6 | 11 | - |
| % Hit: | | | 45.4 | 5% | 100 | - |
| type_option.weight=1 | | | | | | |
| type_option.goal=100 | | | | | | |
| type_option.comment= | | | | | | |
| bin opcode_types[0] | | | | 3 | 1 | _ |
| Covered | | | | | | |
| bin opcode_types[1] | | | | 20 | 1 | - |
| Covered | | | | | | |
| <pre>bin opcode_types[2]</pre> | | | | 1 | 1 | - |
| Covered | | | | | | |

bin opcode_types[3]

| 2210 | bin opcode_types[4] | 6 | 1 | - |
|------------|--|--------|-----|---|
| Covered | | 0 | 1 | |
| ZERO | bin opcode_types[5] | 0 | 1 | _ |
| | bin opcode_types[6] | 0 | 1 | - |
| ZERO | him amanda tuman[7] | 0 | 1 | |
| ZERO | bin opcode_types[7] | 0 | 1 | - |
| | bin opcode_types[8] | 5 | 1 | - |
| Covered | | 0 | 1 | |
| ZERO | bin opcode_types[9] | 0 | 1 | - |
| | bin opcode_types[10] | 0 | 1 | - |
| ZERO | | 00.550 | 100 | |
| Cov | verpoint #coverpoint1# | 28.57% | 100 | _ |
| 01100 (01 | covered/total bins: | 4 | 14 | - |
| | missing/total bins: | 10 | 14 | - |
| | % Hit: | 28.57% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin alu_ops[0] | 0 | 1 | - |
| ZERO | him als ang[1] | 11 | 1 | |
| Covered | bin alu_ops[1] | 11 | 1 | _ |
| | bin alu_ops[2] | 4 | 1 | - |
| Covered | ı | | | |
| 7500 | bin alu_ops[3] | 0 | 1 | - |
| ZERO | bin alu_ops[4] | 1 | 1 | - |
| Covered | | | | |
| | bin alu_ops[5] | 0 | 1 | _ |
| ZERO | bin alu_ops[6] | 0 | 1 | _ |
| ZERO | #=== #================================ | | | |
| | bin alu_ops[7] | 0 | 1 | - |
| ZERO | bin alu_ops[8] | 3 | 1 | _ |
| Covered | | J | 1 | |
| | bin alu_ops[9] | 0 | 1 | - |
| ZERO | | | | |

| | bin alu_ops[10] | 0 | 1 | - |
|---------|------------------------|---------|-----|---|
| ZERO | 1. 1 [11] | 2 | 1 | |
| ZERO | bin alu_ops[11] | 0 | 1 | _ |
| | bin alu_ops[12] | 0 | 1 | _ |
| ZERO | | | | |
| ZERO | bin alu_ops[13] | 0 | 1 | _ |
| | verpoint #coverpoint2# | 100.00% | 100 | _ |
| Covered | 1 | | | |
| | covered/total bins: | 2 | 2 | - |
| | missing/total bins: | 0 | 2 | - |
| | % Hit: | 100.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 55 | 1 | _ |
| Covered | 1 | | | |
| | bin auto[1] | 10 | 1 | - |
| Covered | | | | |
| | verpoint #coverpoint3# | 100.00% | 100 | - |
| Covered | | | | |
| | covered/total bins: | 1 | 1 | _ |
| | missing/total bins: | 0 | 1 | - |
| | % Hit: | 100.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin pc_values | 65 | 1 | - |
| Covered | | | | |
| | verpoint #coverpoint4# | 0.00% | 100 | - |
| ZERO | covered/total bins: | 0 | 2 | _ |
| | covered, total bills. | v | ۷ | |
| | missing/total bins: | 2 | 2 | - |
| | % Hit: | 0.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | | | | |

| | type_option.comment= | | | |
|---------|------------------------|--------|-----|---|
| | bin auto[0] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[1] | 0 | 1 | _ |
| ZERO | | | | |
| Cov | verpoint #coverpoint5# | 0.00% | 100 | _ |
| ZERO | | | | |
| | covered/total bins: | 0 | 2 | _ |
| | | | | |
| | missing/total bins: | 2 | 2 | _ |
| | _ | | | |
| | % Hit: | 0.00% | 100 | _ |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[1] | 0 | 1 | _ |
| ZERO | | | | |
| | verpoint #coverpoint6# | 0.00% | 100 | _ |
| ZERO | | | | |
| | covered/total bins: | 0 | 1 | _ |
| | | | | |
| | missing/total bins: | 1 | 1 | _ |
| | 5. | | | |
| | % Hit: | 0.00% | 100 | _ |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin rd_addr | 0 | 1 | _ |
| ZERO | | | | |
| | verpoint #coverpoint7# | 50.00% | 100 | _ |
| Uncover | | | | |
| | covered/total bins: | 1 | 2 | _ |
| | | | | |
| | missing/total bins: | 1 | 2 | _ |
| | J. 1111 | | | |
| | % Hit: | 50.00% | 100 | _ |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 0 | 1 | _ |
| ZERO | 221 4460[0] | O | 1 | |

| Covered Sp.00% Sp.00% Covered Covered Sp.00% Sp.00% Covered Covered Sp.00% Sp.00% Covered Sp.00% Sp.00% Covered Sp.00% Sp.00% Covered Sp.00% Sp | | bin auto[1] | 65 | 1 | - |
|--|---------|-------------------------|--------|-----|---|
| Covered Cove | Covered | | | | |
| covered/total bins: 1 2 | Cov | verpoint #coverpoint8# | 50.00% | 100 | - |
| ### ### ### ### ### ### ### ### ### ## | Uncover | red | | | |
| <pre>type_option.weight=1 type_option.comment= bin auto[0] 65 1 Covered bin auto[1] 0 1 ZERO Coverpoint #coverpoint_9# 50.00% 100 missing/total bins: 1 2 % Hit: 50.00% 100 type_option.weight=1 type_option.comment= bin auto[0] 65 1 Covered % Hit: 50.00% 100 #### Touch and the coverpoint of t</pre> | | covered/total bins: | 1 | 2 | - |
| type_option.weight=1 type_option.comment= bin auto[0] 65 1 Covered bin auto[1] 0 1 ZERO Coverpoint #coverpoint_9# 50.00% 100 missing/total bins: 1 2 % Hit: 50.00% 100 type_option.weight=1 type_option.comment= bin auto[1] 65 1 Covered bin auto[1] 65 1 Covered % Hit: 50.00% 100 Lovered covered/total bins: 1 2 % Hit: 50.00% 100 Lovered type_option.weight=1 type_option.comment= bin auto[0] 65 1 Covered covered/total bins: 1 2 # Hit: 50.00% 100 Uncovered Lovered covered/total bins: 1 2 % Hit: 50.00% 100 type_option.weight=1 type_option.weight=1 type_option.weight=1 type_option.weight=1 type_option.weight=1 type_option.weight=1 type_option.comment= bin auto[0] 65 1 Covered type_option.comment= bin auto[0] 65 1 Covered Covered/total bins: 1 2 % Hit: 50.00% 100 Lovered type_option.comment= bin auto[0] 65 1 Covered Covered/total bins: 1 2 % Hit: 50.00% 100 Lovered type_option.comment= bin auto[0] 65 1 Covered | | missing/total bins: | 1 | 2 | - |
| type_option.goal=100 type_option.comment= bin auto[0] 65 1 | | % Hit: | 50.00% | 100 | - |
| type_option.comment= bin auto[0] 65 1 Covered bin auto[1] 0 1 EERO Coverpoint #coverpoint_9# 50.00% 100 Uncovered covered/total bins: 1 2 % Hit: 50.00% 100 type_option.weight=1 type_option.comment= bin auto[0] 65 1 Covered Coverpoint #coverpoint_10# 50.00% 100 EERO Coverpoint #coverpoint_10# 50.00% 100 Uncovered covered/total bins: 1 2 missing/total bins: 1 2 type_option.comment= bin auto[1] 50.00% 100 EERO Coverpoint #coverpoint_10# 50.00% 100 Uncovered type_option.weight=1 type_option.weight=1 type_option.weight=1 type_option.weight=1 type_option.weight=1 type_option.comment= bin auto[0] 65 1 Covered type_option.comment= bin auto[0] 65 1 Covered Covered | | type_option.weight=1 | | | |
| Din auto[0] 65 1 - Covered 50 1 - ZERO | | type_option.goal=100 | | | |
| Covered | | type_option.comment= | | | |
| Din auto[1] 0 1 | | bin auto[0] | 65 | 1 | - |
| Coverpoint #coverpoint_9# 50.00% 100 - Uncovered | Covered | | | | |
| Coverpoint #coverpoint_9# 50.00% 100 - 1 100 | | bin auto[1] | 0 | 1 | - |
| Covered Cove | ZERO | | | | |
| Covered/total bins: 1 2 - | Cov | verpoint #coverpoint9# | 50.00% | 100 | - |
| missing/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.comment= bin auto[0] 65 1 - Covered bin auto[1] 0 1 - ZERO Coverpoint #coverpoint_10# 50.00% 100 - Uncovered covered/total bins: 1 2 - missing/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.weight=1 type_option.comment= bin auto[0] 65 1 - Covered Covered/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.comment= bin auto[0] 65 1 - Covered | Uncover | | | | |
| % Hit: 50.00% 100 - type_option.weight=1 type_option.comment= bin auto[0] 65 1 - Covered 0 1 - ZERO 50.00% 100 - Uncovered 1 2 - missing/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] 65 1 - Covered 65 1 - | | covered/total bins: | 1 | 2 | - |
| type_option.weight=1 type_option.comment= bin auto[0] 65 1 - Covered bin auto[1] 0 10 10 10 10 10 10 10 10 10 10 10 10 1 | | missing/total bins: | 1 | 2 | - |
| type_option.goal=100 type_option.comment= bin auto[0] 65 1 - Covered 0 1 - ZERO 50.00% 100 - Uncovered 1 2 - missing/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.goal=100 type_option.comment= tipe_option.comment= 65 1 - bin auto[0] 65 1 - - | | % Hit: | 50.00% | 100 | - |
| type_option.comment= bin auto[0] 65 1 - Covered 0 1 - ZERO 50.00% 100 - Uncovered 2 - missing/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.goal=100 + - type_option.comment= bin auto[0] 65 1 - Covered | | type_option.weight=1 | | | |
| Din auto[0] | | type_option.goal=100 | | | |
| Covered bin auto[1] 0 1 - ZERO 50.00% 100 - Uncovered - - covered/total bins: 1 2 - missing/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.goal=100 - - type_option.comment= - - - bin auto[0] 65 1 - Covered | | type_option.comment= | | | |
| Din auto[1] 0 1 | | bin auto[0] | 65 | 1 | _ |
| ZERO Coverpoint #coverpoint_10# 50.00% 100 - Uncovered 1 2 - missing/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.goal=100 type_option.comment= - bin auto[0] 65 1 - Covered | Covered | | | | |
| Coverpoint #coverpoint_10# 50.00% 100 - Uncovered 1 2 - missing/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.goal=100 - - type_option.comment= bin auto[0] 65 1 - Covered Covered - - - | | bin auto[1] | 0 | 1 | - |
| Uncovered | ZERO | | | | |
| covered/total bins: 1 2 - missing/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.goal=100 - - type_option.comment= - - - bin auto[0] 65 1 - Covered | Cov | verpoint #coverpoint10# | 50.00% | 100 | - |
| missing/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] 65 1 Covered | Uncover | red | | | |
| <pre>% Hit: 50.00% 100 - type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] 65 1 -</pre> Covered | | covered/total bins: | 1 | 2 | - |
| <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] 65 1 -</pre> | | missing/total bins: | 1 | 2 | - |
| <pre>type_option.goal=100 type_option.comment= bin auto[0] 65 1 -</pre> Covered | | % Hit: | 50.00% | 100 | - |
| <pre>type_option.comment= bin auto[0] 65 1 - Covered</pre> | | type_option.weight=1 | | | |
| bin auto[0] 65 1 - Covered | | type_option.goal=100 | | | |
| Covered | | type_option.comment= | | | |
| | G. | | 65 | 1 | - |
| | covered | | 0 | 1 | - |

| Cor | verpoint #coverpoint11# | 50.00% | 100 | _ |
|------------|-------------------------|---------|-----|---|
| Uncover | | 30.000 | 100 | |
| 31100 V CI | covered/total bins: | 1 | 2 | - |
| | | _ | • | |
| | missing/total bins: | 1 | 2 | _ |
| | % Hit: | 50.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 65 | 1 | _ |
| Covered | | 03 | 1 | _ |
| covered | bin auto[1] | 0 | 1 | |
| ZEDO | bin auto[i] | 0 | 1 | _ |
| ZERO | romaint Haarramaint 12H | E0 00% | 100 | |
| | verpoint #coverpoint12# | 50.00% | 100 | _ |
| Uncover | | 1 | 0 | |
| | covered/total bins: | 1 | 2 | _ |
| | missing/total bins: | 1 | 2 | _ |
| | | | | |
| | % Hit: | 50.00% | 100 | - |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 65 | 1 | - |
| Covered | l | | | |
| | bin auto[1] | 0 | 1 | - |
| ZERO | | | | |
| Cov | verpoint #coverpoint13# | 100.00% | 100 | - |
| Covered | l | | | |
| | covered/total bins: | 2 | 2 | - |
| | | | | |
| | missing/total bins: | 0 | 2 | - |
| | | | | |
| | % Hit: | 100.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 55 | 1 | _ |
| Covered | I | | | |
| | bin auto[1] | 10 | 1 | _ |
| Covered | | | | |
| | | | | |

| | verpoint #coverpoint14# | 0.00% | 100 | - |
|----------------------------|---|-----------------------------|-------------------------|-------------|
| ZERO | covered/total bins: | 0 | 4 | - |
| | missing/total bins: | 4 | 4 | - |
| | % Hit: | 0.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin exceptions[0] | 0 | 1 | - |
| ZERO | | | | |
| | bin exceptions[1] | 0 | 1 | - |
| ZERO | | | | |
| | bin exceptions[2] | 0 | 1 | - |
| ZERO | | | | |
| | bin exceptions[3] | 0 | 1 | - |
| ZERO | | | | |
| Cor | verpoint #vif.i_opcode15# | 10.93% | 100 | - |
| Uncover | | | | |
| | covered/total bins: | 7 | 64 | _ |
| | | | | |
| | missing/total bins: | 57 | 64 | _ |
| | <pre>missing/total bins: % Hit:</pre> | 10.93% | 100 | - |
| | | | | - |
| | % Hit: | | | - |
| | % Hit: type_option.weight=1 | | | - |
| | <pre>% Hit: type_option.weight=1 type_option.goal=100</pre> | | | - |
| Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31]</pre> | 10.93% | 100 | - |
| Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31]</pre> | 10.93% | 100 | |
| Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] d bin auto[32:63]</pre> | 10.93% | 100 | - |
| | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] d bin auto[32:63]</pre> | 10.93% | 100 | |
| | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63]</pre> <pre>d bin auto[64:95]</pre> | 10.93% | 100 | - |
| Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63]</pre> <pre>d bin auto[64:95]</pre> | 10.93% | 100 | - - - |
| Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] d bin auto[32:63] d bin auto[64:95]</pre> | 10.93% 41 4 3 | 100 | - |
| Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] d bin auto[32:63] d bin auto[64:95]</pre> | 10.93% 41 4 3 | 100 | - |
| Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63] bin auto[4:95] bin auto[96:127]</pre> | 10.93% 41 4 3 | 100 1 1 1 | - |
| Covered Covered ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63] bin auto[4:95] bin auto[96:127]</pre> | 10.93% 41 4 3 | 100 1 1 1 | |
| Covered Covered ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63] bin auto[64:95] bin auto[64:95]</pre> bin auto[96:127] | 10.93% 41 4 3 0 | 100 1 1 1 1 | |
| Covered ZERO Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63] bin auto[64:95] bin auto[64:95]</pre> bin auto[96:127] | 10.93% 41 4 3 0 | 100 1 1 1 1 | |
| Covered ZERO Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63] bin auto[64:95] bin auto[64:95] bin auto[128:159] bin auto[128:159]</pre> | 10.93% 41 4 3 0 | 100 1 1 1 1 | |
| Covered ZERO Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:31] bin auto[32:63] bin auto[4:95] bin auto[96:127] bin auto[128:159] dibin auto[160:191]</pre> | 10.93% 41 4 3 0 | 100 1 1 1 1 | |

| Covered | bin auto[256:287] | 7 | 1 | - |
|---------|-------------------|---|---|---|
| ZERO | bin auto[288:319] | 0 | 1 | - |
| ZERO | bin auto[320:351] | 0 | 1 | - |
| ZERO | bin auto[352:383] | 0 | 1 | - |
| ZERO | bin auto[384:415] | 0 | 1 | - |
| ZERO | bin auto[416:447] | 0 | 1 | - |
| ZERO | bin auto[448:479] | 0 | 1 | - |
| ZERO | bin auto[480:511] | 0 | 1 | - |
| Covered | bin auto[512:543] | 6 | 1 | - |
| ZERO | bin auto[544:575] | 0 | 1 | - |
| ZERO | bin auto[576:607] | 0 | 1 | - |
| ZERO | bin auto[608:639] | 0 | 1 | - |
| ZERO | bin auto[640:671] | 0 | 1 | - |
| ZERO | bin auto[672:703] | 0 | 1 | - |
| ZERO | bin auto[704:735] | 0 | 1 | - |
| ZERO | bin auto[736:767] | 0 | 1 | - |
| ZERO | bin auto[768:799] | 0 | 1 | _ |
| ZERO | bin auto[800:831] | 0 | 1 | _ |
| ZERO | bin auto[832:863] | 0 | 1 | _ |
| ZERO | bin auto[864:895] | 0 | 1 | _ |
| ZERO | bin auto[896:927] | 0 | 1 | _ |
| ZERO | bin auto[928:959] | 0 | 1 | _ |
| ZERO | bin auto[960:991] | 0 | 1 | _ |

| ZERO | bin auto[992:1023] | 0 | 1 | - |
|---------|---|---|---|---|
| Covered | bin auto[1024:1055] | 1 | 1 | - |
| ZERO | bin auto[1056:1087] | 0 | 1 | - |
| ZERO | bin auto[1088:1119] | 0 | 1 | - |
| ZERO | bin auto[1120:1151] | 0 | 1 | - |
| ZERO | bin auto[1152:1183] | 0 | 1 | - |
| ZERO | bin auto[1184:1215] | 0 | 1 | - |
| ZERO | bin auto[1216:1247] | 0 | 1 | - |
| ZERO | bin auto[1248:1279] | 0 | 1 | - |
| ZERO | bin auto[1280:1311] | 0 | 1 | _ |
| ZERO | bin auto[1312:1343] | 0 | 1 | - |
| ZERO | bin auto[1344:1375] | 0 | 1 | - |
| ZERO | bin auto[1376:1407] | 0 | 1 | - |
| ZERO | bin auto[1408:1439] | 0 | 1 | - |
| ZERO | bin auto[1440:1471] | 0 | 1 | - |
| ZERO | bin auto[1472:1503] | 0 | 1 | - |
| ZERO | bin auto[1504:1535] | 0 | 1 | - |
| ZERO | bin auto[1536:1567] | 0 | 1 | - |
| ZERO | bin auto[1568:1599] | 0 | 1 | - |
| ZERO | bin auto[1600:1631] | 0 | 1 | _ |
| ZERO | bin auto[1632:1663] | 0 | 1 | - |
| ZERO | bin auto[1664:1695] bin auto[1696:1727] | 0 | 1 | _ |
| ZERO | DIN auto[1070.1727] | J | _ | _ |

| ZEDO | bin auto[1728:1759] | 0 | 1 | - |
|----------------------|---|-------------|------------------------------|------------------|
| ZERO | bin auto[1760:1791] | 0 | 1 | - |
| ZERO | bin auto[1792:1823] | 0 | 1 | - |
| ZERO | bin auto[1824:1855] | 0 | 1 | - |
| ZERO | bin auto[1856:1887] | 0 | 1 | - |
| ZERO | bin auto[1888:1919] | 0 | 1 | - |
| ZERO | bin auto[1920:1951] | 0 | 1 | - |
| ZERO | bin auto[1952:1983] | 0 | 1 | _ |
| ZERO | bin auto[1984:2015] | 0 | 1 | _ |
| ZERO | bin auto[2016:2047] | 0 | 1 | _ |
| ZERO | verpoint #vif.i_exception16# | 0.00% | 100 | |
| ZERO | verpoint #vii.i_exception10# | 0.00% | 100 | _ |
| | covered/total bins: | 0 | 16 | _ |
| | | | | |
| | missing/total bins: | 16 | 16 | - |
| | missing/total bins: % Hit: | 16 0.00% | 16 | - |
| | | | | - |
| | % Hit: | | | - |
| | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment=</pre> | 0.00% | 100 | - |
| | <pre>% Hit: type_option.weight=1 type_option.goal=100</pre> | | | - |
| ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0]</pre> | 0.00% | 100 | - |
| | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment=</pre> | 0.00% | 100 | - |
| ZERO ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0]</pre> | 0.00% | 100 | - |
| ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0]</pre> | 0.00% | 100 | - |
| | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0]</pre> | 0.00% | 100 | - - - |
| ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] bin auto[1]</pre> | 0.00% | 100 | - |
| ZERO ZERO ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] bin auto[1]</pre> | 0.00% | 100 | |
| ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] bin auto[1] bin auto[2]</pre> | 0.00% | 100 1 1 1 | - - - - |
| ZERO ZERO ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] bin auto[1] bin auto[2] bin auto[3] bin auto[4]</pre> | 0.00% | 100 1 1 1 1 1 | |
| ZERO ZERO ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] bin auto[1] bin auto[2] bin auto[3]</pre> | 0.00% | 100 1 1 1 1 | |

| ZERO | | | | |
|--------------------------------|---|-----------------------------|-----------------------|---|
| 2210 | bin auto[8] | 0 | 1 | _ |
| ZERO | ZII ddeo[o] | · · | _ | |
| | bin auto[9] | 0 | 1 | _ |
| ZERO | 211 000()] | Ç | _ | |
| 2110 | bin auto[10] | 0 | 1 | _ |
| ZERO | DIII ddco[10] | O | 1 | |
| ZEKO | bin auto[11] | 0 | 1 | |
| ZEDO. | DIN AULO[11] | U | 1 | _ |
| ZERO | 1.1 | | - | |
| | bin auto[12] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[13] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[14] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[15] | 0 | 1 | _ |
| ZERO | | | | |
| Cov | verpoint #vif.i_alu17# | 10.93% | 100 | _ |
| Uncover | red | | | |
| | covered/total bins: | 7 | 64 | _ |
| | | | | |
| | missing/total bins: | 57 | 64 | _ |
| | | | | |
| | | | | |
| | % Hit: | 10.93% | 100 | _ |
| | % Hit: | 10.93% | 100 | - |
| | | 10.93% | 100 | - |
| | type_option.weight=1 | 10.93% | 100 | - |
| | <pre>type_option.weight=1 type_option.goal=100</pre> | 10.93% | 100 | - |
| | <pre>type_option.weight=1 type_option.goal=100 type_option.comment=</pre> | | | - |
| Corrorad | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:255]</pre> | 10.93% | 100 | - |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:255]</pre> | 39 | 1 | - |
| | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511]</pre> | | | - |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511]</pre> | 39 | 1 | - |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767]</pre> | 39 | 1 | - |
| | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767]</pre> | 39 8 5 | 1 1 1 | - |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767]</pre> | 39 | 1 | - |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023]</pre> | 39 8 5 | 1 1 1 | - |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767]</pre> | 39 8 5 | 1 1 1 | |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279]</pre> | 39 8 5 | 1 1 1 | - |
| Covered Covered ZERO | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279]</pre> | 39 8 5 | 1 1 1 | - |
| Covered Covered ZERO | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279]</pre> | 39 8 5 0 | 1 1 1 1 | |
| Covered ZERO Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279]</pre> | 39 8 5 0 | 1 1 1 1 | |
| Covered ZERO Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279] bin auto[1280:1535]</pre> | 39 8 5 0 | 1 1 1 1 | |
| Covered ZERO Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279] bin auto[1280:1535]</pre> | 39 8 5 0 | 1 1 1 1 | |
| Covered ZERO Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279] bin auto[1280:1535]</pre> | 39 8 5 0 5 | 1 1 1 1 1 | |
| Covered ZERO Covered ZERO ZERO | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279] bin auto[1280:1535]</pre> | 39 8 5 0 5 | 1 1 1 1 1 | |
| Covered ZERO Covered ZERO ZERO | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0:255] bin auto[256:511] bin auto[512:767] bin auto[768:1023] bin auto[1024:1279] bin auto[1280:1535] bin auto[1792:2047] bin auto[2048:2303]</pre> | 39 8 5 0 5 0 | 1 1 1 1 1 | |

| ZERO | bin auto[2304:2559] | 0 | 1 | - |
|---------|---------------------|---|---|---|
| ZERO | bin auto[2560:2815] | 0 | 1 | - |
| ZERO | bin auto[2816:3071] | 0 | 1 | - |
| | bin auto[3072:3327] | 0 | 1 | - |
| ZERO | bin auto[3328:3583] | 0 | 1 | - |
| ZERO | bin auto[3584:3839] | 0 | 1 | - |
| ZERO | bin auto[3840:4095] | 0 | 1 | - |
| ZERO | bin auto[4096:4351] | 3 | 1 | - |
| Covered | bin auto[4352:4607] | 0 | 1 | - |
| ZERO | bin auto[4608:4863] | 0 | 1 | - |
| ZERO | bin auto[4864:5119] | 0 | 1 | _ |
| ZERO | bin auto[5120:5375] | 0 | 1 | - |
| ZERO | bin auto[5376:5631] | 0 | 1 | - |
| ZERO | bin auto[5632:5887] | 0 | 1 | - |
| ZERO | bin auto[5888:6143] | 0 | 1 | _ |
| ZERO | bin auto[6144:6399] | 0 | 1 | _ |
| ZERO | bin auto[6400:6655] | 0 | 1 | _ |
| ZERO | bin auto[6656:6911] | 0 | 1 | _ |
| ZERO | bin auto[6912:7167] | 0 | 1 | _ |
| ZERO | bin auto[7168:7423] | 0 | 1 | _ |
| ZERO | bin auto[7424:7679] | 0 | 1 | _ |
| ZERO | bin auto[7680:7935] | 0 | 1 | _ |
| ZERO | bin auto[7936:8191] | 0 | 1 | _ |
| ZERO | | | | |

| Covered | bin auto[8192:8447] | 3 | 1 | - |
|---------|-----------------------|---|---|---|
| ZERO | bin auto[8448:8703] | 0 | 1 | - |
| ZERO | bin auto[8704:8959] | 0 | 1 | - |
| ZERO | bin auto[8960:9215] | 0 | 1 | - |
| ZERO | bin auto[9216:9471] | 0 | 1 | - |
| ZERO | bin auto[9472:9727] | 0 | 1 | - |
| ZERO | bin auto[9728:9983] | 0 | 1 | - |
| ZERO | bin auto[9984:10239] | 0 | 1 | - |
| ZERO | bin auto[10240:10495] | 0 | 1 | - |
| ZERO | bin auto[10496:10751] | 0 | 1 | - |
| ZERO | bin auto[10752:11007] | 0 | 1 | - |
| ZERO | bin auto[11008:11263] | 0 | 1 | - |
| ZERO | bin auto[11264:11519] | 0 | 1 | - |
| ZERO | bin auto[11520:11775] | 0 | 1 | - |
| ZERO | bin auto[11776:12031] | 0 | 1 | - |
| ZERO | bin auto[12032:12287] | 0 | 1 | - |
| ZERO | bin auto[12288:12543] | 0 | 1 | - |
| ZERO | bin auto[12544:12799] | 0 | 1 | - |
| ZERO | bin auto[12800:13055] | 0 | 1 | - |
| ZERO | bin auto[13056:13311] | 0 | 1 | - |
| ZERO | bin auto[13312:13567] | 0 | 1 | - |
| ZERO | bin auto[13568:13823] | 0 | 1 | - |
| ZERO | bin auto[13824:14079] | 0 | 1 | - |
| | | | | |

| | bin auto[14080:14335] | 0 | 1 | - |
|---------------------------------|--|-----------------------|------------------|---|
| ZERO | bin auto[14336:14591] | 0 | 1 | - |
| ZERO | bin auto[14592:14847] | 0 | 1 | _ |
| ZERO | bin auto[14848:15103] | 0 | 1 | _ |
| ZERO | bin auto[15104:15359] | 0 | 1 | _ |
| ZERO | DIN auto[15104·15359] | Ü | 1 | _ |
| ZERO | bin auto[15360:15615] | 0 | 1 | - |
| ZERO | bin auto[15616:15871] | 0 | 1 | - |
| | bin auto[15872:16127] | 0 | 1 | - |
| ZERO | bin auto[16128:16383] | 0 | 1 | _ |
| ZERO | oss #cross0# | 0.41% | 100 | _ |
| Uncover | | 0.41% | 100 | |
| 01100 V C1 | covered/total bins: | 17 | 4096 | - |
| | missing/total bins: | 4079 | 4096 | - |
| | | | | |
| | % Hit: | 0.41% | 100 | - |
| | <pre>% Hit: type_option.weight=1</pre> | 0.41% | 100 | - |
| | | 0.41% | 100 | - |
| | <pre>type_option.weight=1 type_option.goal=100 type_option.comment=</pre> | 0.41% | 100 | - |
| | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins:</pre> | | | _ |
| | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[256:287],auto[8192:8447]></auto[256:287],auto[8192:8447]></pre> | 0.41% | 100 | - |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[256:287],auto[8192:8447]></auto[256:287],auto[8192:8447]></pre> | | | - |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[256:287],auto[8192:8447]> bin <auto[0:31],auto[8192:8447]></auto[0:31],auto[8192:8447]></auto[256:287],auto[8192:8447]></pre> | 1 | 1 | - |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[256:287],auto[8192:8447]> bin <auto[0:31],auto[8192:8447]> bin <auto[0:31],auto[4096:4351]></auto[0:31],auto[4096:4351]></auto[0:31],auto[8192:8447]></auto[256:287],auto[8192:8447]></pre> | 1 | 1 | - |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[256:287],auto[8192:8447]> bin <auto[0:31],auto[8192:8447]> bin <auto[0:31],auto[4096:4351]> bin <auto[512:543],auto[2048:2303]></auto[512:543],auto[2048:2303]></auto[0:31],auto[4096:4351]></auto[0:31],auto[8192:8447]></auto[256:287],auto[8192:8447]></pre> | 1 | 1 | |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[256:287],auto[8192:8447]> bin <auto[0:31],auto[8192:8447]> bin <auto[0:31],auto[4096:4351]> bin <auto[512:543],auto[2048:2303]></auto[512:543],auto[2048:2303]></auto[0:31],auto[4096:4351]></auto[0:31],auto[8192:8447]></auto[256:287],auto[8192:8447]></pre> | 1 2 3 | 1 1 1 | |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[256:287],auto[8192:8447]> bin <auto[0:31],auto[8192:8447]> bin <auto[0:31],auto[4096:4351]> bin <auto[512:543],auto[2048:2303]> bin <auto[0:31],auto[1024:1279]></auto[0:31],auto[1024:1279]></auto[512:543],auto[2048:2303]></auto[0:31],auto[4096:4351]></auto[0:31],auto[8192:8447]></auto[256:287],auto[8192:8447]></pre> | 1 2 3 2 | 1 1 1 | |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[256:287],auto[8192:8447]> bin <auto[0:31],auto[8192:8447]> bin <auto[0:31],auto[4096:4351]> bin <auto[512:543],auto[2048:2303]> bin <auto[0:31],auto[1024:1279]> bin <auto[32:63],auto[512:767]></auto[32:63],auto[512:767]></auto[0:31],auto[1024:1279]></auto[512:543],auto[2048:2303]></auto[0:31],auto[4096:4351]></auto[0:31],auto[8192:8447]></auto[256:287],auto[8192:8447]></pre> | 1 2 3 2 5 | 1 1 1 1 | |
| Covered Covered Covered Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[256:287],auto[8192:8447]> bin <auto[0:31],auto[8192:8447]> bin <auto[0:31],auto[4096:4351]> bin <auto[512:543],auto[2048:2303]> bin <auto[0:31],auto[1024:1279]> bin <auto[0:31],auto[512:767]> bin <auto[0:31],auto[512:767]></auto[0:31],auto[512:767]></auto[0:31],auto[512:767]></auto[0:31],auto[1024:1279]></auto[512:543],auto[2048:2303]></auto[0:31],auto[4096:4351]></auto[0:31],auto[8192:8447]></auto[256:287],auto[8192:8447]></pre> | 1 2 3 2 5 | 1 1 1 1 | |
| Covered | <pre>type_option.weight=1 type_option.goal=100 type_option.comment= Auto, Default and User Defined Bins: bin <auto[256:287],auto[8192:8447]> bin <auto[0:31],auto[8192:8447]> bin <auto[0:31],auto[4096:4351]> bin <auto[512:543],auto[2048:2303]> bin <auto[0:31],auto[1024:1279]> bin <auto[0:31],auto[512:767]> bin <auto[0:31],auto[512:767]></auto[0:31],auto[512:767]></auto[0:31],auto[512:767]></auto[0:31],auto[1024:1279]></auto[512:543],auto[2048:2303]></auto[0:31],auto[4096:4351]></auto[0:31],auto[8192:8447]></auto[256:287],auto[8192:8447]></pre> | 1 2 3 2 5 | 1 1 1 1 | |

| C | bin <auto[256:287],auto[256:511]></auto[256:287],auto[256:511]> | 1 | 1 | - |
|---------|---|----|---|----|
| Covered | bin <auto[0:31],auto[256:511]></auto[0:31],auto[256:511]> | 6 | 1 | - |
| Covered | bin <auto[1024:1055],auto[0:255]></auto[1024:1055],auto[0:255]> | 1 | 1 | - |
| Covered | bin <auto[512:543],auto[0:255]></auto[512:543],auto[0:255]> | 3 | 1 | _ |
| Covered | bin <auto[256:287],auto[0:255]></auto[256:287],auto[0:255]> | 5 | 1 | _ |
| Covered | bin <auto[128:159],auto[0:255]></auto[128:159],auto[0:255]> | 3 | 1 | _ |
| Covered | bin <auto[64:95],auto[0:255]></auto[64:95],auto[0:255]> | 3 | 1 | |
| Covered | | | | _ |
| Covered | bin <auto[32:63],auto[0:255]></auto[32:63],auto[0:255]> | 3 | 1 | - |
| Covered | bin <auto[0:31],auto[0:255]></auto[0:31],auto[0:255]> | 21 | 1 | - |
| ZERO | bin <auto[2016:2047],*></auto[2016:2047],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1984:2015],*></auto[1984:2015],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1952:1983],*></auto[1952:1983],*> | 0 | 1 | 64 |
| | bin <auto[1920:1951],*></auto[1920:1951],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1888:1919],*></auto[1888:1919],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1856:1887],*></auto[1856:1887],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1824:1855],*></auto[1824:1855],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1792:1823],*></auto[1792:1823],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1760:1791],*></auto[1760:1791],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1728:1759],*></auto[1728:1759],*> | 0 | 1 | 64 |
| ZERO | | | | |
| ZERO | bin <auto[1696:1727],*></auto[1696:1727],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1664:1695],*></auto[1664:1695],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1632:1663],*></auto[1632:1663],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1600:1631],*></auto[1600:1631],*> | 0 | 1 | 64 |
| | | | | |

| ZERO | bin <auto[1568:1599],*></auto[1568:1599],*> | 0 | 1 | 64 |
|------|---|---|---|----|
| ZERO | bin <auto[1536:1567],*></auto[1536:1567],*> | 0 | 1 | 64 |
| | bin <auto[1504:1535],*></auto[1504:1535],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1472:1503],*></auto[1472:1503],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1440:1471],*></auto[1440:1471],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1408:1439],*></auto[1408:1439],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1376:1407],*></auto[1376:1407],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1344:1375],*></auto[1344:1375],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1312:1343],*></auto[1312:1343],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1280:1311],*></auto[1280:1311],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1248:1279],*></auto[1248:1279],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1216:1247],*></auto[1216:1247],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1184:1215],*></auto[1184:1215],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1152:1183],*></auto[1152:1183],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1120:1151],*></auto[1120:1151],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1088:1119],*></auto[1088:1119],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1056:1087],*></auto[1056:1087],*> | 0 | 1 | 64 |
| ZERO | bin <auto[992:1023],*></auto[992:1023],*> | 0 | 1 | 64 |
| ZERO | bin <auto[960:991],*></auto[960:991],*> | 0 | 1 | 64 |
| ZERO | bin <auto[928:959],*></auto[928:959],*> | 0 | 1 | 64 |
| ZERO | bin <auto[896:927],*></auto[896:927],*> | 0 | 1 | 64 |
| ZERO | bin <auto[864:895],*></auto[864:895],*> | 0 | 1 | 64 |
| ZERO | bin <auto[832:863],*></auto[832:863],*> | 0 | 1 | 64 |
| ZERO | | | | |

| ZERO | bin <auto[800:831],*></auto[800:831],*> | 0 | 1 | 64 |
|--------------|---|---|---|----|
| | bin <auto[768:799],*></auto[768:799],*> | 0 | 1 | 64 |
| ZERO ZERO | bin <auto[736:767],*></auto[736:767],*> | 0 | 1 | 64 |
| | bin <auto[704:735],*></auto[704:735],*> | 0 | 1 | 64 |
| ZERO | bin <auto[672:703],*></auto[672:703],*> | 0 | 1 | 64 |
| ZERO | bin <auto[640:671],*></auto[640:671],*> | 0 | 1 | 64 |
| ZERO | bin <auto[608:639],*></auto[608:639],*> | 0 | 1 | 64 |
| ZERO | bin <auto[576:607],*></auto[576:607],*> | 0 | 1 | 64 |
| ZERO | bin <auto[544:575],*></auto[544:575],*> | 0 | 1 | 64 |
| ZERO | bin <auto[480:511],*></auto[480:511],*> | 0 | 1 | 64 |
| ZERO | bin <auto[448:479],*></auto[448:479],*> | 0 | 1 | 64 |
| ZERO | bin <auto[416:447],*></auto[416:447],*> | 0 | 1 | 64 |
| ZERO | bin <auto[384:415],*></auto[384:415],*> | 0 | 1 | 64 |
| ZERO | bin <auto[352:383],*></auto[352:383],*> | 0 | 1 | 64 |
| ZERO | bin <auto[320:351],*></auto[320:351],*> | 0 | 1 | 64 |
| ZERO | bin <auto[288:319],*></auto[288:319],*> | 0 | 1 | 64 |
| ZERO | bin <auto[224:255],*></auto[224:255],*> | 0 | 1 | 64 |
| ZERO | bin <auto[192:223],*></auto[192:223],*> | 0 | 1 | 64 |
| ZERO | bin <auto[160:191],*></auto[160:191],*> | 0 | 1 | 64 |
| ZERO | bin <auto[96:127],*></auto[96:127],*> | 0 | 1 | 64 |
| ZERO | bin <*,auto[16128:16383]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[15872:16127]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[15616:15871]> | 0 | 1 | 64 |
| ZERO | | | | |

| ZERO | bin <*,auto[15360:15615]> | 0 | 1 | 64 |
|------|---------------------------|---|---|----|
| ZERO | bin <*,auto[15104:15359]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[14848:15103]> | 0 | 1 | 64 |
| | bin <*,auto[14592:14847]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[14336:14591]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[14080:14335]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[13824:14079]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[13568:13823]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[13312:13567]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[13056:13311]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[12800:13055]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[12544:12799]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[12288:12543]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[12032:12287]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[11776:12031]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[11520:11775]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[11264:11519]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[11008:11263]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[10752:11007]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[10496:10751]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[10240:10495]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[9984:10239]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[9728:9983]> | 0 | 1 | 64 |
| ZERO | | | | |

| ZEDO | bin <*,auto[9472:9727]> | 0 | 1 | 64 |
|--------------|-------------------------|---|---|----|
| ZERO ZERO | bin <*,auto[9216:9471]> | 0 | 1 | 64 |
| | bin <*,auto[8960:9215]> | 0 | 1 | 64 |
| ZERO ZERO | bin <*,auto[8704:8959]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[8448:8703]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[7936:8191]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[7680:7935]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[7424:7679]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[7168:7423]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[6912:7167]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[6656:6911]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[6400:6655]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[6144:6399]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[5888:6143]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[5632:5887]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[5376:5631]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[5120:5375]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[4864:5119]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[4608:4863]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[4352:4607]> | 0 | 1 | 64 |
| | bin <*,auto[3840:4095]> | 0 | 1 | 64 |
| ZERO ZERO | bin <*,auto[3584:3839]> | 0 | 1 | 64 |
| | bin <*,auto[3328:3583]> | 0 | 1 | 64 |
| ZERO | | | | |

| | bin <*,auto[3072:3327]> | 0 | 1 | 64 |
|------|---|---|---|----|
| ZERO | bin <*,auto[2816:3071]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[2560:2815]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[2304:2559]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[1792:2047]> | 0 | 1 | 64 |
| ZERO | | | | |
| ZERO | bin <*,auto[1536:1791]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[1280:1535]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[768:1023]> | 0 | 1 | 64 |
| | bin <auto[1024:1055],auto[8192:8447]></auto[1024:1055],auto[8192:8447]> | 0 | 1 | 1 |
| ZERO | bin <auto[512:543],auto[8192:8447]></auto[512:543],auto[8192:8447]> | 0 | 1 | 1 |
| ZERO | bin <auto[128:159],auto[8192:8447]></auto[128:159],auto[8192:8447]> | 0 | 1 | 1 |
| ZERO | bin <auto[64:95],auto[8192:8447]></auto[64:95],auto[8192:8447]> | 0 | 1 | 1 |
| ZERO | | | | |
| ZERO | bin <auto[32:63],auto[8192:8447]></auto[32:63],auto[8192:8447]> | 0 | 1 | 1 |
| ZERO | bin <auto[1024:1055],auto[4096:4351]></auto[1024:1055],auto[4096:4351]> | 0 | 1 | 1 |
| ZERO | bin <auto[512:543],auto[4096:4351]></auto[512:543],auto[4096:4351]> | 0 | 1 | 1 |
| ZERO | bin <auto[256:287],auto[4096:4351]></auto[256:287],auto[4096:4351]> | 0 | 1 | 1 |
| | bin <auto[128:159],auto[4096:4351]></auto[128:159],auto[4096:4351]> | 0 | 1 | 1 |
| ZERO | bin <auto[64:95],auto[4096:4351]></auto[64:95],auto[4096:4351]> | 0 | 1 | 1 |
| ZERO | bin <auto[32:63],auto[4096:4351]></auto[32:63],auto[4096:4351]> | 0 | 1 | 1 |
| ZERO | bin <auto[1024:1055],auto[2048:2303]></auto[1024:1055],auto[2048:2303]> | 0 | 1 | 1 |
| ZERO | bin <auto[256:287],auto[2048:2303]></auto[256:287],auto[2048:2303]> | 0 | 1 | 1 |
| ZERO | | | | |
| ZERO | bin <auto[128:159],auto[2048:2303]></auto[128:159],auto[2048:2303]> | 0 | 1 | 1 |
| ZERO | bin <auto[64:95],auto[2048:2303]></auto[64:95],auto[2048:2303]> | 0 | 1 | 1 |
| | | | | |

| 5550 | bin <auto[32:63],auto[2048:2303]></auto[32:63],auto[2048:2303]> | 0 | 1 | 1 |
|-------------|---|-------|------|---|
| ZERO | bin <auto[0:31],auto[2048:2303]></auto[0:31],auto[2048:2303]> | 0 | 1 | 1 |
| ZERO | bin <auto[1024:1055],auto[1024:1279]></auto[1024:1055],auto[1024:1279]> | 0 | 1 | 1 |
| ZERO | bin <auto[512:543],auto[1024:1279]></auto[512:543],auto[1024:1279]> | 0 | 1 | 1 |
| ZERO | | | | |
| ZERO | bin <auto[256:287],auto[1024:1279]></auto[256:287],auto[1024:1279]> | 0 | 1 | 1 |
| ZERO | bin <auto[128:159],auto[1024:1279]></auto[128:159],auto[1024:1279]> | 0 | 1 | 1 |
| | bin <auto[64:95],auto[1024:1279]></auto[64:95],auto[1024:1279]> | 0 | 1 | 1 |
| ZERO | bin <auto[32:63],auto[1024:1279]></auto[32:63],auto[1024:1279]> | 0 | 1 | 1 |
| ZERO | bin <auto[1024:1055],auto[512:767]></auto[1024:1055],auto[512:767]> | 0 | 1 | 1 |
| ZERO | bin <auto[512:543],auto[512:767]></auto[512:543],auto[512:767]> | 0 | 1 | 1 |
| ZERO | | | | |
| ZERO | bin <auto[256:287],auto[512:767]></auto[256:287],auto[512:767]> | 0 | 1 | 1 |
| ZERO | bin <auto[128:159],auto[512:767]></auto[128:159],auto[512:767]> | 0 | 1 | 1 |
| ZERO | bin <auto[64:95],auto[512:767]></auto[64:95],auto[512:767]> | 0 | 1 | 1 |
| | bin <auto[1024:1055],auto[256:511]></auto[1024:1055],auto[256:511]> | 0 | 1 | 1 |
| ZERO | bin <auto[128:159],auto[256:511]></auto[128:159],auto[256:511]> | 0 | 1 | 1 |
| ZERO | bin <auto[64:95],auto[256:511]></auto[64:95],auto[256:511]> | 0 | 1 | 1 |
| ZERO | | 0 | 1 | |
| ZERO | bin <auto[32:63],auto[256:511]></auto[32:63],auto[256:511]> | 0 | 1 | 1 |
| Cro ZERO | oss #cross1# | 0.00% | 100 | - |
| | covered/total bins: | 0 | 1024 | - |
| | missing/total bins: | 1024 | 1024 | - |
| | % Hit: | 0.00% | 100 | _ |
| | | | | |

type_option.weight=1
type_option.goal=100

type_option.comment=

Auto, Default and User Defined Bins:

ZERO

Statement Coverage:

| Enabled Coverage | Bins | Hits | Misses | Coverage |
|------------------|------|------|--------|----------|
| | | | | |
| Statements | 391 | 298 | 93 | 76.21% |

Statement Coverage for Design Unit work.coverage_sv_unit --

| | | | - |
|-------------|------|-------|--------|
| Line | Item | Count | Source |
| | | | |
| File transa | | | |
| 143 | 1 | 579 | |
| 144 | 1 | 579 | |
| 145 | 1 | 579 | |
| 146 | 1 | 579 | |
| 147 | 1 | 579 | |
| 148 | 1 | 579 | |
| 149 | 1 | 579 | |
| 152 | 1 | 579 | |
| 153 | 1 | 579 | |
| 154 | 1 | 579 | |
| 155 | 1 | 579 | |
| 156 | 1 | 579 | |
| 157 | 1 | 579 | |
| 158 | 1 | 579 | |
| 159 | 1 | 579 | |
| 160 | 1 | 579 | |
| 161 | 1 | 579 | |
| 164 | 1 | 579 | |
| 165 | 1 | 579 | |
| 166 | 1 | 579 | |
| 167 | 1 | 579 | |
| 168 | 1 | 579 | |
| 169 | 1 | 579 | |
| 170 | 1 | 579 | |
| 171 | 1 | 579 | |
| 172 | 1 | 579 | |
| 173 | 1 | 579 | |
| 174 | 1 | 579 | |
| 175 | 1 | 579 | |
| 176 | 1 | 579 | |
| 177 | 1 | 579 | |
| 178 | 1 | 579 | |
| | | | |

| 1 | 79 | 1 | 579 |
|--------|---------------|---|---------|
| 1 | 80 | 1 | 579 |
| 1 | 81 | 1 | 579 |
| 1 | 82 | 1 | 579 |
| 1 | 99 | 1 | 25 |
| 2 | 00 | 1 | 25 |
| 2 | 01 | 1 | 25 |
| 2 | 02 | 1 | 25 |
| 2 | 03 | 1 | 25 |
| 2 | 04 | 1 | 25 |
| 2 | 05 | 1 | 25 |
| 2 | 26 | 1 | 12 |
| 2 | 28 | 1 | 6 |
| 2 | 30 | 1 | 2 |
| 2 | 32 | 1 | 3 |
| 2 | 34 | 1 | 6 |
| 2 | 36 | 1 | 9 |
| 2 | 38 | 1 | 4 |
| 2 | 40 | 1 | 5 |
| 2 | 43 | 1 | 9 |
| 2 | 44 | 1 | 6 |
| 2 | 45 | 1 | 5 |
| 2 | 46 | 1 | 2 |
| 2 | 48 | 1 | 3 |
| 2 | 49 | 1 | 3 |
| 2 | 50 | 1 | ***0*** |
| 2 | 52 | 1 | 75 |
| 2 | 64 | 1 | 75 |
| | 65 | 1 | 75 |
| | 66 | 1 | 75 |
| | 67 | 1 | 75 |
| | 68 | 1 | 75 |
| | 69 | 1 | 75 |
| | 70 | 1 | 75 |
| | 71 | 1 | 75 |
| | 72 | 1 | 75 |
| | e coverage.sv | 1 | |
| 1 6 | | 1 | 1 |
| 6 | | 1 | 1 |
| 6 | | 1 | 1 |
| 6 | | 1 | 1 |
| 6 | | 1 | 502 |
| 7 | | 1 | 65 |
| 7 | | 1 | ***0*** |
| 7 | | 1 | ***0*** |
| , | - | _ | ŭ |

| 79 | | 1 | ***0*** |
|------|--------------|---|---------|
| 80 | | 1 | ***0*** |
| 81 | | 1 | ***0*** |
| 82 | | 1 | ***0*** |
| 87 | | 1 | ***0*** |
| 88 | | 1 | ***0*** |
| 89 | | 1 | ***0*** |
| 90 | | 1 | ***0*** |
| 91 | | 1 | ***0*** |
| 92 | | 1 | ***0*** |
| 93 | | 1 | ***0*** |
| 98 | | 1 | 1 |
| 99 | | 1 | ***0*** |
| 100 | 0 | 1 | ***0*** |
| File | driver.sv | | |
| 27 | | 1 | 1 |
| 28 | | 1 | 1 |
| 34 | | 1 | 1 |
| 35 | | 1 | 76 |
| 36 | | 1 | 75 |
| 37 | | 1 | 75 |
| 46 | | 1 | 75 |
| 47 | | 1 | 75 |
| 48 | | 1 | 75 |
| 49 | | 1 | 75 |
| 50 | | 1 | 75 |
| 51 | | 1 | 75 |
| 52 | | 1 | 75 |
| 53 | | 1 | 75 |
| 54 | | 1 | 75 |
| 55 | | 1 | 75 |
| 56 | | 1 | 75 |
| 57 | | 1 | 75 |
| 58 | | 1 | 75 |
| 61 | | 1 | 75 |
| 63 | | 1 | 75 |
| 64 | | 1 | 75 |
| | generator.sv | | |
| 55 | | 1 | 1 |
| 62 | | 1 | 1 |
| 63 | | 1 | 1 |
| 72 | | 1 | 1 |
| 75 | | 1 | 1 |
| 77 | | 1 | 1 |
| 80 | | 1 | 1 |
| 91 | | 1 | 1 |
| | | | - |

| 94 | 1 | 1 |
|-----|---|---------------|
| 97 | 1 | 1 |
| 100 | 1 | 1 |
| 103 | 1 | 1 |
| 106 | 1 | 1 |
| 109 | 1 | 1 |
| 112 | 1 | 1 |
| 115 | 1 | 1 |
| 125 | 1 | 1 |
| 125 | 2 | 50 |
| 127 | 1 | 50 |
| 128 | 1 | 50 |
| 134 | 1 | 17 |
| 138 | 1 | 17 |
| 150 | 1 | * * * 0 * * * |
| 153 | 1 | 50 |
| 156 | 1 | 50 |
| 159 | 1 | 50 |
| 169 | 1 | 1 |
| 171 | 1 | 1 |
| 172 | 1 | 1 |
| 175 | 1 | 1 |
| 177 | 1 | 1 |
| 178 | 1 | 1 |
| 181 | 1 | 1 |
| 183 | 1 | 1 |
| 184 | 1 | 1 |
| 187 | 1 | 1 |
| 189 | 1 | 1 |
| 190 | 1 | 1 |
| 199 | 1 | 1 |
| 201 | 1 | 1 |
| 202 | 1 | 1 |
| 205 | 1 | 1 |
| 207 | 1 | 1 |
| 208 | 1 | 1 |
| 211 | 1 | 1 |
| 213 | 1 | 1 |
| 214 | 1 | 1 |
| 223 | 1 | 1 |
| 225 | 1 | 1 |
| 226 | 1 | 1 |
| 229 | 1 | 1 |
| 231 | 1 | 1 |
| 232 | 1 | 1 |
| 235 | 1 | 1 |

| 237 | 1 | 1 |
|-----|---|---|
| 238 | 1 | 1 |
| 247 | 1 | 1 |
| 249 | 1 | 1 |
| 250 | 1 | 1 |
| 253 | 1 | 1 |
| 255 | 1 | 1 |
| 256 | 1 | 1 |
| 259 | 1 | 1 |
| 261 | 1 | 1 |
| 262 | 1 | 1 |
| 265 | 1 | 1 |
| 267 | 1 | 1 |
| 268 | 1 | 1 |
| 277 | 1 | 1 |
| 278 | 1 | 1 |
| 279 | 1 | 1 |
| 282 | 1 | 1 |
| 283 | 1 | 1 |
| 284 | 1 | 1 |
| 293 | 1 | 1 |
| 295 | 1 | 1 |
| 296 | 1 | 1 |
| 299 | 1 | 1 |
| 301 | 1 | 1 |
| 302 | 1 | 1 |
| 311 | 1 | 1 |
| 312 | 1 | 1 |
| 313 | 1 | 1 |
| 316 | 1 | 1 |
| 317 | 1 | 1 |
| 318 | 1 | 1 |
| 327 | 1 | 1 |
| 328 | 1 | 1 |
| 329 | 1 | 1 |
| 332 | 1 | 1 |
| 333 | 1 | 1 |
| 334 | 1 | 1 |
| 343 | 1 | 1 |
| 344 | 1 | 1 |
| 345 | 1 | 1 |
| 348 | 1 | 1 |
| 349 | 1 | 1 |
| 350 | 1 | 1 |
| 356 | 1 | 1 |
| 357 | 1 | 1 |
| | | |

| 358 | 1 | 1 |
|-----------------|---|---------|
| 373 | 1 | 12 |
| 374 | 1 | 6 |
| 375 | 1 | 2 |
| 376 | 1 | 3 |
| 377 | 1 | 6 |
| 378 | 1 | 9 |
| 379 | 1 | 4 |
| 380 | 1 | 5 |
| 381 | 1 | 9 |
| 382 | 1 | 6 |
| 383 | 1 | 5 |
| 384 | 1 | 2 |
| 385 | 1 | 3 |
| 386 | 1 | 3 |
| 387 | 1 | ***0*** |
| 392 | 1 | 21 |
| 393 | 1 | 4 |
| 394 | 1 | 6 |
| 395 | 1 | 7 |
| 396 | 1 | 7 |
| 397 | 1 | 4 |
| 398 | 1 | 4 |
| 399 | 1 | 3 |
| 400 | 1 | 7 |
| 401 | 1 | 6 |
| 402 | 1 | 2 |
| 403 | 1 | 4 |
| 408 | 1 | 75 |
| 409 | 1 | 75 |
| 410 | 1 | 75 |
| 411 | 1 | 75 |
| 412 | 1 | 75 |
| 413 | 1 | 75 |
| 414 | 1 | 75 |
| 415 | 1 | 75 |
| 416 | 1 | 75 |
| 417 | 1 | 75 |
| 420 | 1 | 75 |
| File monitor.sv | τ | |
| 18 | 1 | 1 |
| 31 | 1 | 1 |
| 32 | 1 | 1 |
| 44 | 1 | 1 |
| 45 | 1 | 1 |
| 47 | 1 | 502 |
| | | |

| 49 | 1 | 502 |
|-----|---|---------------|
| 52 | 1 | 65 |
| 53 | 1 | 65 |
| 54 | 1 | 65 |
| 55 | 1 | 65 |
| 56 | 1 | 65 |
| 57 | 1 | 65 |
| 58 | 1 | 65 |
| 59 | 1 | 65 |
| 60 | 1 | 65 |
| 61 | 1 | 65 |
| 62 | 1 | 65 |
| 63 | 1 | 65 |
| 64 | 1 | 65 |
| 65 | 1 | 65 |
| 66 | 1 | 65 |
| 67 | 1 | 65 |
| 70 | 1 | 65 |
| 73 | 1 | ***0*** |
| 88 | 1 | 1 |
| 92 | 1 | 1 |
| 105 | 1 | 1 |
| 106 | 1 | 1 |
| 119 | 1 | 1 |
| 120 | 1 | 1 |
| 122 | 1 | 1 |
| 124 | 1 | 1 |
| 126 | 1 | 1 |
| 129 | 1 | ***0*** |
| 130 | 1 | * * * 0 * * * |
| 131 | 1 | ***0*** |
| 132 | 1 | * * * 0 * * * |
| 133 | 1 | ***0*** |
| 134 | 1 | ***0*** |
| 135 | 1 | ***0*** |
| 136 | 1 | ***0*** |
| 137 | 1 | ***0*** |
| 138 | 1 | ***0*** |
| 139 | 1 | ***0*** |
| 140 | 1 | ***0*** |
| 141 | 1 | ***0*** |
| 142 | 1 | ***0*** |
| 143 | 1 | ***0*** |
| 144 | 1 | ***0*** |
| 145 | 1 | ***0*** |
| 146 | 1 | ***0*** |
| | | |

| 147 | 1 | ***0*** |
|-------------|---------|----------|
| 150 | 1 | ***0*** |
| 152 | 1 | ***0*** |
| 154 | 1 | ***0*** |
| File scoreb | oard.sv | |
| 16 | 1 | 1 |
| 17 | 1 | 1 |
| 43 | 1 | 1 |
| 44 | 1 | 1 |
| 51 | 1 | 1 |
| 52 | 1 | 1 |
| 61 | 1 | 1 |
| 62 | 1 | 1 |
| 73 | 1 | 1 |
| 74 | 1 | 66 |
| 75 | 1 | 66 |
| 76 | 1 | 65 |
| 77 | 1 | 65 |
| 80 | 1 | 65 |
| 81 | 1 | 65 |
| 82 | 1 | 65 |
| 83 | 1 | 65 |
| 84 | 1 | 65 |
| 85 | 1 | 65 |
| 86 | 1 | 65 |
| 87 | 1 | 65 |
| 88 | 1 | 65 |
| 89 | 1 | 65 |
| 90 | 1 | 65 65 |
| 91 | 1 | |
| 92 93 | 1 1 | 65 65 |
| 93 | 1 | 65 |
| 95 | 1 | 65 |
| 131 | 1 | 1 |
| 132 | 1 | 1 |
| 133 | 1 | ***0*** |
| 134 | 1 | ***0*** |
| 135 | 1 | ***0*** |
| 136 | 1 | ***0*** |
| 137 | 1 | ***0*** |
| 140 | 1 | ***0*** |
| 141 | 1 | ***0*** |
| 142 | 1 | ***0*** |
| 143 | 1 | ***0*** |
| 144 | 1 | ***0*** |
| | | |

| 145 | 1 | ***0*** |
|-----|---|---------|
| 146 | 1 | ***0*** |
| 147 | 1 | ***0*** |
| 148 | 1 | ***0*** |
| 149 | 1 | ***0*** |
| 150 | 1 | ***0*** |
| 151 | 1 | ***0*** |
| 152 | 1 | ***0*** |
| 153 | 1 | ***0*** |
| 154 | 1 | ***0*** |
| 161 | 1 | ***0*** |
| 164 | 1 | ***0*** |
| 173 | 1 | ***0*** |
| 183 | 1 | ***0*** |
| 189 | 1 | ***0*** |
| 192 | 1 | ***0*** |
| 196 | 1 | ***0*** |
| 202 | 1 | ***0*** |
| 207 | 1 | ***0*** |
| 211 | 1 | ***0*** |
| 218 | 1 | ***0*** |
| 222 | 1 | ***0*** |
| 242 | 1 | ***0*** |
| 248 | 1 | ***0*** |
| 250 | 1 | ***0*** |
| 252 | 1 | ***0*** |
| 258 | 1 | ***0*** |
| 308 | 1 | ***0*** |
| 309 | 1 | ***0*** |
| 310 | 1 | ***0*** |
| 312 | 1 | ***0*** |
| 313 | 1 | ***0*** |
| 314 | 1 | ***0*** |
| 315 | 1 | ***0*** |
| 316 | 1 | ***0*** |
| 317 | 1 | ***0*** |
| 318 | 1 | ***0*** |
| 319 | 1 | ***0*** |
| 320 | 1 | ***0*** |
| 321 | 1 | ***0*** |
| 322 | 1 | ***0*** |
| 323 | 1 | ***0*** |
| | | |

=== Design Unit: work.rv32i_alu

Branch Coverage:

| Enabled Coverage | Bins | Hits | Misses | Coverage |
|------------------|------|------|--------|----------|
| | | | | |
| Branches | 62 | 54 | 8 | 87.09% |

| Branch Coverage for Design Unit work.rv32i_alu | | | | | | | |
|--|-------------------|----------------|-----------------------|--|--|--|--|
| Line | Item | Count | Source | | | | |
| | | | | | | | |
| File rv32i_ | alu.sv | | | | | | |
| | | IF Branch | | | | | |
| 174 | | 76 | Count coming in to IF | | | | |
| 174 | 1 | 76 | | | | | |
| 178 | 1 | ***0*** | | | | | |
| Branch totals | : 1 hit of 2 bran | nches = 50.00% | | | | | |
| | | | | | | | |
| | | IF Branch | | | | | |
| 179 | | ***0*** | Count coming in to IF | | | | |
| 179 | 1 | ***0*** | | | | | |
| | | ***0*** | All False Count | | | | |
| Branch totals: 0 hits of 2 branches = 0.00% | | | | | | | |
| | | | | | | | |
| | | IF Branch | | | | | |
| 198 | | ***0*** | Count coming in to IF | | | | |
| 198 | 1 | ***0*** | | | | | |
| 201 | 1 | ***0*** | | | | | |
| 204 | 1 | ***0*** | | | | | |
| | | ***0*** | All False Count | | | | |
| Pranch totals: 0 hits of 4 hranches - 0 00% | | | | | | | |

Branch totals: 0 hits of 4 branches = 0.00%

| | | IF Branch | |
|-----|---|-----------|-----------------------|
| 218 | | 75 | Count coming in to IF |
| 218 | 1 | 11 | |
| 218 | 2 | 64 | |

Branch totals: 2 hits of 2 branches = 100.00%

| | | IF Branch | |
|-----|---|-----------------|----------|
| 220 | | 75 Count coming | in to IF |
| 220 | 1 | 28 | |
| 220 | 2 | 47 | |

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch------

64 All False Count

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

224 76 Count coming in to IF

224 1 6

70 All False Count

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

225 76 Count coming in to IF

225 1 5

71 All False Count

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

227 5 Count coming in to IF

227 1 2

3 All False Count

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

227 2 Count coming in to IF

227 2

227 3 ***0***

Branch totals: 1 hit of 2 branches = 50.00%

-----IF Branch-----

229 76 Count coming in to IF

229 1 6

70 All False Count

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

230 76 Count coming in to IF

230 1 9

67 All False Count

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

231 76 Count coming in to IF

231 1

72 All False Count

Branch totals: 2 hits of 2 branches = 100.00%

| | | IF Branch | |
|---|--|--|--|
| 232 | | 76 | |
| 232 | 1 | 5 | |
| | _ | | All False Count |
| Branch totals: | 2 hits of 2 br | anches = 100.00% | 1122 2 4 2 5 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 |
| 2241311 000412 | _ 11102 01 _ 21 | 200,000 | |
| | | IF Branch | |
| 233 | | 76 | Count coming in to IF |
| 233 | 1 | 9 | |
| | | 67 | All False Count |
| Branch totals: | 2 hits of 2 br | anches = 100.00% | |
| | | | |
| | | IF Branch | |
| 234 | | 76 | Count coming in to IF |
| 234 | 1 | 6 | |
| | | 70 | All False Count |
| Branch totals: | 2 hits of 2 br | anches = 100.00% | |
| | | | |
| | | IF Branch | |
| 235 | | 76 | Count coming in to IF |
| 235 | 1 | 7 | |
| | | 69 | All False Count |
| Branch totals: | 2 hits of 2 br | anches = 100.00% | |
| | | | |
| | | | |
| | | IF Branch | |
| 237 | | IF Branch7 | Count coming in to IF |
| | 1 | | |
| 237 | | 7 | |
| 237 237 | 1 | 7 2 | Count coming in to IF |
| 237 237 | 1 | 7 2 5 | Count coming in to IF |
| 237 237 Branch totals: | 1 2 hits of 2 br | 7 2 5 anches = 100.00% | Count coming in to IF |
| 237 237 Branch totals: | 1 2 hits of 2 br | 7 2 5 anches = 100.00% | Count coming in to IF All False Count |
| 237 237 Branch totals: | 1 2 hits of 2 br | 7 2 5 anches = 100.00% | Count coming in to IF All False Count |
| 237 237 Branch totals: | 1 2 hits of 2 br | 7 2 5 anches = 100.00% IF Branch | Count coming in to IF All False Count |
| 237 237 Branch totals: | 1 2 hits of 2 br | 7 2 5 anches = 100.00% IF Branch 76 6 | Count coming in to IF All False Count Count coming in to IF |
| 237 237 Branch totals:239 239 Branch totals: | 1 2 hits of 2 br 1 2 hits of 2 br | 7 2 5 anches = 100.00%IF Branch 76 6 70 anches = 100.00% | Count coming in to IF All False Count Count coming in to IF All False Count |
| 237 237 Branch totals: 239 239 Branch totals: | 1 2 hits of 2 br 1 2 hits of 2 br | 7 2 5 anches = 100.00%IF Branch 76 6 70 anches = 100.00% | Count coming in to IF All False Count Count coming in to IF All False Count |
| 237 237 Branch totals: 239 239 Branch totals: | 1 2 hits of 2 br 1 2 hits of 2 br | 7 2 5 anches = 100.00% IF Branch 76 6 70 anches = 100.00% IF Branch 6 | Count coming in to IF All False Count Count coming in to IF All False Count |
| 237 237 Branch totals: 239 239 Branch totals: | 1 2 hits of 2 br 1 2 hits of 2 br | 7 2 5 anches = 100.00%IF Branch 76 6 70 anches = 100.00%IF Branch 6 3 | Count coming in to IF All False Count Count coming in to IF All False Count Count coming in to IF |
| 237 237 Branch totals: 239 239 Branch totals: 241 241 | 1 2 hits of 2 br 1 2 hits of 2 br | 7 2 5 anches = 100.00% IF Branch 76 6 70 anches = 100.00% IF Branch 6 3 3 | Count coming in to IF All False Count Count coming in to IF All False Count |
| 237 237 Branch totals: 239 239 Branch totals: 241 241 | 1 2 hits of 2 br 1 2 hits of 2 br | 7 2 5 anches = 100.00%IF Branch 76 6 70 anches = 100.00%IF Branch 6 3 | Count coming in to IF All False Count Count coming in to IF All False Count Count coming in to IF |
| 237 237 Branch totals: | 1 2 hits of 2 br 1 2 hits of 2 br 1 2 hits of 2 br | 7 2 5 anches = 100.00%IF Branch 76 6 70 anches = 100.00%IF Branch 6 3 3 anches = 100.00% | Count coming in to IF All False Count Count coming in to IF All False Count Count coming in to IF All False Count |
| 237 237 Branch totals: 239 239 Branch totals: 241 241 Branch totals: | 1 2 hits of 2 br 1 2 hits of 2 br 1 2 hits of 2 br | 7 2 5 anches = 100.00% IF Branch 76 6 70 anches = 100.00% IF Branch 6 3 3 anches = 100.00% | Count coming in to IF All False Count Count coming in to IF All False Count Count coming in to IF All False Count |
| 237 237 Branch totals: | 1 2 hits of 2 br 1 2 hits of 2 br 1 2 hits of 2 br | 7 2 5 anches = 100.00% IF Branch 76 6 70 anches = 100.00% IF Branch 6 3 3 anches = 100.00% | Count coming in to IF All False Count Count coming in to IF All False Count Count coming in to IF All False Count |
| 237 237 Branch totals: 239 239 Branch totals: 241 241 Branch totals: | 1 2 hits of 2 br 1 2 hits of 2 br 1 2 hits of 2 br | 7 2 5 anches = 100.00% IF Branch 76 6 70 anches = 100.00% IF Branch 6 3 3 anches = 100.00% | Count coming in to IF All False Count Count coming in to IF All False Count Count coming in to IF All False Count |

| | Z IIICS OI Z DIGIICI | nes = 100.00% | |
|----------------|----------------------|---------------|-----------------------|
| | | IF Branch | |
| 257 | | 96 | Count coming in to IF |
| 257 | 1 | 94 | J |
| | | 2 | All False Count |
| Branch totals: | 2 hits of 2 branch | nes = 100.00% | |
| | | IF Branch | |
| 258 | | 94 | Count coming in to IF |
| 258 | 1 | 37 | |
| | | | All False Count |
| ranch totals: | 2 hits of 2 branch | nes = 100.00% | |
| | | IF Branch | |
| 259 | | 94 | Count coming in to IF |
| 259 | 1 | 3 | |
| | | 91 | All False Count |
| ranch totals: | 2 hits of 2 branch | nes = 100.00% | |
| | | IF Branch | |
| 266 | | 94 | Count coming in to IF |
| 266 | 1 | 12 | |
| | | 82 | All False Count |
| ranch totals: | 2 hits of 2 branch | nes = 100.00% | |
| | | IF Branch | |
| 267 | | 12 | Count coming in to IF |
| 267 | 1 | 8 | |
| | | 4 | All False Count |
| ranch totals: | 2 hits of 2 branch | nes = 100.00% | |
| | | IF Branch | |
| 277 | | 96 | Count coming in to IF |
| 277 | 1 | 4 | |
| | | 92 | All False Count |
| Branch totals: | 2 hits of 2 branch | nes = 100.00% | |

| | | IF Branch | |
|----------------|-------------|--------------------|-----------------------|
| 278 | | 96 | Count coming in to IF |
| 278 | 1 | 7 | |
| | | 89 | All False Count |
| Branch totals: | 2 hits of 2 | branches = 100.00% | |

-----IF Branch-----

 280
 1
 23

 283
 1
 73

Branch totals: 2 hits of 2 branches = 100.00%

-----IF Branch-----

287 96 Count coming in to IF

287 1 6

290 1 90

Branch totals: 2 hits of 2 branches = 100.00%

Condition Coverage:

Enabled Coverage
Bins Covered Misses Coverage
Conditions
Bins Covered Misses Coverage

Condition Coverage for Design Unit work.rv32i_alu --

File rv32i_alu.sv

-----Focused Condition View-----

Line 179 Item 1 (i_ce && ~stall_bit)

Condition totals: 0 of 2 input terms covered = 0.00%

Input Term Covered Reason for no coverage Hint

------ ------ -------

i_ce N No hits Hit '_0' and '_1'

stall_bit N No hits Hit '_0' and '_1'

Rows: Hits FEC Target Non-masking condition(s)

Row 1: ***0*** i_ce_0 -

Row 2: ***0*** i_ce_1 ~stall_bit

Row 3: ***0*** stall_bit_0 i_ce

Row 4: ***0*** stall_bit_1 i_ce

------Focused Condition View------

Line 198 Item 1 (i_flush && ~stall_bit)

Condition totals: 0 of 2 input terms covered = 0.00%

Input Term Covered Reason for no coverage Hint

i_flush N No hits Hit '_0' and '_1'

stall_bit N No hits Hit '_0' and '_1'

```
Rows:
         Hits FEC Target
                                Non-masking condition(s)
 Row 1: ***0*** i_flush_0
         ***0*** i_flush_1
 Row 2:
                                ~stall_bit
 Row 3: ***0*** stall_bit_0
                                i_flush
         ***0*** stall_bit_1
 Row 4:
                                i_flush
------Focused Condition View------
Line 204 Item 1 (stall_bit && ~i_stall)
Condition totals: 0 of 2 input terms covered = 0.00%
 Input Term Covered Reason for no coverage Hint
______
  stall_bit
              N No hits
                                   Hit '_0' and '_1'
             N No hits
                                   Hit '_0' and '_1'
   i_stall
   Rows: Hits FEC Target
                                Non-masking condition(s)
 -----
 Row 1: ***0*** stall_bit_0
         ***0*** stall_bit_1
 Row 2:
                                ~i_stall
 Row 3: ***0*** i_stall_0
                                stall_bit
         ***0*** i_stall_1
 Row 4:
                                stall_bit
-----Focused Condition View-----
        218 Item 1 (opcode_jal || opcode_auipc)
Condition totals: 2 of 2 input terms covered = 100.00%
  Input Term Covered Reason for no coverage Hint
  opcode_jal
                Y
 opcode_auipc
   Rows: Hits FEC Target
                                Non-masking condition(s)
 ______ ____
 Row 1:
             1 opcode_jal_0
                                ~opcode_auipc
 Row 2:
             1 opcode_jal_1
 Row 3:
             1 opcode_auipc_0
                                ~opcode_jal
           1 opcode_auipc_1
 Row
    4:
                               ~opcode_jal
------Focused Condition View------
        220 Item 1 (opcode_rtype || opcode_branch)
Line
Condition totals: 2 of 2 input terms covered = 100.00%
   Input Term Covered Reason for no coverage Hint
  opcode_rtype
```

0

0 b[31]_1

4:

Row

| | | | FEC Target | | | condition(s) |
|--------------------------------------|----------|-----------|---------------|------------|--------------|--------------------------|
| | 1: | 1 | | | | |
| | 2: | | opcode_rtype | | ~opcode_brar | 1011 |
| | 3: | | | | ~opcode_rtyp | ne. |
| | 4: | | | | ~opcode_rtyp | |
| | | | <u>-</u> | <u>-</u> - | or or mo 1/1 | |
| | | Focused | d Condition ' | View | | - |
| Line | 225 | 5 Item | 1 (alu_slt | alu_sl | tu) | |
| Conditi | ion tota | als: 2 of | 2 input term | ms covered | = 100.00% | |
| | | | Reason for | | ge Hint | |
| | | Y | | | | |
| | | Y | | | | |
| | | | | | | |
| Ro | | | FEC Target | | | condition(s) |
| Row | 1: | 1 | alu_slt_0 | | ~alu_sltu | |
| Row | 2: | 1 | alu_slt_1 | | _ | |
| Row | 3: | 1 | alu_sltu_0 | | ~alu_slt | |
| Row | 4: | 1 | alu_sltu_1 | | ~alu_slt | |
| | | | | | | |
| Focused Cond | | | | | | - |
| Line 227 Item Condition totals: 0 of | | | | 0.00% | | |
| Conditi | ION LOLA | ars. U or | 2 input teri | us covered | = 0.00% | |
| Input | t Term | Covered | Reason for | | ge | Hint |
| | a[31] | N | '_1' hit b | ut '_0' is | not hit | Hit '_0' for output ->0 |
| | b[31] | N | '_0' hit b | ut '_1' is | not hit | Hit '_1' for output ->0 |
| | | | | | | |
| Rot | ws: H | its(->0) | Hits(->1) | FEC Targe | t | Non-masking condition(s) |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| Row | 1: | 0 | 0 | a[31]_0 | | _ |
| | | | | | | |
| Row | 2: | 0 | 1 | a[31]_1 | | - |
| _ | | _ | | 1.504.3 | | |
| Row | 3: | 0 | 1 | b[31]_0 | | - |
| | | | | | | |

------Focused Condition View------

235 Item 1 (alu_eq | alu_neq) Line

Condition totals: 2 of 2 input terms covered = 100.00%

Input Term Covered Reason for no coverage Hint

______ ____

Y alu_eq alu_neq Y

Hits FEC Target Non-masking condition(s)

______ ____

Row 1: $1 alu_eq_0$ ~alu_neq

Row 2: 1 alu_eq_1

Row 3: 1 alu_neq_0 ~alu_eq

1 alu_neq_1 Row 4: ~alu_eq

-----Focused Condition View-----

239 Item 1 (alu_ge || alu_geu) Line

Y

Condition totals: 2 of 2 input terms covered = 100.00%

Input Term Covered Reason for no coverage Hint

alu_ge Y

alu_geu

Rows: Hits FEC Target Non-masking condition(s)

_____ ____

Row 1: 1 alu_ge_0 ~alu_geu

Row 2: 1 alu_ge_1

Row 3: 1 alu_geu_0 ~alu_ge

1 alu_geu_1 Row 4: ~alu_ge

-----Focused Condition View (Bimodal)-----

241 Item 1 (a[31] ^ b[31]) Line

Condition totals: 2 of 2 input terms covered = 100.00%

Input Term Covered Reason for no coverage Hint

a[31] Y b[31] Y

Rows: Hits(->0) Hits(->1) FEC Target Non-masking condition(s)

```
Row 1:
       0
                  1 a[31]_0
Row 2:
              1
                      1 a[31] 1
Row 3:
                      1 b[31]_0
              0
Row 4:
                      0 b[31]_1
              1
------Focused Condition View------
       258 Item 1 (opcode_rtype || opcode_itype)
Condition totals: 2 of 2 input terms covered = 100.00%
  Input Term Covered Reason for no coverage Hint
 opcode rtype
 opcode_itype
               Y
   Rows: Hits FEC Target
                               Non-masking condition(s)
______
 Row 1:
             1 opcode_rtype_0
                              ~opcode_itype
 Row 2:
             1 opcode_rtype_1
 Row 3:
             1 opcode_itype_0
                              ~opcode_rtype
            1 opcode_itype_1
 Row
    4:
                             ~opcode_rtype
------Focused Condition View------
       259 Item 1 (opcode_branch && y_d[0])
Condition totals: 2 of 2 input terms covered = 100.00%
   Input Term Covered Reason for no coverage Hint
   ______ _____
 opcode_branch
               Y
      y_d[0]
               Y
   Rows: Hits FEC Target
                              Non-masking condition(s)
______
             1 opcode_branch_0
 Row 1:
             1 opcode_branch_1
 Row 2:
                             y_d[0]
             1 y_d[0]_0
 Row 3:
                               opcode_branch
    4: 1 y_d[0]_1
                               opcode_branch
 Row
------Focused Condition View------
       266 Item 1 (opcode_jal || opcode_jalr)
Line
```

Condition totals: 2 of 2 input terms covered = 100.00%

```
Input Term Covered Reason for no coverage Hint
  opcode_jal
                 Y
 opcode_jalr
                Υ
   Rows: Hits FEC Target
                              Non-masking condition(s)
         _____
      1:
                1 opcode_jal_0
 Row
                                   ~opcode_jalr
               1 opcode_jal_1
 Row 2:
               1 opcode_jalr_0
 Row
      3:
                                   ~opcode_jal
               1 opcode_jalr_1
 Row
      4:
                                    ~opcode_jal
-------Focused Condition View------
           280 Item 1 (((opcode_branch || opcode_store) || (opcode_system &&
Line
(i_funct3 == 0))) || opcode_fence)
Condition totals: 4 of 5 input terms covered = 80.00%
     Input Term Covered Reason for no coverage Hint
                   Y
   opcode_branch
   opcode_store
                    Y
   opcode_system
                    Y
 (i_funct3 == 0)
                    N '_0' not hit
                                    Hit '_0'
    opcode_fence
                    Y
                             Non-masking condition(s)
    Rows: Hits FEC Target
 ______ _____
                   1 opcode_branch_0 (~opcode_fence && ~(opcode_system &&
(i_funct3 == 0)) && ~opcode_store)
               1 opcode branch 1
                   1 opcode_store_0 (~opcode_fence && ~(opcode_system &&
(i_funct3 == 0)) && ~opcode_branch)
 Row
               1 opcode_store_1 ~opcode_branch
  Row 5:
                   1 opcode_system_0
                                         (~opcode_fence && ~(opcode_branch | |
opcode_store))
                  1 opcode_system_1
  Row 6:
                                         (~(opcode_branch | opcode_store) &&
(i funct3 == 0))
       7:
             ***0*** (i_funct3 == 0)_0
                                         (~opcode_fence && ~(opcode_branch | |
opcode_store) && opcode_system)
  Row 8:
                                         (~(opcode_branch || opcode_store) &&
                   1 (i_funct3 == 0)_1
opcode_system)
                                          ~((opcode_branch | opcode_store) |
  Row
      9:
                   1 opcode_fence_0
(opcode_system && (i_funct3 == 0)))
                                         ~((opcode_branch || opcode_store) ||
 Row
      10:
                   1 opcode_fence_1
(opcode_system && (i_funct3 == 0)))
```

```
------ View-----Focused Condition View-----
Line
       287 Item 1 (opcode_load | | (opcode_system && (i_funct3 != 0)))
Condition totals: 1 of 3 input terms covered = 33.33%
     Input Term Covered Reason for no coverage Hint
    ______ ____
                 Y
    opcode_load
                 N '_1' not hit
  opcode_system
                                     Hit '_1'
                 N '_1' not hit
 (i_funct3 != 0)
                                     Hit '_1'
          Hits FEC Target
   Rows:
                               Non-masking condition(s)
______ ____
 Row
     1:
              1 opcode_load_0
                                ~(opcode_system && (i_funct3 != 0))
             1 opcode_load_1
 Row
     2:
 Row
     3:
             1 opcode_system_0
                               ~opcode_load
 Row 4: ***0*** opcode_system_1
                               (~opcode_load && (i_funct3 != 0))
 Row
     5:
          1 (i_funct3 != 0)_0
                               (~opcode_load && opcode_system)
     6: ***0*** (i_funct3 != 0)_1 (~opcode_load && opcode_system)
 Row
Expression Coverage:
  Enabled Coverage
                     Bins Covered Misses Coverage
   _____
                               ____
                        ----
                                    _____
                         7 0
                                     7 0.00%
  Expressions
Expression Coverage for Design Unit work.rv32i_alu --
 File rv32i_alu.sv
-----Focused Expression View------
       193 Item 1 (i_opcode[3] | i_opcode[2])
Expression totals: 0 of 2 input terms covered = 0.00%
  Input Term Covered Reason for no coverage Hint
 i_opcode[3]
              N No hits
                                   Hit '_0' and '_1'
 i_opcode[2]
              N No hits
                                   Hit '_0' and '_1'
          Hits FEC Target
   Rows:
                               Non-masking condition(s)
_____
                               ______
         ***0*** i_opcode[3]_0
     1:
 Row
                                ~i opcode[2]
     2: ***0*** i_opcode[3]_1
 Row
         ***0*** i_opcode[2]_0
     3:
 Row
                               ~i_opcode[3]
     4: ***0*** i_opcode[2]_1
 Row
                              ~i_opcode[3]
```

```
Line
       Expression totals: 0 of 3 input terms covered = 0.00%
   Input Term Covered Reason for no coverage Hint
  ______
               N '_1' not hit
     i_stall
                                 Hit '_1'
 i_force_stall
              N '_1' not hit
                                 Hit '_1'
     i_flush
              N No hits
                                 Hit '_0' and '_1'
   Rows: Hits FEC Target
                             Non-masking condition(s)
______
 Row
     1:
             1 i_stall_0
                             ~i_force_stall
     2: ***0*** i_stall_1
                             ~i_flush
 Row
 Row
           1 i_force_stall_0
                             ~i_stall
 Row 4: ***0*** i_force_stall_1
                             (~i_flush && ~i_stall)
 Row
     5:
        ***0*** i_flush_0
                             (i_stall || i_force_stall)
 Row 6: ***0*** i_flush_1
                             (i_stall || i_force_stall)
-----Focused Expression View-----
      299 Item 1 (o_stall | i_stall)
Expression totals: 0 of 2 input terms covered = 0.00%
 Input Term Covered Reason for no coverage Hint
______
   o stall
         N '_1' not hit
                               Hit ' 1'
   i_stall N '_1' not hit
                               Hit '_1'
   Rows: Hits FEC Target
                         Non-masking condition(s)
______ ____
 Row 1:
         1 o_stall_0
                             ~i_stall
 Row 2:
        ***0*** o_stall_1
 Row 3:
         1 i_stall_0
                             ~o stall
 Row 4: ***0*** i_stall_1
                             ~o_stall
Statement Coverage:
                     Bins
                            Hits Misses Coverage
  Enabled Coverage
  _____
                      ----
                            ----
                       65
                             48
                                    17 73.84%
  Statements
```

-----Focused Expression View------

| Line | Item | Count | Source |
|-----------|------|---------------|--------|
| File rv32 | | | |
| 173 | 1 | 76 | |
| 175 | 1 | 76 | |
| 176 | 1 | 76 | |
| 177 | 1 | 76 | |
| 181 | 1 | ***0*** | |
| 182 | 1 | ***0*** | |
| 183 | 1 | ***0*** | |
| 184 | 1 | ***0*** | |
| 185 | 1 | ***0*** | |
| 186 | 1 | ***0*** | |
| 187 | 1 | ***0*** | |
| 188 | 1 | ***0*** | |
| 189 | 1 | * * * 0 * * * | |
| 190 | 1 | * * * 0 * * * | |
| 191 | 1 | * * * 0 * * * | |
| 192 | 1 | * * * 0 * * * | |
| 193 | 1 | ***0*** | |
| 195 | 1 | ***0*** | |
| 200 | 1 | ***0*** | |
| 203 | 1 | ***0*** | |
| 205 | 1 | ***0*** | |
| 215 | 1 | 76 | |
| 216 | 1 | 76 | |
| 218 | 1 | 76 | |
| 220 | 1 | 76 | |
| 223 | 1 | 12 | |
| 224 | 1 | 6 | |
| 226 | 1 | 5 | |
| 227 | 1 | 2 | |
| 229 | 1 | 6 | |
| 230 | 1 | 9 | |
| 231 | 1 | 4 | |
| 232 | 1 | 5 | |
| 233 | 1 | 9 | |
| 234 | 1 | 6 | |
| 236 | 1 | 7 | |
| 237 | 1 | 2 | |
| 240 | 1 | 6 | |
| 241 | 1 | 3 | |
| 248 | 1 | 96 | |
| 249 | 1 | 96 | |
| 251 | 1 | 96 | |
| 252 | 1 | 96 | |

| 253 | 1 | 96 |
|-----|---|----|
| 254 | 1 | 96 |
| 255 | 1 | 96 |
| 256 | 1 | 96 |
| 258 | 1 | 37 |
| 260 | 1 | 3 |
| 262 | 1 | 3 |
| 264 | 1 | 3 |
| 267 | 1 | 8 |
| 268 | 1 | 12 |
| 270 | 1 | 12 |
| 272 | 1 | 12 |
| 273 | 1 | 12 |
| 277 | 1 | 4 |
| 278 | 1 | 7 |
| 281 | 1 | 23 |
| 284 | 1 | 73 |
| 288 | 1 | 6 |
| 290 | 1 | 90 |
| 294 | 1 | 96 |
| 298 | 1 | 70 |
| 299 | 1 | 3 |
| | | |

=== Design Unit: work.rv32i_alu_tb

Branch Coverage:

268

| Enabled Coverage | Bins | Hits | Misses | Coverage |
|------------------|------|------|--------|----------|
| | | | | |
| Branches | 27 | 0 | 27 | 0.00% |

Branch Coverage for Design Unit work.rv32i_alu_tb

1

| Line | Item | Count So | ource |
|--------------|----------|-------------|------------------------|
| | | | |
| File rv32i_a | lu_tb.sv | | |
| | | CASE Branch | |
| 259 | | ***0*** Co | ount coming in to CASE |
| 262 | 1 | ***0*** | |
| 263 | 1 | ***0*** | |
| 264 | 1 | ***0*** | |
| 265 | 1 | ***0** | |
| 267 | 1 | ***0** | |

0

| 269 | 1 | * * * 0 * * * | |
|---------------|-------------------|-----------------|-----------------------|
| 270 | 1 | * * * 0 * * * | |
| 271 | 1 | ***0*** | |
| 272 | 1 | * * * 0 * * * | |
| 273 | 1 | * * * 0 * * * | |
| 274 | 1 | ***0*** | |
| 275 | 1 | ***0*** | |
| 276 | 1 | ***0*** | |
| 278 | 1 | ***0*** | |
| | s: 0 hits of 15 b | ranches = 0.00% | |
| | | IF Branch | |
| 264 | | ***0*** | Count coming in to IF |
| 264 | 2 | ***0*** | |
| 264 | 3 | ***0*** | |
| Branch total: | s: 0 hits of 2 br | anches = 0.00% | |
| | | | |
| | | IF Branch | |
| 266 | | ***0*** | Count coming in to IF |
| 266 | 1 | ***0*** | |
| 266 | 2 | ***0*** | |
| Branch total: | s: 0 hits of 2 br | anches = 0.00% | |
| | | | |
| | | IF Branch | |
| 273 | | * * * 0 * * * | Count coming in to IF |
| 273 | 2 | ***0*** | |
| 273 | 3 | ***0*** | |
| Branch totals | s: 0 hits of 2 br | anches = 0.00% | |
| | | | |
| | | IF Branch | |
| 274 | | ***0*** | Count coming in to IF |
| 274 | 2 | ***0*** | |
| 274 | 3 | ***0*** | |
| Branch total: | s: 0 hits of 2 br | anches = 0.00% | |
| | | | |
| | | IF Branch | |
| 275 | | ***0*** | Count coming in to IF |
| 275 | 2 | ***0*** | |
| 275 | 3 | ***0*** | |
| Branch total: | s: 0 hits of 2 br | anches = 0.00% | |
| | | | |
| | | IF Branch | |
| 276 | | ***0*** | Count coming in to IF |
| 276 | 2 | * * * 0 * * * | |
| 276 | 3 | ***0*** | |
| Branch totals | s: 0 hits of 2 br | anches = 0.00% | |
| | | | |

```
Condition Coverage:
  Enabled Coverage
                     Bins Covered Misses Coverage
                           ____
                      ____
                                 -----
  Conditions
                             0
                                   6
                       6
                                        0.00%
Condition Coverage for Design Unit work.rv32i_alu_tb --
 File rv32i_alu_tb.sv
-----Focused Condition View-----
      264 Item 1 (a < b)
Condition totals: 0 of 1 input term covered = 0.00%
 Input Term Covered Reason for no coverage Hint
   (a < b) N No hits
                               Hit '_0' and '_1'
   Rows: Hits FEC Target
                       Non-masking condition(s)
______
 Row 1: ***0*** (a < b)_0
 Row 2: ***0*** (a < b)_1
-----Focused Condition View-----
Line
       266 Item 1 (a < b)
Condition totals: 0 of 1 input term covered = 0.00%
 Input Term Covered Reason for no coverage Hint
______ _____
   (a < b) N No hits
                               Hit '_0' and '_1'
         Hits FEC Target
                         Non-masking condition(s)
   Rows:
______ ____
 Row 1: ***0*** (a < b)_0
 Row 2:
        ***0*** (a < b)_1
------Focused Condition View------
```

273 Item 1 (a == b)

Condition totals: 0 of 1 input term covered = 0.00%

Line

```
Rows:
        Hits FEC Target
                              Non-masking condition(s)
 Row 1: ***0*** (a == b)_0
        ***0*** (a == b)_1
 Row 2:
-----Focused Condition View------
       274 Item 1 (a != b)
Line
Condition totals: 0 of 1 input term covered = 0.00%
 Input Term Covered Reason for no coverage Hint
  (a != b)
            N No hits
                                 Hit '_0' and '_1'
   Rows:
          Hits FEC Target
                              Non-masking condition(s)
        -----
        ***0*** (a != b)_0
 Row 1:
 Row 2: ***0*** (a != b)_1
-----Focused Condition View-----
       275 Item 1 (a >= b)
Line
Condition totals: 0 of 1 input term covered = 0.00%
 Input Term Covered Reason for no coverage Hint
(a >= b)
            N No hits
                                 Hit '_0' and '_1'
        Hits FEC Target
                             Non-masking condition(s)
_____ ____
 Row 1: ***0*** (a >= b)_0
 Row 2: ***0*** (a >= b)_1
------Focused Condition View------
       276 Item 1 (a >= b)
Condition totals: 0 of 1 input term covered = 0.00%
 Input Term Covered Reason for no coverage Hint
______ _____
                                 Hit '\_0' and '\_1'
  (a >= b) N No hits
        Hits FEC Target
   Rows:
                         Non-masking condition(s)
_____ ____
 Row 1: ***0*** (a >= b)_0
 Row 2: ***0*** (a >= b)_1
```

| Enabled Coverage | Bins | Hits | Misses | Coverage |
|------------------|------|------|--------|----------|
| | | | | |
| Statements | 56 | 39 | 17 | 69.64% |

Statement Coverage for Design Unit work.rv32i_alu_tb --

| | _ | | |
|------------|------|-------|--------|
| Line | Item | Count | Source |
| | | | |
| File rv32i | | | |
| 98 | 1 | 1 | |
| 99 | 1 | 1 | |
| 100 | 1 | 1 | |
| 152 | 1 | 1 | |
| 153 | 1 | 1 | |
| 154 | 1 | 1002 | |
| 155 | 1 | 1001 | |
| 161 | 1 | 1 | |
| 162 | 1 | 1 | |
| 163 | 1 | 1 | |
| 164 | 1 | 1 | |
| 165 | 1 | 1 | |
| 166 | 1 | 1 | |
| 167 | 1 | 1 | |
| 168 | 1 | 1 | |
| 169 | 1 | 1 | |
| 170 | 1 | 1 | |
| 171 | 1 | 1 | |
| 172 | 1 | 1 | |
| 173 | 1 | 1 | |
| 174 | 1 | 1 | |
| 175 | 1 | 1 | |
| 176 | 1 | 1 | |
| 181 | 1 | 1 | |
| 182 | 1 | 1 | |
| 183 | 1 | 1 | |
| 184 | 1 | 1 | |
| 185 | 1 | 1 | |
| 186 | 1 | 1 | |
| 192 | 1 | 1 | |
| 193 | 1 | 1 | |
| 194 | 1 | 1 | |
| 195 | 1 | 1 | |
| 196 | 1 | 1 | |
| 197 | 1 | 1 | |
| | | | |

| | 200 | _ | - | | | |
|-----|------------------|-----------------------|-----------|--------|------|------|
| | 242 | 1 | 1 | | | |
| | 242 | 2 | 1 | | | |
| | 247 | 1 | 1 | | | |
| | 248 | 1 | ***0*** | | | |
| | 249 | 1 | ***0*** | | | |
| | 262 | 1 | ***0*** | | | |
| | 263 | 1 | ***0*** | | | |
| | 264 | 1 | ***0*** | | | |
| | 266 | 1 | ***0*** | | | |
| | 267 | 1 | ***0*** | | | |
| | 268 | 1 | ***0*** | | | |
| | 269 | 1 | ***0*** | | | |
| | 270 | 1 | ***0*** | | | |
| | 271 | 1 | ***0*** | | | |
| | 272 | 1 | ***0*** | | | |
| | 273 | 1 | ***0*** | | | |
| | 274 | 1 | ***0*** | | | |
| | 275 | 1 | ***0*** | | | |
| | 276 | 1 | ***0*** | | | |
| | 278 | 1 | ***0*** | | | |
| | vergroup | | | Metric | Goal | Bins |
| | PE work.coverage | e_sv_unit::coverage/a | lu_cg | 34.81% | 100 | |
| | covered/total b | oins: | | 51 | 5315 | - |
| | missing/total b | oins: | | 5264 | 5315 | - |
| | % Hit: | | | 0.95% | 100 | - |
| | type_option.wei | ght=1 | | | | |
| | type_option.goa | 1=100 | | | | |
| | type_option.com | ment= | | | | |
| | type_option.str | robe=0 | | | | |
| | type_option.mer | ge_instances=auto(1) | | | | |
| | Coverpoint #cov | verpoint0# | | 45.45% | 100 | _ |
| T.T | | | | | | |

Uncovered

| | covered/total bins: | 5 | 11 | - |
|---------|--------------------------------|--------|-----|---|
| | missing/total bins: | 6 | 11 | - |
| | % Hit: | 45.45% | 100 | _ |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | <pre>bin opcode_types[0]</pre> | 3 | 1 | - |
| Covered | | | | |
| | <pre>bin opcode_types[1]</pre> | 20 | 1 | _ |
| Covered | | | | |
| | <pre>bin opcode_types[2]</pre> | 1 | 1 | _ |
| Covered | | | | |
| | <pre>bin opcode_types[3]</pre> | 0 | 1 | - |
| ZERO | | | | |
| | <pre>bin opcode_types[4]</pre> | 6 | 1 | - |
| Covered | | | | |
| | bin opcode_types[5] | 0 | 1 | _ |
| ZERO | | | | |
| | bin opcode_types[6] | 0 | 1 | _ |
| ZERO | | | | |
| | bin opcode_types[7] | 0 | 1 | - |
| ZERO | | | | |
| | bin opcode_types[8] | 5 | 1 | - |
| Covered | | | | |
| | bin opcode_types[9] | 0 | 1 | _ |
| ZERO | | | | |
| | bin opcode_types[10] | 0 | 1 | _ |
| ZERO | | | | |
| | erpoint #coverpoint1# | 28.57% | 100 | _ |
| Uncover | | 4 | 1.4 | |
| | covered/total bins: | 4 | 14 | _ |
| | missing/total bins: | 10 | 14 | - |
| | % Hit: | 28.57% | 100 | - |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin alu_ops[0] | 0 | 1 | _ |
| ZERO | | | | |
| _ | bin alu_ops[1] | 11 | 1 | - |
| Covered | | | | |

| | bin alu_ops[2] | 4 | 1 | - |
|---------|------------------------|---------|-----|--------|
| Covered | bin alu_ops[3] | 0 | 1 | _ |
| ZERO | | _ | _ | |
| Covered | bin alu_ops[4] | 1 | 1 | _ |
| 777.0 | bin alu_ops[5] | 0 | 1 | _ |
| ZERO | bin alu_ops[6] | 0 | 1 | - |
| ZERO | | • | - | |
| ZERO | bin alu_ops[7] | 0 | 1 | _ |
| G | bin alu_ops[8] | 3 | 1 | _ |
| Covered | bin alu_ops[9] | 0 | 1 | _ |
| ZERO | bin alu_ops[10] | 0 | 1 | |
| ZERO | pin alu_ops[10] | 0 | 1 | _ |
| ZERO | bin alu_ops[11] | 0 | 1 | - |
| ZERO | bin alu_ops[12] | 0 | 1 | _ |
| ZERO | bin alu_ops[13] | 0 | 1 | |
| ZERO | pin alu_ops[13] | 0 | 1 | _ |
| | verpoint #coverpoint2# | 100.00% | 100 | - |
| Covered | d covered/total bins: | 2 | 2 | _ |
| | | | | |
| | missing/total bins: | 0 | 2 | _ |
| | % Hit: | 100.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 55 | 1 | _ |
| Covered | bin auto[1] | 10 | 1 | _ |
| Covered | A | | | |
| Cor | | | | |
| | verpoint #coverpoint3# | 100.00% | 100 | - |
| Covered | A | 100.00% | 100 | - |
| | | 100.00% | 100 | - |
| | A | | | - - |

| | type_option.weight=1 | | | |
|---------|--|-------|-----|---|
| | type_option.weight=1 type_option.goal=100 | | | |
| | type_option.godi=100 type_option.comment= | | | |
| | bin pc_values | 65 | 1 | _ |
| Covered | | 03 | Δ, | |
| | | 0.00% | 100 | |
| ZERO | rerpoint #coverpoint4# | 0.00% | 100 | _ |
| ZERO | covered/total bins: | 0 | 2 | |
| | covered/total bins. | U | 2 | _ |
| | missing/total bins: | 2 | 2 | - |
| | | | | |
| | % Hit: | 0.00% | 100 | - |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[1] | 0 | 1 | _ |
| ZERO | | | | |
| Cov | erpoint #coverpoint5# | 0.00% | 100 | _ |
| ZERO | | | | |
| | covered/total bins: | 0 | 2 | - |
| | missing/total bins: | 2 | 2 | - |
| | | | | |
| | % Hit: | 0.00% | 100 | - |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[1] | 0 | 1 | _ |
| ZERO | | | | |
| | erpoint #coverpoint6# | 0.00% | 100 | _ |
| ZERO | <u> </u> | | | |
| | covered/total bins: | 0 | 1 | - |
| | | | | |
| | missing/total bins: | 1 | 1 | - |
| | % Hit: | 0.00% | 100 | _ |
| | o 11TC. | 0.00% | 100 | _ |
| | time ention weight-1 | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |

| | type_option.comment= | | | |
|------------|--|-----------------------------|--------------------------------|-------------|
| | bin rd_addr | 0 | 1 | - |
| ZERO | | | | |
| Co | verpoint #coverpoint7# | 50.00% | 100 | - |
| Uncove | red | | | |
| | covered/total bins: | 1 | 2 | - |
| | mi min m/h sh - 1. him s | 1 | 2 | |
| | missing/total bins: | 1 | 2 | _ |
| | % Hit: | 50.00% | 100 | - |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 0 | 1 | - |
| ZERO | | | | |
| | bin auto[1] | 65 | 1 | - |
| Covered | d | | | |
| Co | verpoint #coverpoint8# | 50.00% | 100 | - |
| Uncove | | | | |
| | covered/total bins: | 1 | 2 | - |
| | | | 0 | |
| | missing/total bins: | 1 | 2 | _ |
| | % Hit: | 50.00% | 100 | - |
| | | | | - |
| | % Hit: | | | - |
| | <pre>% Hit: type_option.weight=1</pre> | | | - |
| | <pre>% Hit: type_option.weight=1 type_option.goal=100</pre> | | | - |
| Covered | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0]</pre> | 50.00% | 100 | - |
| | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0]</pre> | 50.00% | 100 | - |
| ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] d bin auto[1]</pre> | 50.00% 65 0 | 100 | - |
| ZERO Co | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] d bin auto[1]</pre> | 50.00% 65 | 100 | - - |
| ZERO | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] d bin auto[1] verpoint #coverpoint9# red</pre> | 50.00% 65 0 50.00% | 100 1 1 | - |
| ZERO Co | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] d bin auto[1]</pre> | 50.00% 65 0 | 100 | - |
| ZERO Co | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] d bin auto[1] verpoint #coverpoint9# red</pre> | 50.00% 65 0 50.00% | 100 1 1 | - - - |
| ZERO Co | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] d bin auto[1] verpoint #coverpoint9# red covered/total bins:</pre> | 50.00% 65 0 50.00% | 100 1 1 100 2 | - |
| ZERO Co | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] d bin auto[1] verpoint #coverpoint9# red covered/total bins: missing/total bins:</pre> | 50.00% 65 0 50.00% 1 1 | 100 1 1 100 2 2 | - |
| ZERO Co | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] d bin auto[1] verpoint #coverpoint9# red covered/total bins: missing/total bins: % Hit:</pre> | 50.00% 65 0 50.00% 1 1 | 100 1 1 100 2 2 | - |
| ZERO Co | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] d bin auto[1] verpoint #coverpoint9# red covered/total bins: missing/total bins: % Hit: type_option.weight=1</pre> | 50.00% 65 0 50.00% 1 1 | 100 1 1 100 2 2 | |
| ZERO Co | <pre>% Hit: type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] d bin auto[1] verpoint #coverpoint9# red covered/total bins: missing/total bins: % Hit: type_option.weight=1 type_option.goal=100</pre> | 50.00% 65 0 50.00% 1 1 | 100 1 1 100 2 2 | |

| Note | | bin auto[1] | 0 | 1 | _ |
|--|---------|------------------------|--------|-----|---|
| ### Covered | ZERO | | | | |
| Covered/total bins: 1 2 | Cov | erpoint #coverpoint10# | 50.00% | 100 | _ |
| missing/total bins: 1 2 | Uncover | ed | | | |
| # Hit: 50.00% 100 - type_option.weight=1 type_option.comment= bin auto[0] 65 1 - Covered bin auto[1] 0 1 - ZERO Coverpoint #coverpoint_11# 50.00% 100 - missing/total bins: 1 2 - # Hit: 50.00% 100 - * Hit: 50.00% 100 - * Hit: 50.00% 100 - * Lype_option.weight=1 type_option.comment= bin auto[0] 65 1 - Covered Covered Covered Covered * bin auto[1] 0 1 - ZERO Covered bin auto[1] 50.00% 100 - * Hit: 50.00% 100 - | | covered/total bins: | 1 | 2 | _ |
| type_option.weight=1 type_option.comment= bin auto[0] 65 1 - Covered bin auto[1] 0 1 - ZERO Coverpoint #coverpoint_11# 50.00% 100 - Misaing/total bins: 1 2 - * Hit: 50.00% 100 - type_option.weight=1 type_option.comment= bin auto[1] 0 1 - ZERO Covered * Hit: 50.00% 100 - * Hit: 50.00% 100 - * Hit: 50.00% 100 - * Whit: 50.00% 100 - * Hit: 50.00% 100 - | | missing/total bins: | 1 | 2 | - |
| type_option.goal=100 type_option.comment= bin auto[0] 65 1 - Covered bin auto[1] 0 1 - ZERO Coverpoint #coverpoint11# 50.00% 100 - Uncovered covered/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.comment= bin auto[0] 65 1 - Covered Coverpoint #coverpoint12# 50.00% 100 - Covered covered/total bins: 1 2 - % Hit: 50.00% 100 - Covered bin auto[0] 65 1 - Covered covered/total bins: 1 2 - # Kithing 50.00% 100 - Uncovered covered/total bins: 1 2 - # Kithing 50.00% 100 - Uncovered covered/total bins: 1 2 - # Hit: 50.00% 100 - Uncovered type_option.weight=1 type_option.weight=1 type_option.weight=1 type_option.weight=1 type_option.omment= bin auto[0] 65 1 Covered Covered type_option.comment= bin auto[0] 65 1 Covered | | % Hit: | 50.00% | 100 | - |
| type_option.comment= bin auto[0] | | type_option.weight=1 | | | |
| Din auto[0] 65 1 - Covered | | type_option.goal=100 | | | |
| Covered | | type_option.comment= | | | |
| Din auto[1] 0 1 | | bin auto[0] | 65 | 1 | - |
| Coverpoint #coverpoint_ll# 50.00% 100 - Cuncovered | Covered | | | | |
| Coverpoint #coverpoint11# 50.00% 100 - Uncovered | | bin auto[1] | 0 | 1 | - |
| Uncovered | ZERO | | | | |
| covered/total bins: 1 2 - | | | 50.00% | 100 | - |
| missing/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.comment= bin auto[0] 65 1 - Covered bin auto[1] 0 1 - ZERO Coverpoint #coverpoint_12# 50.00% 100 - Uncovered covered/total bins: 1 2 - missing/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.weight=1 type_option.comment= bin auto[0] 65 1 - Covered | Uncover | | | | |
| <pre>% Hit: 50.00% 100 - type_option.weight=1 type_option.comment= bin auto[0] 65 1 Covered Coverpoint #coverpoint_12# 50.00% 100 Uncovered covered/total bins: 1 2 missing/total bins: 1 2 % Hit: 50.00% 100 type_option.weight=1 type_option.weight=1 type_option.comment= bin auto[0] 65 1 Covered</pre> | | covered/total bins: | 1 | 2 | _ |
| type_option.weight=1 type_option.comment= bin auto[0] 65 1 Covered bin auto[1] 0 10 10 ZERO Coverpoint #coverpoint_12# 50.00% 100 Uncovered covered/total bins: 1 2 missing/total bins: 1 2 % Hit: 50.00% 100 type_option.weight=1 type_option.weight=1 type_option.comment= bin auto[0] 65 1 Covered Covered | | missing/total bins: | 1 | 2 | - |
| type_option.goal=100 type_option.comment= bin auto[0] 65 1 Covered bin auto[1] 0 1 ZERO Coverpoint #coverpoint_12# 50.00% 100 Uncovered covered/total bins: 1 2 missing/total bins: 1 2 % Hit: 50.00% 100 type_option.weight=1 type_option.weight=1 type_option.comment= bin auto[0] 65 1 Covered Covered | | % Hit: | 50.00% | 100 | - |
| type_option.comment= bin auto[0] 65 1 - Covered bin auto[1] 0 1 - ZERO Coverpoint #coverpoint12# 50.00% 100 - Uncovered 1 2 - missing/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] 65 1 - Covered Covered - - - - - | | type_option.weight=1 | | | |
| Din auto[0] | | type_option.goal=100 | | | |
| Covered bin auto[1] 0 1 - ZERO Coverpoint #coverpoint12# 50.00% 100 - Uncovered covered/total bins: 1 2 - missing/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.goal=100 + + type_option.comment= bin auto[0] 65 1 - Covered Covered - - - | | type_option.comment= | | | |
| Din auto[1] 0 1 | | bin auto[0] | 65 | 1 | _ |
| Coverpoint #coverpoint_12# 50.00% 100 - | Covered | | | | |
| Coverpoint #coverpoint_12# 50.00% 100 - Uncovered 1 2 - missing/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.goal=100 - - type_option.comment= bin auto[0] 65 1 - Covered - - - - | | bin auto[1] | 0 | 1 | - |
| Uncovered covered/total bins: 1 2 - missing/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] 65 1 Covered | ZERO | | | | |
| covered/total bins: 1 2 - missing/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.goal=100 - - type_option.comment= - - bin auto[0] 65 1 - Covered | Cov | erpoint #coverpoint12# | 50.00% | 100 | _ |
| missing/total bins: 1 2 - % Hit: 50.00% 100 - type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] 65 1 Covered | Uncover | ed | | | |
| <pre>% Hit: 50.00% 100 - type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] 65 1 -</pre> Covered | | covered/total bins: | 1 | 2 | _ |
| <pre>type_option.weight=1 type_option.goal=100 type_option.comment= bin auto[0] 65 1 -</pre> | | missing/total bins: | 1 | 2 | _ |
| <pre>type_option.goal=100 type_option.comment= bin auto[0] 65 1 -</pre> Covered | | % Hit: | 50.00% | 100 | - |
| <pre>type_option.comment= bin auto[0] 65 1 - Covered</pre> | | type_option.weight=1 | | | |
| bin auto[0] 65 1 - Covered | | type_option.goal=100 | | | |
| Covered | | type_option.comment= | | | |
| | ~ - | | 65 | 1 | _ |
| | Covered | | 0 | 1 | - |

| ZEKU | | | | |
|---------|---------------------------|---------|-----|---|
| Co | verpoint #coverpoint13# | 100.00% | 100 | _ |
| Covered | d | | | |
| | covered/total bins: | 2 | 2 | _ |
| | | | | |
| | missing/total bins: | 0 | 2 | _ |
| | % Hit: | 100.00% | 100 | |
| | % nic. | 100.00% | 100 | _ |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0] | 55 | 1 | _ |
| Covere | | | _ | |
| | bin auto[1] | 10 | 1 | _ |
| Covered | | | | |
| Со | verpoint #coverpoint14# | 0.00% | 100 | _ |
| ZERO | | | | |
| | covered/total bins: | 0 | 4 | _ |
| | | | | |
| | missing/total bins: | 4 | 4 | - |
| | | | | |
| | % Hit: | 0.00% | 100 | _ |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin exceptions[0] | 0 | 1 | - |
| ZERO | | | | |
| | bin exceptions[1] | 0 | 1 | _ |
| ZERO | | | | |
| | bin exceptions[2] | 0 | 1 | _ |
| ZERO | | | | |
| | bin exceptions[3] | 0 | 1 | _ |
| ZERO | | | | |
| Со | verpoint #vif.i_opcode15# | 10.93% | 100 | _ |
| Uncove | | | | |
| | covered/total bins: | 7 | 64 | _ |
| | | | | |
| | missing/total bins: | 57 | 64 | _ |
| | | | | |
| | % Hit: | 10.93% | 100 | _ |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | F | | | |

type_option.comment=

| Covered | bin auto[0:31] | 41 | 1 | - |
|---------|-------------------|----|---|---|
| | bin auto[32:63] | 4 | 1 | - |
| Covered | bin auto[64:95] | 3 | 1 | - |
| Covered | bin auto[96:127] | 0 | 1 | - |
| ZERO | bin auto[128:159] | 3 | 1 | - |
| Covered | bin auto[160:191] | 0 | 1 | - |
| ZERO | bin auto[192:223] | 0 | 1 | - |
| ZERO | bin auto[224:255] | 0 | 1 | - |
| ZERO | bin auto[256:287] | 7 | 1 | - |
| Covered | bin auto[288:319] | 0 | 1 | - |
| ZERO | bin auto[320:351] | 0 | 1 | _ |
| ZERO | bin auto[352:383] | 0 | 1 | _ |
| ZERO | bin auto[384:415] | 0 | 1 | _ |
| ZERO | bin auto[416:447] | 0 | 1 | _ |
| ZERO | bin auto[448:479] | 0 | 1 | |
| ZERO | | | | _ |
| ZERO | bin auto[480:511] | 0 | 1 | - |
| Covered | | 6 | 1 | - |
| ZERO | bin auto[544:575] | 0 | 1 | - |
| ZERO | bin auto[576:607] | 0 | 1 | - |
| ZERO | bin auto[608:639] | 0 | 1 | - |
| ZERO | bin auto[640:671] | 0 | 1 | - |
| ZERO | bin auto[672:703] | 0 | 1 | - |
| ZERO | bin auto[704:735] | 0 | 1 | - |
| | | | | |

| ZERO | bin auto[736:767] | 0 | 1 | - |
|---------|---------------------|---|---|---|
| ZERO | bin auto[768:799] | 0 | 1 | - |
| ZERO | bin auto[800:831] | 0 | 1 | - |
| | bin auto[832:863] | 0 | 1 | - |
| ZERO | bin auto[864:895] | 0 | 1 | - |
| ZERO | bin auto[896:927] | 0 | 1 | - |
| ZERO | bin auto[928:959] | 0 | 1 | - |
| ZERO | bin auto[960:991] | 0 | 1 | - |
| ZERO | bin auto[992:1023] | 0 | 1 | - |
| ZERO | bin auto[1024:1055] | 1 | 1 | - |
| Covered | bin auto[1056:1087] | 0 | 1 | _ |
| ZERO | bin auto[1088:1119] | 0 | 1 | - |
| ZERO | bin auto[1120:1151] | 0 | 1 | - |
| ZERO | bin auto[1152:1183] | 0 | 1 | - |
| ZERO | bin auto[1184:1215] | 0 | 1 | - |
| ZERO | bin auto[1216:1247] | 0 | 1 | _ |
| ZERO | bin auto[1248:1279] | 0 | 1 | _ |
| ZERO | bin auto[1280:1311] | 0 | 1 | _ |
| ZERO | bin auto[1312:1343] | 0 | 1 | _ |
| ZERO | bin auto[1344:1375] | 0 | 1 | _ |
| ZERO | bin auto[1376:1407] | 0 | 1 | _ |
| ZERO | bin auto[1408:1439] | 0 | 1 | - |
| ZERO | bin auto[1440:1471] | 0 | 1 | - |
| ZERO | | | | |

| | bin auto[1472:1503] | 0 | 1 | - |
|------|------------------------------|-------|-----|---|
| ZERO | bin auto[1504:1535] | 0 | 1 | - |
| ZERO | bin auto[1536:1567] | 0 | 1 | - |
| ZERO | bin auto[1568:1599] | 0 | 1 | _ |
| ZERO | bin auto[1600:1631] | 0 | 1 | _ |
| ZERO | | | | |
| ZERO | bin auto[1632:1663] | 0 | 1 | - |
| ZERO | bin auto[1664:1695] | 0 | 1 | - |
| ZERO | bin auto[1696:1727] | 0 | 1 | - |
| ZERO | bin auto[1728:1759] | 0 | 1 | - |
| | bin auto[1760:1791] | 0 | 1 | - |
| ZERO | bin auto[1792:1823] | 0 | 1 | - |
| ZERO | bin auto[1824:1855] | 0 | 1 | _ |
| ZERO | bin auto[1856:1887] | 0 | 1 | _ |
| ZERO | bin auto[1888:1919] | 0 | 1 | _ |
| ZERO | bin auto[1920:1951] | | 1 | |
| ZERO | | 0 | | _ |
| ZERO | bin auto[1952:1983] | 0 | 1 | _ |
| ZERO | bin auto[1984:2015] | 0 | 1 | - |
| ZERO | bin auto[2016:2047] | 0 | 1 | _ |
| | verpoint #vif.i_exception16# | 0.00% | 100 | _ |
| ZERO | covered/total bins: | 0 | 16 | - |
| | missing/total bins: | 16 | 16 | _ |
| | % Hit: | 0.00% | 100 | _ |
| | type_option.weight=1 | | | |

type_option.goal=100

| | type_option.comment= | | | |
|---------|------------------------|--------|-----|---|
| | bin auto[0] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[1] | 0 | 1 | - |
| ZERO | 1 | 0 | 1 | |
| ZERO | bin auto[2] | 0 | 1 | _ |
| ZERO | bin auto[3] | 0 | 1 | _ |
| ZERO | DIN ddee(5) | Ü | _ | |
| | bin auto[4] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[5] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[6] | 0 | 1 | - |
| ZERO | | | | |
| | bin auto[7] | 0 | 1 | _ |
| ZERO | | | - | |
| ZEDO | bin auto[8] | 0 | 1 | _ |
| ZERO | bin auto[9] | 0 | 1 | _ |
| ZERO | DIN auto[9] | U | 1 | |
| ZERO | bin auto[10] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[11] | 0 | 1 | _ |
| ZERO | | | | |
| | bin auto[12] | 0 | 1 | - |
| ZERO | | | | |
| | bin auto[13] | 0 | 1 | - |
| ZERO | | | | |
| | bin auto[14] | 0 | 1 | - |
| ZERO | | | | |
| | bin auto[15] | 0 | 1 | _ |
| ZERO | | 10.03% | 100 | |
| Uncover | verpoint #vif.i_alu17# | 10.93% | 100 | - |
| oncover | covered/total bins: | 7 | 64 | _ |
| | covered, coedi bino | , | 01 | |
| | missing/total bins: | 57 | 64 | _ |
| | - | | | |
| | % Hit: | 10.93% | 100 | _ |
| | | | | |
| | type_option.weight=1 | | | |
| | type_option.goal=100 | | | |
| | type_option.comment= | | | |
| | bin auto[0:255] | 39 | 1 | - |
| Covered | | | | |

| Covered | bin auto[256:511] | 8 | 1 | _ |
|---------|---------------------|---|---|---|
| Covered | bin auto[512:767] | 5 | 1 | - |
| ZERO | bin auto[768:1023] | 0 | 1 | - |
| Covered | bin auto[1024:1279] | 5 | 1 | - |
| ZERO | bin auto[1280:1535] | 0 | 1 | - |
| ZERO | bin auto[1536:1791] | 0 | 1 | _ |
| ZERO | bin auto[1792:2047] | 0 | 1 | _ |
| Covered | bin auto[2048:2303] | 2 | 1 | - |
| ZERO | bin auto[2304:2559] | 0 | 1 | - |
| ZERO | bin auto[2560:2815] | 0 | 1 | - |
| ZERO | bin auto[2816:3071] | 0 | 1 | - |
| ZERO | bin auto[3072:3327] | 0 | 1 | - |
| ZERO | bin auto[3328:3583] | 0 | 1 | - |
| ZERO | bin auto[3584:3839] | 0 | 1 | - |
| ZERO | bin auto[3840:4095] | 0 | 1 | - |
| Covered | bin auto[4096:4351] | 3 | 1 | - |
| ZERO | bin auto[4352:4607] | 0 | 1 | - |
| ZERO | bin auto[4608:4863] | 0 | 1 | - |
| ZERO | bin auto[4864:5119] | 0 | 1 | - |
| ZERO | bin auto[5120:5375] | 0 | 1 | - |
| ZERO | bin auto[5376:5631] | 0 | 1 | - |
| | bin auto[5632:5887] | 0 | 1 | _ |
| ZERO | bin auto[5888:6143] | 0 | 1 | - |
| ZERO | | | | |

| ZERO | bin auto[6144:6399] | 0 | 1 | - |
|---------|-----------------------|---|---|---|
| ZERO | bin auto[6400:6655] | 0 | 1 | - |
| ZERO | bin auto[6656:6911] | 0 | 1 | - |
| | bin auto[6912:7167] | 0 | 1 | - |
| ZERO | bin auto[7168:7423] | 0 | 1 | - |
| ZERO | bin auto[7424:7679] | 0 | 1 | - |
| ZERO | bin auto[7680:7935] | 0 | 1 | - |
| ZERO | bin auto[7936:8191] | 0 | 1 | - |
| ZERO | bin auto[8192:8447] | 3 | 1 | - |
| Covered | bin auto[8448:8703] | 0 | 1 | - |
| ZERO | bin auto[8704:8959] | 0 | 1 | _ |
| ZERO | bin auto[8960:9215] | 0 | 1 | - |
| ZERO | bin auto[9216:9471] | 0 | 1 | - |
| ZERO | bin auto[9472:9727] | 0 | 1 | - |
| ZERO | bin auto[9728:9983] | 0 | 1 | _ |
| ZERO | bin auto[9984:10239] | 0 | 1 | _ |
| ZERO | bin auto[10240:10495] | 0 | 1 | _ |
| ZERO | bin auto[10496:10751] | 0 | 1 | _ |
| ZERO | bin auto[10752:11007] | 0 | 1 | _ |
| ZERO | bin auto[11008:11263] | 0 | 1 | _ |
| ZERO | bin auto[11264:11519] | 0 | 1 | _ |
| ZERO | bin auto[11520:11775] | 0 | 1 | _ |
| ZERO | bin auto[11776:12031] | 0 | 1 | _ |
| ZERO | | | | |

| | bin auto[12032:12287] | 0 | 1 | - |
|---------|------------------------|-------|------|---|
| ZERO | bin auto[12288:12543] | 0 | 1 | - |
| ZERO | bin auto[12544:12799] | 0 | 1 | _ |
| ZERO | | | | |
| ZERO | bin auto[12800:13055] | 0 | 1 | - |
| ZERO | bin auto[13056:13311] | 0 | 1 | - |
| | bin auto[13312:13567] | 0 | 1 | - |
| ZERO | bin auto[13568:13823] | 0 | 1 | - |
| ZERO | bin auto[13824:14079] | 0 | 1 | _ |
| ZERO | bin auto[14080:14335] | 0 | 1 | |
| ZERO | | Ü | | |
| ZERO | bin auto[14336:14591] | 0 | 1 | _ |
| ZERO | bin auto[14592:14847] | 0 | 1 | - |
| | bin auto[14848:15103] | 0 | 1 | - |
| ZERO | bin auto[15104:15359] | 0 | 1 | - |
| ZERO | bin auto[15360:15615] | 0 | 1 | - |
| ZERO | bin auto[15616:15871] | 0 | 1 | |
| ZERO | | Ü | 1 | |
| ZERO | bin auto[15872:16127] | 0 | 1 | - |
| ZERO | bin auto[16128:16383] | 0 | 1 | - |
| Cro | ess #cross0# | 0.41% | 100 | - |
| Uncover | ed covered/total bins: | 17 | 4096 | - |
| | missing/total bins: | 4079 | 4096 | _ |
| | % Hit: | 0.41% | 100 | _ |
| | | | | |

type_option.weight=1 type_option.goal=100 type_option.comment=

Auto, Default and User Defined Bins:

| Covered | bin <auto[256:287],auto[8192:8447]></auto[256:287],auto[8192:8447]> | 1 | 1 | - |
|---------|---|----|---|----|
| Covered | bin <auto[0:31],auto[8192:8447]></auto[0:31],auto[8192:8447]> | 2 | 1 | - |
| | bin <auto[0:31],auto[4096:4351]></auto[0:31],auto[4096:4351]> | 3 | 1 | _ |
| Covered | bin <auto[512:543],auto[2048:2303]></auto[512:543],auto[2048:2303]> | 2 | 1 | - |
| Covered | bin <auto[0:31],auto[1024:1279]></auto[0:31],auto[1024:1279]> | 5 | 1 | - |
| Covered | bin <auto[32:63],auto[512:767]></auto[32:63],auto[512:767]> | 1 | 1 | - |
| Covered | bin <auto[0:31],auto[512:767]></auto[0:31],auto[512:767]> | 4 | 1 | - |
| Covered | bin <auto[512:543],auto[256:511]></auto[512:543],auto[256:511]> | 1 | 1 | - |
| Covered | bin <auto[256:287],auto[256:511]></auto[256:287],auto[256:511]> | 1 | 1 | - |
| Covered | bin <auto[0:31],auto[256:511]></auto[0:31],auto[256:511]> | 6 | 1 | - |
| Covered | bin <auto[1024:1055],auto[0:255]></auto[1024:1055],auto[0:255]> | 1 | 1 | - |
| Covered | bin <auto[512:543],auto[0:255]></auto[512:543],auto[0:255]> | 3 | 1 | - |
| Covered | bin <auto[256:287],auto[0:255]></auto[256:287],auto[0:255]> | 5 | 1 | - |
| Covered | bin <auto[128:159],auto[0:255]></auto[128:159],auto[0:255]> | 3 | 1 | - |
| Covered | bin <auto[64:95],auto[0:255]></auto[64:95],auto[0:255]> | 3 | 1 | - |
| Covered | bin <auto[32:63],auto[0:255]></auto[32:63],auto[0:255]> | 3 | 1 | - |
| Covered | bin <auto[0:31],auto[0:255]></auto[0:31],auto[0:255]> | 21 | 1 | - |
| Covered | bin <auto[2016:2047],*></auto[2016:2047],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1984:2015],*></auto[1984:2015],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1952:1983],*></auto[1952:1983],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1920:1951],*></auto[1920:1951],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1888:1919],*></auto[1888:1919],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1856:1887],*></auto[1856:1887],*> | 0 | 1 | 64 |
| ZERO | | | | |

| ZEDO | bin <auto[1824:1855],*></auto[1824:1855],*> | 0 | 1 | 64 |
|--------------|---|---|---|----|
| ZERO ZERO | bin <auto[1792:1823],*></auto[1792:1823],*> | 0 | 1 | 64 |
| | bin <auto[1760:1791],*></auto[1760:1791],*> | 0 | 1 | 64 |
| ZERO ZERO | bin <auto[1728:1759],*></auto[1728:1759],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1696:1727],*></auto[1696:1727],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1664:1695],*></auto[1664:1695],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1632:1663],*></auto[1632:1663],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1600:1631],*></auto[1600:1631],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1568:1599],*></auto[1568:1599],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1536:1567],*></auto[1536:1567],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1504:1535],*></auto[1504:1535],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1472:1503],*></auto[1472:1503],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1440:1471],*></auto[1440:1471],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1408:1439],*></auto[1408:1439],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1376:1407],*></auto[1376:1407],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1344:1375],*></auto[1344:1375],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1312:1343],*></auto[1312:1343],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1280:1311],*></auto[1280:1311],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1248:1279],*></auto[1248:1279],*> | 0 | 1 | 64 |
| ZERO | bin <auto[1216:1247],*></auto[1216:1247],*> | 0 | 1 | 64 |
| | bin <auto[1184:1215],*></auto[1184:1215],*> | 0 | 1 | 64 |
| ZERO ZERO | bin <auto[1152:1183],*></auto[1152:1183],*> | 0 | 1 | 64 |
| | bin <auto[1120:1151],*></auto[1120:1151],*> | 0 | 1 | 64 |
| ZERO | | | | |

| ZEDO | bin <auto[1088:1119],*></auto[1088:1119],*> | 0 | 1 | 64 |
|--------------|---|---|---|----|
| ZERO ZERO | bin <auto[1056:1087],*></auto[1056:1087],*> | 0 | 1 | 64 |
| ZERO | bin <auto[992:1023],*></auto[992:1023],*> | 0 | 1 | 64 |
| ZERO | bin <auto[960:991],*></auto[960:991],*> | 0 | 1 | 64 |
| ZERO | bin <auto[928:959],*></auto[928:959],*> | 0 | 1 | 64 |
| ZERO | bin <auto[896:927],*></auto[896:927],*> | 0 | 1 | 64 |
| ZERO | bin <auto[864:895],*></auto[864:895],*> | 0 | 1 | 64 |
| ZERO | bin <auto[832:863],*></auto[832:863],*> | 0 | 1 | 64 |
| ZERO | bin <auto[800:831],*></auto[800:831],*> | 0 | 1 | 64 |
| ZERO | bin <auto[768:799],*></auto[768:799],*> | 0 | 1 | 64 |
| ZERO | bin <auto[736:767],*></auto[736:767],*> | 0 | 1 | 64 |
| ZERO | bin <auto[704:735],*></auto[704:735],*> | 0 | 1 | 64 |
| ZERO | bin <auto[672:703],*></auto[672:703],*> | 0 | 1 | 64 |
| ZERO | bin <auto[640:671],*></auto[640:671],*> | 0 | 1 | 64 |
| ZERO | bin <auto[608:639],*></auto[608:639],*> | 0 | 1 | 64 |
| ZERO | bin <auto[576:607],*></auto[576:607],*> | 0 | 1 | 64 |
| ZERO | bin <auto[544:575],*></auto[544:575],*> | 0 | 1 | 64 |
| ZERO | bin <auto[480:511],*></auto[480:511],*> | 0 | 1 | 64 |
| ZERO | bin <auto[448:479],*></auto[448:479],*> | 0 | 1 | 64 |
| ZERO | bin <auto[416:447],*></auto[416:447],*> | 0 | 1 | 64 |
| ZERO | bin <auto[384:415],*></auto[384:415],*> | 0 | 1 | 64 |
| ZERO | bin <auto[352:383],*></auto[352:383],*> | 0 | 1 | 64 |
| ZERO | bin <auto[320:351],*></auto[320:351],*> | 0 | 1 | 64 |
| | | | | |

| ZEDO | bin <auto[288:319],*></auto[288:319],*> | 0 | 1 | 64 |
|--------------|---|---|---|----|
| ZERO | bin <auto[224:255],*></auto[224:255],*> | 0 | 1 | 64 |
| ZERO | bin <auto[192:223],*></auto[192:223],*> | 0 | 1 | 64 |
| ZERO ZERO | bin <auto[160:191],*></auto[160:191],*> | 0 | 1 | 64 |
| ZERO | bin <auto[96:127],*></auto[96:127],*> | 0 | 1 | 64 |
| ZERO | bin <*,auto[16128:16383]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[15872:16127]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[15616:15871]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[15360:15615]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[15104:15359]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[14848:15103]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[14592:14847]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[14336:14591]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[14080:14335]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[13824:14079]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[13568:13823]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[13312:13567]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[13056:13311]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[12800:13055]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[12544:12799]> | 0 | 1 | 64 |
| | bin <*,auto[12288:12543]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[12032:12287]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[11776:12031]> | 0 | 1 | 64 |
| ZERO | | | | |

| 700 | bin <*,auto[11520:11775]> | 0 | 1 | 64 |
|--------------|---------------------------|---|---|----|
| ZERO ZERO | bin <*,auto[11264:11519]> | 0 | 1 | 64 |
| | bin <*,auto[11008:11263]> | 0 | 1 | 64 |
| ZERO ZERO | bin <*,auto[10752:11007]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[10496:10751]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[10240:10495]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[9984:10239]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[9728:9983]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[9472:9727]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[9216:9471]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[8960:9215]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[8704:8959]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[8448:8703]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[7936:8191]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[7680:7935]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[7424:7679]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[7168:7423]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[6912:7167]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[6656:6911]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[6400:6655]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[6144:6399]> | 0 | 1 | 64 |
| | bin <*,auto[5888:6143]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[5632:5887]> | 0 | 1 | 64 |
| ZERO | | | | |

| ZERO | bin <*,auto[5376:5631]> | 0 | 1 | 64 |
|------|---|---|---|----|
| ZERO | bin <*,auto[5120:5375]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[4864:5119]> | 0 | 1 | 64 |
| | bin <*,auto[4608:4863]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[4352:4607]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[3840:4095]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[3584:3839]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[3328:3583]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[3072:3327]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[2816:3071]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[2560:2815]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[2304:2559]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[1792:2047]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[1536:1791]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[1280:1535]> | 0 | 1 | 64 |
| ZERO | bin <*,auto[768:1023]> | 0 | 1 | 64 |
| ZERO | bin <auto[1024:1055],auto[8192:8447]></auto[1024:1055],auto[8192:8447]> | 0 | 1 | 1 |
| ZERO | bin <auto[512:543],auto[8192:8447]></auto[512:543],auto[8192:8447]> | 0 | 1 | 1 |
| ZERO | bin <auto[128:159],auto[8192:8447]></auto[128:159],auto[8192:8447]> | 0 | 1 | 1 |
| ZERO | bin <auto[64:95],auto[8192:8447]></auto[64:95],auto[8192:8447]> | 0 | 1 | 1 |
| ZERO | bin <auto[32:63],auto[8192:8447]></auto[32:63],auto[8192:8447]> | 0 | 1 | 1 |
| ZERO | bin <auto[1024:1055],auto[4096:4351]></auto[1024:1055],auto[4096:4351]> | 0 | 1 | 1 |
| ZERO | bin <auto[512:543],auto[4096:4351]></auto[512:543],auto[4096:4351]> | 0 | 1 | 1 |
| ZERO | | | | |

| ZED O | bin <auto[256:287],auto[4096:4351]></auto[256:287],auto[4096:4351]> | 0 | 1 | 1 |
|-------|---|---|---|---|
| ZERO | bin <auto[128:159],auto[4096:4351]></auto[128:159],auto[4096:4351]> | 0 | 1 | 1 |
| ZERO | bin <auto[64:95],auto[4096:4351]></auto[64:95],auto[4096:4351]> | 0 | 1 | 1 |
| ZERO | bin <auto[32:63],auto[4096:4351]></auto[32:63],auto[4096:4351]> | 0 | 1 | 1 |
| ZERO | bin <auto[1024:1055],auto[2048:2303]></auto[1024:1055],auto[2048:2303]> | 0 | 1 | 1 |
| ZERO | bin <auto[256:287],auto[2048:2303]></auto[256:287],auto[2048:2303]> | 0 | 1 | 1 |
| ZERO | bin <auto[128:159],auto[2048:2303]></auto[128:159],auto[2048:2303]> | 0 | 1 | 1 |
| ZERO | bin <auto[64:95],auto[2048:2303]></auto[64:95],auto[2048:2303]> | 0 | 1 | 1 |
| ZERO | bin <auto[32:63],auto[2048:2303]></auto[32:63],auto[2048:2303]> | 0 | 1 | 1 |
| ZERO | bin <auto[0:31],auto[2048:2303]></auto[0:31],auto[2048:2303]> | 0 | 1 | 1 |
| ZERO | bin <auto[1024:1055],auto[1024:1279]></auto[1024:1055],auto[1024:1279]> | 0 | 1 | 1 |
| ZERO | bin <auto[512:543],auto[1024:1279]></auto[512:543],auto[1024:1279]> | 0 | 1 | 1 |
| ZERO | | | | |
| ZERO | bin <auto[256:287],auto[1024:1279]></auto[256:287],auto[1024:1279]> | 0 | 1 | 1 |
| ZERO | bin <auto[128:159],auto[1024:1279]></auto[128:159],auto[1024:1279]> | 0 | 1 | 1 |
| ZERO | bin <auto[64:95],auto[1024:1279]></auto[64:95],auto[1024:1279]> | 0 | 1 | 1 |
| ZERO | bin <auto[32:63],auto[1024:1279]></auto[32:63],auto[1024:1279]> | 0 | 1 | 1 |
| ZERO | bin <auto[1024:1055],auto[512:767]></auto[1024:1055],auto[512:767]> | 0 | 1 | 1 |
| ZERO | bin <auto[512:543],auto[512:767]></auto[512:543],auto[512:767]> | 0 | 1 | 1 |
| ZERO | bin <auto[256:287],auto[512:767]></auto[256:287],auto[512:767]> | 0 | 1 | 1 |
| ZERO | bin <auto[128:159],auto[512:767]></auto[128:159],auto[512:767]> | 0 | 1 | 1 |
| ZERO | bin <auto[64:95],auto[512:767]></auto[64:95],auto[512:767]> | 0 | 1 | 1 |
| ZERO | bin <auto[1024:1055],auto[256:511]></auto[1024:1055],auto[256:511]> | 0 | 1 | 1 |
| ZERO | bin <auto[128:159],auto[256:511]></auto[128:159],auto[256:511]> | 0 | 1 | 1 |
| - | | | | |

| bin <auto[64:95],auto[256:511]></auto[64:95],auto[256:511]> | 0 | 1 | 1 |
|---|-------|------|------|
| ZERO | | | |
| bin <auto[32:63],auto[256:511]></auto[32:63],auto[256:511]> | 0 | 1 | 1 |
| ZERO | | | |
| Cross #cross1# | 0.00% | 100 | - |
| ZERO | | | |
| covered/total bins: | 0 | 1024 | - |
| | | | |
| missing/total bins: | 1024 | 1024 | - |
| | | | |
| % Hit: | 0.00% | 100 | - |
| | | | |
| type_option.weight=1 | | | |
| type_option.goal=100 | | | |
| type_option.comment= | | | |
| Auto, Default and User Defined Bins: | | | |
| bin <*,*> | 0 | 1 | 1024 |
| | | | |

ZERO

TOTAL COVERGROUP COVERAGE: 34.81% COVERGROUP TYPES: 1

Total Coverage By Design Unit (filtered view): 38.36%