Coverage and Run Reports

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Total Files: 7

File: Functional coverage report.txt

```
# Coverage Report by instance with details
#
# ================================================================================
# === Instance: /top_sv_unit
# === Design Unit: work.top_sv_unit
# ================================================================================
#
# Covergroup Coverage:
#     Covergroups                     1        na        na    81.25%
#         Coverpoints/Crosses         8        na        na        na
#             Covergroup Bins        56        52         4    92.85%
#
----------------------------------------------------------------------------------
------------------
# Covergroup                                            Metric       Goal       Bins
Status
#

#
----------------------------------------------------------------------------------
------------------
#  TYPE /top_sv_unit/alu_coverage/alu_cg                 81.25%        100          -
Uncovered
#     covered/total bins:                                    52         56          -

#     missing/total bins:                                     4         56          -

#     % Hit:                                             92.85%        100          -

#     Coverpoint opcode_check                            100.00%        100          -
Covered
#         covered/total bins:                                 2          2          -

#         missing/total bins:                                 0          2          -

#         % Hit:                                         100.00%        100          -

#         bin r_type                                       2464          1          -
Covered
#         bin i_type                                       2544          1          -
Covered
#     Coverpoint alu_check                               100.00%        100          -
Covered
```

```
#         covered/total bins:                              14         14          -

#         missing/total bins:                               0         14          -

#         % Hit:                                       100.00%        100          -

#         bin add                                          380          1          -
Covered
#         bin sub                                          340          1          -
Covered
#         bin and_op                                       353          1          -
Covered
#         bin or_op                                        365          1          -
Covered
#         bin xor_op                                       385          1          -
Covered
#         bin sll                                          379          1          -
Covered
#         bin srl                                          334          1          -
Covered
#         bin sra                                          355          1          -
Covered
#         bin slt                                          340          1          -
Covered
#         bin sltu                                         350          1          -
Covered
#         bin eq                                           325          1          -
Covered
#         bin neq                                          365          1          -
Covered
#         bin ge                                           364          1          -
Covered
#         bin geu                                          373          1          -
Covered
#     Coverpoint #coverpoint__0#                       100.00%        100          -
Covered
#         covered/total bins:                               2          2          -

#         missing/total bins:                               0          2          -

#         % Hit:                                       100.00%        100          -

#         bin reset_asserted                               282          1          -
Covered
#         bin reset_deasserted                            4726          1          -
Covered
```

```
#     Coverpoint #coverpoint__1#                          50.00%        100          -
Uncovered
#         covered/total bins:                                 1          2          -

#         missing/total bins:                               1          2          -

#         % Hit:                                          50.00%        100          -

#         bin disabled                                      0          1          -
ZERO
#         bin enabled                                    5008          1          -
Covered
#     Coverpoint #tr.rst_n__2#                          100.00%        100          -
Covered
#         covered/total bins:                               2          2          -

#         missing/total bins:                               0          2          -

#         % Hit:                                        100.00%        100          -

#         bin auto[0]                                     282          1          -
Covered
#         bin auto[1]                                    4726          1          -
Covered
#     Coverpoint #tr.i_ce__3#                           50.00%        100          -
Uncovered
#         covered/total bins:                               1          2          -

#         missing/total bins:                               1          2          -

#         % Hit:                                          50.00%        100          -

#         bin auto[0]                                       0          1          -
ZERO
#         bin auto[1]                                    5008          1          -
Covered
#     Cross #cross__0#                                  100.00%        100          -
Covered
#         covered/total bins:                              28         28          -

#         missing/total bins:                               0         28          -

#         % Hit:                                        100.00%        100          -

#         Auto, Default and User Defined Bins:
#             bin r_type_add                              194          1          -
```

Covered
bin r_type_sub 163 1 -
Covered
bin r_type_and 180 1 -
Covered
bin r_type_or 188 1 -
Covered
bin r_type_xor 181 1 -
Covered
bin r_type_sll 179 1 -
Covered
bin r_type_srl 169 1 -
Covered
bin r_type_sra 173 1 -
Covered
bin r_type_slt 167 1 -
Covered
bin r_type_sltu 170 1 -
Covered
bin r_type_eq 165 1 -
Covered
bin r_type_neq 177 1 -
Covered
bin r_type_ge 170 1 -
Covered
bin r_type_geu 188 1 -
Covered
bin i_type_add 186 1 -
Covered
bin i_type_sub 177 1 -
Covered
bin i_type_and 173 1 -
Covered
bin i_type_or 177 1 -
Covered
bin i_type_xor 204 1 -
Covered
bin i_type_sll 200 1 -
Covered
bin i_type_srl 165 1 -
Covered
bin i_type_sra 182 1 -
Covered
bin i_type_slt 173 1 -
Covered
bin i_type_sltu 180 1 -

```
Covered
#             bin i_type_eq                                  160          1          -
Covered
#             bin i_type_neq                                 188          1          -
Covered
#             bin i_type_ge                                  194          1          -
Covered
#             bin i_type_geu                                 185          1          -
Covered
#     Cross #cross__1#                                    50.00%        100          -
Uncovered
#         covered/total bins:                                 2          4          -

#         missing/total bins:                                 2          4          -

#         % Hit:                                          50.00%        100          -

#         Auto, Default and User Defined Bins:
#             bin <auto[1],auto[1]>                        4726          1          -
Covered
#             bin <auto[0],auto[1]>                         282          1          -
Covered
#             bin <*,auto[0]>                                 0          1          2
ZERO
#
# COVERGROUP COVERAGE:
#
------------------------------------------------------------------------------------
------------------
# Covergroup                                            Metric       Goal       Bins
Status
#

#
------------------------------------------------------------------------------------
------------------
#  TYPE /top_sv_unit/alu_coverage/alu_cg                81.25%        100          -
Uncovered
#     covered/total bins:                                  52         56          -

#     missing/total bins:                                   4         56          -

#     % Hit:                                           92.85%        100          -

#     Coverpoint opcode_check                         100.00%        100          -
Covered
```

```
#         covered/total bins:                                2          2          -

#         missing/total bins:                                0          2          -

#         % Hit:                                        100.00%        100          -

#         bin r_type                                      2464          1          -
Covered
#         bin i_type                                      2544          1          -
Covered
#     Coverpoint alu_check                              100.00%        100          -
Covered
#         covered/total bins:                               14         14          -

#         missing/total bins:                                0         14          -

#         % Hit:                                        100.00%        100          -

#         bin add                                          380          1          -
Covered
#         bin sub                                          340          1          -
Covered
#         bin and_op                                       353          1          -
Covered
#         bin or_op                                        365          1          -
Covered
#         bin xor_op                                       385          1          -
Covered
#         bin sll                                          379          1          -
Covered
#         bin srl                                          334          1          -
Covered
#         bin sra                                          355          1          -
Covered
#         bin slt                                          340          1          -
Covered
#         bin sltu                                         350          1          -
Covered
#         bin eq                                           325          1          -
Covered
#         bin neq                                          365          1          -
Covered
#         bin ge                                           364          1          -
Covered
#         bin geu                                          373          1          -
Covered
```

```
#     Coverpoint #coverpoint__0#                    100.00%        100          -
Covered
#         covered/total bins:                             2          2          -

#         missing/total bins:                             0          2          -

#         % Hit:                                    100.00%        100          -

#         bin reset_asserted                            282          1          -
Covered
#         bin reset_deasserted                         4726          1          -
Covered
#     Coverpoint #coverpoint__1#                     50.00%        100          -
Uncovered
#         covered/total bins:                             1          2          -

#         missing/total bins:                             1          2          -

#         % Hit:                                     50.00%        100          -

#         bin disabled                                    0          1          -
ZERO
#         bin enabled                                  5008          1          -
Covered
#     Coverpoint #tr.rst_n__2#                      100.00%        100          -
Covered
#         covered/total bins:                             2          2          -

#         missing/total bins:                             0          2          -

#         % Hit:                                    100.00%        100          -

#         bin auto[0]                                   282          1          -
Covered
#         bin auto[1]                                  4726          1          -
Covered
#     Coverpoint #tr.i_ce__3#                        50.00%        100          -
Uncovered
#         covered/total bins:                             1          2          -

#         missing/total bins:                             1          2          -

#         % Hit:                                     50.00%        100          -

#         bin auto[0]                                     0          1          -
ZERO
```

```
#         bin auto[1]                                  5008          1          -
Covered
#     Cross #cross__0#                               100.00%        100          -
Covered
#         covered/total bins:                            28         28          -

#         missing/total bins:                             0         28          -

#         % Hit:                                     100.00%        100          -

#         Auto, Default and User Defined Bins:
#             bin r_type_add                           194          1          -
Covered
#             bin r_type_sub                           163          1          -
Covered
#             bin r_type_and                           180          1          -
Covered
#             bin r_type_or                            188          1          -
Covered
#             bin r_type_xor                           181          1          -
Covered
#             bin r_type_sll                           179          1          -
Covered
#             bin r_type_srl                           169          1          -
Covered
#             bin r_type_sra                           173          1          -
Covered
#             bin r_type_slt                           167          1          -
Covered
#             bin r_type_sltu                          170          1          -
Covered
#             bin r_type_eq                            165          1          -
Covered
#             bin r_type_neq                           177          1          -
Covered
#             bin r_type_ge                            170          1          -
Covered
#             bin r_type_geu                           188          1          -
Covered
#             bin i_type_add                           186          1          -
Covered
#             bin i_type_sub                           177          1          -
Covered
#             bin i_type_and                           173          1          -
Covered
#             bin i_type_or                            177          1          -
```

```
Covered
#             bin i_type_xor                                  204          1          -
Covered
#             bin i_type_sll                                  200          1          -
Covered
#             bin i_type_srl                                  165          1          -
Covered
#             bin i_type_sra                                  182          1          -
Covered
#             bin i_type_slt                                  173          1          -
Covered
#             bin i_type_sltu                                 180          1          -
Covered
#             bin i_type_eq                                   160          1          -
Covered
#             bin i_type_neq                                  188          1          -
Covered
#             bin i_type_ge                                   194          1          -
Covered
#             bin i_type_geu                                  185          1          -
Covered
#     Cross #cross__1#                                    50.00%        100          -
Uncovered
#         covered/total bins:                                 2          4          -

#         missing/total bins:                                 2          4          -

#         % Hit:                                          50.00%        100          -

#         Auto, Default and User Defined Bins:
#             bin <auto[1],auto[1]>                        4726          1          -
Covered
#             bin <auto[0],auto[1]>                         282          1          -
Covered
#             bin <*,auto[0]>                                 0          1          2
ZERO
#
# TOTAL COVERGROUP COVERAGE: 81.25%  COVERGROUP TYPES: 1
#
# Total Coverage By Instance (filtered view): 81.25%
#
#
```

File: UVM topology.txt

```
# ----------------------------------------------------------------
# Name                        Type                     Size  Value
# ----------------------------------------------------------------
# uvm_test_top                alu_base_test            -     @472
#   env                       alu_env                  -     @479
#     agent                   alu_agent                -     @486
#       driver                alu_driver               -     @644
#         rsp_port            uvm_analysis_port        -     @659
#         seq_item_port       uvm_seq_item_pull_port   -     @651
#       monitor               alu_monitor              -     @520
#         mon2scb             uvm_analysis_port        -     @527
#       sequencer             uvm_sequencer            -     @535
#         rsp_export          uvm_analysis_export      -     @542
#         seq_item_export     uvm_seq_item_pull_imp    -     @636
#         arbitration_queue   array                    0     -
#         lock_queue          array                    0     -
#         num_last_reqs       integral                 32    'd1
#         num_last_rsps       integral                 32    'd1
#     coverage                alu_coverage             -     @500
#       analysis_imp          uvm_analysis_imp         -     @507
#     scoreboard              alu_scoreboard           -     @493
#       scb_port              uvm_analysis_imp         -     @674
# ----------------------------------------------------------------
#
```

File: code_coverage.txt

Coverage Report by DU with details

```
================================================================================
=== Design Unit: work.rv32i_alu
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        43        43         0   100.00%

================================Branch Details================================

Branch Coverage for Design Unit work.rv32i_alu

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File rv32i_alu.sv
------------------------------------IF Branch------------------------------------
    150                                     5273     Count coming in to IF
    150             1                        546             if (!i_rst_n) begin
    154             1                       4727             end else begin
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    156                                     4727     Count coming in to IF
    156             1                       4725                 if (i_ce && !stall_bit)
begin  //update logicister only if this stage is enabled
                                               2     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    176                                     4727     Count coming in to IF
     179              1                             4726                     end else if
(!stall_bit) begin  //clock-enable will change only when not stalled
Branch totals: 1 hit of 1 branch = 100.00%

------------------------------------IF Branch------------------------------------
    196                                     5008     Count coming in to IF
     196              1                          2463              b    = (opcode_rtype ||
opcode_branch) ? i_rs2 : i_imm;  // b can either be rs2 or imm
     196              2                          2545              b    = (opcode_rtype ||
opcode_branch) ? i_rs2 : i_imm;  // b can either be rs2 or imm
Branch totals: 2 hits of 2 branches = 100.00%
```

```
------------------------------------IF Branch------------------------------------
    197                                     5009     Count coming in to IF
    197             1                        380              if (alu_add) y_d = a + b;
                                            4629     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    198                                     5009     Count coming in to IF
    198             1                        340              if (alu_sub) y_d = a - b;
                                            4669     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    199                                     5009     Count coming in to IF
    199              1                          718              if (alu_slt || alu_sltu)
begin
                                            4291     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    201                                      718     Count coming in to IF
    201              1                           353                   if (alu_slt) y_d =
(a[31] ^ b[31]) ? {31'b0, a[31]} : y_d;
                                             365     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    201                                      353     Count coming in to IF
    201              2                           169                   if (alu_slt) y_d =
(a[31] ^ b[31]) ? {31'b0, a[31]} : y_d;
    201              3                           184                   if (alu_slt) y_d =
(a[31] ^ b[31]) ? {31'b0, a[31]} : y_d;
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    203                                     5009     Count coming in to IF
    203             1                        385              if (alu_xor) y_d = a ^ b;
                                            4624     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    204                                     5009     Count coming in to IF
    204             1                        379              if (alu_or) y_d = a | b;
                                            4630     All False Count
Branch totals: 2 hits of 2 branches = 100.00%
```

```
------------------------------------IF Branch------------------------------------
    205                                     5009     Count coming in to IF
    205             1                        334             if (alu_and) y_d = a & b;
                                            4675     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    206                                     5009     Count coming in to IF
    206             1                           355             if (alu_sll) y_d = a <<
b[4:0];
                                            4654     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    207                                     5009     Count coming in to IF
    207             1                           340             if (alu_srl) y_d = a >>
b[4:0];
                                            4669     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    208                                     5009     Count coming in to IF
    208              1                          350               if (alu_sra) y_d =
$signed(a) >>> b[4:0];
                                            4659     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    209                                     5009     Count coming in to IF
    209             1                           690              if (alu_eq || alu_neq)
begin
                                            4319     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    211                                      690     Count coming in to IF
    211             1                           365                  if (alu_neq) y_d =
{31'b0, !y_d[0]};
                                             325     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    213                                     5009     Count coming in to IF
    213             1                           737              if (alu_ge || alu_geu)
begin
```

```
                                          4272     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-------------------------------------
    215                                   737     Count coming in to IF
     215              1                         364                   if (alu_ge) y_d =
(a[31] ^ b[31]) ? {31'b0, b[31]} : y_d;
                                          373     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-------------------------------------
    215                                   364     Count coming in to IF
     215              2                         179                   if (alu_ge) y_d =
(a[31] ^ b[31]) ? {31'b0, b[31]} : y_d;
     215              3                         185                   if (alu_ge) y_d =
(a[31] ^ b[31]) ? {31'b0, b[31]} : y_d;
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-------------------------------------
    227                                 10015     Count coming in to IF
    227             1                   10013             if (!i_flush) begin
                                            2     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-------------------------------------
    228                                 10013     Count coming in to IF
     228             1                    10011                   if (opcode_rtype ||
opcode_itype) rd_d = y_d;
                                             2     All False Count
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Conditions                      12        12         0   100.00%

================================Condition Details================================

Condition Coverage for Design Unit work.rv32i_alu --

  File rv32i_alu.sv
----------------Focused Condition View-------------------
Line       199 Item    1  (alu_slt || alu_sltu)
Condition totals: 2 of 2 input terms covered = 100.00%
```

```
-----------Focused Condition View (Bimodal)-------------
Line       201 Item    1  (a[31] ^ b[31])
Condition totals: 2 of 2 input terms covered = 100.00%

----------------Focused Condition View-------------------
Line       209 Item    1  (alu_eq || alu_neq)
Condition totals: 2 of 2 input terms covered = 100.00%

----------------Focused Condition View-------------------
Line       213 Item    1  (alu_ge || alu_geu)
Condition totals: 2 of 2 input terms covered = 100.00%

-----------Focused Condition View (Bimodal)-------------
Line       215 Item    1  (a[31] ^ b[31])
Condition totals: 2 of 2 input terms covered = 100.00%

----------------Focused Condition View-------------------
Line       228 Item    1  (opcode_rtype || opcode_itype)
Condition totals: 2 of 2 input terms covered = 100.00%


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      47        47         0   100.00%

================================Statement Details================================

Statement Coverage for Design Unit work.rv32i_alu --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File rv32i_alu.sv
    31                                               module rv32i_alu (
    32                                                   i_clk,
    33                                                   i_rst_n,
    34                                                   i_alu,
    35                                                   i_rs1_addr,
    36                                                   i_rs1,
    37                                                   i_rs2,
    38                                                   i_imm,
    39                                                   i_funct3,
    40                                                   i_opcode,
    41                                                   i_exception,
    42                                                   i_pc,
    43                                                   i_rd_addr,
```

```
    44                                                  i_ce,
    45                                                  i_stall,
    46                                                  i_force_stall,
    47                                                  i_flush,
    48                                                  o_rs1_addr,
    49                                                  o_rs1,
    50                                                  o_rs2,
    51                                                  o_imm,
    52                                                  o_funct3,
    53                                                  o_opcode,
    54                                                  o_exception,
    55                                                  o_y,
    56                                                  o_pc,
    57                                                  o_next_pc,
    58                                                  o_change_pc,
    59                                                  o_wr_rd,
    60                                                  o_rd_addr,
    61                                                  o_rd,
    62                                                  o_rd_valid,
    63                                                  o_stall_from_alu,
    64                                                  o_ce,
    65                                                  o_stall,
    66                                                  o_flush
    67                                              );
    68                                                  input logic i_clk, i_rst_n;
    69                                                      input logic [`ALU_WIDTH-1:0]
i_alu;  //alu operation type from previous stage
    70                                                    input logic [4:0] i_rs1_addr;
//address for logicister source 1
    71                                                     input logic [31:0] i_rs1;  //
Source logicister 1 value
    72                                                        input logic [31:0] i_rs2;
//Source logicister 2 value
    73                                                        input logic [31:0] i_imm;
//Immediate value from previous stage
    74                                                     input logic [2:0] i_funct3;
//function type from previous stage
    75                                                   input logic [`OPCODE_WIDTH-1:0]
i_opcode;  //opcode type from previous stage
     76                                                                          input logic
[`EXCEPTION_WIDTH-1:0] i_exception;  //exception from decoder stage
    77                                                         input logic [31:0] i_pc;
//Program Counter
    78                                                    input logic [4:0] i_rd_addr;
//address for destination logicister (from previous stage)
    79                                                  input logic i_ce;  // input clk
```

```
enable for pipeline stalling of this stage
    80                                                      // coverage off
    81                                                       input logic i_stall;  //informs
this stage to stall
    82                                                          input logic i_force_stall;
//force this stage to stall
    83                                                        input logic i_flush;  //flush
this stage
    84                                                      // coverage on
    85                                                       output logic [4:0] o_rs1_addr;
//address for logicister source 1
    86                                                          output logic [31:0] o_rs1;
//Source logicister 1 value
    87                                                          output logic [31:0] o_rs2;
//Source logicister 2 value
    88                                                          output logic [11:0] o_imm;
//Immediate value
    89                                                        output logic [2:0] o_funct3;
// function type
     90                                                                          output logic
[`OPCODE_WIDTH-1:0] o_opcode;  //opcode type
     91                                                                          output logic
[`EXCEPTION_WIDTH-1:0] o_exception;  //exception: illegal inst,ecall,ebreak,mret
    92                                                           output logic [31:0] o_y;
//result of arithmetic operation
    93                                                       output logic [31:0] o_pc;  //pc
logicister in pipeline
    94                                                       output logic [31:0] o_next_pc;
//new pc value
    95                                                           output logic o_change_pc;
//high if PC needs to jump
    96                                                        output logic o_wr_rd;  //write
rd to the base logic if enabled
    97                                                        output logic [4:0] o_rd_addr;
//address for destination logicister
    98                                                           output logic [31:0] o_rd;
//value to be written back to destination logicister
    99                                                            output logic o_rd_valid;
//high if o_rd is valid (not load nor csr instruction)
    100                                                     // coverage off
    101                                                     output logic o_stall_from_alu
    102                                                           ;  //prepare to stall next
stage(memory-access stage) for load/store instruction
    103                                                     // coverage on
    104                                                       output logic o_ce;  // output
clk enable for pipeline stalling of next stage
```

```
    105                                                 // coverage off
     106                                                         output logic o_stall;
//informs pipeline to stall
    107                                                  output logic o_flush;  //flush
previous stages
    108                                                 // coverage on
    109                                                 // Internal signals
    110                                                 logic        alu_add;
    111                                                 logic        alu_sub;
    112                                                 logic        alu_slt;
    113                                                 logic        alu_sltu;
    114                                                 logic        alu_xor;
    115                                                 logic        alu_or;
    116                                                 logic        alu_and;
    117                                                 logic        alu_sll;
    118                                                 logic        alu_srl;
    119                                                 logic        alu_sra;
    120                                                 logic        alu_eq;
    121                                                 logic        alu_neq;
    122                                                 logic        alu_ge;
    123                                                 logic        alu_geu;
    124                                                 logic        opcode_rtype;
    125                                                 logic        opcode_itype;
    126                                                 // coverage off
    127                                                 logic        opcode_load;
    128                                                 logic        opcode_store;
    129                                                 logic        opcode_branch;
    130                                                 logic        opcode_jal;
    131                                                 logic        opcode_jalr;
    132                                                 logic        opcode_lui;
    133                                                 logic        opcode_auipc;
    134                                                 logic        opcode_system;
    135                                                 logic        opcode_fence;
    136                                                 // coverage on
    137                                                 logic [31:0] a;  //operand A
    138                                                 logic [31:0] b;  //operand B
    139                                                 logic [31:0] y_d;  //ALU output
     140                                                      logic [31:0] rd_d;  //next
value to be written back to destination logicister
    141                                                  logic        wr_rd_d;  //write
rd to baselogic if enabled
     142                                                      logic         rd_valid_d;
//high if rd is valid (not load nor csr instruction)
    143                                                 logic [31:0] a_pc;
    144                                                 logic [31:0] sum;
    145                                                 // coverage off
```

```
    146                                                 logic        stall_bit;
    147                                                 // coverage on
     148                                                      //logicister the output of
i_alu
     149              1                          5273          always_ff @(posedge i_clk,
negedge i_rst_n) begin
    150                                                     if (!i_rst_n) begin
    151              1                           546                o_exception      <= 0;
    152              1                           546                o_ce             <= 0;
    153              1                           546                o_stall_from_alu <= 0;
    154                                                     end else begin
    155                                                          // coverage off -item c
1
    156                                                          if (i_ce && !stall_bit)
begin  //update logicister only if this stage is enabled
     157              1                           4725                    o_opcode <=
i_opcode;
     158              1                          4725                   o_exception <=
i_exception;
    159              1                         4725                  o_y <= y_d;
     160              1                          4725                    o_rs1_addr <=
i_rs1_addr;
    161              1                         4725                  o_rs1 <= i_rs1;
    162              1                         4725                  o_rs2 <= i_rs2;
     163              1                          4725                    o_rd_addr <=
i_rd_addr;
     164              1                           4725                      o_imm <=
i_imm[11:0];
     165              1                          4725                    o_funct3 <=
i_funct3;
    166              1                         4725                  o_rd <= rd_d;
     167              1                          4725                    o_rd_valid <=
rd_valid_d;
    168              1                         4725                  o_wr_rd <= wr_rd_d;
    169                                                     // coverage off
    170                                                      o_stall_from_alu <=
i_opcode[`STORE] || i_opcode[`LOAD]
    171                                                          ;  //stall next
stage(memory-access stage) when need to store/load
    172                                                     // coverage on
     173              1                          4725                   o_pc <= i_pc;
//since accessing data memory always takes more than 1 cycle
    174                                                 end
    175                                                 // coverage off
     176                                                          if (i_flush &&
!stall_bit) begin  //flush this stage so clock-enable of next stage is disabled at next
```

```
clock cycle
    177                                                         o_ce <= 0;
    178                                                         // coverage on
     179                                                                 end else if
(!stall_bit) begin  //clock-enable will change only when not stalled
    180             1                       4726                o_ce <= i_ce;
    181                                                         // coverage off
    182                                                       end else if (stall_bit
&& !i_stall)
    183                                                           o_ce <= 0;  //if
this stage is stalled but next stage is not, disable
    184                                                     // coverage on
    185                                                       //clock enable of next
stage at next clock cycle (pipeline bubble)
    186                                                 end
    187                                             end
    188                                                  // determine operation used
then compute for y output
    189
    190             1                       5009        always_comb begin
    191             1                       5009            y_d = 0;
    192                                                     // coverage off
    193                                                            a   = (opcode_jal ||
opcode_auipc) ? i_pc : i_rs1;  // a can either be pc or rs1
    194                                                     // coverage on
    195                                                     // coverage off -item c 1
    196              1                         5009              b   = (opcode_rtype ||
opcode_branch) ? i_rs2 : i_imm;  // b can either be rs2 or imm
    197             1                        380             if (alu_add) y_d = a + b;
    198             1                        340             if (alu_sub) y_d = a - b;
    199                                                     if (alu_slt || alu_sltu)
begin
    200             1                        718                 y_d = {31'b0, (a < b)};
    201              1                           353                 if (alu_slt) y_d =
(a[31] ^ b[31]) ? {31'b0, a[31]} : y_d;
    202                                                     end
    203             1                        385             if (alu_xor) y_d = a ^ b;
    204             1                        379             if (alu_or) y_d = a | b;
    205             1                        334             if (alu_and) y_d = a & b;
    206              1                          355              if (alu_sll) y_d = a <<
b[4:0];
    207              1                          340              if (alu_srl) y_d = a >>
b[4:0];
     208               1                             350               if (alu_sra) y_d =
$signed(a) >>> b[4:0];
    209                                                      if (alu_eq || alu_neq)
```

```
begin
    210              1                          690                  y_d = {31'b0, (a ==
b)};
    211              1                          365                   if (alu_neq) y_d =
{31'b0, !y_d[0]};
    212                                                          end
    213                                                               if (alu_ge || alu_geu)
begin
    214              1                          737                  y_d = {31'b0, (a >=
b)};
    215              1                          364                   if (alu_ge) y_d =
(a[31] ^ b[31]) ? {31'b0, b[31]} : y_d;
    216                                                          end
    217                                                      end
    218                                                       //determine o_rd to be saved to
baseg and next value of PC
    219              1                      10015        always_comb begin
    220              1                      10015                o_flush     = i_flush;
//flush this stage along with the previous stages
    221              1                      10015            rd_d        = 0;
    222              1                      10015            rd_valid_d  = 0;
    223              1                      10015            o_change_pc = 0;
    224              1                      10015            o_next_pc   = 0;
    225              1                      10015            wr_rd_d     = 0;
    226              1                      10015            a_pc        = i_pc;
    227                                                       if (!i_flush) begin
    228              1                      10011                 if (opcode_rtype ||
opcode_itype) rd_d = y_d;
    229                                                           // coverage off
    230                                                              if (opcode_branch &&
y_d[0]) begin
    231                                                                 o_next_pc = sum;
//branch iff value of ALU is 1(true)
    232                                                              o_change_pc =
    233                                                                   i_ce;  //change
PC when ce of this stage is high (o_change_pc is valid)
    234                                                              o_flush = i_ce;
    235                                                          end
    236                                                                 if (opcode_jal ||
opcode_jalr) begin
    237                                                                  if (opcode_jalr)
a_pc = i_rs1;
    238                                                                 o_next_pc = sum;
//jump to new PC
    239                                                              o_change_pc =
    240                                                                   i_ce;  //change
```

PC when ce of this stage is high (o_change_pc is valid)
241 o_flush = i_ce;
242 rd_d = i_pc + 4;
//logicister the next pc value to destination logicister
243 end
244 // coverage on
245 end
246 // coverage off
247 if (opcode_lui) rd_d =
i_imm;
248 if (opcode_auipc) rd_d =
sum;
249 if (opcode_branch ||
opcode_store || (opcode_system && i_funct3 == 0) || opcode_fence)
250 wr_rd_d = 0;
//i_funct3==0 are the non-csr system instructions
251 else
252 wr_rd_d = 1; //always
write to the destination logic except when instruction is BRANCH or STORE or
SYSTEM(except CSR system instruction)
253 if (opcode_load ||
(opcode_system && i_funct3 != 0))
254 rd_valid_d =
255 0; //value of o_rd
for load and CSR write is not yet available at this stage
256 else rd_valid_d = 1;
257 // coverage on
258 //stall logic (stall when
upper stages are stalled, when forced to stall, or when needs to flush previous stages
but are still stalled)
259 1 10015 o_stall = (i_stall ||
i_force_stall) && !i_flush; //stall when alu needs wait time
260 end
261
262 assign
263 1 10004 sum = a_pc + i_imm;
//share adder for all addition operation for less resource utilization
264 1 3 assign stall_bit = o_stall ||
i_stall;

Total Coverage By Design Unit (filtered view): 100.00%

File: coverage_all_files_default.txt

Coverage Report Summary Data by file

```
================================================================================
=== File: agent.sv
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        12         5         7    41.66%
    Statements                      20        16         4    80.00%

================================================================================
=== File: coverage.sv
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         4         2         2    50.00%
    Conditions                       2         0         2     0.00%
    Statements                       9         6         3    66.66%

================================================================================
=== File: driver.sv
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        16         6        10    37.50%
    Statements                      50        31        19    62.00%

================================================================================
=== File: environment.sv
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         2         1         1    50.00%
    Statements                      15        12         3    80.00%

================================================================================
=== File: interface.sv
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      37        37         0   100.00%

================================================================================
```

```
=== File: monitor.sv
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        16         6        10    37.50%
    Statements                      59        52         7    88.13%

================================================================================
=== File: rv32i_alu.sv
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        43        42         1    97.67%
    Conditions                      12        10         2    83.33%
    Statements                      47        47         0   100.00%

================================================================================
=== File: scoreboard.sv
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                       139        74        65    53.23%
    Conditions                      29        10        19    34.48%
    Statements                      98        62        36    63.26%

================================================================================
=== File: sequencer.sv
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        58        30        28    51.72%
    Conditions                       2         0         2     0.00%
    Statements                     798       776        22    97.24%

================================================================================
=== File: test.sv
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                         6         2         4    33.33%
    Statements                      21        18         3    85.71%

================================================================================
=== File: top.sv
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
```

```
    ---------------               ----      ----    ------  --------
    Statements                       7         6         1    85.71%

================================================================================
=== File: transaction.sv
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        45         0        45     0.00%
    Conditions                       9         0         9     0.00%
    Statements                      80        13        67    16.25%


TOTAL COVERGROUP COVERAGE: 81.25%  COVERGROUP TYPES: 1

TOTAL ASSERTION COVERAGE: 0.00%  ASSERTIONS: 2

Total Coverage By File (code coverage only, filtered view): 57.66%
```

File: report.txt

Recursive Coverage Report Summary Data by DU

```
================================================================================
=== Design Unit: work.top_sv_unit
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                       298       126       172    42.28%
    Conditions                      42        10        32    23.80%
    Covergroups                      1        na        na    81.25%
        Coverpoints/Crosses          8        na        na       na
            Covergroup Bins         56        52         4    92.85%
    Statements                    1150       986       164    85.73%

================================================================================
=== Design Unit: work.alu_if
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Assertions                       2         0         2     0.00%
    Statements                      37        37         0   100.00%

================================================================================
=== Design Unit: work.rv32i_alu
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        43        42         1    97.67%
    Conditions                      12        10         2    83.33%
    Statements                      47        47         0   100.00%

================================================================================
=== Design Unit: work.top
================================================================================
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Assertions                       2         0         2     0.00%
    Branches                        43        42         1    97.67%
    Conditions                      12        10         2    83.33%
    Statements                      91        90         1    98.90%


Total Coverage By Design Unit (filtered view): 50.85%
```

File: report_1000.txt

Coverage Report by DU with details

```
================================================================================
=== Design Unit: work.coverage_sv_unit
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                       145        75        70    51.72%

================================Branch Details================================

Branch Coverage for Design Unit work.coverage_sv_unit

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File transaction.sv
------------------------------------CASE Branch------------------------------------
    224                                     1025     Count coming in to CASE
    225             1                         68
    227             1                         83
    229             1                         74
    231             1                         61
    233             1                         79
    235             1                         70
    237             1                         79
    239             1                         68
    242             1                         84
    244             1                         79
    245             1                         82
    246             1                         70
    247             1                         70
    249             1                         58
    250             1                    ***0***
Branch totals: 14 hits of 15 branches = 93.33%

-----------------------------------IF Branch-----------------------------------
    226                                       68     Count coming in to IF
    226             1                         10
    226             2                         58
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
```

```
    228                                   83     Count coming in to IF
    228             1                      9
    228             2                     74
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    230                                   74     Count coming in to IF
    230             1                      7
    230             2                     67
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    232                                   61     Count coming in to IF
    232             1                      8
    232             2                     53
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    234                                   79     Count coming in to IF
    234             1                      9
    234             2                     70
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    236                                   70     Count coming in to IF
    236             1                      7
    236             2                     63
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    238                                   79     Count coming in to IF
    238             1                      7
    238             2                     72
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    241                                   68     Count coming in to IF
    241             1                      4
    241             2                     64
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    243                                   84     Count coming in to IF
    243             1                     42
    243             2                     42
Branch totals: 2 hits of 2 branches = 100.00%
```

```
------------------------------------IF Branch------------------------------------
    244                                     79     Count coming in to IF
    244             2                       42
    244             3                       37
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    245                                     82     Count coming in to IF
    245             2                        2
    245             3                       80
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    246                                     70     Count coming in to IF
    246             2                       70
    246             3                    ***0***
Branch totals: 1 hit of 2 branches = 50.00%

------------------------------------IF Branch------------------------------------
    248                                     70     Count coming in to IF
    248             1                       31
    248             2                       39
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    249                                     58     Count coming in to IF
    249             2                       25
    249             3                       33
Branch totals: 2 hits of 2 branches = 100.00%


  File coverage.sv
------------------------------------IF Branch------------------------------------
    69                                   50001     Count coming in to IF
    69              1                      914
                                         49087     All False Count
Branch totals: 2 hits of 2 branches = 100.00%


  File generator.sv
-----------------------------------CASE Branch-----------------------------------
    131                                   1000     Count coming in to CASE
    132             1                      334
    136             1                      333
    140             1                      333
```

```
    143             1                     ***0***
Branch totals: 3 hits of 4 branches = 75.00%

-----------------------------------IF Branch-----------------------------------
    149                                     1000     Count coming in to IF
    149             1                     ***0***
                                            1000     All False Count
Branch totals: 1 hit of 2 branches = 50.00%

----------------------------------CASE Branch----------------------------------
    372                                     1025     Count coming in to CASE
    373             1                         68
    374             1                         83
    375             1                         74
    376             1                         61
    377             1                         79
    378             1                         70
    379             1                         79
    380             1                         68
    381             1                         84
    382             1                         79
    383             1                         82
    384             1                         70
    385             1                         70
    386             1                         58
    387             1                     ***0***
Branch totals: 14 hits of 15 branches = 93.33%

----------------------------------CASE Branch----------------------------------
    391                                     1025     Count coming in to CASE
    392             1                        113
    393             1                         91
    394             1                        102
    395             1                         91
    396             1                        109
    397             1                         88
    398             1                         82
    399             1                         76
    400             1                         77
    401             1                        105
    402             1                          2
    403             1                         89
Branch totals: 12 hits of 12 branches = 100.00%


  File monitor.sv
```

```
-----------------------------------IF Branch-----------------------------------
    51                                    50001     Count coming in to IF
    51              1                       914
                                          49087     All False Count
Branch totals: 2 hits of 2 branches = 100.00%


  File scoreboard.sv
-----------------------------------IF Branch-----------------------------------
    160                                   ***0***     Count coming in to IF
    160             1                     ***0***
    162             1                     ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    165                                   ***0***     Count coming in to IF
    165             1                     ***0***
    165             2                     ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    166                                   ***0***     Count coming in to IF
    166             1                     ***0***
    166             2                     ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    170                                   ***0***     Count coming in to IF
    170             1                     ***0***
                                          ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    172                                   ***0***     Count coming in to IF
    172             1                     ***0***
                                          ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    177                                   ***0***     Count coming in to IF
    177             1                     ***0***
                                          ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    187                                   ***0***     Count coming in to IF
```

```
    187             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-------------------------------------
    188                                 ***0***     Count coming in to IF
    188             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-------------------------------------
    191                                 ***0***     Count coming in to IF
    191             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-------------------------------------
    201                                 ***0***     Count coming in to IF
    201             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-------------------------------------
    206                                 ***0***     Count coming in to IF
    206             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-------------------------------------
    215                                 ***0***     Count coming in to IF
    215             1                   ***0***
    215             2                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-------------------------------------
    218                                 ***0***     Count coming in to IF
    218             1                   ***0***
    218             2                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-------------------------------------
    221                                 ***0***     Count coming in to IF
    221             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%
```

```
-----------------------------------IF Branch-----------------------------------
    226                                 ***0***     Count coming in to IF
    226             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    227                                 ***0***     Count coming in to IF
    227             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    247                                 ***0***     Count coming in to IF
    247             1                   ***0***
    249             1                   ***0***
    251             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 4 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    257                                 ***0***     Count coming in to IF
    257             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

----------------------------------CASE Branch----------------------------------
    305                                 ***0***     Count coming in to CASE
    308             1                   ***0***
    309             1                   ***0***
    310             1                   ***0***
    311             1                   ***0***
    313             1                   ***0***
    314             1                   ***0***
    315             1                   ***0***
    316             1                   ***0***
    317             1                   ***0***
    318             1                   ***0***
    319             1                   ***0***
    320             1                   ***0***
    321             1                   ***0***
    322             1                   ***0***
    323             1                   ***0***
Branch totals: 0 hits of 15 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
```

```
    310                                 ***0***     Count coming in to IF
    310             2                   ***0***
    310             3                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch------------------------------------
    312                                 ***0***     Count coming in to IF
    312             1                   ***0***
    312             2                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch------------------------------------
    319                                 ***0***     Count coming in to IF
    319             2                   ***0***
    319             3                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch------------------------------------
    320                                 ***0***     Count coming in to IF
    320             2                   ***0***
    320             3                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch------------------------------------
    321                                 ***0***     Count coming in to IF
    321             2                   ***0***
    321             3                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch------------------------------------
    322                                 ***0***     Count coming in to IF
    322             2                   ***0***
    322             3                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%


Condition Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Conditions                      65         5        60     7.69%

================================Condition Details================================

Condition Coverage for Design Unit work.coverage_sv_unit --

  File transaction.sv
```

```
----------------Focused Condition View-------------------
Line       243 Item    1  (rs1 < rs2)
Condition totals: 1 of 1 input term covered = 100.00%

   Input Term   Covered  Reason for no coverage   Hint
  -----------  --------  ----------------------  --------------
  (rs1 < rs2)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (rs1 < rs2)_0         -
  Row   2:          1  (rs1 < rs2)_1         -

----------------Focused Condition View-------------------
Line       244 Item    1  (rs1 < rs2)
Condition totals: 1 of 1 input term covered = 100.00%

   Input Term   Covered  Reason for no coverage   Hint
  -----------  --------  ----------------------  --------------
  (rs1 < rs2)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (rs1 < rs2)_0         -
  Row   2:          1  (rs1 < rs2)_1         -

----------------Focused Condition View-------------------
Line       245 Item    1  (rs1 == rs2)
Condition totals: 1 of 1 input term covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  ----------------------  --------------
  (rs1 == rs2)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (rs1 == rs2)_0        -
  Row   2:          1  (rs1 == rs2)_1        -

----------------Focused Condition View-------------------
Line       246 Item    1  (rs1 != rs2)
Condition totals: 0 of 1 input term covered = 0.00%

    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  ----------------------  --------------
  (rs1 != rs2)         N  '_0' not hit            Hit '_0'
```

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(rs1 != rs2)_0	-
Row 2:	1	(rs1 != rs2)_1	-

----------Focused Condition View----------
Line 248 Item 1 (rs1 >= rs2)
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(rs1 >= rs2)	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(rs1 >= rs2)_0	-
Row 2:	1	(rs1 >= rs2)_1	-

----------Focused Condition View----------
Line 249 Item 1 (rs1 >= rs2)
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(rs1 >= rs2)	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(rs1 >= rs2)_0	-
Row 2:	1	(rs1 >= rs2)_1	-

----------Focused Condition View----------
Line 160 Item 1 ((rst_n === 1'b0) && (tx.o_exception !== 0) && (tx.o_ce !== 1'b0) && (tx.o_stall_from_alu !== 1'b0))
Condition totals: 0 of 4 input terms covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(rst_n === 1'b0)	N	No hits	Hit '_0' and '_1'
(tx.o_exception !== 0)	N	No hits	Hit '_0' and '_1'

```
             (tx.o_ce !== 1'b0)        N  No hits                  Hit '_0' and '_1'
  (tx.o_stall_from_alu !== 1'b0)       N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target                        Non-masking condition(s)
 ---------  ---------  --------------------              ------------------------
  Row   1:    ***0***  (rst_n === 1'b0)_0                -
  Row   2:    ***0***  (rst_n === 1'b0)_1                     ((tx.o_exception !== 0) &&
((tx.o_ce !== 1'b0) && (tx.o_stall_from_alu !== 1'b0)))
  Row   3:    ***0***  (tx.o_exception !== 0)_0          (rst_n === 1'b0)
  Row   4:    ***0***  (tx.o_exception !== 0)_1           ((rst_n === 1'b0) && ((tx.o_ce
!== 1'b0) && (tx.o_stall_from_alu !== 1'b0)))
  Row   5:    ***0***  (tx.o_ce !== 1'b0)_0                   ((rst_n === 1'b0) &&
(tx.o_exception !== 0))
  Row   6:    ***0***  (tx.o_ce !== 1'b0)_1                   ((rst_n === 1'b0) &&
(tx.o_exception !== 0) && (tx.o_stall_from_alu !== 1'b0))
  Row   7:    ***0***  (tx.o_stall_from_alu !== 1'b0)_0   ((rst_n === 1'b0) &&
(tx.o_exception !== 0) && (tx.o_ce !== 1'b0))
  Row   8:    ***0***  (tx.o_stall_from_alu !== 1'b0)_1   ((rst_n === 1'b0) &&
(tx.o_exception !== 0) && (tx.o_ce !== 1'b0))

----------------Focused Condition View-------------------
Line       165 Item    1  (opcode[5] || opcode[8])
Condition totals: 0 of 2 input terms covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
  opcode[5]         N  No hits                  Hit '_0' and '_1'
  opcode[8]         N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  opcode[5]_0           ~opcode[8]
  Row   2:    ***0***  opcode[5]_1           -
  Row   3:    ***0***  opcode[8]_0           ~opcode[5]
  Row   4:    ***0***  opcode[8]_1           ~opcode[5]

----------------Focused Condition View-------------------
Line       166 Item    1  (opcode[0] || opcode[4])
Condition totals: 0 of 2 input terms covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
  opcode[0]         N  No hits                  Hit '_0' and '_1'
  opcode[4]         N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
```

```
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  opcode[0]_0           ~opcode[4]
  Row   2:    ***0***  opcode[0]_1           -
  Row   3:    ***0***  opcode[4]_0           ~opcode[0]
  Row   4:    ***0***  opcode[4]_1           ~opcode[0]

----------------Focused Condition View-------------------
Line       172 Item    1  (opcode[0] || opcode[1])
Condition totals: 0 of 2 input terms covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
   opcode[0]         N  No hits                 Hit '_0' and '_1'
   opcode[1]         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  opcode[0]_0           ~opcode[1]
  Row   2:    ***0***  opcode[0]_1           -
  Row   3:    ***0***  opcode[1]_0           ~opcode[0]
  Row   4:    ***0***  opcode[1]_1           ~opcode[0]

----------------Focused Condition View-------------------
Line       177 Item    1  (opcode[4] && out && (((pc + imm) !== tx.o_next_pc) || (ce !==
tx.o_change_pc) || (ce !== tx.o_flush)))
Condition totals: 0 of 1 input term covered = 0.00%


      Input Term   Covered  Reason for no coverage   Hint

     -----------  --------  ----------------------  --------------
  (opcode[4] && out && (((pc + imm) !== tx.o_next_pc) || (ce !== tx.o_change_pc) || (ce
!== tx.o_flush)))         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target
                                          Non-masking condition(s)
 ---------  ---------  --------------------
                                          -------------------------
  Row   1:    ***0***  (opcode[4] && out && (((pc + imm) !== tx.o_next_pc) || (ce !==
tx.o_change_pc) || (ce !== tx.o_flush)))_0  -
  Row   2:    ***0***  (opcode[4] && out && (((pc + imm) !== tx.o_next_pc) || (ce !==
tx.o_change_pc) || (ce !== tx.o_flush)))_1  -

----------------Focused Condition View-------------------
Line       187 Item    1  (opcode[5] || opcode[6])
Condition totals: 0 of 2 input terms covered = 0.00%
```

```
  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
   opcode[5]         N  No hits                 Hit '_0' and '_1'
   opcode[6]         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  opcode[5]_0           ~opcode[6]
  Row   2:    ***0***  opcode[5]_1           -
  Row   3:    ***0***  opcode[6]_0           ~opcode[5]
  Row   4:    ***0***  opcode[6]_1           ~opcode[5]

----------------Focused Condition View-------------------
Line       188 Item    1  (opcode[6] === 1'b1)
Condition totals: 0 of 1 input term covered = 0.00%

            Input Term   Covered  Reason for no coverage   Hint
           -----------  --------  ----------------------  --------------
  (opcode[6] === 1'b1)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ---------  ---------  --------------------    -------------------------
  Row   1:    ***0***  (opcode[6] === 1'b1)_0  -
  Row   2:    ***0***  (opcode[6] === 1'b1)_1  -

----------------Focused Condition View-------------------
Line        191 Item    1  ((sum !== tx.o_next_pc) || (ce !== tx.o_change_pc) || (ce !==
tx.o_flush))
Condition totals: 0 of 3 input terms covered = 0.00%

               Input Term   Covered  Reason for no coverage   Hint
              -----------  --------  ----------------------  --------------
   (sum !== tx.o_next_pc)         N  No hits                 Hit '_0' and '_1'
  (ce !== tx.o_change_pc)         N  No hits                 Hit '_0' and '_1'
      (ce !== tx.o_flush)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target                 Non-masking condition(s)
 ---------  ---------  --------------------       -------------------------
   Row   1:    ***0***  (sum !== tx.o_next_pc)_0   ~((ce !== tx.o_change_pc) || (ce !==
tx.o_flush))
  Row   2:    ***0***  (sum !== tx.o_next_pc)_1   -
   Row   3:    ***0***  (ce !== tx.o_change_pc)_0  (~(sum !== tx.o_next_pc) && ~(ce !==
tx.o_flush))
  Row   4:    ***0***  (ce !== tx.o_change_pc)_1  ~(sum !== tx.o_next_pc)
   Row   5:    ***0***  (ce !== tx.o_flush)_0      (~(sum !== tx.o_next_pc) && ~(ce !==
```

```
tx.o_change_pc))
  Row    6:     ***0***  (ce !== tx.o_flush)_1       (~(sum !== tx.o_next_pc) && ~(ce !==
tx.o_change_pc))

----------------Focused Condition View-------------------
Line       211 Item    1  (((opcode[4] || opcode[3]) || (opcode[9] && (funct3 == 0))) ||
opcode[10])
Condition totals: 0 of 5 input terms covered = 0.00%

     Input Term   Covered  Reason for no coverage   Hint
    -----------  --------  ----------------------  --------------
      opcode[4]         N  No hits                 Hit '_0' and '_1'
      opcode[3]         N  No hits                 Hit '_0' and '_1'
      opcode[9]         N  No hits                 Hit '_0' and '_1'
  (funct3 == 0)         N  No hits                 Hit '_0' and '_1'
     opcode[10]         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row    1:     ***0***  opcode[4]_0           (~opcode[10] && ~(opcode[9] && (funct3 ==
0)) && ~opcode[3])
  Row    2:     ***0***  opcode[4]_1           -
  Row    3:     ***0***  opcode[3]_0           (~opcode[10] && ~(opcode[9] && (funct3 ==
0)) && ~opcode[4])
  Row    4:     ***0***  opcode[3]_1           ~opcode[4]
  Row    5:     ***0***  opcode[9]_0           (~opcode[10] && ~(opcode[4] || opcode[3]))
  Row    6:     ***0***  opcode[9]_1            (~(opcode[4] || opcode[3]) && (funct3 ==
0))
  Row    7:     ***0***  (funct3 == 0)_0        (~opcode[10] && ~(opcode[4] || opcode[3])
&& opcode[9])
  Row    8:     ***0***  (funct3 == 0)_1       (~(opcode[4] || opcode[3]) && opcode[9])
  Row    9:     ***0***  opcode[10]_0          ~((opcode[4] || opcode[3]) || (opcode[9] &&
(funct3 == 0)))
 Row   10:     ***0***  opcode[10]_1          ~((opcode[4] || opcode[3]) || (opcode[9] &&
(funct3 == 0)))

----------------Focused Condition View-------------------
Line       218 Item    1  (opcode[2] || (opcode[9] && (funct3 != 0)))
Condition totals: 0 of 3 input terms covered = 0.00%

     Input Term   Covered  Reason for no coverage   Hint
    -----------  --------  ----------------------  --------------
      opcode[2]         N  No hits                 Hit '_0' and '_1'
      opcode[9]         N  No hits                 Hit '_0' and '_1'
  (funct3 != 0)         N  No hits                 Hit '_0' and '_1'
```

```
     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  opcode[2]_0           ~(opcode[9] && (funct3 != 0))
  Row   2:    ***0***  opcode[2]_1           -
  Row   3:    ***0***  opcode[9]_0           ~opcode[2]
  Row   4:    ***0***  opcode[9]_1           (~opcode[2] && (funct3 != 0))
  Row   5:    ***0***  (funct3 != 0)_0       (~opcode[2] && opcode[9])
  Row   6:    ***0***  (funct3 != 0)_1       (~opcode[2] && opcode[9])

----------------Focused Condition View-------------------
Line       221 Item    1  ((tx.o_stall !== (stall || force_stall)) && ~flush)
Condition totals: 0 of 2 input terms covered = 0.00%

                              Input Term   Covered  Reason for no coverage   Hint
                                        -----------   --------   -----------------------
--------------
  (tx.o_stall !== (stall || force_stall))          N  No hits                    Hit '_0'
and '_1'
                                       flush          N  No hits                    Hit '_0'
and '_1'

      Rows:         Hits   FEC Target                                          Non-masking
condition(s)
  ---------    ---------    --------------------
-------------------------
  Row   1:    ***0***  (tx.o_stall !== (stall || force_stall))_0  -

  Row   2:    ***0***  (tx.o_stall !== (stall || force_stall))_1  ~flush

  Row   3:    ***0***  flush_0                                    (tx.o_stall !== (stall
|| force_stall))
  Row   4:    ***0***  flush_1                                    (tx.o_stall !== (stall
|| force_stall))

----------------Focused Condition View-------------------
Line       226 Item    1  (~(tx.o_stall || stall) && (ce === 1'b1))
Condition totals: 0 of 3 input terms covered = 0.00%

     Input Term   Covered  Reason for no coverage   Hint
    -----------  --------  -----------------------  --------------
     tx.o_stall         N  No hits                  Hit '_0' and '_1'
          stall         N  No hits                  Hit '_0' and '_1'
  (ce === 1'b1)         N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
```

```
  Row   1:    ***0***  tx.o_stall_0          ((ce === 1'b1) && ~stall)
  Row   2:    ***0***  tx.o_stall_1          -
  Row   3:    ***0***  stall_0              ((ce === 1'b1) && ~tx.o_stall)
  Row   4:    ***0***  stall_1              ~tx.o_stall
  Row   5:    ***0***  (ce === 1'b1)_0      ~(tx.o_stall || stall)
  Row   6:    ***0***  (ce === 1'b1)_1      ~(tx.o_stall || stall)

----------------Focused Condition View-------------------
Line       227 Item    1  ((opcode !== tx.o_opcode) || (exception !== tx.o_exception) ||
(out !== tx.o_y) || (rs1_addr !== tx.o_rs1_addr) || (rs1 !== tx.o_rs1) || (rs2 !==
tx.o_rs2) || (rd_addr !== tx.o_rd_addr) || (imm !== tx.o_imm) || (funct3 !==
tx.o_funct3) || (rd_d !== tx.o_rd) || (rd_valid !== tx.o_rd_valid) || (wr_rd_d !==
tx.o_wr_rd) || ((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc))
Condition totals: 0 of 14 input terms covered = 0.00%

                                          Input Term   Covered  Reason for no coverage
Hint
                                         -----------  --------  ----------------------
--------------
                           (opcode !== tx.o_opcode)         N  No hits
Hit '_0' and '_1'
                      (exception !== tx.o_exception)         N  No hits
Hit '_0' and '_1'
                                (out !== tx.o_y)         N  No hits
Hit '_0' and '_1'
                        (rs1_addr !== tx.o_rs1_addr)         N  No hits
Hit '_0' and '_1'
                                (rs1 !== tx.o_rs1)         N  No hits
Hit '_0' and '_1'
                                (rs2 !== tx.o_rs2)         N  No hits
Hit '_0' and '_1'
                          (rd_addr !== tx.o_rd_addr)         N  No hits
Hit '_0' and '_1'
                                (imm !== tx.o_imm)         N  No hits
Hit '_0' and '_1'
                           (funct3 !== tx.o_funct3)         N  No hits
Hit '_0' and '_1'
                                (rd_d !== tx.o_rd)         N  No hits
Hit '_0' and '_1'
                       (rd_valid !== tx.o_rd_valid)         N  No hits
Hit '_0' and '_1'
                           (wr_rd_d !== tx.o_wr_rd)         N  No hits
Hit '_0' and '_1'
  ((opcode[3] || opcode[2]) == tx.o_stall_from_alu)         N  No hits
Hit '_0' and '_1'
                                  (pc !== tx.o_pc)         N  No hits
```

Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(opcode !== tx.o_opcode)_0	~((exception !== tx.o_exception) || ((out !== tx.o_y) || ((rs1_addr !== tx.o_rs1_addr) || ((rs1 !== tx.o_rs1) || ((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !== tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc))))))))))))
Row 2:	***0***	(opcode !== tx.o_opcode)_1	-
Row 3:	***0***	(exception !== tx.o_exception)_0	(~(opcode !== tx.o_opcode) && ~((out !== tx.o_y) || ((rs1_addr !== tx.o_rs1_addr) || ((rs1 !== tx.o_rs1) || ((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !== tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc))))))))))))
Row 4:	***0***	(exception !== tx.o_exception)_1	~(opcode !== tx.o_opcode)
Row 5:	***0***	(out !== tx.o_y)_0	(~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~((rs1_addr !== tx.o_rs1_addr) || ((rs1 !== tx.o_rs1) || ((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !== tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc))))))))))))
Row 6:	***0***	(out !== tx.o_y)_1	(~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception))
Row 7:	***0***	(rs1_addr !== tx.o_rs1_addr)_0	(~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~((rs1 !== tx.o_rs1) || ((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !== tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc))))))))))))
Row 8:	***0***	(rs1_addr !== tx.o_rs1_addr)_1	(~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y))
Row 9:	***0***	(rs1 !== tx.o_rs1)_0	(~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !== tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc)))))))))))
Row 10:	***0***	(rs1 !== tx.o_rs1)_1	(~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr

!== tx.o_rs1_addr))

Row 11: ***0*** (rs2 !== tx.o_rs2)_0 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~((rd_addr !== tx.o_rd_addr) || ((imm !== tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc)))))))))

Row 12: ***0*** (rs2 !== tx.o_rs2)_1 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1))

Row 13: ***0*** (rd_addr !== tx.o_rd_addr)_0 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~((imm !== tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc)))))))

Row 14: ***0*** (rd_addr !== tx.o_rd_addr)_1 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2))

Row 15: ***0*** (imm !== tx.o_imm)_0 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc)))))))

Row 16: ***0*** (imm !== tx.o_imm)_1 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr))

Row 17: ***0*** (funct3 !== tx.o_funct3)_0 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc))))))

Row 18: ***0*** (funct3 !== tx.o_funct3)_1 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm))

Row 19: ***0*** (rd_d !== tx.o_rd)_0 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc)))))

Row 20: ***0*** (rd_d !== tx.o_rd)_1 (~(opcode

!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3))

Row 21: ***0*** (rd_valid !== tx.o_rd_valid)_0 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd) && ~((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc))))

Row 22: ***0*** (rd_valid !== tx.o_rd_valid)_1 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd))

Row 23: ***0*** (wr_rd_d !== tx.o_wr_rd)_0 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd) && ~(rd_valid !== tx.o_rd_valid) && ~(((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc)))

Row 24: ***0*** (wr_rd_d !== tx.o_wr_rd)_1 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd) && ~(rd_valid !== tx.o_rd_valid))

Row 25: ***0*** ((opcode[3] || opcode[2]) == tx.o_stall_from_alu)_0 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd) && ~(rd_valid !== tx.o_rd_valid) && ~(wr_rd_d !== tx.o_wr_rd) && ~(pc !== tx.o_pc))

Row 26: ***0*** ((opcode[3] || opcode[2]) == tx.o_stall_from_alu)_1 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd) && ~(rd_valid !== tx.o_rd_valid) && ~(wr_rd_d !== tx.o_wr_rd))

Row 27: ***0*** (pc !== tx.o_pc)_0 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd) && ~(rd_valid !== tx.o_rd_valid) && ~(wr_rd_d !== tx.o_wr_rd) && ~((opcode[3] || opcode[2]) == tx.o_stall_from_alu))

Row 28: ***0*** (pc !== tx.o_pc)_1 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd) && ~(rd_valid !== tx.o_rd_valid) && ~(wr_rd_d !== tx.o_wr_rd) && ~((opcode[3] ||

```
opcode[2]) == tx.o_stall_from_alu))

----------------Focused Condition View-------------------
Line       247 Item    1  (flush && ~(tx.o_stall || stall) && (tx.o_ce !== 1'b0))
Condition totals: 0 of 4 input terms covered = 0.00%

          Input Term   Covered  Reason for no coverage   Hint
         -----------  --------  ----------------------  --------------
               flush         N  No hits                 Hit '_0' and '_1'
          tx.o_stall         N  No hits                 Hit '_0' and '_1'
               stall         N  No hits                 Hit '_0' and '_1'
  (tx.o_ce !== 1'b0)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  flush_0               -
  Row   2:    ***0***  flush_1               (~(tx.o_stall || stall) && (tx.o_ce !==
1'b0))
  Row   3:    ***0***  tx.o_stall_0          (flush && (tx.o_ce !== 1'b0) && ~stall)
  Row   4:    ***0***  tx.o_stall_1          flush
  Row   5:    ***0***  stall_0               (flush && (tx.o_ce !== 1'b0) &&
~tx.o_stall)
  Row   6:    ***0***  stall_1               (flush && ~tx.o_stall)
  Row   7:    ***0***  (tx.o_ce !== 1'b0)_0  (flush && ~(tx.o_stall || stall))
  Row   8:    ***0***  (tx.o_ce !== 1'b0)_1  (flush && ~(tx.o_stall || stall))

----------------Focused Condition View-------------------
Line       249 Item    1  (~(tx.o_stall || stall) && (tx.o_ce !== ce))
Condition totals: 0 of 3 input terms covered = 0.00%

        Input Term   Covered  Reason for no coverage   Hint
       -----------  --------  ----------------------  --------------
        tx.o_stall         N  No hits                 Hit '_0' and '_1'
             stall         N  No hits                 Hit '_0' and '_1'
  (tx.o_ce !== ce)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  tx.o_stall_0          ((tx.o_ce !== ce) && ~stall)
  Row   2:    ***0***  tx.o_stall_1          -
  Row   3:    ***0***  stall_0               ((tx.o_ce !== ce) && ~tx.o_stall)
  Row   4:    ***0***  stall_1               ~tx.o_stall
  Row   5:    ***0***  (tx.o_ce !== ce)_0    ~(tx.o_stall || stall)
  Row   6:    ***0***  (tx.o_ce !== ce)_1    ~(tx.o_stall || stall)

----------------Focused Condition View-------------------
```

```
Line       251 Item    1  (tx.o_stall && (tx.o_ce !== 1'b0))
Condition totals: 0 of 2 input terms covered = 0.00%

          Input Term   Covered  Reason for no coverage   Hint
         -----------  --------  ----------------------  --------------
          tx.o_stall         N  No hits                  Hit '_0' and '_1'
  (tx.o_ce !== 1'b0)         N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  tx.o_stall_0          -
  Row   2:    ***0***  tx.o_stall_1          (tx.o_ce !== 1'b0)
  Row   3:    ***0***  (tx.o_ce !== 1'b0)_0  tx.o_stall
  Row   4:    ***0***  (tx.o_ce !== 1'b0)_1  tx.o_stall

----------------Focused Condition View-------------------
Line       310 Item    1  (a < b)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
     (a < b)         N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (a < b)_0             -
  Row   2:    ***0***  (a < b)_1             -

----------------Focused Condition View-------------------
Line       312 Item    1  (a < b)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
     (a < b)         N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (a < b)_0             -
  Row   2:    ***0***  (a < b)_1             -

----------------Focused Condition View-------------------
Line       319 Item    1  (a == b)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
```

```
 -----------  --------  ----------------------  --------------
    (a == b)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (a == b)_0            -
  Row   2:    ***0***  (a == b)_1            -

----------------Focused Condition View-------------------
Line       320 Item    1  (a != b)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
    (a != b)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (a != b)_0            -
  Row   2:    ***0***  (a != b)_1            -

----------------Focused Condition View-------------------
Line       321 Item    1  (a >= b)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
    (a >= b)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (a >= b)_0            -
  Row   2:    ***0***  (a >= b)_1            -

----------------Focused Condition View-------------------
Line       322 Item    1  (a >= b)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
    (a >= b)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (a >= b)_0            -
  Row   2:    ***0***  (a >= b)_1            -
```

```
Covergroup Coverage:
    Covergroups                     1        na        na    34.84%
        Coverpoints/Crosses        20        na        na        na
            Covergroup Bins      5315        77      5238     1.44%
--------------------------------------------------------------------------------
-----------------
Covergroup                                          Metric       Goal       Bins
Status


--------------------------------------------------------------------------------
-----------------
 TYPE work.coverage_sv_unit::coverage/alu_cg          34.84%        100          -
Uncovered
    covered/total bins:                                 77       5315          -

    missing/total bins:                               5238       5315          -

    % Hit:                                           1.44%        100          -

    type_option.weight=1
    type_option.goal=100
    type_option.comment=
    type_option.strobe=0
    type_option.merge_instances=auto(1)
    Coverpoint #coverpoint__0#                       45.45%        100          -
Uncovered
        covered/total bins:                             5         11          -

        missing/total bins:                             6         11          -

        % Hit:                                      45.45%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin opcode_types[0]                            78          1          -
Covered
        bin opcode_types[1]                           103          1          -
Covered
        bin opcode_types[2]                            82          1          -
Covered
        bin opcode_types[3]                             0          1          -
```

```
ZERO
        bin opcode_types[4]                                90          1          -
Covered
        bin opcode_types[5]                                 0          1          -
ZERO
        bin opcode_types[6]                                 0          1          -
ZERO
        bin opcode_types[7]                                 0          1          -
ZERO
        bin opcode_types[8]                                79          1          -
Covered
        bin opcode_types[9]                                 0          1          -
ZERO
        bin opcode_types[10]                                0          1          -
ZERO
    Coverpoint #coverpoint__1#                         28.57%        100          -
Uncovered
        covered/total bins:                                 4         14          -

        missing/total bins:                                10         14          -

        % Hit:                                         28.57%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin alu_ops[0]                                      0          1          -
ZERO
        bin alu_ops[1]                                     60          1          -
Covered
        bin alu_ops[2]                                     71          1          -
Covered
        bin alu_ops[3]                                      0          1          -
ZERO
        bin alu_ops[4]                                     64          1          -
Covered
        bin alu_ops[5]                                      0          1          -
ZERO
        bin alu_ops[6]                                      0          1          -
ZERO
        bin alu_ops[7]                                      0          1          -
ZERO
        bin alu_ops[8]                                     58          1          -
Covered
        bin alu_ops[9]                                      0          1          -
ZERO
```

```
        bin alu_ops[10]                                  0          1          -
ZERO
        bin alu_ops[11]                                  0          1          -
ZERO
        bin alu_ops[12]                                  0          1          -
ZERO
        bin alu_ops[13]                                  0          1          -
ZERO
    Coverpoint #coverpoint__2#                      100.00%        100          -
Covered
        covered/total bins:                              2          2          -

        missing/total bins:                              0          2          -

        % Hit:                                      100.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                    714          1          -
Covered
        bin auto[1]                                    200          1          -
Covered
    Coverpoint #coverpoint__3#                      100.00%        100          -
Covered
        covered/total bins:                              1          1          -

        missing/total bins:                              0          1          -

        % Hit:                                      100.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin pc_values                                  914          1          -
Covered
    Coverpoint #coverpoint__4#                        0.00%        100          -
ZERO
        covered/total bins:                              0          2          -

        missing/total bins:                              2          2          -

        % Hit:                                        0.00%        100          -

        type_option.weight=1
        type_option.goal=100
```

```
        type_option.comment=
        bin auto[0]                                    0          1          -
ZERO
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__5#                      0.00%       100          -
ZERO
        covered/total bins:                            0          2          -

        missing/total bins:                            2          2          -

        % Hit:                                      0.00%       100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                    0          1          -
ZERO
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__6#                      0.00%       100          -
ZERO
        covered/total bins:                            0          1          -

        missing/total bins:                            1          1          -

        % Hit:                                      0.00%       100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin rd_addr                                    0          1          -
ZERO
    Coverpoint #coverpoint__7#                     50.00%       100          -
Uncovered
        covered/total bins:                            1          2          -

        missing/total bins:                            1          2          -

        % Hit:                                     50.00%       100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                    0          1          -
ZERO
```

```
        bin auto[1]                                  914          1          -
Covered
    Coverpoint #coverpoint__8#                    50.00%        100          -
Uncovered
        covered/total bins:                          1          2          -

        missing/total bins:                          1          2          -

        % Hit:                                    50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                  914          1          -
Covered
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__9#                    50.00%        100          -
Uncovered
        covered/total bins:                          1          2          -

        missing/total bins:                          1          2          -

        % Hit:                                    50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                  914          1          -
Covered
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__10#                   50.00%        100          -
Uncovered
        covered/total bins:                          1          2          -

        missing/total bins:                          1          2          -

        % Hit:                                    50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                  914          1          -
Covered
        bin auto[1]                                    0          1          -
```

```
ZERO
    Coverpoint #coverpoint__11#                    50.00%        100          -
Uncovered
        covered/total bins:                            1          2          -

        missing/total bins:                            1          2          -

        % Hit:                                     50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                  914          1          -
Covered
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__12#                    50.00%        100          -
Uncovered
        covered/total bins:                            1          2          -

        missing/total bins:                            1          2          -

        % Hit:                                     50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                  914          1          -
Covered
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__13#                   100.00%        100          -
Covered
        covered/total bins:                            2          2          -

        missing/total bins:                            0          2          -

        % Hit:                                    100.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                  714          1          -
Covered
        bin auto[1]                                  200          1          -
Covered
```

```
    Coverpoint #coverpoint__14#                          0.00%        100          -
ZERO
        covered/total bins:                                 0          4          -

        missing/total bins:                                 4          4          -

        % Hit:                                          0.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin exceptions[0]                                   0          1          -
ZERO
        bin exceptions[1]                                   0          1          -
ZERO
        bin exceptions[2]                                   0          1          -
ZERO
        bin exceptions[3]                                   0          1          -
ZERO
    Coverpoint #vif.i_opcode__15#                        10.93%        100          -
Uncovered
        covered/total bins:                                 7         64          -

        missing/total bins:                                57         64          -

        % Hit:                                          10.93%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0:31]                                    527          1          -
Covered
        bin auto[32:63]                                    81          1          -
Covered
        bin auto[64:95]                                    73          1          -
Covered
        bin auto[96:127]                                    0          1          -
ZERO
        bin auto[128:159]                                  70          1          -
Covered
        bin auto[160:191]                                   0          1          -
ZERO
        bin auto[192:223]                                   0          1          -
ZERO
        bin auto[224:255]                                   0          1          -
ZERO
```

```
        bin auto[256:287]                                67          1          -
Covered
        bin auto[288:319]                                 0          1          -
ZERO
        bin auto[320:351]                                 0          1          -
ZERO
        bin auto[352:383]                                 0          1          -
ZERO
        bin auto[384:415]                                 0          1          -
ZERO
        bin auto[416:447]                                 0          1          -
ZERO
        bin auto[448:479]                                 0          1          -
ZERO
        bin auto[480:511]                                 0          1          -
ZERO
        bin auto[512:543]                                95          1          -
Covered
        bin auto[544:575]                                 0          1          -
ZERO
        bin auto[576:607]                                 0          1          -
ZERO
        bin auto[608:639]                                 0          1          -
ZERO
        bin auto[640:671]                                 0          1          -
ZERO
        bin auto[672:703]                                 0          1          -
ZERO
        bin auto[704:735]                                 0          1          -
ZERO
        bin auto[736:767]                                 0          1          -
ZERO
        bin auto[768:799]                                 0          1          -
ZERO
        bin auto[800:831]                                 0          1          -
ZERO
        bin auto[832:863]                                 0          1          -
ZERO
        bin auto[864:895]                                 0          1          -
ZERO
        bin auto[896:927]                                 0          1          -
ZERO
        bin auto[928:959]                                 0          1          -
ZERO
        bin auto[960:991]                                 0          1          -
ZERO
```

```
        bin auto[992:1023]                                  0          1          -
ZERO
        bin auto[1024:1055]                                 1          1          -
Covered
        bin auto[1056:1087]                                 0          1          -
ZERO
        bin auto[1088:1119]                                 0          1          -
ZERO
        bin auto[1120:1151]                                 0          1          -
ZERO
        bin auto[1152:1183]                                 0          1          -
ZERO
        bin auto[1184:1215]                                 0          1          -
ZERO
        bin auto[1216:1247]                                 0          1          -
ZERO
        bin auto[1248:1279]                                 0          1          -
ZERO
        bin auto[1280:1311]                                 0          1          -
ZERO
        bin auto[1312:1343]                                 0          1          -
ZERO
        bin auto[1344:1375]                                 0          1          -
ZERO
        bin auto[1376:1407]                                 0          1          -
ZERO
        bin auto[1408:1439]                                 0          1          -
ZERO
        bin auto[1440:1471]                                 0          1          -
ZERO
        bin auto[1472:1503]                                 0          1          -
ZERO
        bin auto[1504:1535]                                 0          1          -
ZERO
        bin auto[1536:1567]                                 0          1          -
ZERO
        bin auto[1568:1599]                                 0          1          -
ZERO
        bin auto[1600:1631]                                 0          1          -
ZERO
        bin auto[1632:1663]                                 0          1          -
ZERO
        bin auto[1664:1695]                                 0          1          -
ZERO
        bin auto[1696:1727]                                 0          1          -
ZERO
```

```
        bin auto[1728:1759]                                  0          1          -
ZERO
        bin auto[1760:1791]                                  0          1          -
ZERO
        bin auto[1792:1823]                                  0          1          -
ZERO
        bin auto[1824:1855]                                  0          1          -
ZERO
        bin auto[1856:1887]                                  0          1          -
ZERO
        bin auto[1888:1919]                                  0          1          -
ZERO
        bin auto[1920:1951]                                  0          1          -
ZERO
        bin auto[1952:1983]                                  0          1          -
ZERO
        bin auto[1984:2015]                                  0          1          -
ZERO
        bin auto[2016:2047]                                  0          1          -
ZERO
    Coverpoint #vif.i_exception__16#                      0.00%        100          -
ZERO
        covered/total bins:                                  0         16          -

        missing/total bins:                                 16         16          -

        % Hit:                                            0.00%       100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                          0          1          -
ZERO
        bin auto[1]                                          0          1          -
ZERO
        bin auto[2]                                          0          1          -
ZERO
        bin auto[3]                                          0          1          -
ZERO
        bin auto[4]                                          0          1          -
ZERO
        bin auto[5]                                          0          1          -
ZERO
        bin auto[6]                                          0          1          -
ZERO
        bin auto[7]                                          0          1          -
```

```
ZERO
        bin auto[8]                                    0          1          -
ZERO
        bin auto[9]                                    0          1          -
ZERO
        bin auto[10]                                   0          1          -
ZERO
        bin auto[11]                                   0          1          -
ZERO
        bin auto[12]                                   0          1          -
ZERO
        bin auto[13]                                   0          1          -
ZERO
        bin auto[14]                                   0          1          -
ZERO
        bin auto[15]                                   0          1          -
ZERO
    Coverpoint #vif.i_alu__17#                    10.93%        100          -
Uncovered
        covered/total bins:                            7         64          -

        missing/total bins:                           57         64          -

        % Hit:                                    10.93%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0:255]                              520          1          -
Covered
        bin auto[256:511]                             77          1          -
Covered
        bin auto[512:767]                             73          1          -
Covered
        bin auto[768:1023]                             0          1          -
ZERO
        bin auto[1024:1279]                           70          1          -
Covered
        bin auto[1280:1535]                            0          1          -
ZERO
        bin auto[1536:1791]                            0          1          -
ZERO
        bin auto[1792:2047]                            0          1          -
ZERO
        bin auto[2048:2303]                           62          1          -
Covered
```

```
        bin auto[2304:2559]                                 0          1          -
ZERO
        bin auto[2560:2815]                                 0          1          -
ZERO
        bin auto[2816:3071]                                 0          1          -
ZERO
        bin auto[3072:3327]                                 0          1          -
ZERO
        bin auto[3328:3583]                                 0          1          -
ZERO
        bin auto[3584:3839]                                 0          1          -
ZERO
        bin auto[3840:4095]                                 0          1          -
ZERO
        bin auto[4096:4351]                                56          1          -
Covered
        bin auto[4352:4607]                                 0          1          -
ZERO
        bin auto[4608:4863]                                 0          1          -
ZERO
        bin auto[4864:5119]                                 0          1          -
ZERO
        bin auto[5120:5375]                                 0          1          -
ZERO
        bin auto[5376:5631]                                 0          1          -
ZERO
        bin auto[5632:5887]                                 0          1          -
ZERO
        bin auto[5888:6143]                                 0          1          -
ZERO
        bin auto[6144:6399]                                 0          1          -
ZERO
        bin auto[6400:6655]                                 0          1          -
ZERO
        bin auto[6656:6911]                                 0          1          -
ZERO
        bin auto[6912:7167]                                 0          1          -
ZERO
        bin auto[7168:7423]                                 0          1          -
ZERO
        bin auto[7424:7679]                                 0          1          -
ZERO
        bin auto[7680:7935]                                 0          1          -
ZERO
        bin auto[7936:8191]                                 0          1          -
ZERO
```

```
        bin auto[8192:8447]                                  56          1          -
Covered
        bin auto[8448:8703]                                   0          1          -
ZERO
        bin auto[8704:8959]                                   0          1          -
ZERO
        bin auto[8960:9215]                                   0          1          -
ZERO
        bin auto[9216:9471]                                   0          1          -
ZERO
        bin auto[9472:9727]                                   0          1          -
ZERO
        bin auto[9728:9983]                                   0          1          -
ZERO
        bin auto[9984:10239]                                  0          1          -
ZERO
        bin auto[10240:10495]                                 0          1          -
ZERO
        bin auto[10496:10751]                                 0          1          -
ZERO
        bin auto[10752:11007]                                 0          1          -
ZERO
        bin auto[11008:11263]                                 0          1          -
ZERO
        bin auto[11264:11519]                                 0          1          -
ZERO
        bin auto[11520:11775]                                 0          1          -
ZERO
        bin auto[11776:12031]                                 0          1          -
ZERO
        bin auto[12032:12287]                                 0          1          -
ZERO
        bin auto[12288:12543]                                 0          1          -
ZERO
        bin auto[12544:12799]                                 0          1          -
ZERO
        bin auto[12800:13055]                                 0          1          -
ZERO
        bin auto[13056:13311]                                 0          1          -
ZERO
        bin auto[13312:13567]                                 0          1          -
ZERO
        bin auto[13568:13823]                                 0          1          -
ZERO
        bin auto[13824:14079]                                 0          1          -
ZERO
```

```
        bin auto[14080:14335]                                0          1          -
ZERO
        bin auto[14336:14591]                                0          1          -
ZERO
        bin auto[14592:14847]                                0          1          -
ZERO
        bin auto[14848:15103]                                0          1          -
ZERO
        bin auto[15104:15359]                                0          1          -
ZERO
        bin auto[15360:15615]                                0          1          -
ZERO
        bin auto[15616:15871]                                0          1          -
ZERO
        bin auto[15872:16127]                                0          1          -
ZERO
        bin auto[16128:16383]                                0          1          -
ZERO
    Cross #cross__0#                                      1.04%        100          -
Uncovered
        covered/total bins:                                 43       4096          -

        missing/total bins:                               4053       4096          -

        % Hit:                                            1.04%       100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        Auto, Default and User Defined Bins:
            bin <auto[512:543],auto[8192:8447]>              5          1          -
Covered
            bin <auto[256:287],auto[8192:8447]>              3          1          -
Covered
            bin <auto[128:159],auto[8192:8447]>              3          1          -
Covered
            bin <auto[64:95],auto[8192:8447]>                7          1          -
Covered
            bin <auto[32:63],auto[8192:8447]>                7          1          -
Covered
            bin <auto[0:31],auto[8192:8447]>                31          1          -
Covered
            bin <auto[512:543],auto[4096:4351]>              3          1          -
Covered
            bin <auto[256:287],auto[4096:4351]>              2          1          -
Covered
```

```
            bin <auto[128:159],auto[4096:4351]>              3          1          -
Covered
            bin <auto[64:95],auto[4096:4351]>                2          1          -
Covered
            bin <auto[32:63],auto[4096:4351]>                7          1          -
Covered
            bin <auto[0:31],auto[4096:4351]>                39          1          -
Covered
            bin <auto[512:543],auto[2048:2303]>              3          1          -
Covered
            bin <auto[256:287],auto[2048:2303]>              4          1          -
Covered
            bin <auto[128:159],auto[2048:2303]>             11          1          -
Covered
            bin <auto[64:95],auto[2048:2303]>                3          1          -
Covered
            bin <auto[32:63],auto[2048:2303]>                3          1          -
Covered
            bin <auto[0:31],auto[2048:2303]>                38          1          -
Covered
            bin <auto[512:543],auto[1024:1279]>              4          1          -
Covered
            bin <auto[256:287],auto[1024:1279]>              6          1          -
Covered
            bin <auto[128:159],auto[1024:1279]>              6          1          -
Covered
            bin <auto[64:95],auto[1024:1279]>               10          1          -
Covered
            bin <auto[32:63],auto[1024:1279]>                9          1          -
Covered
            bin <auto[0:31],auto[1024:1279]>                35          1          -
Covered
            bin <auto[512:543],auto[512:767]>                8          1          -
Covered
            bin <auto[256:287],auto[512:767]>                7          1          -
Covered
            bin <auto[128:159],auto[512:767]>                7          1          -
Covered
            bin <auto[64:95],auto[512:767]>                  2          1          -
Covered
            bin <auto[32:63],auto[512:767]>                  5          1          -
Covered
            bin <auto[0:31],auto[512:767]>                  44          1          -
Covered
            bin <auto[512:543],auto[256:511]>                8          1          -
Covered
```

```
            bin <auto[256:287],auto[256:511]>                8          1          -
Covered
            bin <auto[128:159],auto[256:511]>                7          1          -
Covered
            bin <auto[64:95],auto[256:511]>                  6          1          -
Covered
            bin <auto[32:63],auto[256:511]>                  4          1          -
Covered
            bin <auto[0:31],auto[256:511]>                  44          1          -
Covered
            bin <auto[1024:1055],auto[0:255]>                1          1          -
Covered
            bin <auto[512:543],auto[0:255]>                 64          1          -
Covered
            bin <auto[256:287],auto[0:255]>                 37          1          -
Covered
            bin <auto[128:159],auto[0:255]>                 33          1          -
Covered
            bin <auto[64:95],auto[0:255]>                   43          1          -
Covered
            bin <auto[32:63],auto[0:255]>                   46          1          -
Covered
            bin <auto[0:31],auto[0:255]>                   296          1          -
Covered
            bin <auto[2016:2047],*>                          0          1         64
ZERO
            bin <auto[1984:2015],*>                          0          1         64
ZERO
            bin <auto[1952:1983],*>                          0          1         64
ZERO
            bin <auto[1920:1951],*>                          0          1         64
ZERO
            bin <auto[1888:1919],*>                          0          1         64
ZERO
            bin <auto[1856:1887],*>                          0          1         64
ZERO
            bin <auto[1824:1855],*>                          0          1         64
ZERO
            bin <auto[1792:1823],*>                          0          1         64
ZERO
            bin <auto[1760:1791],*>                          0          1         64
ZERO
            bin <auto[1728:1759],*>                          0          1         64
ZERO
            bin <auto[1696:1727],*>                          0          1         64
ZERO
```

```
            bin <auto[1664:1695],*>                         0          1          64
ZERO
            bin <auto[1632:1663],*>                         0          1          64
ZERO
            bin <auto[1600:1631],*>                         0          1          64
ZERO
            bin <auto[1568:1599],*>                         0          1          64
ZERO
            bin <auto[1536:1567],*>                         0          1          64
ZERO
            bin <auto[1504:1535],*>                         0          1          64
ZERO
            bin <auto[1472:1503],*>                         0          1          64
ZERO
            bin <auto[1440:1471],*>                         0          1          64
ZERO
            bin <auto[1408:1439],*>                         0          1          64
ZERO
            bin <auto[1376:1407],*>                         0          1          64
ZERO
            bin <auto[1344:1375],*>                         0          1          64
ZERO
            bin <auto[1312:1343],*>                         0          1          64
ZERO
            bin <auto[1280:1311],*>                         0          1          64
ZERO
            bin <auto[1248:1279],*>                         0          1          64
ZERO
            bin <auto[1216:1247],*>                         0          1          64
ZERO
            bin <auto[1184:1215],*>                         0          1          64
ZERO
            bin <auto[1152:1183],*>                         0          1          64
ZERO
            bin <auto[1120:1151],*>                         0          1          64
ZERO
            bin <auto[1088:1119],*>                         0          1          64
ZERO
            bin <auto[1056:1087],*>                         0          1          64
ZERO
            bin <auto[992:1023],*>                          0          1          64
ZERO
            bin <auto[960:991],*>                           0          1          64
ZERO
            bin <auto[928:959],*>                           0          1          64
ZERO
```

```
            bin <auto[896:927],*>                       0          1          64
ZERO
            bin <auto[864:895],*>                       0          1          64
ZERO
            bin <auto[832:863],*>                       0          1          64
ZERO
            bin <auto[800:831],*>                       0          1          64
ZERO
            bin <auto[768:799],*>                       0          1          64
ZERO
            bin <auto[736:767],*>                       0          1          64
ZERO
            bin <auto[704:735],*>                       0          1          64
ZERO
            bin <auto[672:703],*>                       0          1          64
ZERO
            bin <auto[640:671],*>                       0          1          64
ZERO
            bin <auto[608:639],*>                       0          1          64
ZERO
            bin <auto[576:607],*>                       0          1          64
ZERO
            bin <auto[544:575],*>                       0          1          64
ZERO
            bin <auto[480:511],*>                       0          1          64
ZERO
            bin <auto[448:479],*>                       0          1          64
ZERO
            bin <auto[416:447],*>                       0          1          64
ZERO
            bin <auto[384:415],*>                       0          1          64
ZERO
            bin <auto[352:383],*>                       0          1          64
ZERO
            bin <auto[320:351],*>                       0          1          64
ZERO
            bin <auto[288:319],*>                       0          1          64
ZERO
            bin <auto[224:255],*>                       0          1          64
ZERO
            bin <auto[192:223],*>                       0          1          64
ZERO
            bin <auto[160:191],*>                       0          1          64
ZERO
            bin <auto[96:127],*>                        0          1          64
ZERO
```

```
            bin <*,auto[16128:16383]>                    0          1          64
ZERO
            bin <*,auto[15872:16127]>                    0          1          64
ZERO
            bin <*,auto[15616:15871]>                    0          1          64
ZERO
            bin <*,auto[15360:15615]>                    0          1          64
ZERO
            bin <*,auto[15104:15359]>                    0          1          64
ZERO
            bin <*,auto[14848:15103]>                    0          1          64
ZERO
            bin <*,auto[14592:14847]>                    0          1          64
ZERO
            bin <*,auto[14336:14591]>                    0          1          64
ZERO
            bin <*,auto[14080:14335]>                    0          1          64
ZERO
            bin <*,auto[13824:14079]>                    0          1          64
ZERO
            bin <*,auto[13568:13823]>                    0          1          64
ZERO
            bin <*,auto[13312:13567]>                    0          1          64
ZERO
            bin <*,auto[13056:13311]>                    0          1          64
ZERO
            bin <*,auto[12800:13055]>                    0          1          64
ZERO
            bin <*,auto[12544:12799]>                    0          1          64
ZERO
            bin <*,auto[12288:12543]>                    0          1          64
ZERO
            bin <*,auto[12032:12287]>                    0          1          64
ZERO
            bin <*,auto[11776:12031]>                    0          1          64
ZERO
            bin <*,auto[11520:11775]>                    0          1          64
ZERO
            bin <*,auto[11264:11519]>                    0          1          64
ZERO
            bin <*,auto[11008:11263]>                    0          1          64
ZERO
            bin <*,auto[10752:11007]>                    0          1          64
ZERO
            bin <*,auto[10496:10751]>                    0          1          64
ZERO
```

```
            bin <*,auto[10240:10495]>                    0          1          64
ZERO
            bin <*,auto[9984:10239]>                     0          1          64
ZERO
            bin <*,auto[9728:9983]>                      0          1          64
ZERO
            bin <*,auto[9472:9727]>                      0          1          64
ZERO
            bin <*,auto[9216:9471]>                      0          1          64
ZERO
            bin <*,auto[8960:9215]>                      0          1          64
ZERO
            bin <*,auto[8704:8959]>                      0          1          64
ZERO
            bin <*,auto[8448:8703]>                      0          1          64
ZERO
            bin <*,auto[7936:8191]>                      0          1          64
ZERO
            bin <*,auto[7680:7935]>                      0          1          64
ZERO
            bin <*,auto[7424:7679]>                      0          1          64
ZERO
            bin <*,auto[7168:7423]>                      0          1          64
ZERO
            bin <*,auto[6912:7167]>                      0          1          64
ZERO
            bin <*,auto[6656:6911]>                      0          1          64
ZERO
            bin <*,auto[6400:6655]>                      0          1          64
ZERO
            bin <*,auto[6144:6399]>                      0          1          64
ZERO
            bin <*,auto[5888:6143]>                      0          1          64
ZERO
            bin <*,auto[5632:5887]>                      0          1          64
ZERO
            bin <*,auto[5376:5631]>                      0          1          64
ZERO
            bin <*,auto[5120:5375]>                      0          1          64
ZERO
            bin <*,auto[4864:5119]>                      0          1          64
ZERO
            bin <*,auto[4608:4863]>                      0          1          64
ZERO
            bin <*,auto[4352:4607]>                      0          1          64
ZERO
```

```
            bin <*,auto[3840:4095]>                          0          1          64
ZERO
            bin <*,auto[3584:3839]>                          0          1          64
ZERO
            bin <*,auto[3328:3583]>                          0          1          64
ZERO
            bin <*,auto[3072:3327]>                          0          1          64
ZERO
            bin <*,auto[2816:3071]>                          0          1          64
ZERO
            bin <*,auto[2560:2815]>                          0          1          64
ZERO
            bin <*,auto[2304:2559]>                          0          1          64
ZERO
            bin <*,auto[1792:2047]>                          0          1          64
ZERO
            bin <*,auto[1536:1791]>                          0          1          64
ZERO
            bin <*,auto[1280:1535]>                          0          1          64
ZERO
            bin <*,auto[768:1023]>                           0          1          64
ZERO
            bin <auto[1024:1055],auto[8192:8447]>            0          1           1
ZERO
            bin <auto[1024:1055],auto[4096:4351]>            0          1           1
ZERO
            bin <auto[1024:1055],auto[2048:2303]>            0          1           1
ZERO
            bin <auto[1024:1055],auto[1024:1279]>            0          1           1
ZERO
            bin <auto[1024:1055],auto[512:767]>              0          1           1
ZERO
            bin <auto[1024:1055],auto[256:511]>              0          1           1
ZERO
    Cross #cross__1#                                      0.00%        100           -
ZERO
        covered/total bins:                                  0       1024           -

        missing/total bins:                               1024       1024           -

        % Hit:                                            0.00%       100           -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        Auto, Default and User Defined Bins:
```

```
            bin <*,*>                                       0          1       1024
ZERO
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                     391       298        93    76.21%

================================Statement Details================================

Statement Coverage for Design Unit work.coverage_sv_unit --

    Line         Item                     Count     Source
    ----         ----                     -----     ------
  File transaction.sv
    143             1                     51029
    144             1                     51029
    145             1                     51029
    146             1                     51029
    147             1                     51029
    148             1                     51029
    149             1                     51029
    152             1                     51029
    153             1                     51029
    154             1                     51029
    155             1                     51029
    156             1                     51029
    157             1                     51029
    158             1                     51029
    159             1                     51029
    160             1                     51029
    161             1                     51029
    164             1                     51029
    165             1                     51029
    166             1                     51029
    167             1                     51029
    168             1                     51029
    169             1                     51029
    170             1                     51029
    171             1                     51029
    172             1                     51029
    173             1                     51029
    174             1                     51029
    175             1                     51029
    176             1                     51029
    177             1                     51029
    178             1                     51029
```

179	1	51029
180	1	51029
181	1	51029
182	1	51029
199	1	25
200	1	25
201	1	25
202	1	25
203	1	25
204	1	25
205	1	25
226	1	68
228	1	83
230	1	74
232	1	61
234	1	79
236	1	70
238	1	79
240	1	68
243	1	84
244	1	79
245	1	82
246	1	70
248	1	70
249	1	58
250	1	***0***
252	1	1025
264	1	1025
265	1	1025
266	1	1025
267	1	1025
268	1	1025
269	1	1025
270	1	1025
271	1	1025
272	1	1025

File coverage.sv

18	1	1
60	1	1
61	1	1
66	1	1
67	1	1
68	1	50002
70	1	914
73	1	***0***
78	1	***0***

```
  79              1                    ***0***
  80              1                    ***0***
  81              1                    ***0***
  82              1                    ***0***
  87              1                    ***0***
  88              1                    ***0***
  89              1                    ***0***
  90              1                    ***0***
  91              1                    ***0***
  92              1                    ***0***
  93              1                    ***0***
  98              1                       1
  99              1                    ***0***
  100             1                    ***0***
File driver.sv
  27              1                       1
  28              1                       1
  34              1                       1
  35              1                    1026
  36              1                    1025
  37              1                    1025
  46              1                    1025
  47              1                    1025
  48              1                    1025
  49              1                    1025
  50              1                    1025
  51              1                    1025
  52              1                    1025
  53              1                    1025
  54              1                    1025
  55              1                    1025
  56              1                    1025
  57              1                    1025
  58              1                    1025
  61              1                    1025
  63              1                    1025
  64              1                    1025
File generator.sv
  55              1                       1
  62              1                       1
  63              1                       1
  72              1                       1
  75              1                       1
  77              1                       1
  80              1                       1
  91              1                       1
```

94	1	1
97	1	1
100	1	1
103	1	1
106	1	1
109	1	1
112	1	1
115	1	1
125	1	1
125	2	1000
127	1	1000
128	1	1000
134	1	334
138	1	333
150	1	***0***
153	1	1000
156	1	1000
159	1	1000
169	1	1
171	1	1
172	1	1
175	1	1
177	1	1
178	1	1
181	1	1
183	1	1
184	1	1
187	1	1
189	1	1
190	1	1
199	1	1
201	1	1
202	1	1
205	1	1
207	1	1
208	1	1
211	1	1
213	1	1
214	1	1
223	1	1
225	1	1
226	1	1
229	1	1
231	1	1
232	1	1
235	1	1

237	1	1
238	1	1
247	1	1
249	1	1
250	1	1
253	1	1
255	1	1
256	1	1
259	1	1
261	1	1
262	1	1
265	1	1
267	1	1
268	1	1
277	1	1
278	1	1
279	1	1
282	1	1
283	1	1
284	1	1
293	1	1
295	1	1
296	1	1
299	1	1
301	1	1
302	1	1
311	1	1
312	1	1
313	1	1
316	1	1
317	1	1
318	1	1
327	1	1
328	1	1
329	1	1
332	1	1
333	1	1
334	1	1
343	1	1
344	1	1
345	1	1
348	1	1
349	1	1
350	1	1
356	1	1
357	1	1

```
  358             1                        1
  373             1                       68
  374             1                       83
  375             1                       74
  376             1                       61
  377             1                       79
  378             1                       70
  379             1                       79
  380             1                       68
  381             1                       84
  382             1                       79
  383             1                       82
  384             1                       70
  385             1                       70
  386             1                       58
  387             1                    ***0***
  392             1                      113
  393             1                       91
  394             1                      102
  395             1                       91
  396             1                      109
  397             1                       88
  398             1                       82
  399             1                       76
  400             1                       77
  401             1                      105
  402             1                        2
  403             1                       89
  408             1                     1025
  409             1                     1025
  410             1                     1025
  411             1                     1025
  412             1                     1025
  413             1                     1025
  414             1                     1025
  415             1                     1025
  416             1                     1025
  417             1                     1025
  420             1                     1025
File monitor.sv
  18              1                        1
  31              1                        1
  32              1                        1
  44              1                        1
  45              1                        1
  47              1                    50002
```

49	1	50002
52	1	914
53	1	914
54	1	914
55	1	914
56	1	914
57	1	914
58	1	914
59	1	914
60	1	914
61	1	914
62	1	914
63	1	914
64	1	914
65	1	914
66	1	914
67	1	914
70	1	914
73	1	***0***
88	1	1
92	1	1
105	1	1
106	1	1
119	1	1
120	1	1
122	1	1
124	1	1
126	1	1
129	1	***0***
130	1	***0***
131	1	***0***
132	1	***0***
133	1	***0***
134	1	***0***
135	1	***0***
136	1	***0***
137	1	***0***
138	1	***0***
139	1	***0***
140	1	***0***
141	1	***0***
142	1	***0***
143	1	***0***
144	1	***0***
145	1	***0***
146	1	***0***

```
  147             1                   ***0***
  150             1                   ***0***
  152             1                   ***0***
  154             1                   ***0***
File scoreboard.sv
  16              1                      1
  17              1                      1
  43              1                      1
  44              1                      1
  51              1                      1
  52              1                      1
  61              1                      1
  62              1                      1
  73              1                      1
  74              1                    915
  75              1                    915
  76              1                    914
  77              1                    914
  80              1                    914
  81              1                    914
  82              1                    914
  83              1                    914
  84              1                    914
  85              1                    914
  86              1                    914
  87              1                    914
  88              1                    914
  89              1                    914
  90              1                    914
  91              1                    914
  92              1                    914
  93              1                    914
  94              1                    914
  95              1                    914
  131             1                      1
  132             1                      1
  133             1                   ***0***
  134             1                   ***0***
  135             1                   ***0***
  136             1                   ***0***
  137             1                   ***0***
  140             1                   ***0***
  141             1                   ***0***
  142             1                   ***0***
  143             1                   ***0***
  144             1                   ***0***
```

145	1	***0***
146	1	***0***
147	1	***0***
148	1	***0***
149	1	***0***
150	1	***0***
151	1	***0***
152	1	***0***
153	1	***0***
154	1	***0***
161	1	***0***
164	1	***0***
173	1	***0***
183	1	***0***
189	1	***0***
192	1	***0***
196	1	***0***
202	1	***0***
207	1	***0***
211	1	***0***
218	1	***0***
222	1	***0***
242	1	***0***
248	1	***0***
250	1	***0***
252	1	***0***
258	1	***0***
308	1	***0***
309	1	***0***
310	1	***0***
312	1	***0***
313	1	***0***
314	1	***0***
315	1	***0***
316	1	***0***
317	1	***0***
318	1	***0***
319	1	***0***
320	1	***0***
321	1	***0***
322	1	***0***
323	1	***0***

```
================================================================================
=== Design Unit: work.rv32i_alu
================================================================================
```

```
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        62        55         7    88.70%

================================Branch Details================================

Branch Coverage for Design Unit work.rv32i_alu

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File rv32i_alu.sv
-----------------------------------IF Branch-----------------------------------
    174                                     1026     Count coming in to IF
    174             1                       1026
    178             1                     ***0***
Branch totals: 1 hit of 2 branches = 50.00%

-----------------------------------IF Branch-----------------------------------
    179                                   ***0***     Count coming in to IF
    179             1                     ***0***
                                          ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    198                                   ***0***     Count coming in to IF
    198             1                     ***0***
    201             1                     ***0***
    204             1                     ***0***
                                          ***0***     All False Count
Branch totals: 0 hits of 4 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    218                                     1025     Count coming in to IF
    218             1                        165
    218             2                        860
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    220                                     1025     Count coming in to IF
    220             1                        222
    220             2                        803
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    223                                     1026     Count coming in to IF
```

```
    223             1                       68
                                           958     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    224                                   1026     Count coming in to IF
    224             1                       83
                                           943     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    225                                   1026     Count coming in to IF
    225             1                      135
                                           891     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    227                                    135     Count coming in to IF
    227             1                       74
                                            61     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    227                                     74     Count coming in to IF
    227             2                       40
    227             3                       34
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    229                                   1026     Count coming in to IF
    229             1                       79
                                           947     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    230                                   1026     Count coming in to IF
    230             1                       70
                                           956     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    231                                   1026     Count coming in to IF
    231             1                       79
                                           947     All False Count
Branch totals: 2 hits of 2 branches = 100.00%
```

```
-----------------------------------IF Branch-----------------------------------
    232                                   1026     Count coming in to IF
    232             1                       68
                                            958     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    233                                   1026     Count coming in to IF
    233             1                       84
                                            942     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    234                                   1026     Count coming in to IF
    234             1                       79
                                            947     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    235                                   1026     Count coming in to IF
    235             1                      152
                                            874     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    237                                    152     Count coming in to IF
    237             1                       70
                                             82     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    239                                   1026     Count coming in to IF
    239             1                      128
                                            898     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    241                                    128     Count coming in to IF
    241             1                       70
                                             58     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    241                                     70     Count coming in to IF
    241             2                       36
    241             3                       34
```

```
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    257                                     1193     Count coming in to IF
    257             1                       1191
                                               2     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    258                                     1191     Count coming in to IF
    258             1                        232
                                             959     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    259                                     1191     Count coming in to IF
    259             1                         55
                                            1136     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    266                                     1191     Count coming in to IF
    266             1                        255
                                             936     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    267                                      255     Count coming in to IF
    267             1                        161
                                              94     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    277                                     1193     Count coming in to IF
    277             1                         81
                                            1112     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    278                                     1193     Count coming in to IF
    278             1                         83
                                            1110     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    280                                     1193     Count coming in to IF
```

```
    280             1                       335
    283             1                       858
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    287                                    1193     Count coming in to IF
    287             1                       109
    290             1                      1084
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Conditions                      34        25         9    73.52%

================================Condition Details================================

Condition Coverage for Design Unit work.rv32i_alu --

  File rv32i_alu.sv
----------------Focused Condition View-------------------
Line       179 Item    1  (i_ce && ~stall_bit)
Condition totals: 0 of 2 input terms covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
        i_ce         N  No hits                 Hit '_0' and '_1'
   stall_bit         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  i_ce_0                -
  Row   2:    ***0***  i_ce_1                ~stall_bit
  Row   3:    ***0***  stall_bit_0           i_ce
  Row   4:    ***0***  stall_bit_1           i_ce

----------------Focused Condition View-------------------
Line       198 Item    1  (i_flush && ~stall_bit)
Condition totals: 0 of 2 input terms covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
     i_flush         N  No hits                 Hit '_0' and '_1'
   stall_bit         N  No hits                 Hit '_0' and '_1'
```

```
     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  i_flush_0             -
  Row   2:    ***0***  i_flush_1             ~stall_bit
  Row   3:    ***0***  stall_bit_0           i_flush
  Row   4:    ***0***  stall_bit_1           i_flush

----------------Focused Condition View-------------------
Line       204 Item    1  (stall_bit && ~i_stall)
Condition totals: 0 of 2 input terms covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
   stall_bit         N  No hits                  Hit '_0' and '_1'
     i_stall         N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  stall_bit_0           -
  Row   2:    ***0***  stall_bit_1           ~i_stall
  Row   3:    ***0***  i_stall_0             stall_bit
  Row   4:    ***0***  i_stall_1             stall_bit

----------------Focused Condition View-------------------
Line       218 Item    1  (opcode_jal || opcode_auipc)
Condition totals: 2 of 2 input terms covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  ----------------------  --------------
    opcode_jal         Y
  opcode_auipc         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  opcode_jal_0          ~opcode_auipc
  Row   2:          1  opcode_jal_1          -
  Row   3:          1  opcode_auipc_0        ~opcode_jal
  Row   4:          1  opcode_auipc_1        ~opcode_jal

----------------Focused Condition View-------------------
Line       220 Item    1  (opcode_rtype || opcode_branch)
Condition totals: 2 of 2 input terms covered = 100.00%

     Input Term   Covered  Reason for no coverage   Hint
    -----------  --------  ----------------------  --------------
   opcode_rtype         Y
```

```
  opcode_branch         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  opcode_rtype_0        ~opcode_branch
  Row   2:          1  opcode_rtype_1        -
  Row   3:          1  opcode_branch_0       ~opcode_rtype
  Row   4:          1  opcode_branch_1       ~opcode_rtype

----------------Focused Condition View-------------------
Line       225 Item    1  (alu_slt || alu_sltu)
Condition totals: 2 of 2 input terms covered = 100.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
     alu_slt         Y
    alu_sltu         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  alu_slt_0             ~alu_sltu
  Row   2:          1  alu_slt_1             -
  Row   3:          1  alu_sltu_0            ~alu_slt
  Row   4:          1  alu_sltu_1            ~alu_slt

-----------Focused Condition View (Bimodal)--------------
Line       227 Item    1  (a[31] ^ b[31])
Condition totals: 2 of 2 input terms covered = 100.00%

  Input Term   Covered  Reason for no coverage                  Hint
 -----------  --------  -------------------------------------  --------------
       a[31]         Y
       b[31]         Y

    Rows:   Hits(->0)   Hits(->1)  FEC Target            Non-masking condition(s)


---------  ----------  ----------  --------------------  -------------------------

 Row   1:           1           0  a[31]_0               -

 Row   2:           0           1  a[31]_1               -

 Row   3:           1           1  b[31]_0               -

 Row   4:           0           1  b[31]_1               -
```

```
----------------Focused Condition View-------------------
Line       235 Item    1  (alu_eq || alu_neq)
Condition totals: 2 of 2 input terms covered = 100.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
      alu_eq         Y
     alu_neq         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  alu_eq_0              ~alu_neq
  Row   2:          1  alu_eq_1              -
  Row   3:          1  alu_neq_0             ~alu_eq
  Row   4:          1  alu_neq_1             ~alu_eq

----------------Focused Condition View-------------------
Line       239 Item    1  (alu_ge || alu_geu)
Condition totals: 2 of 2 input terms covered = 100.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
      alu_ge         Y
     alu_geu         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  alu_ge_0              ~alu_geu
  Row   2:          1  alu_ge_1              -
  Row   3:          1  alu_geu_0             ~alu_ge
  Row   4:          1  alu_geu_1             ~alu_ge

-----------Focused Condition View (Bimodal)--------------
Line       241 Item    1  (a[31] ^ b[31])
Condition totals: 2 of 2 input terms covered = 100.00%

  Input Term   Covered  Reason for no coverage                  Hint
 -----------  --------  -------------------------------------  --------------
       a[31]         Y
       b[31]         Y

    Rows:   Hits(->0)   Hits(->1)  FEC Target            Non-masking condition(s)
```

```
---------  ----------  ----------  --------------------  ------------------------

 Row   1:           0           1  a[31]_0               -

 Row   2:           1           1  a[31]_1               -

 Row   3:           0           1  b[31]_0               -

 Row   4:           1           0  b[31]_1               -


----------------Focused Condition View-------------------
Line       258 Item    1  (opcode_rtype || opcode_itype)
Condition totals: 2 of 2 input terms covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  ----------------------  --------------
  opcode_rtype         Y
  opcode_itype         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  opcode_rtype_0        ~opcode_itype
  Row   2:          1  opcode_rtype_1        -
  Row   3:          1  opcode_itype_0        ~opcode_rtype
  Row   4:          1  opcode_itype_1        ~opcode_rtype

----------------Focused Condition View-------------------
Line       259 Item    1  (opcode_branch && y_d[0])
Condition totals: 2 of 2 input terms covered = 100.00%

     Input Term   Covered  Reason for no coverage   Hint
    -----------  --------  ----------------------  --------------
  opcode_branch         Y
         y_d[0]         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  opcode_branch_0       -
  Row   2:          1  opcode_branch_1       y_d[0]
  Row   3:          1  y_d[0]_0              opcode_branch
  Row   4:          1  y_d[0]_1              opcode_branch

----------------Focused Condition View-------------------
Line       266 Item    1  (opcode_jal || opcode_jalr)
Condition totals: 2 of 2 input terms covered = 100.00%
```

```
   Input Term   Covered  Reason for no coverage   Hint
  -----------  --------  ----------------------  --------------
   opcode_jal         Y
  opcode_jalr         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  opcode_jal_0          ~opcode_jalr
  Row   2:          1  opcode_jal_1          -
  Row   3:          1  opcode_jalr_0         ~opcode_jal
  Row   4:          1  opcode_jalr_1         ~opcode_jal

----------------Focused Condition View-------------------
Line           280  Item      1   (((opcode_branch || opcode_store) || (opcode_system &&
(i_funct3 == 0))) || opcode_fence)
Condition totals: 4 of 5 input terms covered = 80.00%

       Input Term   Covered  Reason for no coverage   Hint
      -----------  --------  ----------------------  --------------
    opcode_branch         Y
     opcode_store         Y
    opcode_system         Y
  (i_funct3 == 0)         N  '_0' not hit             Hit '_0'
     opcode_fence         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
   Row    1:          1   opcode_branch_0         (~opcode_fence && ~(opcode_system &&
(i_funct3 == 0)) && ~opcode_store)
  Row   2:          1  opcode_branch_1       -
   Row    3:          1   opcode_store_0          (~opcode_fence && ~(opcode_system &&
(i_funct3 == 0)) && ~opcode_branch)
  Row   4:          1  opcode_store_1        ~opcode_branch
   Row    5:          1   opcode_system_0         (~opcode_fence && ~(opcode_branch ||
opcode_store))
   Row    6:          1   opcode_system_1         (~(opcode_branch || opcode_store) &&
(i_funct3 == 0))
   Row    7:     ***0***   (i_funct3 == 0)_0       (~opcode_fence && ~(opcode_branch ||
opcode_store) && opcode_system)
   Row    8:          1   (i_funct3 == 0)_1       (~(opcode_branch || opcode_store) &&
opcode_system)
   Row    9:          1   opcode_fence_0          ~((opcode_branch || opcode_store) ||
(opcode_system && (i_funct3 == 0)))
 Row    10:          1   opcode_fence_1          ~((opcode_branch || opcode_store) ||
(opcode_system && (i_funct3 == 0)))
```

```
----------------Focused Condition View-------------------
Line       287 Item    1  (opcode_load || (opcode_system && (i_funct3 != 0)))
Condition totals: 1 of 3 input terms covered = 33.33%

       Input Term   Covered  Reason for no coverage   Hint
      -----------  --------  ----------------------  --------------
      opcode_load         Y
    opcode_system         N  '_1' not hit             Hit '_1'
  (i_funct3 != 0)         N  '_1' not hit             Hit '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  opcode_load_0         ~(opcode_system && (i_funct3 != 0))
  Row   2:          1  opcode_load_1         -
  Row   3:          1  opcode_system_0       ~opcode_load
  Row   4:    ***0***  opcode_system_1       (~opcode_load && (i_funct3 != 0))
  Row   5:          1  (i_funct3 != 0)_0     (~opcode_load && opcode_system)
  Row   6:    ***0***  (i_funct3 != 0)_1     (~opcode_load && opcode_system)


Expression Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Expressions                      7         0         7     0.00%

================================Expression Details================================

Expression Coverage for Design Unit work.rv32i_alu --

  File rv32i_alu.sv
----------------Focused Expression View-----------------
Line       193 Item    1  (i_opcode[3] || i_opcode[2])
Expression totals: 0 of 2 input terms covered = 0.00%

   Input Term   Covered  Reason for no coverage   Hint
  -----------  --------  ----------------------  --------------
  i_opcode[3]         N  No hits                 Hit '_0' and '_1'
  i_opcode[2]         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  i_opcode[3]_0         ~i_opcode[2]
  Row   2:    ***0***  i_opcode[3]_1         -
  Row   3:    ***0***  i_opcode[2]_0         ~i_opcode[3]
  Row   4:    ***0***  i_opcode[2]_1         ~i_opcode[3]
```

```
----------------Focused Expression View-----------------
Line       294 Item    1  ((i_stall || i_force_stall) && ~i_flush)
Expression totals: 0 of 3 input terms covered = 0.00%

     Input Term   Covered  Reason for no coverage   Hint
    -----------  --------  ----------------------  --------------
        i_stall         N  '_1' not hit             Hit '_1'
  i_force_stall         N  '_1' not hit             Hit '_1'
        i_flush         N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  i_stall_0             ~i_force_stall
  Row   2:    ***0***  i_stall_1             ~i_flush
  Row   3:          1  i_force_stall_0       ~i_stall
  Row   4:    ***0***  i_force_stall_1       (~i_flush && ~i_stall)
  Row   5:    ***0***  i_flush_0             (i_stall || i_force_stall)
  Row   6:    ***0***  i_flush_1             (i_stall || i_force_stall)

----------------Focused Expression View-----------------
Line       299 Item    1  (o_stall || i_stall)
Expression totals: 0 of 2 input terms covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
    o_stall         N  '_1' not hit             Hit '_1'
    i_stall         N  '_1' not hit             Hit '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  o_stall_0             ~i_stall
  Row   2:    ***0***  o_stall_1             -
  Row   3:          1  i_stall_0             ~o_stall
  Row   4:    ***0***  i_stall_1             ~o_stall


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      65        48        17    73.84%

================================Statement Details================================

Statement Coverage for Design Unit work.rv32i_alu --
```

Line	Item	Count	Source
File rv32i_alu.sv			
173	1	1026	
175	1	1026	
176	1	1026	
177	1	1026	
181	1	***0***	
182	1	***0***	
183	1	***0***	
184	1	***0***	
185	1	***0***	
186	1	***0***	
187	1	***0***	
188	1	***0***	
189	1	***0***	
190	1	***0***	
191	1	***0***	
192	1	***0***	
193	1	***0***	
195	1	***0***	
200	1	***0***	
203	1	***0***	
205	1	***0***	
215	1	1026	
216	1	1026	
218	1	1026	
220	1	1026	
223	1	68	
224	1	83	
226	1	135	
227	1	74	
229	1	79	
230	1	70	
231	1	79	
232	1	68	
233	1	84	
234	1	79	
236	1	152	
237	1	70	
240	1	128	
241	1	70	
248	1	1193	
249	1	1193	
251	1	1193	
252	1	1193	

```
    253             1                       1193
    254             1                       1193
    255             1                       1193
    256             1                       1193
    258             1                        232
    260             1                         55
    262             1                         55
    264             1                         55
    267             1                        161
    268             1                        255
    270             1                        255
    272             1                        255
    273             1                        255
    277             1                         81
    278             1                         83
    281             1                        335
    284             1                        858
    288             1                        109
    290             1                       1084
    294             1                       1193
    298             1                       1166
    299             1                          3

================================================================================
=== Design Unit: work.rv32i_alu_tb
================================================================================
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      41        39         2    95.12%

================================Statement Details================================

Statement Coverage for Design Unit work.rv32i_alu_tb --

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File rv32i_alu_tb.sv
    98              1                          1
    99              1                          1
    100             1                          1
    152             1                          1
    153             1                          1
    154             1                     100002
    155             1                     100001
    161             1                          1
```

```
    162             1                          1
    163             1                          1
    164             1                          1
    165             1                          1
    166             1                          1
    167             1                          1
    168             1                          1
    169             1                          1
    170             1                          1
    171             1                          1
    172             1                          1
    173             1                          1
    174             1                          1
    175             1                          1
    176             1                          1
    181             1                          1
    182             1                          1
    183             1                          1
    184             1                          1
    185             1                          1
    186             1                          1
    192             1                          1
    193             1                          1
    194             1                          1
    195             1                          1
    196             1                          1
    197             1                          1
    200             1                          1
    242             1                          1
    242             2                          1
    247             1                          1
    248             1                       ***0***
    249             1                       ***0***

COVERGROUP COVERAGE:
----------------------------------------------------------------------------------------
------------------
Covergroup                                                 Metric        Goal        Bins
Status


----------------------------------------------------------------------------------------
------------------
 TYPE work.coverage_sv_unit::coverage/alu_cg             34.84%         100           -
Uncovered
    covered/total bins:                                     77        5315           -
```

```
    missing/total bins:                                 5238        5315          -

    % Hit:                                              1.44%        100          -

    type_option.weight=1
    type_option.goal=100
    type_option.comment=
    type_option.strobe=0
    type_option.merge_instances=auto(1)
    Coverpoint #coverpoint__0#                          45.45%        100          -
Uncovered
        covered/total bins:                                5          11          -

        missing/total bins:                                6          11          -

        % Hit:                                         45.45%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin opcode_types[0]                               78           1          -
Covered
        bin opcode_types[1]                              103           1          -
Covered
        bin opcode_types[2]                               82           1          -
Covered
        bin opcode_types[3]                                0           1          -
ZERO
        bin opcode_types[4]                               90           1          -
Covered
        bin opcode_types[5]                                0           1          -
ZERO
        bin opcode_types[6]                                0           1          -
ZERO
        bin opcode_types[7]                                0           1          -
ZERO
        bin opcode_types[8]                               79           1          -
Covered
        bin opcode_types[9]                                0           1          -
ZERO
        bin opcode_types[10]                               0           1          -
ZERO
    Coverpoint #coverpoint__1#                          28.57%        100          -
Uncovered
        covered/total bins:                                4          14          -
```

```
        missing/total bins:                          10          14          -

        % Hit:                                   28.57%         100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin alu_ops[0]                               0           1          -
ZERO
        bin alu_ops[1]                              60           1          -
Covered
        bin alu_ops[2]                              71           1          -
Covered
        bin alu_ops[3]                               0           1          -
ZERO
        bin alu_ops[4]                              64           1          -
Covered
        bin alu_ops[5]                               0           1          -
ZERO
        bin alu_ops[6]                               0           1          -
ZERO
        bin alu_ops[7]                               0           1          -
ZERO
        bin alu_ops[8]                              58           1          -
Covered
        bin alu_ops[9]                               0           1          -
ZERO
        bin alu_ops[10]                              0           1          -
ZERO
        bin alu_ops[11]                              0           1          -
ZERO
        bin alu_ops[12]                              0           1          -
ZERO
        bin alu_ops[13]                              0           1          -
ZERO
    Coverpoint #coverpoint__2#                   100.00%         100          -
Covered
        covered/total bins:                          2           2          -

        missing/total bins:                          0           2          -

        % Hit:                                   100.00%         100          -

        type_option.weight=1
        type_option.goal=100
```

```
        type_option.comment=
        bin auto[0]                                  714          1          -
Covered
        bin auto[1]                                  200          1          -
Covered
    Coverpoint #coverpoint__3#                    100.00%        100          -
Covered
        covered/total bins:                            1          1          -

        missing/total bins:                            0          1          -

        % Hit:                                    100.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin pc_values                                914          1          -
Covered
    Coverpoint #coverpoint__4#                      0.00%        100          -
ZERO
        covered/total bins:                            0          2          -

        missing/total bins:                            2          2          -

        % Hit:                                      0.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                    0          1          -
ZERO
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__5#                      0.00%        100          -
ZERO
        covered/total bins:                            0          2          -

        missing/total bins:                            2          2          -

        % Hit:                                      0.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                    0          1          -
ZERO
```

```
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__6#                      0.00%        100          -
ZERO
        covered/total bins:                            0          1          -

        missing/total bins:                            1          1          -

        % Hit:                                      0.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin rd_addr                                    0          1          -
ZERO
    Coverpoint #coverpoint__7#                     50.00%        100          -
Uncovered
        covered/total bins:                            1          2          -

        missing/total bins:                            1          2          -

        % Hit:                                     50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                    0          1          -
ZERO
        bin auto[1]                                  914          1          -
Covered
    Coverpoint #coverpoint__8#                     50.00%        100          -
Uncovered
        covered/total bins:                            1          2          -

        missing/total bins:                            1          2          -

        % Hit:                                     50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                  914          1          -
Covered
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__9#                     50.00%        100          -
```

```
Uncovered
        covered/total bins:                                    1          2          -

        missing/total bins:                                    1          2          -

        % Hit:                                            50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                          914          1          -
Covered
        bin auto[1]                                            0          1          -
ZERO
    Coverpoint #coverpoint__10#                           50.00%        100          -
Uncovered
        covered/total bins:                                    1          2          -

        missing/total bins:                                    1          2          -

        % Hit:                                            50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                          914          1          -
Covered
        bin auto[1]                                            0          1          -
ZERO
    Coverpoint #coverpoint__11#                           50.00%        100          -
Uncovered
        covered/total bins:                                    1          2          -

        missing/total bins:                                    1          2          -

        % Hit:                                            50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                          914          1          -
Covered
        bin auto[1]                                            0          1          -
ZERO
    Coverpoint #coverpoint__12#                           50.00%        100          -
Uncovered
```

```
        covered/total bins:                                1          2          -

        missing/total bins:                                1          2          -

        % Hit:                                        50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                      914          1          -
Covered
        bin auto[1]                                        0          1          -
ZERO
    Coverpoint #coverpoint__13#                      100.00%        100          -
Covered
        covered/total bins:                                2          2          -

        missing/total bins:                                0          2          -

        % Hit:                                       100.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                      714          1          -
Covered
        bin auto[1]                                      200          1          -
Covered
    Coverpoint #coverpoint__14#                        0.00%        100          -
ZERO
        covered/total bins:                                0          4          -

        missing/total bins:                                4          4          -

        % Hit:                                         0.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin exceptions[0]                                  0          1          -
ZERO
        bin exceptions[1]                                  0          1          -
ZERO
        bin exceptions[2]                                  0          1          -
ZERO
        bin exceptions[3]                                  0          1          -
```

```
ZERO
    Coverpoint #vif.i_opcode__15#                    10.93%         100          -
Uncovered
        covered/total bins:                              7          64          -

        missing/total bins:                             57          64          -

        % Hit:                                       10.93%         100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0:31]                                 527           1          -
Covered
        bin auto[32:63]                                 81           1          -
Covered
        bin auto[64:95]                                 73           1          -
Covered
        bin auto[96:127]                                 0           1          -
ZERO
        bin auto[128:159]                               70           1          -
Covered
        bin auto[160:191]                                0           1          -
ZERO
        bin auto[192:223]                                0           1          -
ZERO
        bin auto[224:255]                                0           1          -
ZERO
        bin auto[256:287]                               67           1          -
Covered
        bin auto[288:319]                                0           1          -
ZERO
        bin auto[320:351]                                0           1          -
ZERO
        bin auto[352:383]                                0           1          -
ZERO
        bin auto[384:415]                                0           1          -
ZERO
        bin auto[416:447]                                0           1          -
ZERO
        bin auto[448:479]                                0           1          -
ZERO
        bin auto[480:511]                                0           1          -
ZERO
        bin auto[512:543]                               95           1          -
Covered
```

```
        bin auto[544:575]                                   0          1          -
ZERO
        bin auto[576:607]                                   0          1          -
ZERO
        bin auto[608:639]                                   0          1          -
ZERO
        bin auto[640:671]                                   0          1          -
ZERO
        bin auto[672:703]                                   0          1          -
ZERO
        bin auto[704:735]                                   0          1          -
ZERO
        bin auto[736:767]                                   0          1          -
ZERO
        bin auto[768:799]                                   0          1          -
ZERO
        bin auto[800:831]                                   0          1          -
ZERO
        bin auto[832:863]                                   0          1          -
ZERO
        bin auto[864:895]                                   0          1          -
ZERO
        bin auto[896:927]                                   0          1          -
ZERO
        bin auto[928:959]                                   0          1          -
ZERO
        bin auto[960:991]                                   0          1          -
ZERO
        bin auto[992:1023]                                  0          1          -
ZERO
        bin auto[1024:1055]                                 1          1          -
Covered
        bin auto[1056:1087]                                 0          1          -
ZERO
        bin auto[1088:1119]                                 0          1          -
ZERO
        bin auto[1120:1151]                                 0          1          -
ZERO
        bin auto[1152:1183]                                 0          1          -
ZERO
        bin auto[1184:1215]                                 0          1          -
ZERO
        bin auto[1216:1247]                                 0          1          -
ZERO
        bin auto[1248:1279]                                 0          1          -
ZERO
```

```
        bin auto[1280:1311]                                 0          1          -
ZERO
        bin auto[1312:1343]                                 0          1          -
ZERO
        bin auto[1344:1375]                                 0          1          -
ZERO
        bin auto[1376:1407]                                 0          1          -
ZERO
        bin auto[1408:1439]                                 0          1          -
ZERO
        bin auto[1440:1471]                                 0          1          -
ZERO
        bin auto[1472:1503]                                 0          1          -
ZERO
        bin auto[1504:1535]                                 0          1          -
ZERO
        bin auto[1536:1567]                                 0          1          -
ZERO
        bin auto[1568:1599]                                 0          1          -
ZERO
        bin auto[1600:1631]                                 0          1          -
ZERO
        bin auto[1632:1663]                                 0          1          -
ZERO
        bin auto[1664:1695]                                 0          1          -
ZERO
        bin auto[1696:1727]                                 0          1          -
ZERO
        bin auto[1728:1759]                                 0          1          -
ZERO
        bin auto[1760:1791]                                 0          1          -
ZERO
        bin auto[1792:1823]                                 0          1          -
ZERO
        bin auto[1824:1855]                                 0          1          -
ZERO
        bin auto[1856:1887]                                 0          1          -
ZERO
        bin auto[1888:1919]                                 0          1          -
ZERO
        bin auto[1920:1951]                                 0          1          -
ZERO
        bin auto[1952:1983]                                 0          1          -
ZERO
        bin auto[1984:2015]                                 0          1          -
ZERO
```

```
        bin auto[2016:2047]                                0          1          -
ZERO
    Coverpoint #vif.i_exception__16#                    0.00%       100          -
ZERO
        covered/total bins:                                0         16          -

        missing/total bins:                               16         16          -

        % Hit:                                          0.00%       100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                        0          1          -
ZERO
        bin auto[1]                                        0          1          -
ZERO
        bin auto[2]                                        0          1          -
ZERO
        bin auto[3]                                        0          1          -
ZERO
        bin auto[4]                                        0          1          -
ZERO
        bin auto[5]                                        0          1          -
ZERO
        bin auto[6]                                        0          1          -
ZERO
        bin auto[7]                                        0          1          -
ZERO
        bin auto[8]                                        0          1          -
ZERO
        bin auto[9]                                        0          1          -
ZERO
        bin auto[10]                                       0          1          -
ZERO
        bin auto[11]                                       0          1          -
ZERO
        bin auto[12]                                       0          1          -
ZERO
        bin auto[13]                                       0          1          -
ZERO
        bin auto[14]                                       0          1          -
ZERO
        bin auto[15]                                       0          1          -
ZERO
    Coverpoint #vif.i_alu__17#                          10.93%       100          -
```

```
Uncovered
        covered/total bins:                                    7         64          -

        missing/total bins:                                   57         64          -

        % Hit:                                             10.93%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0:255]                                      520          1          -
Covered
        bin auto[256:511]                                     77          1          -
Covered
        bin auto[512:767]                                     73          1          -
Covered
        bin auto[768:1023]                                     0          1          -
ZERO
        bin auto[1024:1279]                                   70          1          -
Covered
        bin auto[1280:1535]                                    0          1          -
ZERO
        bin auto[1536:1791]                                    0          1          -
ZERO
        bin auto[1792:2047]                                    0          1          -
ZERO
        bin auto[2048:2303]                                   62          1          -
Covered
        bin auto[2304:2559]                                    0          1          -
ZERO
        bin auto[2560:2815]                                    0          1          -
ZERO
        bin auto[2816:3071]                                    0          1          -
ZERO
        bin auto[3072:3327]                                    0          1          -
ZERO
        bin auto[3328:3583]                                    0          1          -
ZERO
        bin auto[3584:3839]                                    0          1          -
ZERO
        bin auto[3840:4095]                                    0          1          -
ZERO
        bin auto[4096:4351]                                   56          1          -
Covered
        bin auto[4352:4607]                                    0          1          -
ZERO
```

```
        bin auto[4608:4863]                                 0          1          -
ZERO
        bin auto[4864:5119]                                 0          1          -
ZERO
        bin auto[5120:5375]                                 0          1          -
ZERO
        bin auto[5376:5631]                                 0          1          -
ZERO
        bin auto[5632:5887]                                 0          1          -
ZERO
        bin auto[5888:6143]                                 0          1          -
ZERO
        bin auto[6144:6399]                                 0          1          -
ZERO
        bin auto[6400:6655]                                 0          1          -
ZERO
        bin auto[6656:6911]                                 0          1          -
ZERO
        bin auto[6912:7167]                                 0          1          -
ZERO
        bin auto[7168:7423]                                 0          1          -
ZERO
        bin auto[7424:7679]                                 0          1          -
ZERO
        bin auto[7680:7935]                                 0          1          -
ZERO
        bin auto[7936:8191]                                 0          1          -
ZERO
        bin auto[8192:8447]                                56          1          -
Covered
        bin auto[8448:8703]                                 0          1          -
ZERO
        bin auto[8704:8959]                                 0          1          -
ZERO
        bin auto[8960:9215]                                 0          1          -
ZERO
        bin auto[9216:9471]                                 0          1          -
ZERO
        bin auto[9472:9727]                                 0          1          -
ZERO
        bin auto[9728:9983]                                 0          1          -
ZERO
        bin auto[9984:10239]                                0          1          -
ZERO
        bin auto[10240:10495]                               0          1          -
ZERO
```

```
        bin auto[10496:10751]                                   0          1          -
ZERO
        bin auto[10752:11007]                                   0          1          -
ZERO
        bin auto[11008:11263]                                   0          1          -
ZERO
        bin auto[11264:11519]                                   0          1          -
ZERO
        bin auto[11520:11775]                                   0          1          -
ZERO
        bin auto[11776:12031]                                   0          1          -
ZERO
        bin auto[12032:12287]                                   0          1          -
ZERO
        bin auto[12288:12543]                                   0          1          -
ZERO
        bin auto[12544:12799]                                   0          1          -
ZERO
        bin auto[12800:13055]                                   0          1          -
ZERO
        bin auto[13056:13311]                                   0          1          -
ZERO
        bin auto[13312:13567]                                   0          1          -
ZERO
        bin auto[13568:13823]                                   0          1          -
ZERO
        bin auto[13824:14079]                                   0          1          -
ZERO
        bin auto[14080:14335]                                   0          1          -
ZERO
        bin auto[14336:14591]                                   0          1          -
ZERO
        bin auto[14592:14847]                                   0          1          -
ZERO
        bin auto[14848:15103]                                   0          1          -
ZERO
        bin auto[15104:15359]                                   0          1          -
ZERO
        bin auto[15360:15615]                                   0          1          -
ZERO
        bin auto[15616:15871]                                   0          1          -
ZERO
        bin auto[15872:16127]                                   0          1          -
ZERO
        bin auto[16128:16383]                                   0          1          -
ZERO
```

```
    Cross #cross__0#                                    1.04%        100          -
Uncovered
        covered/total bins:                               43       4096          -

        missing/total bins:                             4053       4096          -

        % Hit:                                          1.04%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        Auto, Default and User Defined Bins:
             bin <auto[512:543],auto[8192:8447]>             5          1          -
Covered
             bin <auto[256:287],auto[8192:8447]>             3          1          -
Covered
             bin <auto[128:159],auto[8192:8447]>             3          1          -
Covered
             bin <auto[64:95],auto[8192:8447]>               7          1          -
Covered
             bin <auto[32:63],auto[8192:8447]>               7          1          -
Covered
             bin <auto[0:31],auto[8192:8447]>               31          1          -
Covered
             bin <auto[512:543],auto[4096:4351]>             3          1          -
Covered
             bin <auto[256:287],auto[4096:4351]>             2          1          -
Covered
             bin <auto[128:159],auto[4096:4351]>             3          1          -
Covered
             bin <auto[64:95],auto[4096:4351]>               2          1          -
Covered
             bin <auto[32:63],auto[4096:4351]>               7          1          -
Covered
             bin <auto[0:31],auto[4096:4351]>               39          1          -
Covered
             bin <auto[512:543],auto[2048:2303]>             3          1          -
Covered
             bin <auto[256:287],auto[2048:2303]>             4          1          -
Covered
             bin <auto[128:159],auto[2048:2303]>            11          1          -
Covered
             bin <auto[64:95],auto[2048:2303]>               3          1          -
Covered
             bin <auto[32:63],auto[2048:2303]>               3          1          -
Covered
```

```
            bin <auto[0:31],auto[2048:2303]>                38          1           -
Covered
            bin <auto[512:543],auto[1024:1279]>              4          1           -
Covered
            bin <auto[256:287],auto[1024:1279]>              6          1           -
Covered
            bin <auto[128:159],auto[1024:1279]>              6          1           -
Covered
            bin <auto[64:95],auto[1024:1279]>               10          1           -
Covered
            bin <auto[32:63],auto[1024:1279]>                9          1           -
Covered
            bin <auto[0:31],auto[1024:1279]>                35          1           -
Covered
            bin <auto[512:543],auto[512:767]>                8          1           -
Covered
            bin <auto[256:287],auto[512:767]>                7          1           -
Covered
            bin <auto[128:159],auto[512:767]>                7          1           -
Covered
            bin <auto[64:95],auto[512:767]>                  2          1           -
Covered
            bin <auto[32:63],auto[512:767]>                  5          1           -
Covered
            bin <auto[0:31],auto[512:767]>                  44          1           -
Covered
            bin <auto[512:543],auto[256:511]>                8          1           -
Covered
            bin <auto[256:287],auto[256:511]>                8          1           -
Covered
            bin <auto[128:159],auto[256:511]>                7          1           -
Covered
            bin <auto[64:95],auto[256:511]>                  6          1           -
Covered
            bin <auto[32:63],auto[256:511]>                  4          1           -
Covered
            bin <auto[0:31],auto[256:511]>                  44          1           -
Covered
            bin <auto[1024:1055],auto[0:255]>                1          1           -
Covered
            bin <auto[512:543],auto[0:255]>                 64          1           -
Covered
            bin <auto[256:287],auto[0:255]>                 37          1           -
Covered
            bin <auto[128:159],auto[0:255]>                 33          1           -
Covered
```

```
            bin <auto[64:95],auto[0:255]>                  43          1           -
Covered
            bin <auto[32:63],auto[0:255]>                  46          1           -
Covered
            bin <auto[0:31],auto[0:255]>                  296          1           -
Covered
            bin <auto[2016:2047],*>                         0          1          64
ZERO
            bin <auto[1984:2015],*>                         0          1          64
ZERO
            bin <auto[1952:1983],*>                         0          1          64
ZERO
            bin <auto[1920:1951],*>                         0          1          64
ZERO
            bin <auto[1888:1919],*>                         0          1          64
ZERO
            bin <auto[1856:1887],*>                         0          1          64
ZERO
            bin <auto[1824:1855],*>                         0          1          64
ZERO
            bin <auto[1792:1823],*>                         0          1          64
ZERO
            bin <auto[1760:1791],*>                         0          1          64
ZERO
            bin <auto[1728:1759],*>                         0          1          64
ZERO
            bin <auto[1696:1727],*>                         0          1          64
ZERO
            bin <auto[1664:1695],*>                         0          1          64
ZERO
            bin <auto[1632:1663],*>                         0          1          64
ZERO
            bin <auto[1600:1631],*>                         0          1          64
ZERO
            bin <auto[1568:1599],*>                         0          1          64
ZERO
            bin <auto[1536:1567],*>                         0          1          64
ZERO
            bin <auto[1504:1535],*>                         0          1          64
ZERO
            bin <auto[1472:1503],*>                         0          1          64
ZERO
            bin <auto[1440:1471],*>                         0          1          64
ZERO
            bin <auto[1408:1439],*>                         0          1          64
ZERO
```

```
            bin <auto[1376:1407],*>                         0          1          64
ZERO
            bin <auto[1344:1375],*>                         0          1          64
ZERO
            bin <auto[1312:1343],*>                         0          1          64
ZERO
            bin <auto[1280:1311],*>                         0          1          64
ZERO
            bin <auto[1248:1279],*>                         0          1          64
ZERO
            bin <auto[1216:1247],*>                         0          1          64
ZERO
            bin <auto[1184:1215],*>                         0          1          64
ZERO
            bin <auto[1152:1183],*>                         0          1          64
ZERO
            bin <auto[1120:1151],*>                         0          1          64
ZERO
            bin <auto[1088:1119],*>                         0          1          64
ZERO
            bin <auto[1056:1087],*>                         0          1          64
ZERO
            bin <auto[992:1023],*>                          0          1          64
ZERO
            bin <auto[960:991],*>                           0          1          64
ZERO
            bin <auto[928:959],*>                           0          1          64
ZERO
            bin <auto[896:927],*>                           0          1          64
ZERO
            bin <auto[864:895],*>                           0          1          64
ZERO
            bin <auto[832:863],*>                           0          1          64
ZERO
            bin <auto[800:831],*>                           0          1          64
ZERO
            bin <auto[768:799],*>                           0          1          64
ZERO
            bin <auto[736:767],*>                           0          1          64
ZERO
            bin <auto[704:735],*>                           0          1          64
ZERO
            bin <auto[672:703],*>                           0          1          64
ZERO
            bin <auto[640:671],*>                           0          1          64
ZERO
```

```
            bin <auto[608:639],*>                    0          1          64
ZERO
            bin <auto[576:607],*>                    0          1          64
ZERO
            bin <auto[544:575],*>                    0          1          64
ZERO
            bin <auto[480:511],*>                    0          1          64
ZERO
            bin <auto[448:479],*>                    0          1          64
ZERO
            bin <auto[416:447],*>                    0          1          64
ZERO
            bin <auto[384:415],*>                    0          1          64
ZERO
            bin <auto[352:383],*>                    0          1          64
ZERO
            bin <auto[320:351],*>                    0          1          64
ZERO
            bin <auto[288:319],*>                    0          1          64
ZERO
            bin <auto[224:255],*>                    0          1          64
ZERO
            bin <auto[192:223],*>                    0          1          64
ZERO
            bin <auto[160:191],*>                    0          1          64
ZERO
            bin <auto[96:127],*>                     0          1          64
ZERO
            bin <*,auto[16128:16383]>                0          1          64
ZERO
            bin <*,auto[15872:16127]>                0          1          64
ZERO
            bin <*,auto[15616:15871]>                0          1          64
ZERO
            bin <*,auto[15360:15615]>                0          1          64
ZERO
            bin <*,auto[15104:15359]>                0          1          64
ZERO
            bin <*,auto[14848:15103]>                0          1          64
ZERO
            bin <*,auto[14592:14847]>                0          1          64
ZERO
            bin <*,auto[14336:14591]>                0          1          64
ZERO
            bin <*,auto[14080:14335]>                0          1          64
ZERO
```

```
            bin <*,auto[13824:14079]>                    0          1          64
ZERO
            bin <*,auto[13568:13823]>                    0          1          64
ZERO
            bin <*,auto[13312:13567]>                    0          1          64
ZERO
            bin <*,auto[13056:13311]>                    0          1          64
ZERO
            bin <*,auto[12800:13055]>                    0          1          64
ZERO
            bin <*,auto[12544:12799]>                    0          1          64
ZERO
            bin <*,auto[12288:12543]>                    0          1          64
ZERO
            bin <*,auto[12032:12287]>                    0          1          64
ZERO
            bin <*,auto[11776:12031]>                    0          1          64
ZERO
            bin <*,auto[11520:11775]>                    0          1          64
ZERO
            bin <*,auto[11264:11519]>                    0          1          64
ZERO
            bin <*,auto[11008:11263]>                    0          1          64
ZERO
            bin <*,auto[10752:11007]>                    0          1          64
ZERO
            bin <*,auto[10496:10751]>                    0          1          64
ZERO
            bin <*,auto[10240:10495]>                    0          1          64
ZERO
            bin <*,auto[9984:10239]>                     0          1          64
ZERO
            bin <*,auto[9728:9983]>                      0          1          64
ZERO
            bin <*,auto[9472:9727]>                      0          1          64
ZERO
            bin <*,auto[9216:9471]>                      0          1          64
ZERO
            bin <*,auto[8960:9215]>                      0          1          64
ZERO
            bin <*,auto[8704:8959]>                      0          1          64
ZERO
            bin <*,auto[8448:8703]>                      0          1          64
ZERO
            bin <*,auto[7936:8191]>                      0          1          64
ZERO
```

```
            bin <*,auto[7680:7935]>                    0          1          64
ZERO
            bin <*,auto[7424:7679]>                    0          1          64
ZERO
            bin <*,auto[7168:7423]>                    0          1          64
ZERO
            bin <*,auto[6912:7167]>                    0          1          64
ZERO
            bin <*,auto[6656:6911]>                    0          1          64
ZERO
            bin <*,auto[6400:6655]>                    0          1          64
ZERO
            bin <*,auto[6144:6399]>                    0          1          64
ZERO
            bin <*,auto[5888:6143]>                    0          1          64
ZERO
            bin <*,auto[5632:5887]>                    0          1          64
ZERO
            bin <*,auto[5376:5631]>                    0          1          64
ZERO
            bin <*,auto[5120:5375]>                    0          1          64
ZERO
            bin <*,auto[4864:5119]>                    0          1          64
ZERO
            bin <*,auto[4608:4863]>                    0          1          64
ZERO
            bin <*,auto[4352:4607]>                    0          1          64
ZERO
            bin <*,auto[3840:4095]>                    0          1          64
ZERO
            bin <*,auto[3584:3839]>                    0          1          64
ZERO
            bin <*,auto[3328:3583]>                    0          1          64
ZERO
            bin <*,auto[3072:3327]>                    0          1          64
ZERO
            bin <*,auto[2816:3071]>                    0          1          64
ZERO
            bin <*,auto[2560:2815]>                    0          1          64
ZERO
            bin <*,auto[2304:2559]>                    0          1          64
ZERO
            bin <*,auto[1792:2047]>                    0          1          64
ZERO
            bin <*,auto[1536:1791]>                    0          1          64
ZERO
```

```
            bin <*,auto[1280:1535]>                          0          1          64
ZERO
            bin <*,auto[768:1023]>                           0          1          64
ZERO
            bin <auto[1024:1055],auto[8192:8447]>            0          1           1
ZERO
            bin <auto[1024:1055],auto[4096:4351]>            0          1           1
ZERO
            bin <auto[1024:1055],auto[2048:2303]>            0          1           1
ZERO
            bin <auto[1024:1055],auto[1024:1279]>            0          1           1
ZERO
            bin <auto[1024:1055],auto[512:767]>              0          1           1
ZERO
            bin <auto[1024:1055],auto[256:511]>              0          1           1
ZERO
    Cross #cross__1#                                      0.00%        100           -
ZERO
        covered/total bins:                                  0       1024           -

        missing/total bins:                               1024       1024           -

        % Hit:                                            0.00%       100           -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        Auto, Default and User Defined Bins:
            bin <*,*>                                        0          1       1024
ZERO

TOTAL COVERGROUP COVERAGE: 34.84%  COVERGROUP TYPES: 1

Total Coverage By Design Unit (filtered view): 41.08%
```

File: report_50.txt

Coverage Report by DU with details

```
================================================================================
=== Design Unit: work.coverage_sv_unit
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                       145        75        70    51.72%

================================Branch Details================================

Branch Coverage for Design Unit work.coverage_sv_unit

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File transaction.sv
------------------------------------CASE Branch------------------------------------
    224                                      75     Count coming in to CASE
    225             1                        12
    227             1                         6
    229             1                         2
    231             1                         3
    233             1                         6
    235             1                         9
    237             1                         4
    239             1                         5
    242             1                         9
    244             1                         6
    245             1                         5
    246             1                         2
    247             1                         3
    249             1                         3
    250             1                    ***0***
Branch totals: 14 hits of 15 branches = 93.33%

-----------------------------------IF Branch-----------------------------------
    226                                      12     Count coming in to IF
    226             1                         3
    226             2                         9
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
```

```
    228                                     6     Count coming in to IF
    228             1                       2
    228             2                       4
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    230                                     2     Count coming in to IF
    230             1                       1
    230             2                       1
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    232                                     3     Count coming in to IF
    232             1                       1
    232             2                       2
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    234                                     6     Count coming in to IF
    234             1                       2
    234             2                       4
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    236                                     9     Count coming in to IF
    236             1                       2
    236             2                       7
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    238                                     4     Count coming in to IF
    238             1                       1
    238             2                       3
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    241                                     5     Count coming in to IF
    241             1                       2
    241             2                       3
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    243                                     9     Count coming in to IF
    243             1                       4
    243             2                       5
Branch totals: 2 hits of 2 branches = 100.00%
```

```
------------------------------------IF Branch------------------------------------
    244                                     6     Count coming in to IF
    244             2                       1
    244             3                       5
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    245                                     5     Count coming in to IF
    245             2                       2
    245             3                       3
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    246                                     2     Count coming in to IF
    246             2                       2
    246             3                  ***0***
Branch totals: 1 hit of 2 branches = 50.00%

------------------------------------IF Branch------------------------------------
    248                                     3     Count coming in to IF
    248             1                       2
    248             2                       1
Branch totals: 2 hits of 2 branches = 100.00%

------------------------------------IF Branch------------------------------------
    249                                     3     Count coming in to IF
    249             2                       2
    249             3                       1
Branch totals: 2 hits of 2 branches = 100.00%


  File coverage.sv
------------------------------------IF Branch------------------------------------
    69                                    501     Count coming in to IF
    69              1                      65
                                          436     All False Count
Branch totals: 2 hits of 2 branches = 100.00%


  File generator.sv
----------------------------------CASE Branch------------------------------------
    131                                    50     Count coming in to CASE
    132             1                      17
    136             1                      17
    140             1                      16
```

```
    143             1                     ***0***
Branch totals: 3 hits of 4 branches = 75.00%

-----------------------------------IF Branch-------------------------------------
    149                                     50     Count coming in to IF
    149             1                     ***0***
                                            50     All False Count
Branch totals: 1 hit of 2 branches = 50.00%

-----------------------------------CASE Branch-----------------------------------
    372                                     75     Count coming in to CASE
    373             1                       12
    374             1                        6
    375             1                        2
    376             1                        3
    377             1                        6
    378             1                        9
    379             1                        4
    380             1                        5
    381             1                        9
    382             1                        6
    383             1                        5
    384             1                        2
    385             1                        3
    386             1                        3
    387             1                     ***0***
Branch totals: 14 hits of 15 branches = 93.33%

-----------------------------------CASE Branch-----------------------------------
    391                                     75     Count coming in to CASE
    392             1                       21
    393             1                        4
    394             1                        6
    395             1                        7
    396             1                        7
    397             1                        4
    398             1                        4
    399             1                        3
    400             1                        7
    401             1                        6
    402             1                        2
    403             1                        4
Branch totals: 12 hits of 12 branches = 100.00%


  File monitor.sv
```

```
-----------------------------------IF Branch-----------------------------------
    51                                    501     Count coming in to IF
    51              1                      65
                                           436     All False Count
Branch totals: 2 hits of 2 branches = 100.00%


  File scoreboard.sv
-----------------------------------IF Branch-----------------------------------
    160                                  ***0***     Count coming in to IF
    160             1                    ***0***
    162             1                    ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    165                                  ***0***     Count coming in to IF
    165             1                    ***0***
    165             2                    ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    166                                  ***0***     Count coming in to IF
    166             1                    ***0***
    166             2                    ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    170                                  ***0***     Count coming in to IF
    170             1                    ***0***
                                         ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    172                                  ***0***     Count coming in to IF
    172             1                    ***0***
                                         ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    177                                  ***0***     Count coming in to IF
    177             1                    ***0***
                                         ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    187                                  ***0***     Count coming in to IF
```

```
    187             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-------------------------------------
    188                                 ***0***     Count coming in to IF
    188             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-------------------------------------
    191                                 ***0***     Count coming in to IF
    191             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-------------------------------------
    201                                 ***0***     Count coming in to IF
    201             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-------------------------------------
    206                                 ***0***     Count coming in to IF
    206             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-------------------------------------
    215                                 ***0***     Count coming in to IF
    215             1                   ***0***
    215             2                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-------------------------------------
    218                                 ***0***     Count coming in to IF
    218             1                   ***0***
    218             2                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-------------------------------------
    221                                 ***0***     Count coming in to IF
    221             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%
```

```
-----------------------------------IF Branch-----------------------------------
    226                                 ***0***     Count coming in to IF
    226             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    227                                 ***0***     Count coming in to IF
    227             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    247                                 ***0***     Count coming in to IF
    247             1                   ***0***
    249             1                   ***0***
    251             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 4 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    257                                 ***0***     Count coming in to IF
    257             1                   ***0***
                                        ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

----------------------------------CASE Branch----------------------------------
    305                                 ***0***     Count coming in to CASE
    308             1                   ***0***
    309             1                   ***0***
    310             1                   ***0***
    311             1                   ***0***
    313             1                   ***0***
    314             1                   ***0***
    315             1                   ***0***
    316             1                   ***0***
    317             1                   ***0***
    318             1                   ***0***
    319             1                   ***0***
    320             1                   ***0***
    321             1                   ***0***
    322             1                   ***0***
    323             1                   ***0***
Branch totals: 0 hits of 15 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
```

```
    310                                 ***0***     Count coming in to IF
    310             2                   ***0***
    310             3                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch------------------------------------
    312                                 ***0***     Count coming in to IF
    312             1                   ***0***
    312             2                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch------------------------------------
    319                                 ***0***     Count coming in to IF
    319             2                   ***0***
    319             3                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch------------------------------------
    320                                 ***0***     Count coming in to IF
    320             2                   ***0***
    320             3                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch------------------------------------
    321                                 ***0***     Count coming in to IF
    321             2                   ***0***
    321             3                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch------------------------------------
    322                                 ***0***     Count coming in to IF
    322             2                   ***0***
    322             3                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%


Condition Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Conditions                      65         5        60     7.69%

================================Condition Details================================

Condition Coverage for Design Unit work.coverage_sv_unit --

  File transaction.sv
```

```
----------------Focused Condition View-------------------
Line       243 Item    1  (rs1 < rs2)
Condition totals: 1 of 1 input term covered = 100.00%

   Input Term   Covered  Reason for no coverage   Hint
  -----------  --------  ----------------------  --------------
  (rs1 < rs2)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (rs1 < rs2)_0         -
  Row   2:          1  (rs1 < rs2)_1         -

----------------Focused Condition View-------------------
Line       244 Item    1  (rs1 < rs2)
Condition totals: 1 of 1 input term covered = 100.00%

   Input Term   Covered  Reason for no coverage   Hint
  -----------  --------  ----------------------  --------------
  (rs1 < rs2)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (rs1 < rs2)_0         -
  Row   2:          1  (rs1 < rs2)_1         -

----------------Focused Condition View-------------------
Line       245 Item    1  (rs1 == rs2)
Condition totals: 1 of 1 input term covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  ----------------------  --------------
  (rs1 == rs2)         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  (rs1 == rs2)_0        -
  Row   2:          1  (rs1 == rs2)_1        -

----------------Focused Condition View-------------------
Line       246 Item    1  (rs1 != rs2)
Condition totals: 0 of 1 input term covered = 0.00%

    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  ----------------------  --------------
  (rs1 != rs2)         N  '_0' not hit            Hit '_0'
```

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(rs1 != rs2)_0	-
Row 2:	1	(rs1 != rs2)_1	-

----------Focused Condition View----------
Line 248 Item 1 (rs1 >= rs2)
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(rs1 >= rs2)	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(rs1 >= rs2)_0	-
Row 2:	1	(rs1 >= rs2)_1	-

----------Focused Condition View----------
Line 249 Item 1 (rs1 >= rs2)
Condition totals: 1 of 1 input term covered = 100.00%

Input Term	Covered	Reason for no coverage	Hint
(rs1 >= rs2)	Y		

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	1	(rs1 >= rs2)_0	-
Row 2:	1	(rs1 >= rs2)_1	-

----------Focused Condition View----------
Line 160 Item 1 ((rst_n === 1'b0) && (tx.o_exception !== 0) && (tx.o_ce !== 1'b0) && (tx.o_stall_from_alu !== 1'b0))
Condition totals: 0 of 4 input terms covered = 0.00%

Input Term	Covered	Reason for no coverage	Hint
(rst_n === 1'b0)	N	No hits	Hit '_0' and '_1'
(tx.o_exception !== 0)	N	No hits	Hit '_0' and '_1'

```
             (tx.o_ce !== 1'b0)        N  No hits                  Hit '_0' and '_1'
  (tx.o_stall_from_alu !== 1'b0)       N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target                        Non-masking condition(s)
 ---------  ---------  --------------------              ------------------------
  Row   1:    ***0***  (rst_n === 1'b0)_0                -
  Row   2:    ***0***  (rst_n === 1'b0)_1                     ((tx.o_exception !== 0) &&
((tx.o_ce !== 1'b0) && (tx.o_stall_from_alu !== 1'b0)))
  Row   3:    ***0***  (tx.o_exception !== 0)_0          (rst_n === 1'b0)
  Row   4:    ***0***  (tx.o_exception !== 0)_1           ((rst_n === 1'b0) && ((tx.o_ce
!== 1'b0) && (tx.o_stall_from_alu !== 1'b0)))
  Row   5:    ***0***  (tx.o_ce !== 1'b0)_0                   ((rst_n === 1'b0) &&
(tx.o_exception !== 0))
  Row   6:    ***0***  (tx.o_ce !== 1'b0)_1                   ((rst_n === 1'b0) &&
(tx.o_exception !== 0) && (tx.o_stall_from_alu !== 1'b0))
  Row   7:    ***0***  (tx.o_stall_from_alu !== 1'b0)_0   ((rst_n === 1'b0) &&
(tx.o_exception !== 0) && (tx.o_ce !== 1'b0))
  Row   8:    ***0***  (tx.o_stall_from_alu !== 1'b0)_1   ((rst_n === 1'b0) &&
(tx.o_exception !== 0) && (tx.o_ce !== 1'b0))

----------------Focused Condition View-------------------
Line       165 Item    1  (opcode[5] || opcode[8])
Condition totals: 0 of 2 input terms covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
  opcode[5]         N  No hits                  Hit '_0' and '_1'
  opcode[8]         N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  opcode[5]_0           ~opcode[8]
  Row   2:    ***0***  opcode[5]_1           -
  Row   3:    ***0***  opcode[8]_0           ~opcode[5]
  Row   4:    ***0***  opcode[8]_1           ~opcode[5]

----------------Focused Condition View-------------------
Line       166 Item    1  (opcode[0] || opcode[4])
Condition totals: 0 of 2 input terms covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
  opcode[0]         N  No hits                  Hit '_0' and '_1'
  opcode[4]         N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
```

```
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  opcode[0]_0           ~opcode[4]
  Row   2:    ***0***  opcode[0]_1           -
  Row   3:    ***0***  opcode[4]_0           ~opcode[0]
  Row   4:    ***0***  opcode[4]_1           ~opcode[0]

----------------Focused Condition View-------------------
Line       172 Item    1  (opcode[0] || opcode[1])
Condition totals: 0 of 2 input terms covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
   opcode[0]         N  No hits                 Hit '_0' and '_1'
   opcode[1]         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  opcode[0]_0           ~opcode[1]
  Row   2:    ***0***  opcode[0]_1           -
  Row   3:    ***0***  opcode[1]_0           ~opcode[0]
  Row   4:    ***0***  opcode[1]_1           ~opcode[0]

----------------Focused Condition View-------------------
Line       177 Item    1  (opcode[4] && out && (((pc + imm) !== tx.o_next_pc) || (ce !==
tx.o_change_pc) || (ce !== tx.o_flush)))
Condition totals: 0 of 1 input term covered = 0.00%


      Input Term   Covered  Reason for no coverage   Hint

     -----------  --------  ----------------------  --------------
  (opcode[4] && out && (((pc + imm) !== tx.o_next_pc) || (ce !== tx.o_change_pc) || (ce
!== tx.o_flush)))         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target
                                          Non-masking condition(s)
 ---------  ---------  --------------------
                                          -------------------------
  Row   1:    ***0***  (opcode[4] && out && (((pc + imm) !== tx.o_next_pc) || (ce !==
tx.o_change_pc) || (ce !== tx.o_flush)))_0  -
  Row   2:    ***0***  (opcode[4] && out && (((pc + imm) !== tx.o_next_pc) || (ce !==
tx.o_change_pc) || (ce !== tx.o_flush)))_1  -

----------------Focused Condition View-------------------
Line       187 Item    1  (opcode[5] || opcode[6])
Condition totals: 0 of 2 input terms covered = 0.00%
```

```
  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
   opcode[5]         N  No hits                 Hit '_0' and '_1'
   opcode[6]         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  opcode[5]_0           ~opcode[6]
  Row   2:    ***0***  opcode[5]_1           -
  Row   3:    ***0***  opcode[6]_0           ~opcode[5]
  Row   4:    ***0***  opcode[6]_1           ~opcode[5]

----------------Focused Condition View-------------------
Line       188 Item    1  (opcode[6] === 1'b1)
Condition totals: 0 of 1 input term covered = 0.00%

            Input Term   Covered  Reason for no coverage   Hint
           -----------  --------  ----------------------  --------------
  (opcode[6] === 1'b1)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target              Non-masking condition(s)
 ---------  ---------  --------------------    -------------------------
  Row   1:    ***0***  (opcode[6] === 1'b1)_0  -
  Row   2:    ***0***  (opcode[6] === 1'b1)_1  -

----------------Focused Condition View-------------------
Line        191 Item    1  ((sum !== tx.o_next_pc) || (ce !== tx.o_change_pc) || (ce !==
tx.o_flush))
Condition totals: 0 of 3 input terms covered = 0.00%

               Input Term   Covered  Reason for no coverage   Hint
              -----------  --------  ----------------------  --------------
   (sum !== tx.o_next_pc)         N  No hits                 Hit '_0' and '_1'
  (ce !== tx.o_change_pc)         N  No hits                 Hit '_0' and '_1'
      (ce !== tx.o_flush)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target                 Non-masking condition(s)
 ---------  ---------  --------------------       -------------------------
   Row   1:    ***0***  (sum !== tx.o_next_pc)_0   ~((ce !== tx.o_change_pc) || (ce !==
tx.o_flush))
  Row   2:    ***0***  (sum !== tx.o_next_pc)_1   -
   Row   3:    ***0***  (ce !== tx.o_change_pc)_0  (~(sum !== tx.o_next_pc) && ~(ce !==
tx.o_flush))
  Row   4:    ***0***  (ce !== tx.o_change_pc)_1  ~(sum !== tx.o_next_pc)
   Row   5:    ***0***  (ce !== tx.o_flush)_0      (~(sum !== tx.o_next_pc) && ~(ce !==
```

```
tx.o_change_pc))
  Row    6:     ***0***  (ce !== tx.o_flush)_1       (~(sum !== tx.o_next_pc) && ~(ce !==
tx.o_change_pc))

----------------Focused Condition View-------------------
Line       211 Item    1  (((opcode[4] || opcode[3]) || (opcode[9] && (funct3 == 0))) ||
opcode[10])
Condition totals: 0 of 5 input terms covered = 0.00%

     Input Term   Covered  Reason for no coverage   Hint
    -----------  --------  ----------------------  --------------
      opcode[4]         N  No hits                 Hit '_0' and '_1'
      opcode[3]         N  No hits                 Hit '_0' and '_1'
      opcode[9]         N  No hits                 Hit '_0' and '_1'
  (funct3 == 0)         N  No hits                 Hit '_0' and '_1'
     opcode[10]         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row    1:     ***0***  opcode[4]_0           (~opcode[10] && ~(opcode[9] && (funct3 ==
0)) && ~opcode[3])
  Row    2:     ***0***  opcode[4]_1           -
  Row    3:     ***0***  opcode[3]_0           (~opcode[10] && ~(opcode[9] && (funct3 ==
0)) && ~opcode[4])
  Row    4:     ***0***  opcode[3]_1           ~opcode[4]
  Row    5:     ***0***  opcode[9]_0           (~opcode[10] && ~(opcode[4] || opcode[3]))
  Row    6:     ***0***  opcode[9]_1            (~(opcode[4] || opcode[3]) && (funct3 ==
0))
  Row    7:     ***0***  (funct3 == 0)_0        (~opcode[10] && ~(opcode[4] || opcode[3])
&& opcode[9])
  Row    8:     ***0***  (funct3 == 0)_1       (~(opcode[4] || opcode[3]) && opcode[9])
  Row    9:     ***0***  opcode[10]_0          ~((opcode[4] || opcode[3]) || (opcode[9] &&
(funct3 == 0)))
 Row   10:     ***0***  opcode[10]_1          ~((opcode[4] || opcode[3]) || (opcode[9] &&
(funct3 == 0)))

----------------Focused Condition View-------------------
Line       218 Item    1  (opcode[2] || (opcode[9] && (funct3 != 0)))
Condition totals: 0 of 3 input terms covered = 0.00%

     Input Term   Covered  Reason for no coverage   Hint
    -----------  --------  ----------------------  --------------
      opcode[2]         N  No hits                 Hit '_0' and '_1'
      opcode[9]         N  No hits                 Hit '_0' and '_1'
  (funct3 != 0)         N  No hits                 Hit '_0' and '_1'
```

```
     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  opcode[2]_0           ~(opcode[9] && (funct3 != 0))
  Row   2:    ***0***  opcode[2]_1           -
  Row   3:    ***0***  opcode[9]_0           ~opcode[2]
  Row   4:    ***0***  opcode[9]_1           (~opcode[2] && (funct3 != 0))
  Row   5:    ***0***  (funct3 != 0)_0       (~opcode[2] && opcode[9])
  Row   6:    ***0***  (funct3 != 0)_1       (~opcode[2] && opcode[9])

----------------Focused Condition View-------------------
Line       221 Item    1  ((tx.o_stall !== (stall || force_stall)) && ~flush)
Condition totals: 0 of 2 input terms covered = 0.00%

                              Input Term   Covered  Reason for no coverage   Hint
                                        -----------   --------   -----------------------
--------------
  (tx.o_stall !== (stall || force_stall))          N  No hits                    Hit '_0'
and '_1'
                                       flush          N  No hits                    Hit '_0'
and '_1'

      Rows:         Hits   FEC Target                                          Non-masking
condition(s)
  ---------    ---------    --------------------
-------------------------
  Row   1:    ***0***  (tx.o_stall !== (stall || force_stall))_0  -

  Row   2:    ***0***  (tx.o_stall !== (stall || force_stall))_1  ~flush

  Row   3:    ***0***  flush_0                                    (tx.o_stall !== (stall
|| force_stall))
  Row   4:    ***0***  flush_1                                    (tx.o_stall !== (stall
|| force_stall))

----------------Focused Condition View-------------------
Line       226 Item    1  (~(tx.o_stall || stall) && (ce === 1'b1))
Condition totals: 0 of 3 input terms covered = 0.00%

     Input Term   Covered  Reason for no coverage   Hint
    -----------  --------  -----------------------  --------------
     tx.o_stall         N  No hits                  Hit '_0' and '_1'
          stall         N  No hits                  Hit '_0' and '_1'
  (ce === 1'b1)         N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
```

```
  Row   1:    ***0***  tx.o_stall_0          ((ce === 1'b1) && ~stall)
  Row   2:    ***0***  tx.o_stall_1          -
  Row   3:    ***0***  stall_0              ((ce === 1'b1) && ~tx.o_stall)
  Row   4:    ***0***  stall_1              ~tx.o_stall
  Row   5:    ***0***  (ce === 1'b1)_0      ~(tx.o_stall || stall)
  Row   6:    ***0***  (ce === 1'b1)_1      ~(tx.o_stall || stall)

----------------Focused Condition View-------------------
Line       227 Item    1  ((opcode !== tx.o_opcode) || (exception !== tx.o_exception) ||
(out !== tx.o_y) || (rs1_addr !== tx.o_rs1_addr) || (rs1 !== tx.o_rs1) || (rs2 !==
tx.o_rs2) || (rd_addr !== tx.o_rd_addr) || (imm !== tx.o_imm) || (funct3 !==
tx.o_funct3) || (rd_d !== tx.o_rd) || (rd_valid !== tx.o_rd_valid) || (wr_rd_d !==
tx.o_wr_rd) || ((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc))
Condition totals: 0 of 14 input terms covered = 0.00%

                                          Input Term   Covered  Reason for no coverage
Hint
                                         -----------  --------  ----------------------
--------------
                           (opcode !== tx.o_opcode)         N  No hits
Hit '_0' and '_1'
                      (exception !== tx.o_exception)         N  No hits
Hit '_0' and '_1'
                                (out !== tx.o_y)         N  No hits
Hit '_0' and '_1'
                        (rs1_addr !== tx.o_rs1_addr)         N  No hits
Hit '_0' and '_1'
                                (rs1 !== tx.o_rs1)         N  No hits
Hit '_0' and '_1'
                                (rs2 !== tx.o_rs2)         N  No hits
Hit '_0' and '_1'
                          (rd_addr !== tx.o_rd_addr)         N  No hits
Hit '_0' and '_1'
                                (imm !== tx.o_imm)         N  No hits
Hit '_0' and '_1'
                           (funct3 !== tx.o_funct3)         N  No hits
Hit '_0' and '_1'
                                (rd_d !== tx.o_rd)         N  No hits
Hit '_0' and '_1'
                       (rd_valid !== tx.o_rd_valid)         N  No hits
Hit '_0' and '_1'
                           (wr_rd_d !== tx.o_wr_rd)         N  No hits
Hit '_0' and '_1'
  ((opcode[3] || opcode[2]) == tx.o_stall_from_alu)         N  No hits
Hit '_0' and '_1'
                                  (pc !== tx.o_pc)         N  No hits
```

Hit '_0' and '_1'

Rows:	Hits	FEC Target	Non-masking condition(s)
Row 1:	***0***	(opcode !== tx.o_opcode)_0	~((exception !== tx.o_exception) || ((out !== tx.o_y) || ((rs1_addr !== tx.o_rs1_addr) || ((rs1 !== tx.o_rs1) || ((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !== tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc))))))))))))
Row 2:	***0***	(opcode !== tx.o_opcode)_1	-
Row 3:	***0***	(exception !== tx.o_exception)_0	(~(opcode !== tx.o_opcode) && ~((out !== tx.o_y) || ((rs1_addr !== tx.o_rs1_addr) || ((rs1 !== tx.o_rs1) || ((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !== tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc))))))))))))
Row 4:	***0***	(exception !== tx.o_exception)_1	~(opcode !== tx.o_opcode)
Row 5:	***0***	(out !== tx.o_y)_0	(~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~((rs1_addr !== tx.o_rs1_addr) || ((rs1 !== tx.o_rs1) || ((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !== tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc))))))))))))
Row 6:	***0***	(out !== tx.o_y)_1	(~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception))
Row 7:	***0***	(rs1_addr !== tx.o_rs1_addr)_0	(~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~((rs1 !== tx.o_rs1) || ((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !== tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc))))))))))))
Row 8:	***0***	(rs1_addr !== tx.o_rs1_addr)_1	(~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y))
Row 9:	***0***	(rs1 !== tx.o_rs1)_0	(~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~((rs2 !== tx.o_rs2) || ((rd_addr !== tx.o_rd_addr) || ((imm !== tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc)))))))))))
Row 10:	***0***	(rs1 !== tx.o_rs1)_1	(~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr

!== tx.o_rs1_addr))

Row 11: ***0*** (rs2 !== tx.o_rs2)_0 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~((rd_addr !== tx.o_rd_addr) || ((imm !== tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc)))))))))

Row 12: ***0*** (rs2 !== tx.o_rs2)_1 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1))

Row 13: ***0*** (rd_addr !== tx.o_rd_addr)_0 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~((imm !== tx.o_imm) || ((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc)))))))

Row 14: ***0*** (rd_addr !== tx.o_rd_addr)_1 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2))

Row 15: ***0*** (imm !== tx.o_imm)_0 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~((funct3 !== tx.o_funct3) || ((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc)))))))

Row 16: ***0*** (imm !== tx.o_imm)_1 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr))

Row 17: ***0*** (funct3 !== tx.o_funct3)_0 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~((rd_d !== tx.o_rd) || ((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc))))))

Row 18: ***0*** (funct3 !== tx.o_funct3)_1 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm))

Row 19: ***0*** (rd_d !== tx.o_rd)_0 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~((rd_valid !== tx.o_rd_valid) || ((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc)))))

Row 20: ***0*** (rd_d !== tx.o_rd)_1 (~(opcode

!== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3))

Row 21: ***0*** (rd_valid !== tx.o_rd_valid)_0 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd) && ~((wr_rd_d !== tx.o_wr_rd) || (((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc))))

Row 22: ***0*** (rd_valid !== tx.o_rd_valid)_1 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd))

Row 23: ***0*** (wr_rd_d !== tx.o_wr_rd)_0 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd) && ~(rd_valid !== tx.o_rd_valid) && ~(((opcode[3] || opcode[2]) == tx.o_stall_from_alu) || (pc !== tx.o_pc)))

Row 24: ***0*** (wr_rd_d !== tx.o_wr_rd)_1 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd) && ~(rd_valid !== tx.o_rd_valid))

Row 25: ***0*** ((opcode[3] || opcode[2]) == tx.o_stall_from_alu)_0 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd) && ~(rd_valid !== tx.o_rd_valid) && ~(wr_rd_d !== tx.o_wr_rd) && ~(pc !== tx.o_pc))

Row 26: ***0*** ((opcode[3] || opcode[2]) == tx.o_stall_from_alu)_1 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd) && ~(rd_valid !== tx.o_rd_valid) && ~(wr_rd_d !== tx.o_wr_rd))

Row 27: ***0*** (pc !== tx.o_pc)_0 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd) && ~(rd_valid !== tx.o_rd_valid) && ~(wr_rd_d !== tx.o_wr_rd) && ~((opcode[3] || opcode[2]) == tx.o_stall_from_alu))

Row 28: ***0*** (pc !== tx.o_pc)_1 (~(opcode !== tx.o_opcode) && ~(exception !== tx.o_exception) && ~(out !== tx.o_y) && ~(rs1_addr !== tx.o_rs1_addr) && ~(rs1 !== tx.o_rs1) && ~(rs2 !== tx.o_rs2) && ~(rd_addr !== tx.o_rd_addr) && ~(imm !== tx.o_imm) && ~(funct3 !== tx.o_funct3) && ~(rd_d !== tx.o_rd) && ~(rd_valid !== tx.o_rd_valid) && ~(wr_rd_d !== tx.o_wr_rd) && ~((opcode[3] ||

```
opcode[2]) == tx.o_stall_from_alu))

----------------Focused Condition View-------------------
Line       247 Item    1  (flush && ~(tx.o_stall || stall) && (tx.o_ce !== 1'b0))
Condition totals: 0 of 4 input terms covered = 0.00%

          Input Term   Covered  Reason for no coverage   Hint
         -----------  --------  ----------------------  --------------
               flush         N  No hits                 Hit '_0' and '_1'
          tx.o_stall         N  No hits                 Hit '_0' and '_1'
               stall         N  No hits                 Hit '_0' and '_1'
  (tx.o_ce !== 1'b0)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  flush_0               -
  Row   2:    ***0***  flush_1               (~(tx.o_stall || stall) && (tx.o_ce !==
1'b0))
  Row   3:    ***0***  tx.o_stall_0          (flush && (tx.o_ce !== 1'b0) && ~stall)
  Row   4:    ***0***  tx.o_stall_1          flush
  Row   5:    ***0***  stall_0               (flush && (tx.o_ce !== 1'b0) &&
~tx.o_stall)
  Row   6:    ***0***  stall_1               (flush && ~tx.o_stall)
  Row   7:    ***0***  (tx.o_ce !== 1'b0)_0  (flush && ~(tx.o_stall || stall))
  Row   8:    ***0***  (tx.o_ce !== 1'b0)_1  (flush && ~(tx.o_stall || stall))

----------------Focused Condition View-------------------
Line       249 Item    1  (~(tx.o_stall || stall) && (tx.o_ce !== ce))
Condition totals: 0 of 3 input terms covered = 0.00%

        Input Term   Covered  Reason for no coverage   Hint
       -----------  --------  ----------------------  --------------
        tx.o_stall         N  No hits                 Hit '_0' and '_1'
             stall         N  No hits                 Hit '_0' and '_1'
  (tx.o_ce !== ce)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  tx.o_stall_0          ((tx.o_ce !== ce) && ~stall)
  Row   2:    ***0***  tx.o_stall_1          -
  Row   3:    ***0***  stall_0               ((tx.o_ce !== ce) && ~tx.o_stall)
  Row   4:    ***0***  stall_1               ~tx.o_stall
  Row   5:    ***0***  (tx.o_ce !== ce)_0    ~(tx.o_stall || stall)
  Row   6:    ***0***  (tx.o_ce !== ce)_1    ~(tx.o_stall || stall)

----------------Focused Condition View-------------------
```

```
Line       251 Item    1  (tx.o_stall && (tx.o_ce !== 1'b0))
Condition totals: 0 of 2 input terms covered = 0.00%

          Input Term   Covered  Reason for no coverage   Hint
         -----------  --------  ----------------------  --------------
          tx.o_stall         N  No hits                  Hit '_0' and '_1'
  (tx.o_ce !== 1'b0)         N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  tx.o_stall_0          -
  Row   2:    ***0***  tx.o_stall_1          (tx.o_ce !== 1'b0)
  Row   3:    ***0***  (tx.o_ce !== 1'b0)_0  tx.o_stall
  Row   4:    ***0***  (tx.o_ce !== 1'b0)_1  tx.o_stall

----------------Focused Condition View-------------------
Line       310 Item    1  (a < b)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
     (a < b)         N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (a < b)_0             -
  Row   2:    ***0***  (a < b)_1             -

----------------Focused Condition View-------------------
Line       312 Item    1  (a < b)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
     (a < b)         N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (a < b)_0             -
  Row   2:    ***0***  (a < b)_1             -

----------------Focused Condition View-------------------
Line       319 Item    1  (a == b)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
```

```
 -----------  --------  ----------------------  --------------
    (a == b)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (a == b)_0            -
  Row   2:    ***0***  (a == b)_1            -

----------------Focused Condition View-------------------
Line       320 Item    1  (a != b)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
    (a != b)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (a != b)_0            -
  Row   2:    ***0***  (a != b)_1            -

----------------Focused Condition View-------------------
Line       321 Item    1  (a >= b)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
    (a >= b)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (a >= b)_0            -
  Row   2:    ***0***  (a >= b)_1            -

----------------Focused Condition View-------------------
Line       322 Item    1  (a >= b)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
    (a >= b)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (a >= b)_0            -
  Row   2:    ***0***  (a >= b)_1            -
```

```
Covergroup Coverage:
    Covergroups                     1        na        na    34.81%
        Coverpoints/Crosses        20        na        na        na
            Covergroup Bins      5315        51      5264     0.95%
--------------------------------------------------------------------------------
-----------------
Covergroup                                          Metric       Goal       Bins
Status


--------------------------------------------------------------------------------
-----------------
 TYPE work.coverage_sv_unit::coverage/alu_cg          34.81%        100          -
Uncovered
    covered/total bins:                                 51       5315          -

    missing/total bins:                               5264       5315          -

    % Hit:                                           0.95%        100          -

    type_option.weight=1
    type_option.goal=100
    type_option.comment=
    type_option.strobe=0
    type_option.merge_instances=auto(1)
    Coverpoint #coverpoint__0#                       45.45%        100          -
Uncovered
        covered/total bins:                             5          11          -

        missing/total bins:                             6          11          -

        % Hit:                                      45.45%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin opcode_types[0]                             3           1          -
Covered
        bin opcode_types[1]                            20           1          -
Covered
        bin opcode_types[2]                             1           1          -
Covered
        bin opcode_types[3]                             0           1          -
```

```
ZERO
        bin opcode_types[4]                                  6          1          -
Covered
        bin opcode_types[5]                                  0          1          -
ZERO
        bin opcode_types[6]                                  0          1          -
ZERO
        bin opcode_types[7]                                  0          1          -
ZERO
        bin opcode_types[8]                                  5          1          -
Covered
        bin opcode_types[9]                                  0          1          -
ZERO
        bin opcode_types[10]                                 0          1          -
ZERO
    Coverpoint #coverpoint__1#                           28.57%        100          -
Uncovered
        covered/total bins:                                  4         14          -

        missing/total bins:                                 10         14          -

        % Hit:                                           28.57%       100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin alu_ops[0]                                       0          1          -
ZERO
        bin alu_ops[1]                                      11          1          -
Covered
        bin alu_ops[2]                                       4          1          -
Covered
        bin alu_ops[3]                                       0          1          -
ZERO
        bin alu_ops[4]                                       1          1          -
Covered
        bin alu_ops[5]                                       0          1          -
ZERO
        bin alu_ops[6]                                       0          1          -
ZERO
        bin alu_ops[7]                                       0          1          -
ZERO
        bin alu_ops[8]                                       3          1          -
Covered
        bin alu_ops[9]                                       0          1          -
ZERO
```

```
        bin alu_ops[10]                                  0          1          -
ZERO
        bin alu_ops[11]                                  0          1          -
ZERO
        bin alu_ops[12]                                  0          1          -
ZERO
        bin alu_ops[13]                                  0          1          -
ZERO
    Coverpoint #coverpoint__2#                      100.00%        100          -
Covered
        covered/total bins:                              2          2          -

        missing/total bins:                              0          2          -

        % Hit:                                      100.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                     55          1          -
Covered
        bin auto[1]                                     10          1          -
Covered
    Coverpoint #coverpoint__3#                      100.00%        100          -
Covered
        covered/total bins:                              1          1          -

        missing/total bins:                              0          1          -

        % Hit:                                      100.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin pc_values                                   65          1          -
Covered
    Coverpoint #coverpoint__4#                        0.00%        100          -
ZERO
        covered/total bins:                              0          2          -

        missing/total bins:                              2          2          -

        % Hit:                                        0.00%        100          -

        type_option.weight=1
        type_option.goal=100
```

```
        type_option.comment=
        bin auto[0]                                    0          1          -
ZERO
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__5#                      0.00%       100          -
ZERO
        covered/total bins:                            0          2          -

        missing/total bins:                            2          2          -

        % Hit:                                      0.00%       100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                    0          1          -
ZERO
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__6#                      0.00%       100          -
ZERO
        covered/total bins:                            0          1          -

        missing/total bins:                            1          1          -

        % Hit:                                      0.00%       100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin rd_addr                                    0          1          -
ZERO
    Coverpoint #coverpoint__7#                     50.00%       100          -
Uncovered
        covered/total bins:                            1          2          -

        missing/total bins:                            1          2          -

        % Hit:                                     50.00%       100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                    0          1          -
ZERO
```

```
        bin auto[1]                                  65          1          -
Covered
    Coverpoint #coverpoint__8#                    50.00%        100          -
Uncovered
        covered/total bins:                           1          2          -

        missing/total bins:                           1          2          -

        % Hit:                                    50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                  65          1          -
Covered
        bin auto[1]                                   0          1          -
ZERO
    Coverpoint #coverpoint__9#                    50.00%        100          -
Uncovered
        covered/total bins:                           1          2          -

        missing/total bins:                           1          2          -

        % Hit:                                    50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                  65          1          -
Covered
        bin auto[1]                                   0          1          -
ZERO
    Coverpoint #coverpoint__10#                   50.00%        100          -
Uncovered
        covered/total bins:                           1          2          -

        missing/total bins:                           1          2          -

        % Hit:                                    50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                  65          1          -
Covered
        bin auto[1]                                   0          1          -
```

```
ZERO
    Coverpoint #coverpoint__11#                    50.00%        100          -
Uncovered
        covered/total bins:                            1          2          -

        missing/total bins:                            1          2          -

        % Hit:                                     50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                   65          1          -
Covered
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__12#                    50.00%        100          -
Uncovered
        covered/total bins:                            1          2          -

        missing/total bins:                            1          2          -

        % Hit:                                     50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                   65          1          -
Covered
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__13#                   100.00%        100          -
Covered
        covered/total bins:                            2          2          -

        missing/total bins:                            0          2          -

        % Hit:                                    100.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                   55          1          -
Covered
        bin auto[1]                                   10          1          -
Covered
```

```
    Coverpoint #coverpoint__14#                          0.00%        100          -
ZERO
        covered/total bins:                                 0          4          -

        missing/total bins:                                 4          4          -

        % Hit:                                          0.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin exceptions[0]                                   0          1          -
ZERO
        bin exceptions[1]                                   0          1          -
ZERO
        bin exceptions[2]                                   0          1          -
ZERO
        bin exceptions[3]                                   0          1          -
ZERO
    Coverpoint #vif.i_opcode__15#                        10.93%        100          -
Uncovered
        covered/total bins:                                 7         64          -

        missing/total bins:                                57         64          -

        % Hit:                                          10.93%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0:31]                                     41          1          -
Covered
        bin auto[32:63]                                     4          1          -
Covered
        bin auto[64:95]                                     3          1          -
Covered
        bin auto[96:127]                                    0          1          -
ZERO
        bin auto[128:159]                                   3          1          -
Covered
        bin auto[160:191]                                   0          1          -
ZERO
        bin auto[192:223]                                   0          1          -
ZERO
        bin auto[224:255]                                   0          1          -
ZERO
```

```
        bin auto[256:287]                                  7          1          -
Covered
        bin auto[288:319]                                  0          1          -
ZERO
        bin auto[320:351]                                  0          1          -
ZERO
        bin auto[352:383]                                  0          1          -
ZERO
        bin auto[384:415]                                  0          1          -
ZERO
        bin auto[416:447]                                  0          1          -
ZERO
        bin auto[448:479]                                  0          1          -
ZERO
        bin auto[480:511]                                  0          1          -
ZERO
        bin auto[512:543]                                  6          1          -
Covered
        bin auto[544:575]                                  0          1          -
ZERO
        bin auto[576:607]                                  0          1          -
ZERO
        bin auto[608:639]                                  0          1          -
ZERO
        bin auto[640:671]                                  0          1          -
ZERO
        bin auto[672:703]                                  0          1          -
ZERO
        bin auto[704:735]                                  0          1          -
ZERO
        bin auto[736:767]                                  0          1          -
ZERO
        bin auto[768:799]                                  0          1          -
ZERO
        bin auto[800:831]                                  0          1          -
ZERO
        bin auto[832:863]                                  0          1          -
ZERO
        bin auto[864:895]                                  0          1          -
ZERO
        bin auto[896:927]                                  0          1          -
ZERO
        bin auto[928:959]                                  0          1          -
ZERO
        bin auto[960:991]                                  0          1          -
ZERO
```

```
        bin auto[992:1023]                                  0          1          -
ZERO
        bin auto[1024:1055]                                 1          1          -
Covered
        bin auto[1056:1087]                                 0          1          -
ZERO
        bin auto[1088:1119]                                 0          1          -
ZERO
        bin auto[1120:1151]                                 0          1          -
ZERO
        bin auto[1152:1183]                                 0          1          -
ZERO
        bin auto[1184:1215]                                 0          1          -
ZERO
        bin auto[1216:1247]                                 0          1          -
ZERO
        bin auto[1248:1279]                                 0          1          -
ZERO
        bin auto[1280:1311]                                 0          1          -
ZERO
        bin auto[1312:1343]                                 0          1          -
ZERO
        bin auto[1344:1375]                                 0          1          -
ZERO
        bin auto[1376:1407]                                 0          1          -
ZERO
        bin auto[1408:1439]                                 0          1          -
ZERO
        bin auto[1440:1471]                                 0          1          -
ZERO
        bin auto[1472:1503]                                 0          1          -
ZERO
        bin auto[1504:1535]                                 0          1          -
ZERO
        bin auto[1536:1567]                                 0          1          -
ZERO
        bin auto[1568:1599]                                 0          1          -
ZERO
        bin auto[1600:1631]                                 0          1          -
ZERO
        bin auto[1632:1663]                                 0          1          -
ZERO
        bin auto[1664:1695]                                 0          1          -
ZERO
        bin auto[1696:1727]                                 0          1          -
ZERO
```

```
        bin auto[1728:1759]                                  0          1          -
ZERO
        bin auto[1760:1791]                                  0          1          -
ZERO
        bin auto[1792:1823]                                  0          1          -
ZERO
        bin auto[1824:1855]                                  0          1          -
ZERO
        bin auto[1856:1887]                                  0          1          -
ZERO
        bin auto[1888:1919]                                  0          1          -
ZERO
        bin auto[1920:1951]                                  0          1          -
ZERO
        bin auto[1952:1983]                                  0          1          -
ZERO
        bin auto[1984:2015]                                  0          1          -
ZERO
        bin auto[2016:2047]                                  0          1          -
ZERO
    Coverpoint #vif.i_exception__16#                      0.00%        100          -
ZERO
        covered/total bins:                                  0         16          -

        missing/total bins:                                 16         16          -

        % Hit:                                            0.00%       100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                          0          1          -
ZERO
        bin auto[1]                                          0          1          -
ZERO
        bin auto[2]                                          0          1          -
ZERO
        bin auto[3]                                          0          1          -
ZERO
        bin auto[4]                                          0          1          -
ZERO
        bin auto[5]                                          0          1          -
ZERO
        bin auto[6]                                          0          1          -
ZERO
        bin auto[7]                                          0          1          -
```

```
ZERO
        bin auto[8]                                     0          1          -
ZERO
        bin auto[9]                                     0          1          -
ZERO
        bin auto[10]                                    0          1          -
ZERO
        bin auto[11]                                    0          1          -
ZERO
        bin auto[12]                                    0          1          -
ZERO
        bin auto[13]                                    0          1          -
ZERO
        bin auto[14]                                    0          1          -
ZERO
        bin auto[15]                                    0          1          -
ZERO
    Coverpoint #vif.i_alu__17#                      10.93%        100          -
Uncovered
        covered/total bins:                             7         64          -

        missing/total bins:                            57         64          -

        % Hit:                                      10.93%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0:255]                                39          1          -
Covered
        bin auto[256:511]                               8          1          -
Covered
        bin auto[512:767]                               5          1          -
Covered
        bin auto[768:1023]                              0          1          -
ZERO
        bin auto[1024:1279]                             5          1          -
Covered
        bin auto[1280:1535]                             0          1          -
ZERO
        bin auto[1536:1791]                             0          1          -
ZERO
        bin auto[1792:2047]                             0          1          -
ZERO
        bin auto[2048:2303]                             2          1          -
Covered
```

```
        bin auto[2304:2559]                                 0          1          -
ZERO
        bin auto[2560:2815]                                 0          1          -
ZERO
        bin auto[2816:3071]                                 0          1          -
ZERO
        bin auto[3072:3327]                                 0          1          -
ZERO
        bin auto[3328:3583]                                 0          1          -
ZERO
        bin auto[3584:3839]                                 0          1          -
ZERO
        bin auto[3840:4095]                                 0          1          -
ZERO
        bin auto[4096:4351]                                 3          1          -
Covered
        bin auto[4352:4607]                                 0          1          -
ZERO
        bin auto[4608:4863]                                 0          1          -
ZERO
        bin auto[4864:5119]                                 0          1          -
ZERO
        bin auto[5120:5375]                                 0          1          -
ZERO
        bin auto[5376:5631]                                 0          1          -
ZERO
        bin auto[5632:5887]                                 0          1          -
ZERO
        bin auto[5888:6143]                                 0          1          -
ZERO
        bin auto[6144:6399]                                 0          1          -
ZERO
        bin auto[6400:6655]                                 0          1          -
ZERO
        bin auto[6656:6911]                                 0          1          -
ZERO
        bin auto[6912:7167]                                 0          1          -
ZERO
        bin auto[7168:7423]                                 0          1          -
ZERO
        bin auto[7424:7679]                                 0          1          -
ZERO
        bin auto[7680:7935]                                 0          1          -
ZERO
        bin auto[7936:8191]                                 0          1          -
ZERO
```

```
        bin auto[8192:8447]                                3          1          -
Covered
        bin auto[8448:8703]                                0          1          -
ZERO
        bin auto[8704:8959]                                0          1          -
ZERO
        bin auto[8960:9215]                                0          1          -
ZERO
        bin auto[9216:9471]                                0          1          -
ZERO
        bin auto[9472:9727]                                0          1          -
ZERO
        bin auto[9728:9983]                                0          1          -
ZERO
        bin auto[9984:10239]                               0          1          -
ZERO
        bin auto[10240:10495]                              0          1          -
ZERO
        bin auto[10496:10751]                              0          1          -
ZERO
        bin auto[10752:11007]                              0          1          -
ZERO
        bin auto[11008:11263]                              0          1          -
ZERO
        bin auto[11264:11519]                              0          1          -
ZERO
        bin auto[11520:11775]                              0          1          -
ZERO
        bin auto[11776:12031]                              0          1          -
ZERO
        bin auto[12032:12287]                              0          1          -
ZERO
        bin auto[12288:12543]                              0          1          -
ZERO
        bin auto[12544:12799]                              0          1          -
ZERO
        bin auto[12800:13055]                              0          1          -
ZERO
        bin auto[13056:13311]                              0          1          -
ZERO
        bin auto[13312:13567]                              0          1          -
ZERO
        bin auto[13568:13823]                              0          1          -
ZERO
        bin auto[13824:14079]                              0          1          -
ZERO
```

```
        bin auto[14080:14335]                                0          1          -
ZERO
        bin auto[14336:14591]                                0          1          -
ZERO
        bin auto[14592:14847]                                0          1          -
ZERO
        bin auto[14848:15103]                                0          1          -
ZERO
        bin auto[15104:15359]                                0          1          -
ZERO
        bin auto[15360:15615]                                0          1          -
ZERO
        bin auto[15616:15871]                                0          1          -
ZERO
        bin auto[15872:16127]                                0          1          -
ZERO
        bin auto[16128:16383]                                0          1          -
ZERO
    Cross #cross__0#                                      0.41%        100          -
Uncovered
        covered/total bins:                                 17       4096          -

        missing/total bins:                               4079       4096          -

        % Hit:                                            0.41%       100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        Auto, Default and User Defined Bins:
            bin <auto[256:287],auto[8192:8447]>              1          1          -
Covered
            bin <auto[0:31],auto[8192:8447]>                 2          1          -
Covered
            bin <auto[0:31],auto[4096:4351]>                 3          1          -
Covered
            bin <auto[512:543],auto[2048:2303]>              2          1          -
Covered
            bin <auto[0:31],auto[1024:1279]>                 5          1          -
Covered
            bin <auto[32:63],auto[512:767]>                  1          1          -
Covered
            bin <auto[0:31],auto[512:767]>                   4          1          -
Covered
            bin <auto[512:543],auto[256:511]>                1          1          -
Covered
```

```
            bin <auto[256:287],auto[256:511]>                1          1           -
Covered
            bin <auto[0:31],auto[256:511]>                   6          1           -
Covered
            bin <auto[1024:1055],auto[0:255]>                1          1           -
Covered
            bin <auto[512:543],auto[0:255]>                  3          1           -
Covered
            bin <auto[256:287],auto[0:255]>                  5          1           -
Covered
            bin <auto[128:159],auto[0:255]>                  3          1           -
Covered
            bin <auto[64:95],auto[0:255]>                    3          1           -
Covered
            bin <auto[32:63],auto[0:255]>                    3          1           -
Covered
            bin <auto[0:31],auto[0:255]>                    21          1           -
Covered
            bin <auto[2016:2047],*>                          0          1          64
ZERO
            bin <auto[1984:2015],*>                          0          1          64
ZERO
            bin <auto[1952:1983],*>                          0          1          64
ZERO
            bin <auto[1920:1951],*>                          0          1          64
ZERO
            bin <auto[1888:1919],*>                          0          1          64
ZERO
            bin <auto[1856:1887],*>                          0          1          64
ZERO
            bin <auto[1824:1855],*>                          0          1          64
ZERO
            bin <auto[1792:1823],*>                          0          1          64
ZERO
            bin <auto[1760:1791],*>                          0          1          64
ZERO
            bin <auto[1728:1759],*>                          0          1          64
ZERO
            bin <auto[1696:1727],*>                          0          1          64
ZERO
            bin <auto[1664:1695],*>                          0          1          64
ZERO
            bin <auto[1632:1663],*>                          0          1          64
ZERO
            bin <auto[1600:1631],*>                          0          1          64
ZERO
```

```
            bin <auto[1568:1599],*>                         0          1          64
ZERO
            bin <auto[1536:1567],*>                         0          1          64
ZERO
            bin <auto[1504:1535],*>                         0          1          64
ZERO
            bin <auto[1472:1503],*>                         0          1          64
ZERO
            bin <auto[1440:1471],*>                         0          1          64
ZERO
            bin <auto[1408:1439],*>                         0          1          64
ZERO
            bin <auto[1376:1407],*>                         0          1          64
ZERO
            bin <auto[1344:1375],*>                         0          1          64
ZERO
            bin <auto[1312:1343],*>                         0          1          64
ZERO
            bin <auto[1280:1311],*>                         0          1          64
ZERO
            bin <auto[1248:1279],*>                         0          1          64
ZERO
            bin <auto[1216:1247],*>                         0          1          64
ZERO
            bin <auto[1184:1215],*>                         0          1          64
ZERO
            bin <auto[1152:1183],*>                         0          1          64
ZERO
            bin <auto[1120:1151],*>                         0          1          64
ZERO
            bin <auto[1088:1119],*>                         0          1          64
ZERO
            bin <auto[1056:1087],*>                         0          1          64
ZERO
            bin <auto[992:1023],*>                          0          1          64
ZERO
            bin <auto[960:991],*>                           0          1          64
ZERO
            bin <auto[928:959],*>                           0          1          64
ZERO
            bin <auto[896:927],*>                           0          1          64
ZERO
            bin <auto[864:895],*>                           0          1          64
ZERO
            bin <auto[832:863],*>                           0          1          64
ZERO
```

```
            bin <auto[800:831],*>                       0          1          64
ZERO
            bin <auto[768:799],*>                       0          1          64
ZERO
            bin <auto[736:767],*>                       0          1          64
ZERO
            bin <auto[704:735],*>                       0          1          64
ZERO
            bin <auto[672:703],*>                       0          1          64
ZERO
            bin <auto[640:671],*>                       0          1          64
ZERO
            bin <auto[608:639],*>                       0          1          64
ZERO
            bin <auto[576:607],*>                       0          1          64
ZERO
            bin <auto[544:575],*>                       0          1          64
ZERO
            bin <auto[480:511],*>                       0          1          64
ZERO
            bin <auto[448:479],*>                       0          1          64
ZERO
            bin <auto[416:447],*>                       0          1          64
ZERO
            bin <auto[384:415],*>                       0          1          64
ZERO
            bin <auto[352:383],*>                       0          1          64
ZERO
            bin <auto[320:351],*>                       0          1          64
ZERO
            bin <auto[288:319],*>                       0          1          64
ZERO
            bin <auto[224:255],*>                       0          1          64
ZERO
            bin <auto[192:223],*>                       0          1          64
ZERO
            bin <auto[160:191],*>                       0          1          64
ZERO
            bin <auto[96:127],*>                        0          1          64
ZERO
            bin <*,auto[16128:16383]>                   0          1          64
ZERO
            bin <*,auto[15872:16127]>                   0          1          64
ZERO
            bin <*,auto[15616:15871]>                   0          1          64
ZERO
```

```
            bin <*,auto[15360:15615]>                    0          1          64
ZERO
            bin <*,auto[15104:15359]>                    0          1          64
ZERO
            bin <*,auto[14848:15103]>                    0          1          64
ZERO
            bin <*,auto[14592:14847]>                    0          1          64
ZERO
            bin <*,auto[14336:14591]>                    0          1          64
ZERO
            bin <*,auto[14080:14335]>                    0          1          64
ZERO
            bin <*,auto[13824:14079]>                    0          1          64
ZERO
            bin <*,auto[13568:13823]>                    0          1          64
ZERO
            bin <*,auto[13312:13567]>                    0          1          64
ZERO
            bin <*,auto[13056:13311]>                    0          1          64
ZERO
            bin <*,auto[12800:13055]>                    0          1          64
ZERO
            bin <*,auto[12544:12799]>                    0          1          64
ZERO
            bin <*,auto[12288:12543]>                    0          1          64
ZERO
            bin <*,auto[12032:12287]>                    0          1          64
ZERO
            bin <*,auto[11776:12031]>                    0          1          64
ZERO
            bin <*,auto[11520:11775]>                    0          1          64
ZERO
            bin <*,auto[11264:11519]>                    0          1          64
ZERO
            bin <*,auto[11008:11263]>                    0          1          64
ZERO
            bin <*,auto[10752:11007]>                    0          1          64
ZERO
            bin <*,auto[10496:10751]>                    0          1          64
ZERO
            bin <*,auto[10240:10495]>                    0          1          64
ZERO
            bin <*,auto[9984:10239]>                     0          1          64
ZERO
            bin <*,auto[9728:9983]>                      0          1          64
ZERO
```

bin <*,auto[9472:9727]> 0 1 64
ZERO
bin <*,auto[9216:9471]> 0 1 64
ZERO
bin <*,auto[8960:9215]> 0 1 64
ZERO
bin <*,auto[8704:8959]> 0 1 64
ZERO
bin <*,auto[8448:8703]> 0 1 64
ZERO
bin <*,auto[7936:8191]> 0 1 64
ZERO
bin <*,auto[7680:7935]> 0 1 64
ZERO
bin <*,auto[7424:7679]> 0 1 64
ZERO
bin <*,auto[7168:7423]> 0 1 64
ZERO
bin <*,auto[6912:7167]> 0 1 64
ZERO
bin <*,auto[6656:6911]> 0 1 64
ZERO
bin <*,auto[6400:6655]> 0 1 64
ZERO
bin <*,auto[6144:6399]> 0 1 64
ZERO
bin <*,auto[5888:6143]> 0 1 64
ZERO
bin <*,auto[5632:5887]> 0 1 64
ZERO
bin <*,auto[5376:5631]> 0 1 64
ZERO
bin <*,auto[5120:5375]> 0 1 64
ZERO
bin <*,auto[4864:5119]> 0 1 64
ZERO
bin <*,auto[4608:4863]> 0 1 64
ZERO
bin <*,auto[4352:4607]> 0 1 64
ZERO
bin <*,auto[3840:4095]> 0 1 64
ZERO
bin <*,auto[3584:3839]> 0 1 64
ZERO
bin <*,auto[3328:3583]> 0 1 64
ZERO

```
            bin <*,auto[3072:3327]>                          0          1          64
ZERO
            bin <*,auto[2816:3071]>                          0          1          64
ZERO
            bin <*,auto[2560:2815]>                          0          1          64
ZERO
            bin <*,auto[2304:2559]>                          0          1          64
ZERO
            bin <*,auto[1792:2047]>                          0          1          64
ZERO
            bin <*,auto[1536:1791]>                          0          1          64
ZERO
            bin <*,auto[1280:1535]>                          0          1          64
ZERO
            bin <*,auto[768:1023]>                           0          1          64
ZERO
            bin <auto[1024:1055],auto[8192:8447]>            0          1           1
ZERO
            bin <auto[512:543],auto[8192:8447]>              0          1           1
ZERO
            bin <auto[128:159],auto[8192:8447]>              0          1           1
ZERO
            bin <auto[64:95],auto[8192:8447]>                0          1           1
ZERO
            bin <auto[32:63],auto[8192:8447]>                0          1           1
ZERO
            bin <auto[1024:1055],auto[4096:4351]>            0          1           1
ZERO
            bin <auto[512:543],auto[4096:4351]>              0          1           1
ZERO
            bin <auto[256:287],auto[4096:4351]>              0          1           1
ZERO
            bin <auto[128:159],auto[4096:4351]>              0          1           1
ZERO
            bin <auto[64:95],auto[4096:4351]>                0          1           1
ZERO
            bin <auto[32:63],auto[4096:4351]>                0          1           1
ZERO
            bin <auto[1024:1055],auto[2048:2303]>            0          1           1
ZERO
            bin <auto[256:287],auto[2048:2303]>              0          1           1
ZERO
            bin <auto[128:159],auto[2048:2303]>              0          1           1
ZERO
            bin <auto[64:95],auto[2048:2303]>                0          1           1
ZERO
```

```
            bin <auto[32:63],auto[2048:2303]>                0          1          1
ZERO
            bin <auto[0:31],auto[2048:2303]>                 0          1          1
ZERO
            bin <auto[1024:1055],auto[1024:1279]>            0          1          1
ZERO
            bin <auto[512:543],auto[1024:1279]>              0          1          1
ZERO
            bin <auto[256:287],auto[1024:1279]>              0          1          1
ZERO
            bin <auto[128:159],auto[1024:1279]>              0          1          1
ZERO
            bin <auto[64:95],auto[1024:1279]>                0          1          1
ZERO
            bin <auto[32:63],auto[1024:1279]>                0          1          1
ZERO
            bin <auto[1024:1055],auto[512:767]>              0          1          1
ZERO
            bin <auto[512:543],auto[512:767]>                0          1          1
ZERO
            bin <auto[256:287],auto[512:767]>                0          1          1
ZERO
            bin <auto[128:159],auto[512:767]>                0          1          1
ZERO
            bin <auto[64:95],auto[512:767]>                  0          1          1
ZERO
            bin <auto[1024:1055],auto[256:511]>              0          1          1
ZERO
            bin <auto[128:159],auto[256:511]>                0          1          1
ZERO
            bin <auto[64:95],auto[256:511]>                  0          1          1
ZERO
            bin <auto[32:63],auto[256:511]>                  0          1          1
ZERO
        Cross #cross__1#                                  0.00%        100          -
ZERO
            covered/total bins:                             0       1024          -

            missing/total bins:                          1024       1024          -

            % Hit:                                       0.00%        100          -

            type_option.weight=1
            type_option.goal=100
            type_option.comment=
            Auto, Default and User Defined Bins:
```

```
            bin <*,*>                                   0          1       1024
ZERO
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                     391       298        93    76.21%

================================Statement Details================================

Statement Coverage for Design Unit work.coverage_sv_unit --

    Line         Item                     Count     Source
    ----         ----                     -----     ------
  File transaction.sv
    143             1                       579
    144             1                       579
    145             1                       579
    146             1                       579
    147             1                       579
    148             1                       579
    149             1                       579
    152             1                       579
    153             1                       579
    154             1                       579
    155             1                       579
    156             1                       579
    157             1                       579
    158             1                       579
    159             1                       579
    160             1                       579
    161             1                       579
    164             1                       579
    165             1                       579
    166             1                       579
    167             1                       579
    168             1                       579
    169             1                       579
    170             1                       579
    171             1                       579
    172             1                       579
    173             1                       579
    174             1                       579
    175             1                       579
    176             1                       579
    177             1                       579
    178             1                       579
```

179	1	579
180	1	579
181	1	579
182	1	579
199	1	25
200	1	25
201	1	25
202	1	25
203	1	25
204	1	25
205	1	25
226	1	12
228	1	6
230	1	2
232	1	3
234	1	6
236	1	9
238	1	4
240	1	5
243	1	9
244	1	6
245	1	5
246	1	2
248	1	3
249	1	3
250	1	***0***
252	1	75
264	1	75
265	1	75
266	1	75
267	1	75
268	1	75
269	1	75
270	1	75
271	1	75
272	1	75

File coverage.sv

18	1	1
60	1	1
61	1	1
66	1	1
67	1	1
68	1	502
70	1	65
73	1	***0***
78	1	***0***

```
  79              1                    ***0***
  80              1                    ***0***
  81              1                    ***0***
  82              1                    ***0***
  87              1                    ***0***
  88              1                    ***0***
  89              1                    ***0***
  90              1                    ***0***
  91              1                    ***0***
  92              1                    ***0***
  93              1                    ***0***
  98              1                        1
  99              1                    ***0***
  100             1                    ***0***
File driver.sv
  27              1                        1
  28              1                        1
  34              1                        1
  35              1                       76
  36              1                       75
  37              1                       75
  46              1                       75
  47              1                       75
  48              1                       75
  49              1                       75
  50              1                       75
  51              1                       75
  52              1                       75
  53              1                       75
  54              1                       75
  55              1                       75
  56              1                       75
  57              1                       75
  58              1                       75
  61              1                       75
  63              1                       75
  64              1                       75
File generator.sv
  55              1                        1
  62              1                        1
  63              1                        1
  72              1                        1
  75              1                        1
  77              1                        1
  80              1                        1
  91              1                        1
```

94	1	1
97	1	1
100	1	1
103	1	1
106	1	1
109	1	1
112	1	1
115	1	1
125	1	1
125	2	50
127	1	50
128	1	50
134	1	17
138	1	17
150	1	***0***
153	1	50
156	1	50
159	1	50
169	1	1
171	1	1
172	1	1
175	1	1
177	1	1
178	1	1
181	1	1
183	1	1
184	1	1
187	1	1
189	1	1
190	1	1
199	1	1
201	1	1
202	1	1
205	1	1
207	1	1
208	1	1
211	1	1
213	1	1
214	1	1
223	1	1
225	1	1
226	1	1
229	1	1
231	1	1
232	1	1
235	1	1

237	1	1
238	1	1
247	1	1
249	1	1
250	1	1
253	1	1
255	1	1
256	1	1
259	1	1
261	1	1
262	1	1
265	1	1
267	1	1
268	1	1
277	1	1
278	1	1
279	1	1
282	1	1
283	1	1
284	1	1
293	1	1
295	1	1
296	1	1
299	1	1
301	1	1
302	1	1
311	1	1
312	1	1
313	1	1
316	1	1
317	1	1
318	1	1
327	1	1
328	1	1
329	1	1
332	1	1
333	1	1
334	1	1
343	1	1
344	1	1
345	1	1
348	1	1
349	1	1
350	1	1
356	1	1
357	1	1

```
  358             1                      1
  373             1                     12
  374             1                      6
  375             1                      2
  376             1                      3
  377             1                      6
  378             1                      9
  379             1                      4
  380             1                      5
  381             1                      9
  382             1                      6
  383             1                      5
  384             1                      2
  385             1                      3
  386             1                      3
  387             1                  ***0***
  392             1                     21
  393             1                      4
  394             1                      6
  395             1                      7
  396             1                      7
  397             1                      4
  398             1                      4
  399             1                      3
  400             1                      7
  401             1                      6
  402             1                      2
  403             1                      4
  408             1                     75
  409             1                     75
  410             1                     75
  411             1                     75
  412             1                     75
  413             1                     75
  414             1                     75
  415             1                     75
  416             1                     75
  417             1                     75
  420             1                     75
File monitor.sv
  18              1                      1
  31              1                      1
  32              1                      1
  44              1                      1
  45              1                      1
  47              1                    502
```

49	1	502
52	1	65
53	1	65
54	1	65
55	1	65
56	1	65
57	1	65
58	1	65
59	1	65
60	1	65
61	1	65
62	1	65
63	1	65
64	1	65
65	1	65
66	1	65
67	1	65
70	1	65
73	1	***0***
88	1	1
92	1	1
105	1	1
106	1	1
119	1	1
120	1	1
122	1	1
124	1	1
126	1	1
129	1	***0***
130	1	***0***
131	1	***0***
132	1	***0***
133	1	***0***
134	1	***0***
135	1	***0***
136	1	***0***
137	1	***0***
138	1	***0***
139	1	***0***
140	1	***0***
141	1	***0***
142	1	***0***
143	1	***0***
144	1	***0***
145	1	***0***
146	1	***0***

```
  147             1                    ***0***
  150             1                    ***0***
  152             1                    ***0***
  154             1                    ***0***
File scoreboard.sv
   16             1                       1
   17             1                       1
   43             1                       1
   44             1                       1
   51             1                       1
   52             1                       1
   61             1                       1
   62             1                       1
   73             1                       1
   74             1                      66
   75             1                      66
   76             1                      65
   77             1                      65
   80             1                      65
   81             1                      65
   82             1                      65
   83             1                      65
   84             1                      65
   85             1                      65
   86             1                      65
   87             1                      65
   88             1                      65
   89             1                      65
   90             1                      65
   91             1                      65
   92             1                      65
   93             1                      65
   94             1                      65
   95             1                      65
  131             1                       1
  132             1                       1
  133             1                    ***0***
  134             1                    ***0***
  135             1                    ***0***
  136             1                    ***0***
  137             1                    ***0***
  140             1                    ***0***
  141             1                    ***0***
  142             1                    ***0***
  143             1                    ***0***
  144             1                    ***0***
```

145	1	***0***
146	1	***0***
147	1	***0***
148	1	***0***
149	1	***0***
150	1	***0***
151	1	***0***
152	1	***0***
153	1	***0***
154	1	***0***
161	1	***0***
164	1	***0***
173	1	***0***
183	1	***0***
189	1	***0***
192	1	***0***
196	1	***0***
202	1	***0***
207	1	***0***
211	1	***0***
218	1	***0***
222	1	***0***
242	1	***0***
248	1	***0***
250	1	***0***
252	1	***0***
258	1	***0***
308	1	***0***
309	1	***0***
310	1	***0***
312	1	***0***
313	1	***0***
314	1	***0***
315	1	***0***
316	1	***0***
317	1	***0***
318	1	***0***
319	1	***0***
320	1	***0***
321	1	***0***
322	1	***0***
323	1	***0***

```
================================================================================
=== Design Unit: work.rv32i_alu
================================================================================
```

```
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        62        54         8    87.09%

================================Branch Details================================

Branch Coverage for Design Unit work.rv32i_alu

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File rv32i_alu.sv
-----------------------------------IF Branch-----------------------------------
    174                                       76     Count coming in to IF
    174             1                         76
    178             1                      ***0***
Branch totals: 1 hit of 2 branches = 50.00%

-----------------------------------IF Branch-----------------------------------
    179                                    ***0***     Count coming in to IF
    179             1                      ***0***
                                           ***0***     All False Count
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    198                                    ***0***     Count coming in to IF
    198             1                      ***0***
    201             1                      ***0***
    204             1                      ***0***
                                           ***0***     All False Count
Branch totals: 0 hits of 4 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    218                                       75     Count coming in to IF
    218             1                         11
    218             2                         64
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    220                                       75     Count coming in to IF
    220             1                         28
    220             2                         47
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    223                                       76     Count coming in to IF
```

```
    223             1                       12
                                            64     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    224                                     76     Count coming in to IF
    224             1                        6
                                            70     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    225                                     76     Count coming in to IF
    225             1                        5
                                            71     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    227                                      5     Count coming in to IF
    227             1                        2
                                             3     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    227                                      2     Count coming in to IF
    227             2                        2
    227             3                    ***0***
Branch totals: 1 hit of 2 branches = 50.00%

-----------------------------------IF Branch-----------------------------------
    229                                     76     Count coming in to IF
    229             1                        6
                                            70     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    230                                     76     Count coming in to IF
    230             1                        9
                                            67     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    231                                     76     Count coming in to IF
    231             1                        4
                                            72     All False Count
Branch totals: 2 hits of 2 branches = 100.00%
```

```
-----------------------------------IF Branch-----------------------------------
    232                                     76     Count coming in to IF
    232             1                        5
                                            71     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    233                                     76     Count coming in to IF
    233             1                        9
                                            67     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    234                                     76     Count coming in to IF
    234             1                        6
                                            70     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    235                                     76     Count coming in to IF
    235             1                        7
                                            69     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    237                                      7     Count coming in to IF
    237             1                        2
                                             5     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    239                                     76     Count coming in to IF
    239             1                        6
                                            70     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    241                                      6     Count coming in to IF
    241             1                        3
                                             3     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    241                                      3     Count coming in to IF
    241             2                        2
    241             3                        1
```

```
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    257                                     96     Count coming in to IF
    257             1                       94
                                             2     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    258                                     94     Count coming in to IF
    258             1                       37
                                            57     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    259                                     94     Count coming in to IF
    259             1                        3
                                            91     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    266                                     94     Count coming in to IF
    266             1                       12
                                            82     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    267                                     12     Count coming in to IF
    267             1                        8
                                             4     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    277                                     96     Count coming in to IF
    277             1                        4
                                            92     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    278                                     96     Count coming in to IF
    278             1                        7
                                            89     All False Count
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    280                                     96     Count coming in to IF
```

```
    280             1                       23
    283             1                       73
Branch totals: 2 hits of 2 branches = 100.00%

-----------------------------------IF Branch-----------------------------------
    287                                     96     Count coming in to IF
    287             1                        6
    290             1                       90
Branch totals: 2 hits of 2 branches = 100.00%


Condition Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Conditions                      34        23        11    67.64%

================================Condition Details================================

Condition Coverage for Design Unit work.rv32i_alu --

  File rv32i_alu.sv
----------------Focused Condition View-------------------
Line       179 Item    1  (i_ce && ~stall_bit)
Condition totals: 0 of 2 input terms covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
        i_ce         N  No hits                 Hit '_0' and '_1'
   stall_bit         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  i_ce_0                -
  Row   2:    ***0***  i_ce_1                ~stall_bit
  Row   3:    ***0***  stall_bit_0           i_ce
  Row   4:    ***0***  stall_bit_1           i_ce

----------------Focused Condition View-------------------
Line       198 Item    1  (i_flush && ~stall_bit)
Condition totals: 0 of 2 input terms covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
     i_flush         N  No hits                 Hit '_0' and '_1'
   stall_bit         N  No hits                 Hit '_0' and '_1'
```

```
     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  i_flush_0             -
  Row   2:    ***0***  i_flush_1             ~stall_bit
  Row   3:    ***0***  stall_bit_0           i_flush
  Row   4:    ***0***  stall_bit_1           i_flush

----------------Focused Condition View-------------------
Line       204 Item    1  (stall_bit && ~i_stall)
Condition totals: 0 of 2 input terms covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
   stall_bit         N  No hits                  Hit '_0' and '_1'
     i_stall         N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  stall_bit_0           -
  Row   2:    ***0***  stall_bit_1           ~i_stall
  Row   3:    ***0***  i_stall_0             stall_bit
  Row   4:    ***0***  i_stall_1             stall_bit

----------------Focused Condition View-------------------
Line       218 Item    1  (opcode_jal || opcode_auipc)
Condition totals: 2 of 2 input terms covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  ----------------------  --------------
    opcode_jal         Y
  opcode_auipc         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  opcode_jal_0          ~opcode_auipc
  Row   2:          1  opcode_jal_1          -
  Row   3:          1  opcode_auipc_0        ~opcode_jal
  Row   4:          1  opcode_auipc_1        ~opcode_jal

----------------Focused Condition View-------------------
Line       220 Item    1  (opcode_rtype || opcode_branch)
Condition totals: 2 of 2 input terms covered = 100.00%

     Input Term   Covered  Reason for no coverage   Hint
    -----------  --------  ----------------------  --------------
   opcode_rtype         Y
```

```
  opcode_branch         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  opcode_rtype_0        ~opcode_branch
  Row   2:          1  opcode_rtype_1        -
  Row   3:          1  opcode_branch_0       ~opcode_rtype
  Row   4:          1  opcode_branch_1       ~opcode_rtype

----------------Focused Condition View-------------------
Line       225 Item    1  (alu_slt || alu_sltu)
Condition totals: 2 of 2 input terms covered = 100.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
     alu_slt         Y
    alu_sltu         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  alu_slt_0             ~alu_sltu
  Row   2:          1  alu_slt_1             -
  Row   3:          1  alu_sltu_0            ~alu_slt
  Row   4:          1  alu_sltu_1            ~alu_slt

-----------Focused Condition View (Bimodal)--------------
Line       227 Item    1  (a[31] ^ b[31])
Condition totals: 0 of 2 input terms covered = 0.00%

  Input Term   Covered  Reason for no coverage                  Hint
 -----------  --------  ------------------------------------  --------------
       a[31]         N  '_1' hit but '_0' is not hit          Hit '_0' for output ->0
       b[31]         N  '_0' hit but '_1' is not hit          Hit '_1' for output ->0

    Rows:   Hits(->0)   Hits(->1)  FEC Target            Non-masking condition(s)


---------  ----------  ----------  --------------------  -------------------------

 Row   1:           0           0  a[31]_0               -

 Row   2:           0           1  a[31]_1               -

 Row   3:           0           1  b[31]_0               -

 Row   4:           0           0  b[31]_1               -
```

```
----------------Focused Condition View-------------------
Line       235 Item    1  (alu_eq || alu_neq)
Condition totals: 2 of 2 input terms covered = 100.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
      alu_eq         Y
     alu_neq         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  alu_eq_0              ~alu_neq
  Row   2:          1  alu_eq_1              -
  Row   3:          1  alu_neq_0             ~alu_eq
  Row   4:          1  alu_neq_1             ~alu_eq

----------------Focused Condition View-------------------
Line       239 Item    1  (alu_ge || alu_geu)
Condition totals: 2 of 2 input terms covered = 100.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
      alu_ge         Y
     alu_geu         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  alu_ge_0              ~alu_geu
  Row   2:          1  alu_ge_1              -
  Row   3:          1  alu_geu_0             ~alu_ge
  Row   4:          1  alu_geu_1             ~alu_ge

-----------Focused Condition View (Bimodal)--------------
Line       241 Item    1  (a[31] ^ b[31])
Condition totals: 2 of 2 input terms covered = 100.00%

  Input Term   Covered  Reason for no coverage                  Hint
 -----------  --------  -------------------------------------  --------------
       a[31]         Y
       b[31]         Y

    Rows:   Hits(->0)   Hits(->1)  FEC Target            Non-masking condition(s)
```

```
---------  ----------  ----------  --------------------  ------------------------

 Row   1:           0           1  a[31]_0               -

 Row   2:           1           1  a[31]_1               -

 Row   3:           0           1  b[31]_0               -

 Row   4:           1           0  b[31]_1               -


----------------Focused Condition View-------------------
Line       258 Item    1  (opcode_rtype || opcode_itype)
Condition totals: 2 of 2 input terms covered = 100.00%

    Input Term   Covered  Reason for no coverage   Hint
   -----------  --------  ----------------------  --------------
  opcode_rtype         Y
  opcode_itype         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  opcode_rtype_0        ~opcode_itype
  Row   2:          1  opcode_rtype_1        -
  Row   3:          1  opcode_itype_0        ~opcode_rtype
  Row   4:          1  opcode_itype_1        ~opcode_rtype

----------------Focused Condition View-------------------
Line       259 Item    1  (opcode_branch && y_d[0])
Condition totals: 2 of 2 input terms covered = 100.00%

     Input Term   Covered  Reason for no coverage   Hint
    -----------  --------  ----------------------  --------------
  opcode_branch         Y
         y_d[0]         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  opcode_branch_0       -
  Row   2:          1  opcode_branch_1       y_d[0]
  Row   3:          1  y_d[0]_0              opcode_branch
  Row   4:          1  y_d[0]_1              opcode_branch

----------------Focused Condition View-------------------
Line       266 Item    1  (opcode_jal || opcode_jalr)
Condition totals: 2 of 2 input terms covered = 100.00%
```

```
   Input Term   Covered  Reason for no coverage   Hint
  -----------  --------  ----------------------  --------------
   opcode_jal         Y
  opcode_jalr         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  opcode_jal_0          ~opcode_jalr
  Row   2:          1  opcode_jal_1          -
  Row   3:          1  opcode_jalr_0         ~opcode_jal
  Row   4:          1  opcode_jalr_1         ~opcode_jal

----------------Focused Condition View-------------------
Line           280  Item      1   (((opcode_branch || opcode_store) || (opcode_system &&
(i_funct3 == 0))) || opcode_fence)
Condition totals: 4 of 5 input terms covered = 80.00%

       Input Term   Covered  Reason for no coverage   Hint
      -----------  --------  ----------------------  --------------
    opcode_branch         Y
     opcode_store         Y
    opcode_system         Y
  (i_funct3 == 0)         N  '_0' not hit             Hit '_0'
     opcode_fence         Y

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
   Row    1:          1   opcode_branch_0         (~opcode_fence && ~(opcode_system &&
(i_funct3 == 0)) && ~opcode_store)
  Row   2:          1  opcode_branch_1       -
   Row    3:          1   opcode_store_0          (~opcode_fence && ~(opcode_system &&
(i_funct3 == 0)) && ~opcode_branch)
  Row   4:          1  opcode_store_1        ~opcode_branch
   Row    5:          1   opcode_system_0         (~opcode_fence && ~(opcode_branch ||
opcode_store))
   Row    6:          1   opcode_system_1         (~(opcode_branch || opcode_store) &&
(i_funct3 == 0))
   Row    7:     ***0***   (i_funct3 == 0)_0       (~opcode_fence && ~(opcode_branch ||
opcode_store) && opcode_system)
   Row    8:          1   (i_funct3 == 0)_1       (~(opcode_branch || opcode_store) &&
opcode_system)
   Row    9:          1   opcode_fence_0          ~((opcode_branch || opcode_store) ||
(opcode_system && (i_funct3 == 0)))
 Row    10:          1   opcode_fence_1          ~((opcode_branch || opcode_store) ||
(opcode_system && (i_funct3 == 0)))
```

```
----------------Focused Condition View-------------------
Line       287 Item    1  (opcode_load || (opcode_system && (i_funct3 != 0)))
Condition totals: 1 of 3 input terms covered = 33.33%

       Input Term   Covered  Reason for no coverage   Hint
      -----------  --------  ----------------------  -------------
      opcode_load         Y
    opcode_system         N  '_1' not hit             Hit '_1'
  (i_funct3 != 0)         N  '_1' not hit             Hit '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  opcode_load_0         ~(opcode_system && (i_funct3 != 0))
  Row   2:          1  opcode_load_1         -
  Row   3:          1  opcode_system_0       ~opcode_load
  Row   4:    ***0***  opcode_system_1       (~opcode_load && (i_funct3 != 0))
  Row   5:          1  (i_funct3 != 0)_0     (~opcode_load && opcode_system)
  Row   6:    ***0***  (i_funct3 != 0)_1     (~opcode_load && opcode_system)


Expression Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Expressions                      7         0         7     0.00%

================================Expression Details================================

Expression Coverage for Design Unit work.rv32i_alu --

  File rv32i_alu.sv
----------------Focused Expression View-----------------
Line       193 Item    1  (i_opcode[3] || i_opcode[2])
Expression totals: 0 of 2 input terms covered = 0.00%

   Input Term   Covered  Reason for no coverage   Hint
  -----------  --------  ----------------------  -------------
  i_opcode[3]         N  No hits                 Hit '_0' and '_1'
  i_opcode[2]         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  i_opcode[3]_0         ~i_opcode[2]
  Row   2:    ***0***  i_opcode[3]_1         -
  Row   3:    ***0***  i_opcode[2]_0         ~i_opcode[3]
  Row   4:    ***0***  i_opcode[2]_1         ~i_opcode[3]
```

```
----------------Focused Expression View-----------------
Line       294 Item    1  ((i_stall || i_force_stall) && ~i_flush)
Expression totals: 0 of 3 input terms covered = 0.00%

     Input Term   Covered  Reason for no coverage   Hint
    -----------  --------  ----------------------  --------------
        i_stall         N  '_1' not hit             Hit '_1'
  i_force_stall         N  '_1' not hit             Hit '_1'
        i_flush         N  No hits                  Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  i_stall_0             ~i_force_stall
  Row   2:    ***0***  i_stall_1             ~i_flush
  Row   3:          1  i_force_stall_0       ~i_stall
  Row   4:    ***0***  i_force_stall_1       (~i_flush && ~i_stall)
  Row   5:    ***0***  i_flush_0             (i_stall || i_force_stall)
  Row   6:    ***0***  i_flush_1             (i_stall || i_force_stall)

----------------Focused Expression View-----------------
Line       299 Item    1  (o_stall || i_stall)
Expression totals: 0 of 2 input terms covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
    o_stall         N  '_1' not hit             Hit '_1'
    i_stall         N  '_1' not hit             Hit '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:          1  o_stall_0             ~i_stall
  Row   2:    ***0***  o_stall_1             -
  Row   3:          1  i_stall_0             ~o_stall
  Row   4:    ***0***  i_stall_1             ~o_stall


Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      65        48        17    73.84%

================================Statement Details================================

Statement Coverage for Design Unit work.rv32i_alu --
```

Line	Item	Count	Source
File rv32i_alu.sv			
173	1	76	
175	1	76	
176	1	76	
177	1	76	
181	1	***0***	
182	1	***0***	
183	1	***0***	
184	1	***0***	
185	1	***0***	
186	1	***0***	
187	1	***0***	
188	1	***0***	
189	1	***0***	
190	1	***0***	
191	1	***0***	
192	1	***0***	
193	1	***0***	
195	1	***0***	
200	1	***0***	
203	1	***0***	
205	1	***0***	
215	1	76	
216	1	76	
218	1	76	
220	1	76	
223	1	12	
224	1	6	
226	1	5	
227	1	2	
229	1	6	
230	1	9	
231	1	4	
232	1	5	
233	1	9	
234	1	6	
236	1	7	
237	1	2	
240	1	6	
241	1	3	
248	1	96	
249	1	96	
251	1	96	
252	1	96	

```
    253             1                         96
    254             1                         96
    255             1                         96
    256             1                         96
    258             1                         37
    260             1                          3
    262             1                          3
    264             1                          3
    267             1                          8
    268             1                         12
    270             1                         12
    272             1                         12
    273             1                         12
    277             1                          4
    278             1                          7
    281             1                         23
    284             1                         73
    288             1                          6
    290             1                         90
    294             1                         96
    298             1                         70
    299             1                          3

================================================================================
=== Design Unit: work.rv32i_alu_tb
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        27         0        27     0.00%

================================Branch Details================================

Branch Coverage for Design Unit work.rv32i_alu_tb

    Line         Item                      Count     Source
    ----         ----                      -----     ------
  File rv32i_alu_tb.sv
------------------------------------CASE Branch------------------------------------
    259                                  ***0***     Count coming in to CASE
    262             1                    ***0***
    263             1                    ***0***
    264             1                    ***0***
    265             1                    ***0***
    267             1                    ***0***
    268             1                    ***0***
```

```
    269             1                   ***0***
    270             1                   ***0***
    271             1                   ***0***
    272             1                   ***0***
    273             1                   ***0***
    274             1                   ***0***
    275             1                   ***0***
    276             1                   ***0***
    278             1                   ***0***
Branch totals: 0 hits of 15 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    264                                 ***0***     Count coming in to IF
    264             2                   ***0***
    264             3                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    266                                 ***0***     Count coming in to IF
    266             1                   ***0***
    266             2                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    273                                 ***0***     Count coming in to IF
    273             2                   ***0***
    273             3                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    274                                 ***0***     Count coming in to IF
    274             2                   ***0***
    274             3                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    275                                 ***0***     Count coming in to IF
    275             2                   ***0***
    275             3                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%

-----------------------------------IF Branch-----------------------------------
    276                                 ***0***     Count coming in to IF
    276             2                   ***0***
    276             3                   ***0***
Branch totals: 0 hits of 2 branches = 0.00%
```

```
Condition Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Conditions                       6         0         6     0.00%

================================Condition Details================================

Condition Coverage for Design Unit work.rv32i_alu_tb --

  File rv32i_alu_tb.sv
----------------Focused Condition View-------------------
Line       264 Item    1  (a < b)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
     (a < b)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (a < b)_0             -
  Row   2:    ***0***  (a < b)_1             -

----------------Focused Condition View-------------------
Line       266 Item    1  (a < b)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
     (a < b)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (a < b)_0             -
  Row   2:    ***0***  (a < b)_1             -

----------------Focused Condition View-------------------
Line       273 Item    1  (a == b)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
    (a == b)         N  No hits                 Hit '_0' and '_1'
```

```
     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (a == b)_0            -
  Row   2:    ***0***  (a == b)_1            -

----------------Focused Condition View-------------------
Line       274 Item    1  (a != b)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
    (a != b)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (a != b)_0            -
  Row   2:    ***0***  (a != b)_1            -

----------------Focused Condition View-------------------
Line       275 Item    1  (a >= b)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
    (a >= b)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (a >= b)_0            -
  Row   2:    ***0***  (a >= b)_1            -

----------------Focused Condition View-------------------
Line       276 Item    1  (a >= b)
Condition totals: 0 of 1 input term covered = 0.00%

  Input Term   Covered  Reason for no coverage   Hint
 -----------  --------  ----------------------  --------------
    (a >= b)         N  No hits                 Hit '_0' and '_1'

     Rows:       Hits  FEC Target            Non-masking condition(s)
 ---------  ---------  --------------------  -------------------------
  Row   1:    ***0***  (a >= b)_0            -
  Row   2:    ***0***  (a >= b)_1            -


Statement Coverage:
```

Enabled Coverage	Bins	Hits	Misses	Coverage
Statements	56	39	17	69.64%

==========Statement Details==========

Statement Coverage for Design Unit work.rv32i_alu_tb --

Line	Item	Count	Source
File rv32i_alu_tb.sv			
98	1	1	
99	1	1	
100	1	1	
152	1	1	
153	1	1	
154	1	1002	
155	1	1001	
161	1	1	
162	1	1	
163	1	1	
164	1	1	
165	1	1	
166	1	1	
167	1	1	
168	1	1	
169	1	1	
170	1	1	
171	1	1	
172	1	1	
173	1	1	
174	1	1	
175	1	1	
176	1	1	
181	1	1	
182	1	1	
183	1	1	
184	1	1	
185	1	1	
186	1	1	
192	1	1	
193	1	1	
194	1	1	
195	1	1	
196	1	1	
197	1	1	

```
    200             1                        1
    242             1                        1
    242             2                        1
    247             1                        1
    248             1                   ***0***
    249             1                   ***0***
    262             1                   ***0***
    263             1                   ***0***
    264             1                   ***0***
    266             1                   ***0***
    267             1                   ***0***
    268             1                   ***0***
    269             1                   ***0***
    270             1                   ***0***
    271             1                   ***0***
    272             1                   ***0***
    273             1                   ***0***
    274             1                   ***0***
    275             1                   ***0***
    276             1                   ***0***
    278             1                   ***0***

COVERGROUP COVERAGE:
----------------------------------------------------------------------------------------
------------------
Covergroup                                                Metric        Goal        Bins
Status


----------------------------------------------------------------------------------------
------------------
 TYPE work.coverage_sv_unit::coverage/alu_cg             34.81%         100           -
Uncovered
    covered/total bins:                                     51        5315           -

    missing/total bins:                                   5264        5315           -

    % Hit:                                              0.95%         100           -

    type_option.weight=1
    type_option.goal=100
    type_option.comment=
    type_option.strobe=0
    type_option.merge_instances=auto(1)
    Coverpoint #coverpoint__0#                          45.45%         100           -
Uncovered
```

```
        covered/total bins:                                    5         11          -

        missing/total bins:                                    6         11          -

        % Hit:                                             45.45%        100         -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
         bin opcode_types[0]                                   3          1          -
Covered
         bin opcode_types[1]                                  20          1          -
Covered
         bin opcode_types[2]                                   1          1          -
Covered
         bin opcode_types[3]                                   0          1          -
ZERO
         bin opcode_types[4]                                   6          1          -
Covered
         bin opcode_types[5]                                   0          1          -
ZERO
         bin opcode_types[6]                                   0          1          -
ZERO
         bin opcode_types[7]                                   0          1          -
ZERO
         bin opcode_types[8]                                   5          1          -
Covered
         bin opcode_types[9]                                   0          1          -
ZERO
         bin opcode_types[10]                                  0          1          -
ZERO
    Coverpoint #coverpoint__1#                            28.57%         100         -
Uncovered
        covered/total bins:                                    4         14          -

        missing/total bins:                                   10         14          -

        % Hit:                                             28.57%        100         -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
         bin alu_ops[0]                                        0          1          -
ZERO
         bin alu_ops[1]                                       11          1          -
Covered
```

```
        bin alu_ops[2]                                  4          1          -
Covered
        bin alu_ops[3]                                  0          1          -
ZERO
        bin alu_ops[4]                                  1          1          -
Covered
        bin alu_ops[5]                                  0          1          -
ZERO
        bin alu_ops[6]                                  0          1          -
ZERO
        bin alu_ops[7]                                  0          1          -
ZERO
        bin alu_ops[8]                                  3          1          -
Covered
        bin alu_ops[9]                                  0          1          -
ZERO
        bin alu_ops[10]                                 0          1          -
ZERO
        bin alu_ops[11]                                 0          1          -
ZERO
        bin alu_ops[12]                                 0          1          -
ZERO
        bin alu_ops[13]                                 0          1          -
ZERO
    Coverpoint #coverpoint__2#                      100.00%        100          -
Covered
        covered/total bins:                             2          2          -

        missing/total bins:                             0          2          -

        % Hit:                                      100.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                    55          1          -
Covered
        bin auto[1]                                    10          1          -
Covered
    Coverpoint #coverpoint__3#                      100.00%        100          -
Covered
        covered/total bins:                             1          1          -

        missing/total bins:                             0          1          -

        % Hit:                                      100.00%        100          -
```

```
        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin pc_values                                  65          1          -
Covered
    Coverpoint #coverpoint__4#                      0.00%        100          -
ZERO
        covered/total bins:                            0          2          -

        missing/total bins:                            2          2          -

        % Hit:                                      0.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                    0          1          -
ZERO
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__5#                      0.00%        100          -
ZERO
        covered/total bins:                            0          2          -

        missing/total bins:                            2          2          -

        % Hit:                                      0.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                    0          1          -
ZERO
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__6#                      0.00%        100          -
ZERO
        covered/total bins:                            0          1          -

        missing/total bins:                            1          1          -

        % Hit:                                      0.00%        100          -

        type_option.weight=1
        type_option.goal=100
```

```
        type_option.comment=
        bin rd_addr                                    0          1          -
ZERO
    Coverpoint #coverpoint__7#                     50.00%        100          -
Uncovered
        covered/total bins:                            1          2          -

        missing/total bins:                            1          2          -

        % Hit:                                     50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                    0          1          -
ZERO
        bin auto[1]                                   65          1          -
Covered
    Coverpoint #coverpoint__8#                     50.00%        100          -
Uncovered
        covered/total bins:                            1          2          -

        missing/total bins:                            1          2          -

        % Hit:                                     50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                   65          1          -
Covered
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__9#                     50.00%        100          -
Uncovered
        covered/total bins:                            1          2          -

        missing/total bins:                            1          2          -

        % Hit:                                     50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                   65          1          -
Covered
```

```
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__10#                    50.00%        100          -
Uncovered
        covered/total bins:                            1          2          -

        missing/total bins:                            1          2          -

        % Hit:                                     50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                   65          1          -
Covered
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__11#                    50.00%        100          -
Uncovered
        covered/total bins:                            1          2          -

        missing/total bins:                            1          2          -

        % Hit:                                     50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                   65          1          -
Covered
        bin auto[1]                                    0          1          -
ZERO
    Coverpoint #coverpoint__12#                    50.00%        100          -
Uncovered
        covered/total bins:                            1          2          -

        missing/total bins:                            1          2          -

        % Hit:                                     50.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                   65          1          -
Covered
        bin auto[1]                                    0          1          -
```

```
ZERO
    Coverpoint #coverpoint__13#                          100.00%        100          -
Covered
        covered/total bins:                                   2          2          -

        missing/total bins:                                   0          2          -

        % Hit:                                          100.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0]                                          55          1          -
Covered
        bin auto[1]                                          10          1          -
Covered
    Coverpoint #coverpoint__14#                           0.00%        100          -
ZERO
        covered/total bins:                                   0          4          -

        missing/total bins:                                   4          4          -

        % Hit:                                            0.00%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin exceptions[0]                                     0          1          -
ZERO
        bin exceptions[1]                                     0          1          -
ZERO
        bin exceptions[2]                                     0          1          -
ZERO
        bin exceptions[3]                                     0          1          -
ZERO
    Coverpoint #vif.i_opcode__15#                        10.93%        100          -
Uncovered
        covered/total bins:                                   7         64          -

        missing/total bins:                                  57         64          -

        % Hit:                                           10.93%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
```

```
        bin auto[0:31]                                  41          1           -
Covered
        bin auto[32:63]                                  4          1           -
Covered
        bin auto[64:95]                                  3          1           -
Covered
        bin auto[96:127]                                 0          1           -
ZERO
        bin auto[128:159]                                3          1           -
Covered
        bin auto[160:191]                                0          1           -
ZERO
        bin auto[192:223]                                0          1           -
ZERO
        bin auto[224:255]                                0          1           -
ZERO
        bin auto[256:287]                                7          1           -
Covered
        bin auto[288:319]                                0          1           -
ZERO
        bin auto[320:351]                                0          1           -
ZERO
        bin auto[352:383]                                0          1           -
ZERO
        bin auto[384:415]                                0          1           -
ZERO
        bin auto[416:447]                                0          1           -
ZERO
        bin auto[448:479]                                0          1           -
ZERO
        bin auto[480:511]                                0          1           -
ZERO
        bin auto[512:543]                                6          1           -
Covered
        bin auto[544:575]                                0          1           -
ZERO
        bin auto[576:607]                                0          1           -
ZERO
        bin auto[608:639]                                0          1           -
ZERO
        bin auto[640:671]                                0          1           -
ZERO
        bin auto[672:703]                                0          1           -
ZERO
        bin auto[704:735]                                0          1           -
ZERO
```

```
        bin auto[736:767]                                   0          1          -
ZERO
        bin auto[768:799]                                   0          1          -
ZERO
        bin auto[800:831]                                   0          1          -
ZERO
        bin auto[832:863]                                   0          1          -
ZERO
        bin auto[864:895]                                   0          1          -
ZERO
        bin auto[896:927]                                   0          1          -
ZERO
        bin auto[928:959]                                   0          1          -
ZERO
        bin auto[960:991]                                   0          1          -
ZERO
        bin auto[992:1023]                                  0          1          -
ZERO
        bin auto[1024:1055]                                 1          1          -
Covered
        bin auto[1056:1087]                                 0          1          -
ZERO
        bin auto[1088:1119]                                 0          1          -
ZERO
        bin auto[1120:1151]                                 0          1          -
ZERO
        bin auto[1152:1183]                                 0          1          -
ZERO
        bin auto[1184:1215]                                 0          1          -
ZERO
        bin auto[1216:1247]                                 0          1          -
ZERO
        bin auto[1248:1279]                                 0          1          -
ZERO
        bin auto[1280:1311]                                 0          1          -
ZERO
        bin auto[1312:1343]                                 0          1          -
ZERO
        bin auto[1344:1375]                                 0          1          -
ZERO
        bin auto[1376:1407]                                 0          1          -
ZERO
        bin auto[1408:1439]                                 0          1          -
ZERO
        bin auto[1440:1471]                                 0          1          -
ZERO
```

```
        bin auto[1472:1503]                                  0          1          -
ZERO
        bin auto[1504:1535]                                  0          1          -
ZERO
        bin auto[1536:1567]                                  0          1          -
ZERO
        bin auto[1568:1599]                                  0          1          -
ZERO
        bin auto[1600:1631]                                  0          1          -
ZERO
        bin auto[1632:1663]                                  0          1          -
ZERO
        bin auto[1664:1695]                                  0          1          -
ZERO
        bin auto[1696:1727]                                  0          1          -
ZERO
        bin auto[1728:1759]                                  0          1          -
ZERO
        bin auto[1760:1791]                                  0          1          -
ZERO
        bin auto[1792:1823]                                  0          1          -
ZERO
        bin auto[1824:1855]                                  0          1          -
ZERO
        bin auto[1856:1887]                                  0          1          -
ZERO
        bin auto[1888:1919]                                  0          1          -
ZERO
        bin auto[1920:1951]                                  0          1          -
ZERO
        bin auto[1952:1983]                                  0          1          -
ZERO
        bin auto[1984:2015]                                  0          1          -
ZERO
        bin auto[2016:2047]                                  0          1          -
ZERO
    Coverpoint #vif.i_exception__16#                      0.00%        100          -
ZERO
        covered/total bins:                                  0         16          -

        missing/total bins:                                 16         16          -

        % Hit:                                           0.00%        100          -

        type_option.weight=1
        type_option.goal=100
```

```
        type_option.comment=
        bin auto[0]                                    0          1          -
ZERO
        bin auto[1]                                    0          1          -
ZERO
        bin auto[2]                                    0          1          -
ZERO
        bin auto[3]                                    0          1          -
ZERO
        bin auto[4]                                    0          1          -
ZERO
        bin auto[5]                                    0          1          -
ZERO
        bin auto[6]                                    0          1          -
ZERO
        bin auto[7]                                    0          1          -
ZERO
        bin auto[8]                                    0          1          -
ZERO
        bin auto[9]                                    0          1          -
ZERO
        bin auto[10]                                   0          1          -
ZERO
        bin auto[11]                                   0          1          -
ZERO
        bin auto[12]                                   0          1          -
ZERO
        bin auto[13]                                   0          1          -
ZERO
        bin auto[14]                                   0          1          -
ZERO
        bin auto[15]                                   0          1          -
ZERO
    Coverpoint #vif.i_alu__17#                    10.93%        100          -
Uncovered
        covered/total bins:                            7         64          -

        missing/total bins:                           57         64          -

        % Hit:                                    10.93%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        bin auto[0:255]                               39          1          -
Covered
```

```
        bin auto[256:511]                                  8          1          -
Covered
        bin auto[512:767]                                  5          1          -
Covered
        bin auto[768:1023]                                 0          1          -
ZERO
        bin auto[1024:1279]                                5          1          -
Covered
        bin auto[1280:1535]                                0          1          -
ZERO
        bin auto[1536:1791]                                0          1          -
ZERO
        bin auto[1792:2047]                                0          1          -
ZERO
        bin auto[2048:2303]                                2          1          -
Covered
        bin auto[2304:2559]                                0          1          -
ZERO
        bin auto[2560:2815]                                0          1          -
ZERO
        bin auto[2816:3071]                                0          1          -
ZERO
        bin auto[3072:3327]                                0          1          -
ZERO
        bin auto[3328:3583]                                0          1          -
ZERO
        bin auto[3584:3839]                                0          1          -
ZERO
        bin auto[3840:4095]                                0          1          -
ZERO
        bin auto[4096:4351]                                3          1          -
Covered
        bin auto[4352:4607]                                0          1          -
ZERO
        bin auto[4608:4863]                                0          1          -
ZERO
        bin auto[4864:5119]                                0          1          -
ZERO
        bin auto[5120:5375]                                0          1          -
ZERO
        bin auto[5376:5631]                                0          1          -
ZERO
        bin auto[5632:5887]                                0          1          -
ZERO
        bin auto[5888:6143]                                0          1          -
ZERO
```

```
        bin auto[6144:6399]                                 0          1          -
ZERO
        bin auto[6400:6655]                                 0          1          -
ZERO
        bin auto[6656:6911]                                 0          1          -
ZERO
        bin auto[6912:7167]                                 0          1          -
ZERO
        bin auto[7168:7423]                                 0          1          -
ZERO
        bin auto[7424:7679]                                 0          1          -
ZERO
        bin auto[7680:7935]                                 0          1          -
ZERO
        bin auto[7936:8191]                                 0          1          -
ZERO
        bin auto[8192:8447]                                 3          1          -
Covered
        bin auto[8448:8703]                                 0          1          -
ZERO
        bin auto[8704:8959]                                 0          1          -
ZERO
        bin auto[8960:9215]                                 0          1          -
ZERO
        bin auto[9216:9471]                                 0          1          -
ZERO
        bin auto[9472:9727]                                 0          1          -
ZERO
        bin auto[9728:9983]                                 0          1          -
ZERO
        bin auto[9984:10239]                                0          1          -
ZERO
        bin auto[10240:10495]                               0          1          -
ZERO
        bin auto[10496:10751]                               0          1          -
ZERO
        bin auto[10752:11007]                               0          1          -
ZERO
        bin auto[11008:11263]                               0          1          -
ZERO
        bin auto[11264:11519]                               0          1          -
ZERO
        bin auto[11520:11775]                               0          1          -
ZERO
        bin auto[11776:12031]                               0          1          -
ZERO
```

```
        bin auto[12032:12287]                                  0          1          -
ZERO
        bin auto[12288:12543]                                  0          1          -
ZERO
        bin auto[12544:12799]                                  0          1          -
ZERO
        bin auto[12800:13055]                                  0          1          -
ZERO
        bin auto[13056:13311]                                  0          1          -
ZERO
        bin auto[13312:13567]                                  0          1          -
ZERO
        bin auto[13568:13823]                                  0          1          -
ZERO
        bin auto[13824:14079]                                  0          1          -
ZERO
        bin auto[14080:14335]                                  0          1          -
ZERO
        bin auto[14336:14591]                                  0          1          -
ZERO
        bin auto[14592:14847]                                  0          1          -
ZERO
        bin auto[14848:15103]                                  0          1          -
ZERO
        bin auto[15104:15359]                                  0          1          -
ZERO
        bin auto[15360:15615]                                  0          1          -
ZERO
        bin auto[15616:15871]                                  0          1          -
ZERO
        bin auto[15872:16127]                                  0          1          -
ZERO
        bin auto[16128:16383]                                  0          1          -
ZERO
    Cross #cross__0#                                       0.41%        100          -
Uncovered
        covered/total bins:                                  17       4096          -

        missing/total bins:                                4079       4096          -

        % Hit:                                             0.41%        100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        Auto, Default and User Defined Bins:
```

```
            bin <auto[256:287],auto[8192:8447]>              1          1           -
Covered
            bin <auto[0:31],auto[8192:8447]>                 2          1           -
Covered
            bin <auto[0:31],auto[4096:4351]>                 3          1           -
Covered
            bin <auto[512:543],auto[2048:2303]>              2          1           -
Covered
            bin <auto[0:31],auto[1024:1279]>                 5          1           -
Covered
            bin <auto[32:63],auto[512:767]>                  1          1           -
Covered
            bin <auto[0:31],auto[512:767]>                   4          1           -
Covered
            bin <auto[512:543],auto[256:511]>                1          1           -
Covered
            bin <auto[256:287],auto[256:511]>                1          1           -
Covered
            bin <auto[0:31],auto[256:511]>                   6          1           -
Covered
            bin <auto[1024:1055],auto[0:255]>                1          1           -
Covered
            bin <auto[512:543],auto[0:255]>                  3          1           -
Covered
            bin <auto[256:287],auto[0:255]>                  5          1           -
Covered
            bin <auto[128:159],auto[0:255]>                  3          1           -
Covered
            bin <auto[64:95],auto[0:255]>                    3          1           -
Covered
            bin <auto[32:63],auto[0:255]>                    3          1           -
Covered
            bin <auto[0:31],auto[0:255]>                    21          1           -
Covered
            bin <auto[2016:2047],*>                          0          1          64
ZERO
            bin <auto[1984:2015],*>                          0          1          64
ZERO
            bin <auto[1952:1983],*>                          0          1          64
ZERO
            bin <auto[1920:1951],*>                          0          1          64
ZERO
            bin <auto[1888:1919],*>                          0          1          64
ZERO
            bin <auto[1856:1887],*>                          0          1          64
ZERO
```

bin <auto[1824:1855],*> 0 1 64
ZERO
bin <auto[1792:1823],*> 0 1 64
ZERO
bin <auto[1760:1791],*> 0 1 64
ZERO
bin <auto[1728:1759],*> 0 1 64
ZERO
bin <auto[1696:1727],*> 0 1 64
ZERO
bin <auto[1664:1695],*> 0 1 64
ZERO
bin <auto[1632:1663],*> 0 1 64
ZERO
bin <auto[1600:1631],*> 0 1 64
ZERO
bin <auto[1568:1599],*> 0 1 64
ZERO
bin <auto[1536:1567],*> 0 1 64
ZERO
bin <auto[1504:1535],*> 0 1 64
ZERO
bin <auto[1472:1503],*> 0 1 64
ZERO
bin <auto[1440:1471],*> 0 1 64
ZERO
bin <auto[1408:1439],*> 0 1 64
ZERO
bin <auto[1376:1407],*> 0 1 64
ZERO
bin <auto[1344:1375],*> 0 1 64
ZERO
bin <auto[1312:1343],*> 0 1 64
ZERO
bin <auto[1280:1311],*> 0 1 64
ZERO
bin <auto[1248:1279],*> 0 1 64
ZERO
bin <auto[1216:1247],*> 0 1 64
ZERO
bin <auto[1184:1215],*> 0 1 64
ZERO
bin <auto[1152:1183],*> 0 1 64
ZERO
bin <auto[1120:1151],*> 0 1 64
ZERO

```
            bin <auto[1088:1119],*>                         0          1          64
ZERO
            bin <auto[1056:1087],*>                         0          1          64
ZERO
            bin <auto[992:1023],*>                          0          1          64
ZERO
            bin <auto[960:991],*>                           0          1          64
ZERO
            bin <auto[928:959],*>                           0          1          64
ZERO
            bin <auto[896:927],*>                           0          1          64
ZERO
            bin <auto[864:895],*>                           0          1          64
ZERO
            bin <auto[832:863],*>                           0          1          64
ZERO
            bin <auto[800:831],*>                           0          1          64
ZERO
            bin <auto[768:799],*>                           0          1          64
ZERO
            bin <auto[736:767],*>                           0          1          64
ZERO
            bin <auto[704:735],*>                           0          1          64
ZERO
            bin <auto[672:703],*>                           0          1          64
ZERO
            bin <auto[640:671],*>                           0          1          64
ZERO
            bin <auto[608:639],*>                           0          1          64
ZERO
            bin <auto[576:607],*>                           0          1          64
ZERO
            bin <auto[544:575],*>                           0          1          64
ZERO
            bin <auto[480:511],*>                           0          1          64
ZERO
            bin <auto[448:479],*>                           0          1          64
ZERO
            bin <auto[416:447],*>                           0          1          64
ZERO
            bin <auto[384:415],*>                           0          1          64
ZERO
            bin <auto[352:383],*>                           0          1          64
ZERO
            bin <auto[320:351],*>                           0          1          64
ZERO
```

```
            bin <auto[288:319],*>                          0          1          64
ZERO
            bin <auto[224:255],*>                          0          1          64
ZERO
            bin <auto[192:223],*>                          0          1          64
ZERO
            bin <auto[160:191],*>                          0          1          64
ZERO
            bin <auto[96:127],*>                           0          1          64
ZERO
            bin <*,auto[16128:16383]>                      0          1          64
ZERO
            bin <*,auto[15872:16127]>                      0          1          64
ZERO
            bin <*,auto[15616:15871]>                      0          1          64
ZERO
            bin <*,auto[15360:15615]>                      0          1          64
ZERO
            bin <*,auto[15104:15359]>                      0          1          64
ZERO
            bin <*,auto[14848:15103]>                      0          1          64
ZERO
            bin <*,auto[14592:14847]>                      0          1          64
ZERO
            bin <*,auto[14336:14591]>                      0          1          64
ZERO
            bin <*,auto[14080:14335]>                      0          1          64
ZERO
            bin <*,auto[13824:14079]>                      0          1          64
ZERO
            bin <*,auto[13568:13823]>                      0          1          64
ZERO
            bin <*,auto[13312:13567]>                      0          1          64
ZERO
            bin <*,auto[13056:13311]>                      0          1          64
ZERO
            bin <*,auto[12800:13055]>                      0          1          64
ZERO
            bin <*,auto[12544:12799]>                      0          1          64
ZERO
            bin <*,auto[12288:12543]>                      0          1          64
ZERO
            bin <*,auto[12032:12287]>                      0          1          64
ZERO
            bin <*,auto[11776:12031]>                      0          1          64
ZERO
```

```
            bin <*,auto[11520:11775]>                    0          1          64
ZERO
            bin <*,auto[11264:11519]>                    0          1          64
ZERO
            bin <*,auto[11008:11263]>                    0          1          64
ZERO
            bin <*,auto[10752:11007]>                    0          1          64
ZERO
            bin <*,auto[10496:10751]>                    0          1          64
ZERO
            bin <*,auto[10240:10495]>                    0          1          64
ZERO
            bin <*,auto[9984:10239]>                     0          1          64
ZERO
            bin <*,auto[9728:9983]>                      0          1          64
ZERO
            bin <*,auto[9472:9727]>                      0          1          64
ZERO
            bin <*,auto[9216:9471]>                      0          1          64
ZERO
            bin <*,auto[8960:9215]>                      0          1          64
ZERO
            bin <*,auto[8704:8959]>                      0          1          64
ZERO
            bin <*,auto[8448:8703]>                      0          1          64
ZERO
            bin <*,auto[7936:8191]>                      0          1          64
ZERO
            bin <*,auto[7680:7935]>                      0          1          64
ZERO
            bin <*,auto[7424:7679]>                      0          1          64
ZERO
            bin <*,auto[7168:7423]>                      0          1          64
ZERO
            bin <*,auto[6912:7167]>                      0          1          64
ZERO
            bin <*,auto[6656:6911]>                      0          1          64
ZERO
            bin <*,auto[6400:6655]>                      0          1          64
ZERO
            bin <*,auto[6144:6399]>                      0          1          64
ZERO
            bin <*,auto[5888:6143]>                      0          1          64
ZERO
            bin <*,auto[5632:5887]>                      0          1          64
ZERO
```

```
            bin <*,auto[5376:5631]>                          0          1          64
ZERO
            bin <*,auto[5120:5375]>                          0          1          64
ZERO
            bin <*,auto[4864:5119]>                          0          1          64
ZERO
            bin <*,auto[4608:4863]>                          0          1          64
ZERO
            bin <*,auto[4352:4607]>                          0          1          64
ZERO
            bin <*,auto[3840:4095]>                          0          1          64
ZERO
            bin <*,auto[3584:3839]>                          0          1          64
ZERO
            bin <*,auto[3328:3583]>                          0          1          64
ZERO
            bin <*,auto[3072:3327]>                          0          1          64
ZERO
            bin <*,auto[2816:3071]>                          0          1          64
ZERO
            bin <*,auto[2560:2815]>                          0          1          64
ZERO
            bin <*,auto[2304:2559]>                          0          1          64
ZERO
            bin <*,auto[1792:2047]>                          0          1          64
ZERO
            bin <*,auto[1536:1791]>                          0          1          64
ZERO
            bin <*,auto[1280:1535]>                          0          1          64
ZERO
            bin <*,auto[768:1023]>                           0          1          64
ZERO
            bin <auto[1024:1055],auto[8192:8447]>            0          1           1
ZERO
            bin <auto[512:543],auto[8192:8447]>              0          1           1
ZERO
            bin <auto[128:159],auto[8192:8447]>              0          1           1
ZERO
            bin <auto[64:95],auto[8192:8447]>                0          1           1
ZERO
            bin <auto[32:63],auto[8192:8447]>                0          1           1
ZERO
            bin <auto[1024:1055],auto[4096:4351]>            0          1           1
ZERO
            bin <auto[512:543],auto[4096:4351]>              0          1           1
ZERO
```

```
            bin <auto[256:287],auto[4096:4351]>              0          1          1
ZERO
            bin <auto[128:159],auto[4096:4351]>              0          1          1
ZERO
            bin <auto[64:95],auto[4096:4351]>                0          1          1
ZERO
            bin <auto[32:63],auto[4096:4351]>                0          1          1
ZERO
            bin <auto[1024:1055],auto[2048:2303]>            0          1          1
ZERO
            bin <auto[256:287],auto[2048:2303]>              0          1          1
ZERO
            bin <auto[128:159],auto[2048:2303]>              0          1          1
ZERO
            bin <auto[64:95],auto[2048:2303]>                0          1          1
ZERO
            bin <auto[32:63],auto[2048:2303]>                0          1          1
ZERO
            bin <auto[0:31],auto[2048:2303]>                 0          1          1
ZERO
            bin <auto[1024:1055],auto[1024:1279]>            0          1          1
ZERO
            bin <auto[512:543],auto[1024:1279]>              0          1          1
ZERO
            bin <auto[256:287],auto[1024:1279]>              0          1          1
ZERO
            bin <auto[128:159],auto[1024:1279]>              0          1          1
ZERO
            bin <auto[64:95],auto[1024:1279]>                0          1          1
ZERO
            bin <auto[32:63],auto[1024:1279]>                0          1          1
ZERO
            bin <auto[1024:1055],auto[512:767]>              0          1          1
ZERO
            bin <auto[512:543],auto[512:767]>                0          1          1
ZERO
            bin <auto[256:287],auto[512:767]>                0          1          1
ZERO
            bin <auto[128:159],auto[512:767]>                0          1          1
ZERO
            bin <auto[64:95],auto[512:767]>                  0          1          1
ZERO
            bin <auto[1024:1055],auto[256:511]>              0          1          1
ZERO
            bin <auto[128:159],auto[256:511]>                0          1          1
ZERO
```

```
            bin <auto[64:95],auto[256:511]>                  0          1          1
ZERO
            bin <auto[32:63],auto[256:511]>                  0          1          1
ZERO
    Cross #cross__1#                                      0.00%        100          -
ZERO
        covered/total bins:                                  0       1024          -

        missing/total bins:                               1024       1024          -

        % Hit:                                            0.00%       100          -

        type_option.weight=1
        type_option.goal=100
        type_option.comment=
        Auto, Default and User Defined Bins:
            bin <*,*>                                        0          1       1024
ZERO

TOTAL COVERGROUP COVERAGE: 34.81%  COVERGROUP TYPES: 1

Total Coverage By Design Unit (filtered view): 38.36%
```