$\overline{\qquad\qquad\qquad\qquad \text{MODULE } petersons\_algo \qquad\qquad\qquad\qquad}$

EXTENDS *Integers*

VARIABLES $pc0$, $pc1$, $turn$, $intr0$, $intr1$

$TypeOK \triangleq$
$\wedge pc0 \in 0 .. 7$
$\wedge pc1 \in 0 .. 7$
$\wedge turn \in \{0, 1\}$
$\wedge intr0 \in \{\text{TRUE, FALSE}\}$
$\wedge intr1 \in \{\text{TRUE, FALSE}\}$

Model *Peterson*'s Algorithm for 2 processes and check mutual exclusion condition

asynchronous system

for $i = 0, 1$

the algorithm is

```
0 : while(True){
1 :     //non critical section
2 :     intr[i] = True
3 :     turn = 1 − i
4 :     while(turn ≜ 1 and intr[1 − i] ≜ 1)//wait
5 :     //critical section
6 :     intr[i] = 0
7 : }
```

$Init0 \triangleq$
$\wedge turn = 0$
$\wedge intr0 = \text{FALSE}$
$\wedge pc0 = 0$

$Init1 \triangleq$
$\wedge turn = 0$
$\wedge intr1 = \text{FALSE}$
$\wedge pc1 = 0$

$Init \triangleq Init0 \wedge Init1$

$L01 \triangleq$
$\wedge pc0 = 0$
$\wedge pc0' = 1$
$\wedge \text{UNCHANGED } \langle turn, intr0, intr1 \rangle$

$L12 \triangleq$
$\wedge pc0 = 1$
$\wedge pc0' = 2$
$\wedge \text{UNCHANGED } \langle turn, intr0, intr1 \rangle$

$L23 \triangleq$
$\land pc0 = 2$
$\land pc0' = 3$
$\land intr0' = \text{TRUE}$
$\land \text{UNCHANGED} \langle intr1, turn \rangle$

$L34 \triangleq$
$\land pc0 = 3$
$\land pc0' = 4$
$\land turn' = 1$
$\land \text{UNCHANGED} \langle intr0, intr1 \rangle$

$L44 \triangleq$
$\land pc0 = 4$
$\land pc0' = 4$
$\land turn = 1$
$\boxed{\land turn' = 1}$
$\land intr1 = \text{TRUE}$
$\boxed{\land intr1' = \text{TRUE}}$
$\land \text{UNCHANGED} \; intr0$

$L45 \triangleq$
$\land pc0 = 4$
$\land pc0' = 5$
$\land (turn = 0 \lor intr1 = \text{FALSE})$
$\land \text{UNCHANGED} \langle turn, intr0, intr1 \rangle$

$L56 \triangleq$
$\land pc0 = 5$
$\land pc0' = 6$
$\land \text{UNCHANGED} \langle intr0, intr1, turn \rangle$

$L67 \triangleq$
$\land pc0 = 6$
$\land pc0' = 7$
$\land intr0' = 0$
$\land \text{UNCHANGED} \langle intr1, turn \rangle$

$L70 \triangleq$
$\land pc0 = 7$
$\land pc0' = 0$
$\land \text{UNCHANGED} \langle turn, intr0, intr1 \rangle$

$SLOGP \triangleq \text{UNCHANGED} \langle pc0, intr0, intr1, turn \rangle$

for the second system

$M01 \triangleq$

$\wedge\ pc1 = 0$
$\wedge\ pc1' = 1$
$\wedge$ UNCHANGED $\langle turn,\ intr0,\ intr1 \rangle$

$M12\ \triangleq$
$\wedge\ pc1 = 1$
$\wedge\ pc1' = 2$
$\wedge$ UNCHANGED $\langle turn,\ intr0,\ intr1 \rangle$

$M23\ \triangleq$
$\wedge\ pc1 = 2$
$\wedge\ pc1' = 3$
$\wedge\ intr1' =$ TRUE
$\wedge$ UNCHANGED $\langle intr0,\ turn \rangle$

$M34\ \triangleq$
$\wedge\ pc1 = 3$
$\wedge\ pc1' = 4$
$\wedge\ turn' = 0$
$\wedge$ UNCHANGED $\langle intr0,\ intr1 \rangle$

$M44\ \triangleq$
$\wedge\ pc1 = 4$
$\wedge\ pc1' = 4$
$\wedge\ turn = 0$
$\boxed{\wedge\ turn' = 0}$
$\wedge\ intr0 =$ TRUE
$\boxed{\wedge\ intr0' =$ TRUE$}$
$\wedge$ UNCHANGED $intr1$

$M45\ \triangleq$
$\wedge\ pc1 = 4$
$\wedge\ pc1' = 5$
$\wedge\ (turn = 1 \vee intr0 =$ FALSE$)$
$\wedge$ UNCHANGED $\langle turn,\ intr0,\ intr1 \rangle$

$M56\ \triangleq$
$\wedge\ pc1 = 5$
$\wedge\ pc1' = 6$
$\wedge$ UNCHANGED $\langle intr0,\ intr1,\ turn \rangle$

$M67\ \triangleq$
$\wedge\ pc1 = 6$
$\wedge\ pc1' = 7$
$\wedge\ intr1' = 0$
$\wedge$ UNCHANGED $\langle intr0,\ turn \rangle$

$M70 \triangleq$
$\wedge\ pc1 = 7$
$\wedge\ pc1' = 0$
$\wedge$ UNCHANGED $\langle turn,\ intr0,\ intr1 \rangle$

$SLOGQ \triangleq$ UNCHANGED $\langle pc1,\ intr0,\ intr1,\ turn \rangle$

$Next\_First \triangleq$
$\vee\ L01$
$\vee\ L12$
$\vee\ L23$
$\vee\ L34$
$\vee\ L45$
$\vee\ L56$
$\vee\ L67$
$\vee\ L70$
$\vee\ SLOGP$

$Next\_Second \triangleq$
$\vee\ M01$
$\vee\ M12$
$\vee\ M23$
$\vee\ M34$
$\vee\ M45$
$\vee\ M56$
$\vee\ M67$
$\vee\ M70$
$\vee\ SLOGQ$

$Next \triangleq (Next\_First \wedge$ UNCHANGED $pc1) \vee (Next\_Second \wedge$ UNCHANGED $pc0)$

$Mutual\_Exclusion \triangleq (pc0 \neq 5) \vee (pc1 \neq 5)$

we need justice conditions, because here in this example, it can happen that
the scheduler never schedules one process
we want to avoid such runs ?????

justice conditions

$J00 \triangleq pc0 \neq 0$
$J02 \triangleq pc0 \neq 2$
$J03 \triangleq pc0 \neq 3$

we cannot write $pc0 \neq 4$, because that's not a requirement, it should be proven
$J04 \triangleq \neg((pc0 = 4) \wedge ((turn = 0) \vee (intr1 = \text{FALSE})))$
$J05 \triangleq pc0 \neq 5$
$J06 \triangleq pc0 \neq 6$

$J07 \triangleq pc0 \neq 7$

$J10 \triangleq pc1 \neq 0$
$J12 \triangleq pc1 \neq 2$
$J13 \triangleq pc1 \neq 3$

$J14 \triangleq \neg((pc1 = 4) \wedge ((turn = 0) \vee (intr0 = \text{FALSE})))$
$J15 \triangleq pc1 \neq 5$
$J16 \triangleq pc1 \neq 6$
$J17 \triangleq pc1 \neq 7$

the below justice conditions are to ensure that the scheduler is fair

$J \triangleq$
$\wedge J00$
$\wedge J02$
$\wedge J03$
$\wedge J04$
$\wedge J05$
$\wedge J06$
$\wedge J07$
$\wedge J10$
$\wedge J12$
$\wedge J13$
$\wedge J14$
$\wedge J15$
$\wedge J16$
$\wedge J17$

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