|  |
| --- |
| TRƯỜNG ĐẠI HỌC BÁCH KHOA HÀ NỘI  **VIỆN ĐIỆN TỬ - VIỄN THÔNG**  logo_128  **Binary multiplier**  *Design Specification*    ***Revision 1.10***  **13/01/2022** |

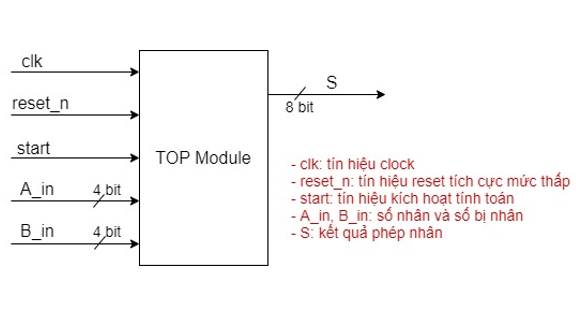
1. **Design Specification**

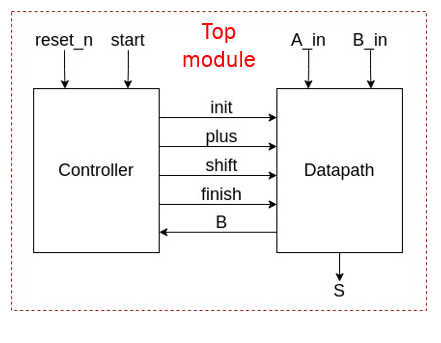
• Đầu vào: 2 số nhị phân n bit A, B

• Đầu ra: tích 2 số A và B

• Máy trạng thái kèm luồng dữ liệu: Finite State Machine with Datapath (FSMD)

• Parameterized binary multiplie





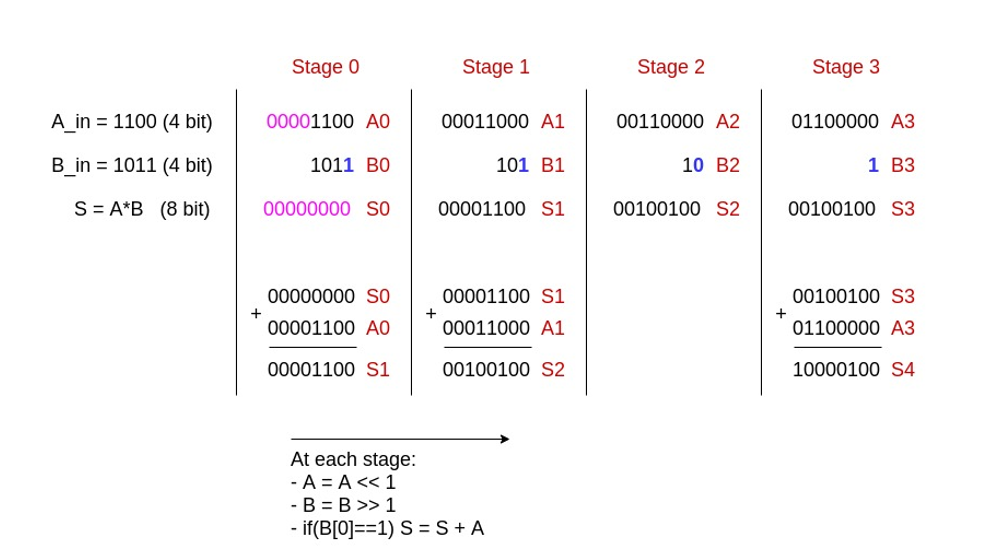
Hình 1: Top Module

1. **Interface signals**

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal name** | Width | I/O | Description |
| Clk | 1 | I | DTI clock Signal |
| Reset\_n | 1 | I | DTI Asynchronous Reset, active LOW |
| Start | 1 | I | Start to calculate |
| A | n | I | Multiplicand |
| B | n | I | Multipiler |
| S | 2n | O | Product of a and b |

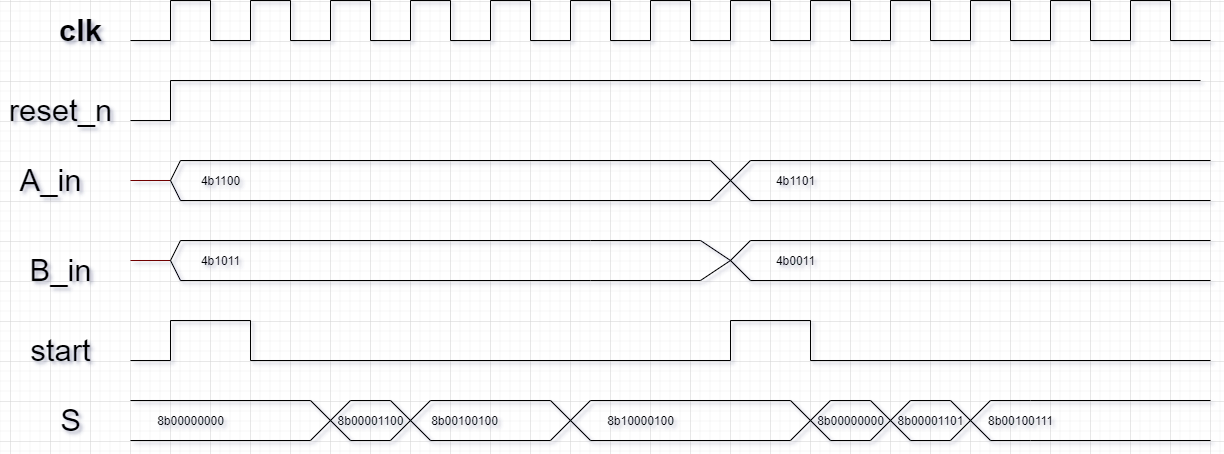
Table 1. signal table

1. **Algorithm**



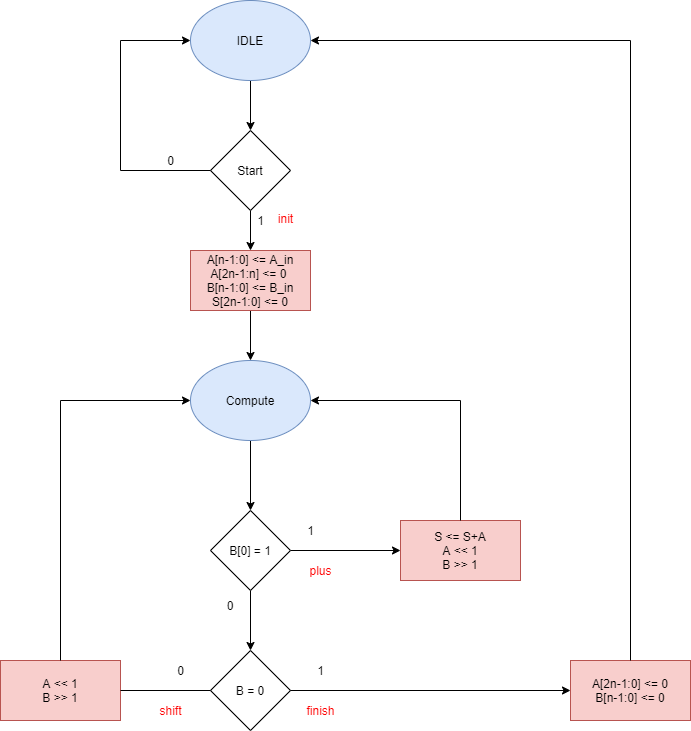
*Hình 3: Algorithm of multi4bit*

1. **Timming diagram**

****

*Hình 2: Timming diagram*

1. **FSMD**



*Hình 4: FSMD of multinbit*