RAMAIAH
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"Design and Optimization of a High-Gain, High-Performance Three-Stage CMOS Amplifier in 90nm Technology"

Submitted as part of Mini project (22ECP67)

BACHELOR OF ENGINEERING

in

Electronics and Communication

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2025

CERTIFICATE

This is to certify that the project work titled **"Design and Optimization of a High-Gain, High-Performance Three-Stage CMOS Amplifier in 90nm Technology"** is carried out by A R Santosh Kumar (1MS22EC002), K Naveen (1MS22EC057), Kishan C (1MS22EC061), Krishna (1MS22EC064) Bonafide students of Ramaiah Institute of Technology, Bangalore, as part of Mini-project work carried out in sixth semester of Bachelor of Engineering in Electronics and Communication during the year 2025. It is certified that all corrections / suggestions indicated for Internal Assessment have been incorporated in the report. The report has been approved as it satisfies the academic requirements prescribed.

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2)

DECLARATION

We hereby declare that the mini project entitled **"Design and Optimization of a High-Gain, High-Performance Three-Stage CMOS Amplifier in 90nm Technology"** has been carried out independently at Ramaiah Institute of Technology under the guidance of **Manjunath C Lakkannavar,** Assistant Professor, Department of Electronics and Communication Engineering, RIT, Bangalore.

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We sincerely thank all the faculty members of Department of E&C, RIT for their kind support to carry out this project successfully.

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ABSTRACT

This project presents the design, simulation, and optimization of a high-gain, three-stage CMOS amplifier implemented in 90nm technology, targeting robust performance for analog signal processing applications. The amplifier architecture comprises a differential input stage for good common-mode rejection, a common-source second stage for primary gain enhancement, and a common-drain output buffer for load driving. Stability for this multi-pole system is achieved using a carefully tuned Nested Miller Compensation network, with a design focus on maximizing DC gain and ensuring excellent phase margin while driving a substantial capacitive load. Cadence Virtuoso was utilized for detailed transistor-level design and comprehensive simulation, with LTspice employed for initial conceptual verification. The final design, when driving a 5 pF load, achieves a DC open-loop gain of approximately 85 dB, an exceptional phase margin of 70 degrees, and a corresponding unity-gain bandwidth of 6.482 kHz, while consuming 840.096uW of power. These results validate the design methodology and the amplifier's suitability for applications requiring high gain and stable operation with significant capacitive loads, such as sensor interface circuits or analog front-ends.

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Acronym	Abbreviation
CD	Common Drain
CS	Common Source
GBW	Gain Bandwidth
NMC	Nested Miller Compensation

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CHAPTER 1

INTRODUCTION AND PROBLEM STATEMENT

1.1 INTRODUCTION

The need for robust and power-efficient analog signal amplification continues to grow with the advancement of modern electronic systems. High-gain amplifiers play a critical role in a variety of applications such as sensor interfaces, biomedical circuits, and analog front-end modules. As CMOS technologies scale down to deep-submicron nodes like **90nm**, the challenges of achieving high gain, stability, and low power operation become more prominent.

This project focuses on the **design and optimization of a high-gain, high-performance three-stage CMOS amplifier implemented in 90nm technology**. The amplifier comprises three main stages:

1. A **differential input stage** for initial signal amplification and common-mode rejection.
2. A **common-source second stage** for gain boosting, and
3. A **common-drain output buffer** for low output impedance.

To ensure frequency stability across the entire gain path, **nested Miller compensation** has been applied and optimized through iterative simulation and tuning.

The final design demonstrates a **DC gain of ~85 dB**, a **phase margin of 70°**, and operates stably at a **bandwidth of approximately 6.482 kHz** when driving a **5 pF load**, all while consuming only **~840mW of power**. These results align well with analog design goals in deep-submicron technology, balancing performance, stability, and efficiency.

The entire design flow was carried out using **Cadence Virtuoso** in the 90nm GPDK, with simulations including AC, DC, and transient analysis. This work demonstrates a practical, optimized approach to multi-stage analog amplifier design in modern CMOS processes.

1.2 PROBLEM STATEMENT

Problem

Designing an amplifier that achieves high gain without compromising stability or efficiency in 90nm CMOS technology.

As technology scales, challenges such as reduced intrinsic gain, short-channel effects, and limited output swing make it increasingly difficult to meet analog performance requirements. This project addresses these limitations through a carefully optimized three-stage architecture with appropriate compensation.

Relevance

Designing high-gain and stable amplifiers in 90nm CMOS is critical for modern analog front-end systems, especially in sensor interfaces, biomedical circuits, and mixed-signal SoCs. Despite scaling challenges, 90nm remains a widely used node in low-power and cost-sensitive applications, making this amplifier design both practically valuable and academically relevant.

1.3 SCOPE

1.Technology Scope

- The project is implemented using **90nm CMOS process**, which offers a good balance between performance and power efficiency.
- Focuses on overcoming **short-channel effects** and **reduced intrinsic gain** typical in deep-submicron nodes.

2. Design Scope

- Involves the complete design of a **three-stage amplifier** consisting of:
- A differential amplifier (Stage 1)
- A common-source gain stage (Stage 2)
- A source follower output buffer (Stage 3)
- Integration of **nested Miller compensation** to ensure stability in multi-stage architecture.

3. Simulation and Optimization Scope

- Includes **DC, AC, transient**, and **corner simulations** to verify gain, phase margin, power, and bandwidth.
- Optimization of transistor sizing and biasing for performance enhancement.
- Design is validated under a capacitive load of **5 pF** with bandwidth target of **6.482 kHz**.

4. Tool Scope

- **Cadence Virtuoso** is used for schematic design, bias setup, simulation, and verification using 90nm GPDK.Ensures industry-relevant skills in transistor-level analog design workflows.

5. Application Scope

- Amplifier design is suitable for:
- **Sensor readout circuits**
- **Biomedical signal amplification**
- **Analog signal conditioning** in mixed-signal SoCs.

CHAPTER 2 : BACKGROUND

2.1 LITERATURE SURVEY

The below mentioned research papers are taken as a reference:

[1] "Design of a Low Power Three-Stage Amplifier in 90nm" (2021)

Full Title:
Design of a Low Power Three-Stage Amplifier in 90nm

Authors:
Bharathesh Patel N, Manju Devi

Conference & DOI:
2021 5th International Conference on Electrical, Electronics, Communication, Computer Technologies and Optimization Techniques (ICEECCOT)
DOI:: 10.1109/ICEECCOT52851.2021.9708042

Technology & Supply:
90 nm CMOS (1.2 V supply) and 180 nm CMOS (1.8 V supply)

Key Findings:

- DC Gain (90 nm): 82 dB
- Phase Margin (90 nm): 63°
- Power Consumption (90 nm): 628.4 μW
- Output swing (90 nm): 325 mV peak-to-peak
- Proposed a novel compensation technique: Double Active Capacitive Feedback Compensation (DACFC)
- DACFC achieved better frequency stability with lower capacitor area
- Gain (180 nm): 120 dB; Phase Margin: 71°
- Demonstrated successful operation with large capacitive loads (as in LDOs)

Key Contributions/Learnings for Our Project:

- Introduced DACFC, a new compensation approach for three-stage amplifiers driving large capacitive loads with improved phase margin.
- Demonstrated clear performance comparison between 180 nm and 90 nm CMOS implementations, highlighting limitations and optimizations in scaled technology.
- Validated the ability of the DACFC scheme to reduce compensation capacitor size and die area, addressing power and area constraints in SoC applications.

- Reinforced the relevance of three-stage architectures for low-voltage analog applications such as LDOs, where large capacitive loads are common.
- Showed that 90 nm implementation can achieve acceptable gain and stability metrics using innovative compensation strategies under area and power limits.

[2] "A Three-Stage CMOS Operational Amplifier with High Gain and Phase Margin" (2021)

Full Title: A Three-Stage CMOS Operational Amplifier with High Gain and Phase Margin

Authors:
Prakash Chandra, Urvashi Bansal

Conference & DOI:
2021 International Conference on Industrial Electronics Research and Applications (ICIERA)
DOI: 10.1109/ICIERA53202.2021.9726738

Technology & Supply:
0.18 µm (180 nm) CMOS, 1.8 V Power Supply

Key Findings:

- Open-loop gain: 122 dB
- Unity Gain Bandwidth (GBW): 2.77 MHz
- Phase Margin (PM): 82.61°
- Load capacitance handled: 125 pF
- Compensation capacitor: 0.4 pF
- Slew rate: 1.29 V/µs
- Biasing achieved without external current sources (uses supply only)

Key Contributions/Learnings for Our Project:

- Presents a compact and high-gain three-stage op-amp optimized for large capacitive load driving.
- Introduces a differential amplifier-based frequency compensation technique in the feedforward path, reducing die area.
- Achieves superior gain and phase margin using a very small Miller capacitor (0.4 pF), highlighting an efficient compensation approach.
- Provides performance benchmarking against other multistage op-amps in 0.18 µm CMOS, showing better GBW, PM, and die-area efficiency.
- Demonstrates an op-amp topology well-suited for high-performance analog systems requiring both high DC gain and output swing under large capacitive loads.

[3] "Design of a Novel CMOS Instrumentation Amplifier Using 90 nm Technology" (2024)

Full Title:
Design of a Novel CMOS Instrumentation Amplifier Using 90 nm Technology

Authors:
Divya Sharma, Vijay Nath

Journal & DOI:
Microsystem Technologies, Volume 31 (2025), Pages 447–459
DOI: 10.1007/s00542-024-05739-3

Technology & Supply:
UMC 90 nm CMOS process, ±0.9 V power supply

Key Findings:

- Differential gain: 97.69 dB
- Common Mode Rejection Ratio (CMRR): 135.72 dB
- Layout area with pads: 79.005 µm × 85.17 µm
- Low power dissipation with improved signal gain
- NMOS used as active loads instead of resistors

Key Contributions/Learnings for Our Project:

- Demonstrates use of NMOS in linear region as active resistive loads to save area and increase gain.
- Highlights effectiveness of instrumentation amplifiers for applications requiring high gain and CMRR.
- Reinforces advantages of active load design in reducing power and die area.
- Shows potential of 90 nm CMOS for achieving high precision analog performance.
- Useful benchmark for gain and CMRR in biomedical and low-voltage analog

[4] "Design and Comparative Analysis of a Two-Stage Ultra-Low-Power Subthreshold Operational Amplifier in 180 nm, 90 nm, and 45 nm Technology" (2020)

Full Title:
Design and Comparative Analysis of a Two-Stage Ultra-Low-Power Subthreshold Operational Amplifier in 180 nm, 90 nm, and 45 nm Technology

Authors:
Sumukh Nitundil, Nihal Singh, Rushabha Balaji, Pankaj Arora

Repository & DOI:
arXiv preprint arXiv:2012.12088v1
arxiv.org/abs/2012.12088

Technology & Supply:
180 nm, 90 nm, and 45 nm CMOS; 0.5 V Supply Voltage

Key Findings:

- DC Gain: 60.86 dB (180 nm), 74.21 dB (90 nm), 73.48 dB (45 nm)
- Phase Margin: 63.5° (180 nm), 73.58° (90 nm), 76° (45 nm)
- Unity Gain Bandwidth: ~27.5 kHz (180 nm), ~31.6 kHz (90 nm & 45 nm)
- Power Consumption: 107.88 nW (180 nm), 131.83 nW (90 nm), 140.3 nW (45 nm)
- Slew Rate: 27.71 mV/µs (180 nm), 22.28 mV/µs (90 nm), 33.17 mV/µs (45 nm)
- Designed using subthreshold MOSFET operation and Miller compensation
- Optimized for biomedical applications (ECG, neural sensing)

Key Contributions/Learnings for Our Project:

- Demonstrates effectiveness of subthreshold operation for ultra-low-power and high-gain amplifier design.
- Compares amplifier performance across three CMOS nodes, showing 90 nm offers a balanced trade-off between gain and power.
- Provides a scalable, low-voltage design methodology suitable for biomedical front-ends such as implantable devices.
- Validates use of Miller compensation for stability in two-stage amplifiers under subthreshold conditions.
- Shows that ultra-low power consumption (<150 nW) is achievable with reasonable phase margin and gain in modern CMOS nodes.

[5] "Design Trade-Offs in Common-Mode Feedback Implementations for Highly Linear Three-Stage Operational Transconductance Amplifiers" (2021)

Full Title: Design Trade-Offs in Common-Mode Feedback Implementations for Highly Linear Three-Stage Operational Transconductance Amplifiers

Authors: Joseph Riad, Sergio Soto-Aguilar, et al.

Journal & DOI: Electronics 2021, 10, 991. DOI: 10.3390/electronics10090991

Technology & Supply (Case Study): 180nm CMOS, 1.8V Power Supply

Key Findings:

- Compares single-loop vs. multi-loop CMFB for 3-stage fully differential OTAs.
- Multi-loop CMFB can offer superior linearity (>6 dB P1dB improvement).
- Single-loop CMFB stability can be challenging and impact overall performance.
- Noise performance similar for both CMFB approaches with equal power.
- Case study in 180nm demonstrates CMFB impact in an active-RC filter.

Key Contributions:

- Highlights CMFB's critical impact on OTA performance (even if ours is SE output).
- Illustrates detailed trade-off analysis in analog design.
- Provides 180nm context for high-speed OTA considerations.
- Emphasizes linearity as a key performance metric in specific applications.

[6] "An Enhanced ACBC Three-Stage Amplifier Using Complementary Indirect Miller Compensation" (2023)

Full Title:
An Enhanced ACBC Three-Stage Amplifier Using Complementary Indirect Miller Compensation

Authors:
Johannes Weber, Lei Zhang, Pengcheng Xu, David Borggreve, Frank Vanselow, Eckhard Hennig

Conference & DOI:
2023 30th IEEE International Conference on Electronics, Circuits and Systems (ICECS)
DOI: 10.1109/ICECS58634.2023.10574859

Technology & Supply:
GlobalFoundries 22FDX (22 nm FD-SOI technology), 0.72 V supply (post-layout worst case, 10% reduced)

Key Findings:

- DC Gain: 103.5 dB
- GBW: 8.5 MHz
- Phase Margin: 41.4°
- Load capacitance driven: 500 pF
- Power efficiency (IFOMs): 231k MHz·pF/mW
- Total current consumed: 18.7 µA including bias network
- Compensation used: Enhanced AC Boosting Compensation (ACBC) with complementary indirect Miller network
- Robust performance under ss-corner at 125 °C with reduced VDD

Key Contributions/Learnings for Our Project:

- Introduces a novel complementary indirect Miller compensation technique that enhances traditional ACBC methods for improved stability and efficiency.
- Demonstrates superior power-efficiency (2× improvement in IFOMs) over conventional three-stage designs using ACBC.
- Successfully drives large capacitive loads (500 pF) while maintaining high gain and moderate bandwidth.
- Highlights challenges of pole-zero management in multi-stage designs and addresses them using advanced compensation.
- Provides a benchmark for low-voltage, energy-efficient analog amplifier design in FD-SOI technology nodes.

[7] "Three Stage Class AB Power Amplifier in 90 nm CMOS Process for IoT Applications" (2020)

Full Title:
Three Stage Class AB Power Amplifier in 90 nm CMOS Process for IoT Applications

Authors:
Maliha Elma, Nahid Hossain Antu, Tanvir Ahmed, Omar Faruqe, Md Tawfiq Amin

Conference & DOI:
2020 IEEE Region 10 Symposium (TENSYMP), Pages 746–749
DOI: 10.1109/TENSYMP50017.2020.9230719

Technology & Supply:
90 nm CMOS process, designed for 2.8 GHz operation targeting IoT and WLAN (802.11n) applications

Key Findings:

- Simulated Output Power: 20.33 dBm
- Power Gain: 20.27 dB
- Power Added Efficiency (PAE): 32.74%
- Frequency of Operation: 2.8 GHz
- Architecture: Fully integrated three-stage Class AB power amplifier
- Achieves linear and efficient performance within WLAN and IoT frequency ranges

Key Contributions/Learnings for Our Project:

- Demonstrates the capability of 90 nm CMOS technology for high-frequency power amplifier integration.
- Highlights the use of a three-stage amplifier architecture for meeting strict linearity and efficiency demands in RF applications.
- Shows effective design targeting IoT and WLAN protocols while maintaining high PAE and power gain.
- Validates the feasibility of combining linear and high-efficiency PA topologies in scaled CMOS nodes.
- Provides a frequency-domain design perspective that complements low-frequency analog amplification efforts.

[8] "Common-Drain CMOS Power Amplifier: An Alternative Power Amplifier" (2017)

Full Title:
Common-Drain CMOS Power Amplifier: An Alternative Power Amplifier

Authors:
Muhammad Abdullah Khan, Renato Negra

Conference & DOI:
2017 47th European Microwave Conference (EuMC)
DOI: 10.23919/EuMC.2017.8231021

Technology & Supply:
130 nm CMOS process; targeted operation frequency: 880 MHz

Key Findings:

- Configuration: Common-Drain Power Amplifier (CDPA)
- Gain: 10.5 dB
- Output 1-dB Compression Point: 27.9 dBm

- Saturated Output Power: 28.5 dBm
- Power Added Efficiency (PAE): 31.9%
- Die Area (including pads): 0.76 mm²
- Stability: Verified by 10-hour test with only 0.15 dB gain deviation

Key Contributions/Learnings for Our Project:

- Introduces a rare CMOS power amplifier topology (common-drain) offering inherent linearity due to voltage-following behavior.
- Demonstrates that CDPA provides better reliability by reducing gate-source voltage stress and improving thermal robustness.
- Achieves high output power with high efficiency, despite CMOS supply limitations—particularly useful for RF/IoT transmit chains.
- Offers a compelling alternative to common-source PAs, which typically suffer from high voltage swings and nonlinearities.
- Reinforces the feasibility of using CDPA in low-frequency (sub-GHz) CMOS RF applications, with measured prototype results validating performance and stability.

[9] "Design and Implementation of Low Noise Amplifier and Variable Gain Amplifier for ECG Systems" (2022)

Full Title:
Design and Implementation of Low Noise Amplifier and Variable Gain Amplifier for ECG Systems

Authors:
Shreelekha Panchal, Shruthi I. T, Sarita Uniyal, Shashidhar Tantry

Conference & DOI:
2022 IEEE 7th International Conference for Convergence in Technology (I2CT)
DOI: 10.1109/I2CT54291.2022.9824947

Technology & Supply:
180 nm CMOS technology, 1.8 V power supply; implemented in Cadence Virtuoso

Key Findings:

- LNA (Low Noise Amplifier) uses a two-phase fully differential OTA architecture.
- LNA Gain: 45.9 dB
- Signal-to-noise ratio (SNR): 18.62 dB (Von), 24.89 dB (Vop)
- Variable Gain Amplifier (VGA) provides additional gain of 25 dB
- Designed for low power operation, making it suitable for wearable biomedical devices.
- Optimized Analog Front-End (AFE) circuit for ECG signal acquisition and processing.

Key Contributions/Learnings for Our Project:

- Highlights the importance of integrating LNAs and VGAs in biomedical analog front ends for high-accuracy ECG acquisition.
- Demonstrates use of fully differential amplifier design for noise suppression and gain control.
- Shows the practical use of 180 nm CMOS technology for low-power biomedical signal

processing.
- Provides valuable metrics for low-noise analog circuit design focused on portable, wearable health monitoring systems.
- Supports analog design goals where power, noise, and gain trade-offs are crucial in real-time biosignal amplification.

[10] "A Transient-Enhanced Output-Capacitor-Free Low-Dropout Regulator With Dynamic Miller Compensation" (2019)

Full Title:
A Transient-Enhanced Output-Capacitor-Free Low-Dropout Regulator With Dynamic Miller Compensation

Authors:
Chenchang Zhan, Guigang Cai, Wing-Hung Ki

Journal & DOI:
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Volume 27, Issue 1, January 2019
DOI: 10.1109/TVLSI.2018.2867850

Technology & Supply:
0.18 μm CMOS process; output-capacitor-free (OCF) LDO design

Key Findings:

- Proposes a Dynamic Miller Compensation (DMC) method using variable Miller capacitors for different load ranges.
- LDO supports up to 100 mA load current with only 8.5 μA quiescent current.
- Undershoot/overshoot with DMC: 38 mV/0.4 μs and 37 mV/1.22 μs respectively (for load transition 100 μA to 100 mA).
- Without DMC: 45 mV/1.3 μs and 200 mV/4.97 μs, demonstrating significant improvement.
- Line transient response also improved with reduced recovery time and voltage deviation.
- Achieves performance enhancements with simple structure and reduced chip area.

Key Contributions/Learnings for Our Project:

- Introduces a scalable and power-efficient compensation strategy (DMC) applicable to three-stage and LDO amplifier topologies.
- Validates the role of adaptive Miller compensation in stabilizing multi-load conditions without sacrificing transient performance.
- Demonstrates low power consumption design while maintaining excellent load regulation and fast response time.
- Reinforces the effectiveness of Miller-based compensation for frequency stability in analog voltage regulation.
- Offers insights for designing analog front-end circuits or amplifiers that must operate reliably under dynamic loads with minimal capacitor usage.

2.2 MOTIVATION AND OBJECTIVES

MOTIVATION

- Modern analog systems in biomedical and portable devices need compact, low-power, high-precision amplifiers.
- Achieving high DC gain in 90 nm CMOS technology is challenging due to reduced intrinsic transistor gain.
- Traditional single-stage amplifiers fall short in meeting performance needs like gain, stability, and bandwidth.
- This project uses multi-stage amplifier topologies along with Miller compensation to overcome these issues.
- The objective is to develop a stable, high-gain amplifier suitable for sensitive and practical analog applications.

OBJECTIVE

Our objective is grounded in the importance of analog amplifiers in interfacing real-world signals with digital systems. These circuits must be carefully designed to maintain high gain, power efficiency, and stability across various operating conditions.

- To design a high-gain multi-stage CMOS amplifier using 90 nm technology.
- To achieve a DC gain close to 90 dB with stable frequency response.
- To implement Nested Miller compensation for improved phase margin and system stability.
- To ensure low power consumption and sufficient output voltage swing.
- To validate performance through schematic and post-layout simulations under PVT variations.

CHAPTER 3
Methodology:

1. Literature Review and Requirement Analysis

- Studied existing multi-stage CMOS amplifier designs and compensation techniques. Identified key performance targets: high voltage gain (>80 dB), phase margin (~70°), low power, and suitable bandwidth.

2. Specification Definition

- Defined parameters such as gain, phase margin, bandwidth, power consumption, and technology constraints for 90nm CMOS.

3. Stage-wise Design Approach

- Stage 1: Designed differential amplifier for high CMRR and initial gain.
- Stage 2: Implemented common-source stage for gain boosting.
- Stage 3: Used common-drain (source follower) for low output impedance and buffering.

4. Frequency Compensation

- Applied Miller compensation with a capacitor and resistor to enhance stability and achieve desired phase margin.

5. Simulation and Iterative Optimization

- Performed DC, AC, transient, and parametric simulations in Cadence Virtuoso. Tuned transistor dimensions, bias currents, and compensation elements to meet target specifications.

6. Performance Validation

- Verified design under process corners and Monte Carlo simulations for robustness.

7. Result Analysis and Application Mapping

- Evaluated final performance and identified suitable real-world applications (e.g., biomedical, sensor front-ends).

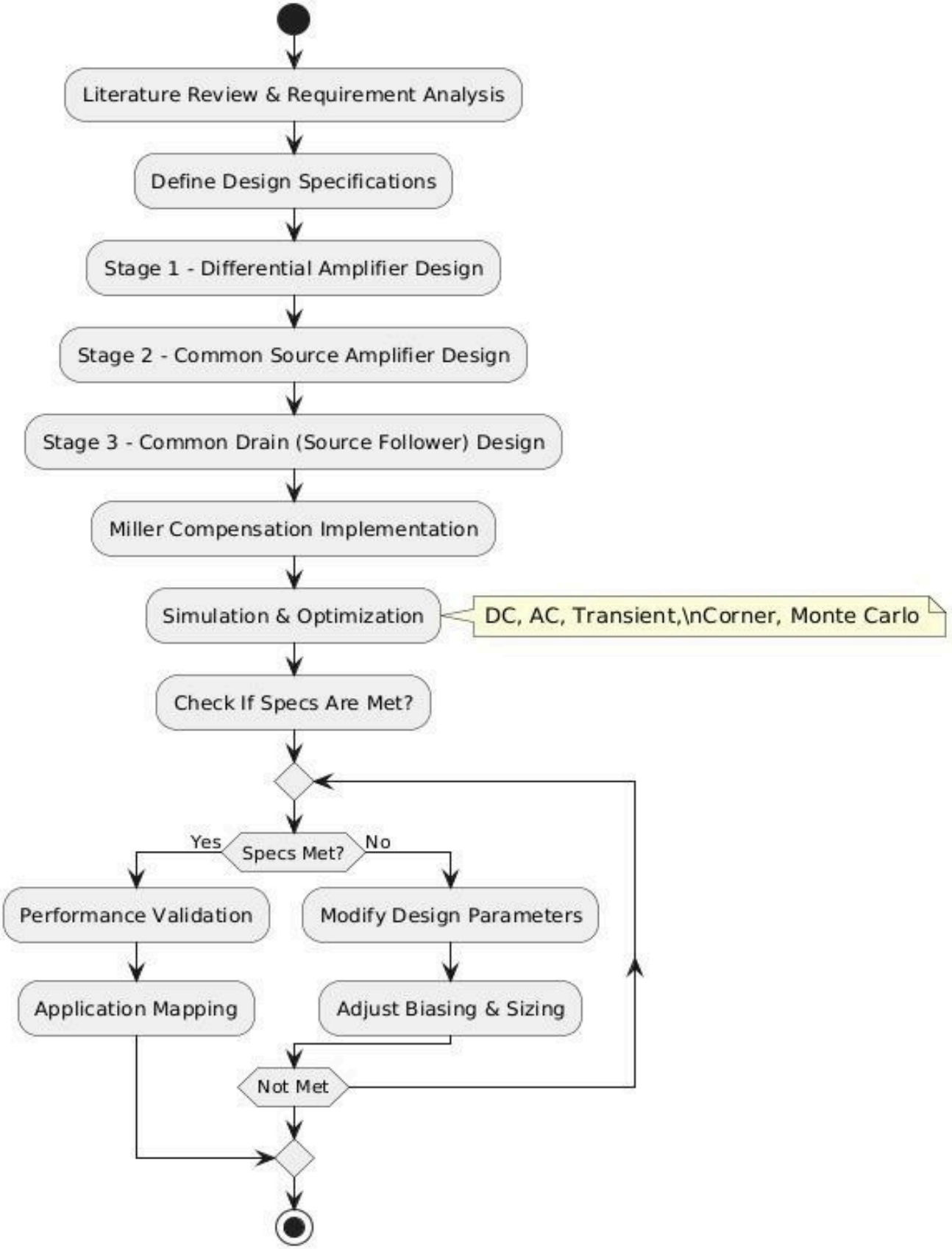

Figure 1 : Flow chart of Methodology

Chapter 4

DESIGN

Design Specifications:

- Overall Gain : >80db
- Phase Margin : > 60 degree
- Power Consumption : < 1mW

DESIGN 1 : 1st Stage

Differential Amplifier:

- **High Gain Foundation in Low-Gain Technology**:
  In 90nm CMOS, the intrinsic gain (gm·ro) is low due to short-channel effects. The differential amplifier, especially with a **PMOS cascode current mirror load**, provides higher output resistance, boosting the gain in the first stage crucial when later stages are operating with low intrinsic gain.

- **Better Noise Performance**:
  The differential pair minimizes low-frequency noise such as flicker (1/f) noise. Since **NMOS transistors** have better noise performance than PMOS, your choice of an **NMOS input pair** further improves the signal-to-noise ratio at the critical first amplification stage.

- **High Common-Mode Rejection Ratio (CMRR)**:
  A differential pair inherently offers high CMRR, making it effective in rejecting noise and interference that may be present equally on both input lines—essential for applications like biomedical and sensor signal processing.

- **Differential Signal Handling**:
  The differential amplifier stage is ideal for amplifying small differential input signals while rejecting common-mode noise. This improves the noise immunity and signal integrity, which is crucial for precision analog applications.

- **Input Impedance and Matching**:
  Differential stages provide high input impedance, which minimizes loading on the previous signal source. Also, symmetry in design ensures good input matching, reducing offset and drift.

- **Initial Gain Boost**:
  The first stage provides a significant portion of the overall voltage gain. By using a differential amplifier with a PMOS current mirror load, the output resistance is increased, thereby enhancing voltage gain.

Formula:

- Transconductance of NMOS Input Pair:

$$g_m = \frac{2I_D}{V_{ov}} = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}$$

- Tail Current Biasing (from Current Mirror):
  ISS=2ID
- Input Common Mode Range (ICMR):

$$V_{ICMR(min)} = V_{SS} + V_{GS,NMOS} + V_{ov,NMOS}$$

$$V_{ICMR(max)} = V_{DD} - V_{SD,PMOS(sat)}$$

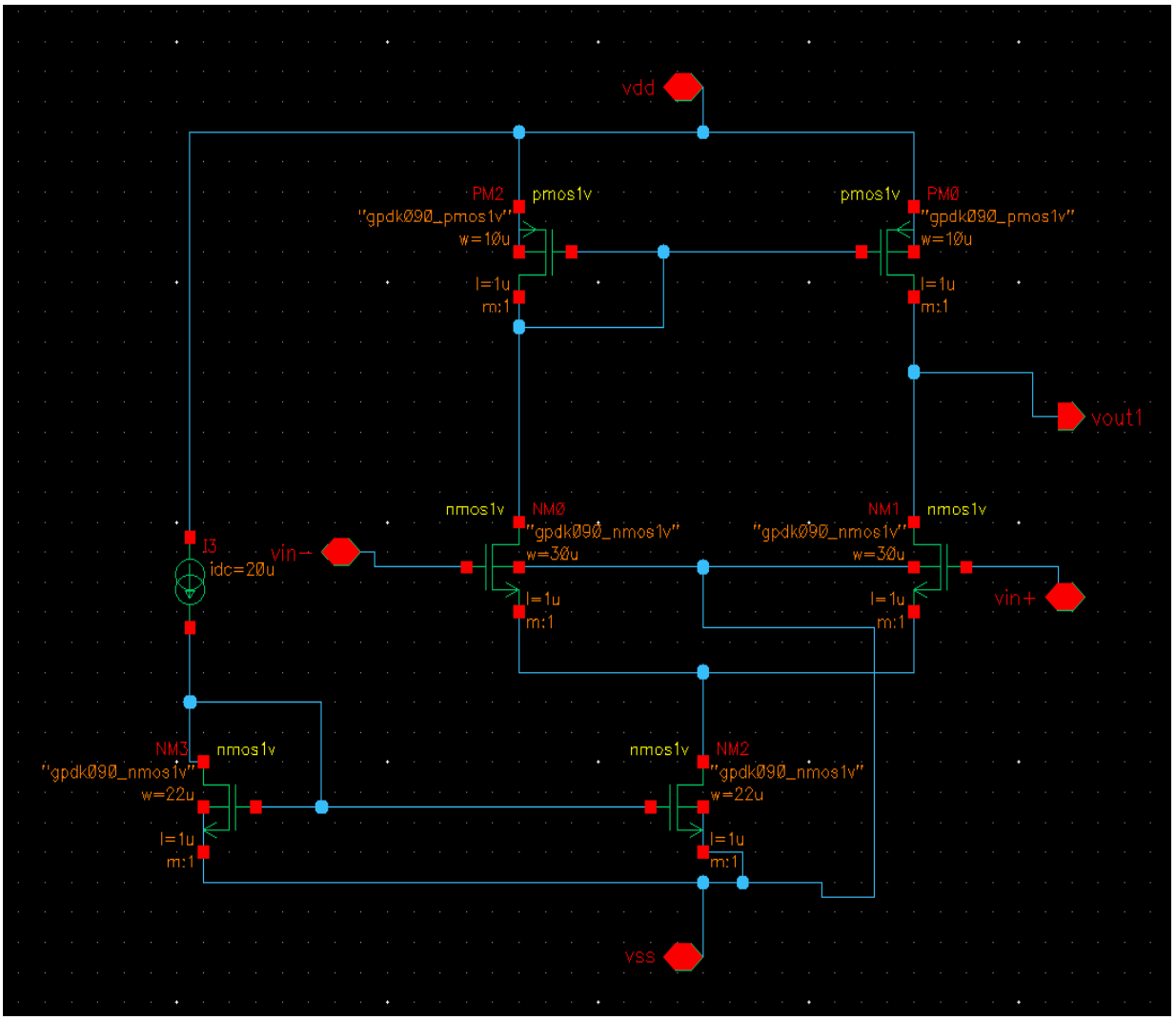

Figure 2 : Differential Amplifier (Stage 1)

DESIGN 2 : 2nd Stage

Common source Amplifier:

- **Gain Enhancement in Cascaded Architecture:**
  The common-source amplifier provides substantial voltage gain, especially important after the differential stage. It boosts the single-ended signal further toward the desired overall gain (~90 dB), compensating for the limited intrinsic gain of devices in 90 nm CMOS.

- **Voltage Swing Improvement:**
  Unlike cascode stages that may limit swing, the CS amplifier allows a wider output voltage swing. This helps in maintaining linearity and ensures the output can drive later stages or loads more effectively.
- **Simple and Efficient Design:**
  The CS configuration is relatively simple to implement and consumes less area and bias current compared to more complex gain stages. This makes it well-suited for low-power and area-constrained applications.
- **Supports Miller Compensation:**
  The output node of the CS stage is ideal for placing Miller compensation capacitors. This configuration introduces a dominant pole and helps control the frequency response, improving phase margin and amplifier stability.
- **Intermediate Impedance Matching:**
  The CS stage presents moderate input and high output impedance, which fits well between the low output impedance of the first differential stage and the low input impedance of the buffer stage. This impedance bridging ensures minimal signal loss.

Formula:

- **Voltage Gain of Common-Source Stage (Av2):**

  $Av_2 = -gm_2 \times Ro_2$

- **Transconductance (gm):**

$$g_m = \frac{2I_D}{V_{ov}} = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}$$

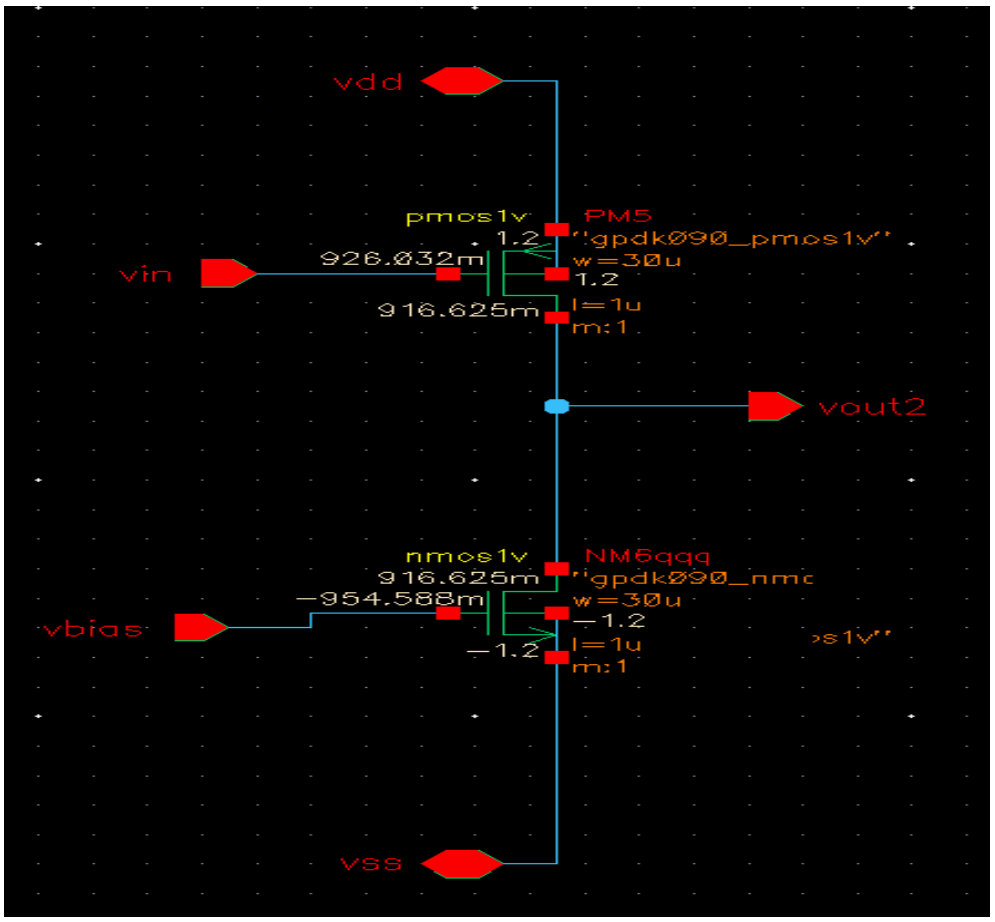

Figure 3 : Common Source Amplifier (2nd stage)

DESIGN 3 : 3rd Stage

Buffer Stage (Common Drain Amplifier):

- **Low Output Impedance for Load Driving:**
  The source follower offers low output impedance, making it ideal for driving capacitive or resistive loads without significant signal loss—essential for delivering a strong, clean output signal.
- **Voltage Buffering with Unity Gain:**
  It provides nearly unity voltage gain (≈1), allowing signal transfer without amplification but with excellent buffering. This helps isolate the gain stages from the load and prevents loading effects
- **Improved Linearity and Swing:**
  The source follower enhances linearity and supports sufficient voltage swing at the output, especially when designed with proper biasing and device sizing.
- **Prevents Signal Degradation:**
  By buffering the high-impedance output of the previous gain stage, it ensures signal integrity is preserved when interfacing with external circuits or measurement equipment.
- **Power and Area Efficient:**
  The configuration is simple and compact, requiring fewer components, making it power- and area-efficient—beneficial for analog front-end systems in portable or biomedical devices.

Formula:

- Voltage Gain (Av):

$$A_v = \frac{g_m \cdot R_{load}}{1 + g_m \cdot R_{load}} \approx 1$$

- Transconductance (gm):

$$g_m = \frac{2I_D}{V_{ov}} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

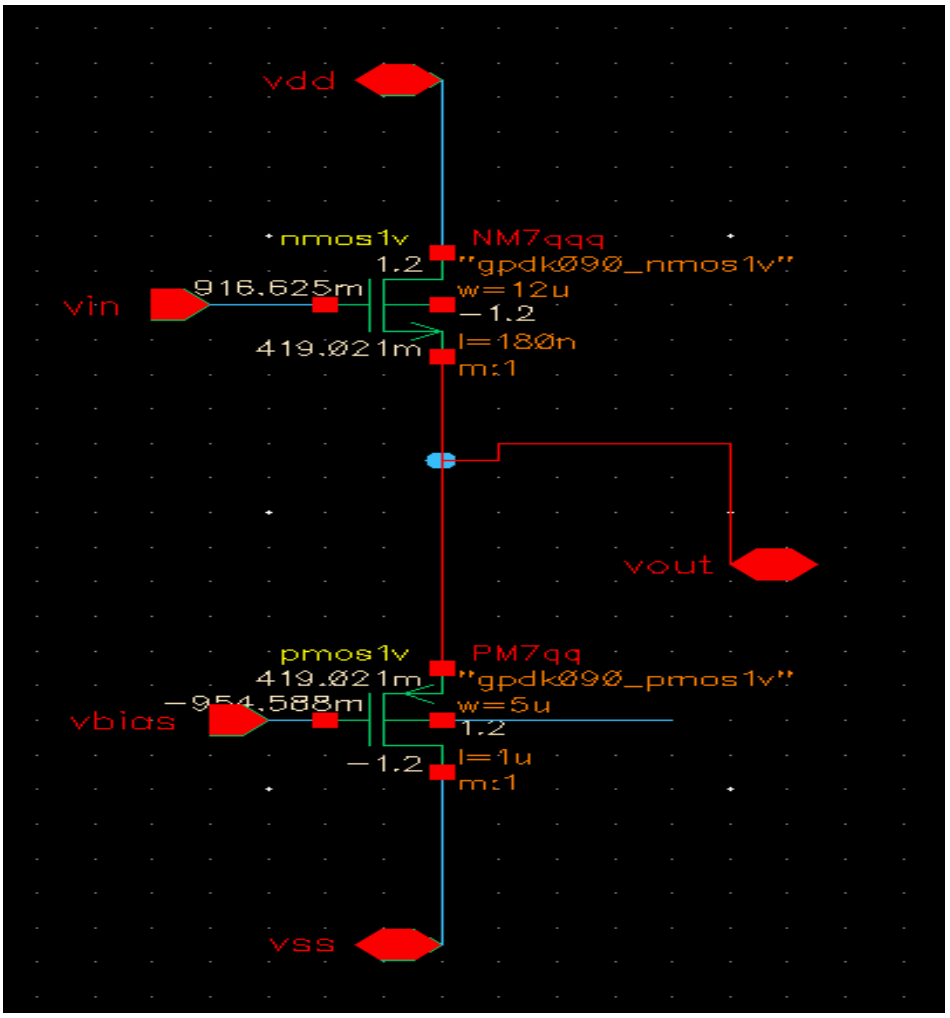

Figure 4: Buffer Stage (Common Drain Amplifier)

DESIGN 4 :

Three Stage Amplifier (Without NMC):

- **Modular and Scalable Design**:
  Each stage can be independently designed, analyzed, and optimized before applying compensation techniques, making this architecture excellent for iterative tuning.

- **Higher Overall Gain**:
  The cascade of three stages (diff amp → CS → buffer) results in a **cumulative high voltage gain**, suitable for applications demanding **>80 dB** gain like data converters and precision analog blocks.

- **Design Simplicity and Debugging**:
  Omitting Miller compensation in early stages simplifies the debugging and analysis process. It allows designers to first establish gain and bandwidth limits without complex pole-zero interactions.

- **Stage Isolation**:
  The use of a source follower ensures that the second stage is **not heavily loaded**, maintaining its gain and dynamic performance even without compensation.

- **Flexible Compensation Insertion**:
  The clear node between stages (especially between stage 2 and 3) offers **ideal locations** for later adding Miller/Nested Miller/Ahuja compensation without requiring major redesign.

- **Good Output Swing and Drive Capability**:
  The buffer stage enhances the amplifier's ability to **drive capacitive loads** and delivers **rail-to-rail output swing**, which is highly desired in low-voltage (1.2V) applications.

- **Benchmark for Performance Comparison**:
  This version serves as a **baseline** to compare how compensation techniques (like Miller, Ahuja, or NMC) improve or trade off between gain, phase margin, and bandwidth.

Formula:

- Total Voltage Gain (Without Compensation):

$$A_v = A_1 \cdot A_2 \cdot A_3$$

If $A_3 \approx 1$, then:

$$A_v \approx A_1 \cdot A_2$$

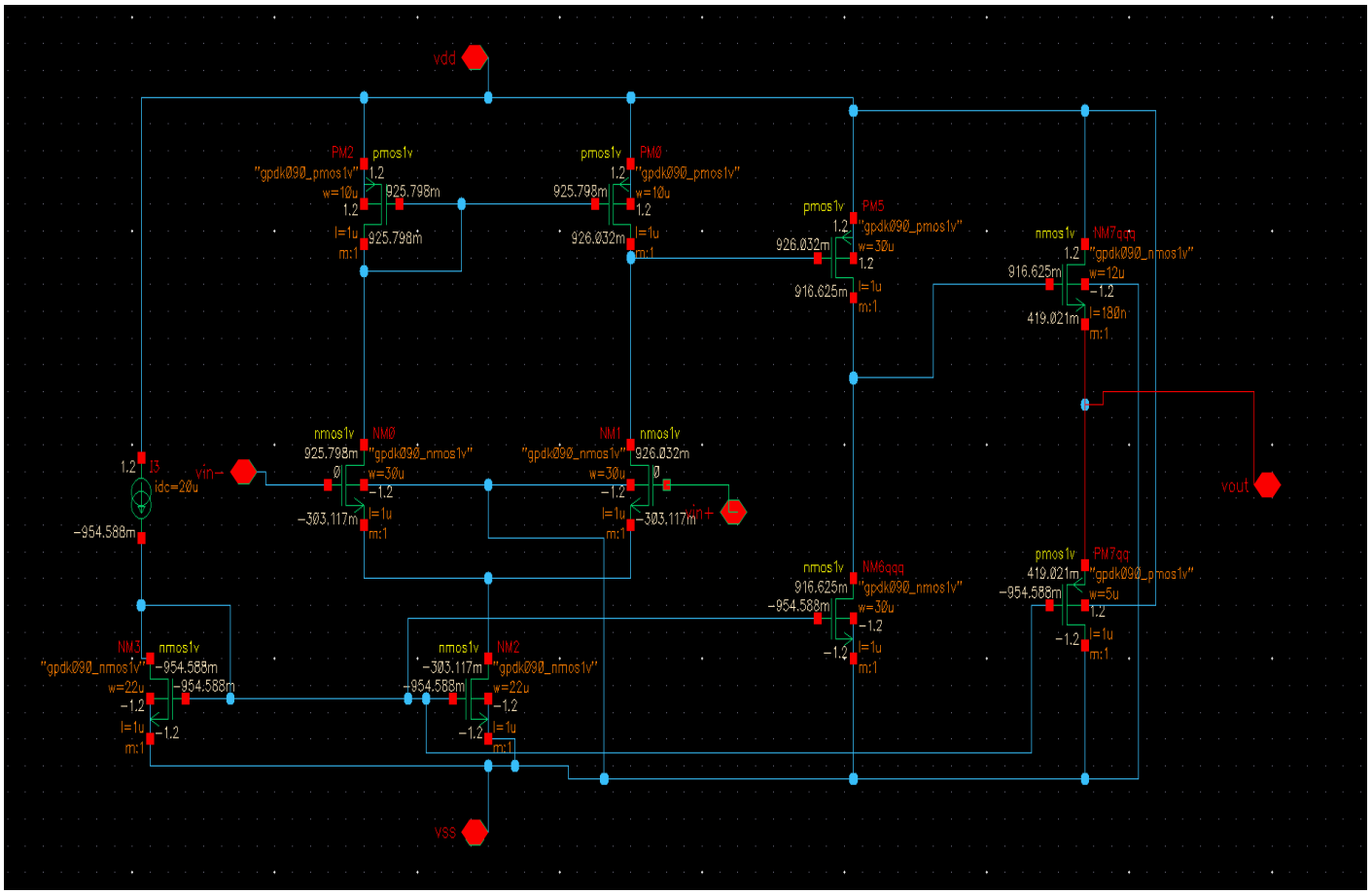

Figure 5: Three Stage Amplifier (Without NMC)

DESIGN 5 :

Three Stage Amplifier (With NMC):

- **Stability for Multi-Stage Amplifier:**

  Without compensation, a three-stage amplifier has multiple high-frequency poles, leading to instability and poor phase margin.

  NMC **introduces dominant pole** and pushes non-dominant poles to higher frequencies, **enhancing phase margin** and ensuring **stable frequency response**.

- **Elimination of Right-Half Plane (RHP) Zero:**

  The resistor Rz in series with the compensation capacitor **shifts the RHP zero to the left-half plane**, avoiding phase lag and improving phase margin.

- **Improved Phase Margin and Bandwidth Balance:**

  Compared to simple Miller compensation, NMC provides **better trade-off** between gain, bandwidth, and stability—often resulting in **phase margins ≥ 60°** and **GBW in the MHz range**.

- **Gain Preservation:**

  Since compensation is placed **between stages**, it does not significantly affect the DC gain of individual stages, preserving the overall gain target (e.g., > 80 dB).

- **Smooth Transition Between Stages:**

  The compensation between the first and second stages **isolates high-frequency interactions** between gain stages, preventing unwanted coupling and phase shifts.
  This helps maintain **consistent phase behavior across operating conditions**.

- **Facilitates High Open-Loop Gain Design**

  The use of NMC supports very **high open-loop gain architectures (≥ 80 dB)** while maintaining phase stability.
  This is beneficial for applications requiring high DC accuracy such as **instrumentation and data converters**.

Formula:

- Dominant Pole (with Compensation Capacitor Cc):

$$f_p \approx \frac{1}{2\pi R_{eq} C_c}$$

- **Miller Approximation of Feedback Capacitance**

  Effective capacitance seen at input of 2nd stage due to Cc:

$$C_{miller} = C_c \cdot (1 + A_2)$$

- Gain-Bandwidth Product (GBW)

$$GBW = \frac{g_{m1}}{2\pi C_c}$$

- **Zero Frequency (with Series Resistor Rz)**

  To eliminate the right-half plane (RHP) zero:

$$f_z = \frac{1}{2\pi R_z C_c}$$

  Rz is chosen so that fzf_zfz lies in the left-half plane (i.e., positive frequency in the s-domain).

- Phase Margin Approximation:

$$PM \approx 180^\circ - \tan^{-1}\left(\frac{GBW}{f_p 2}\right)$$

  Where fp2 is the second non-dominant pole frequency.

  Phase margin improves when dominant pole is well separated from higher-frequency poles.

- Power Consumption:

$$P = V_{DD} \cdot (I_{bias1} + I_{bias2} + I_{bias3})$$

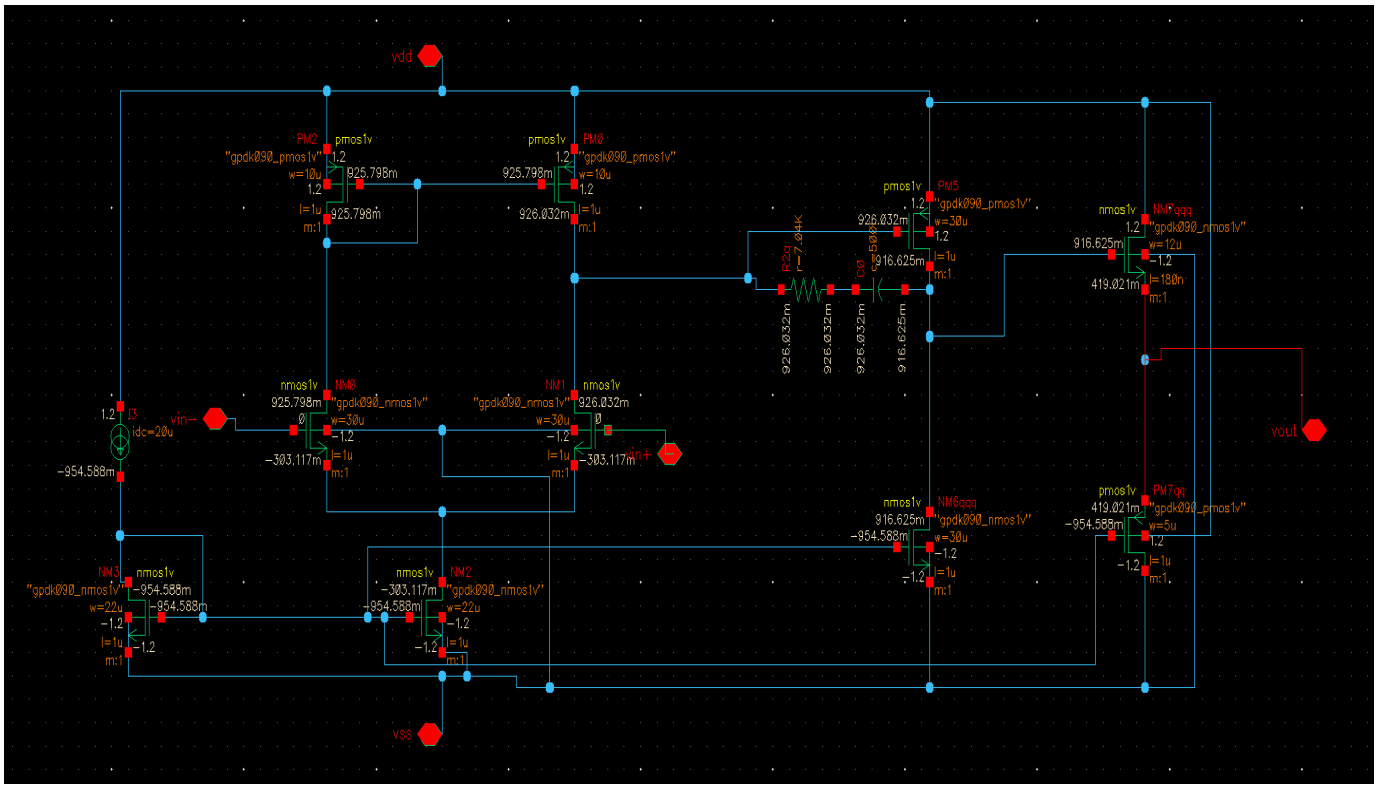

Figure 6: Three Stage Amplifier (With NMC)

Design Values:

Table 1: Input Values

VDD	1.2 V
VSS	-1.2 V
Ibias	20u A

Table 2: Component Values

Transistor Name	**(W/L ratios)**
NM0,NM1	30u/1u
PM0,PM2	10u/1u

NM2,NM3	22u/1u
PM5,NM6	30u/1u
NM7	12u/0.18u
PM7	5u/1u
Compensation Capacitance	500f F
Resistor	7.04k ohm

CHAPTER 5

Results And Discussions

Output Waveforms:

- **Differential Amplifier Gain and Phase plot(1 st stage):**

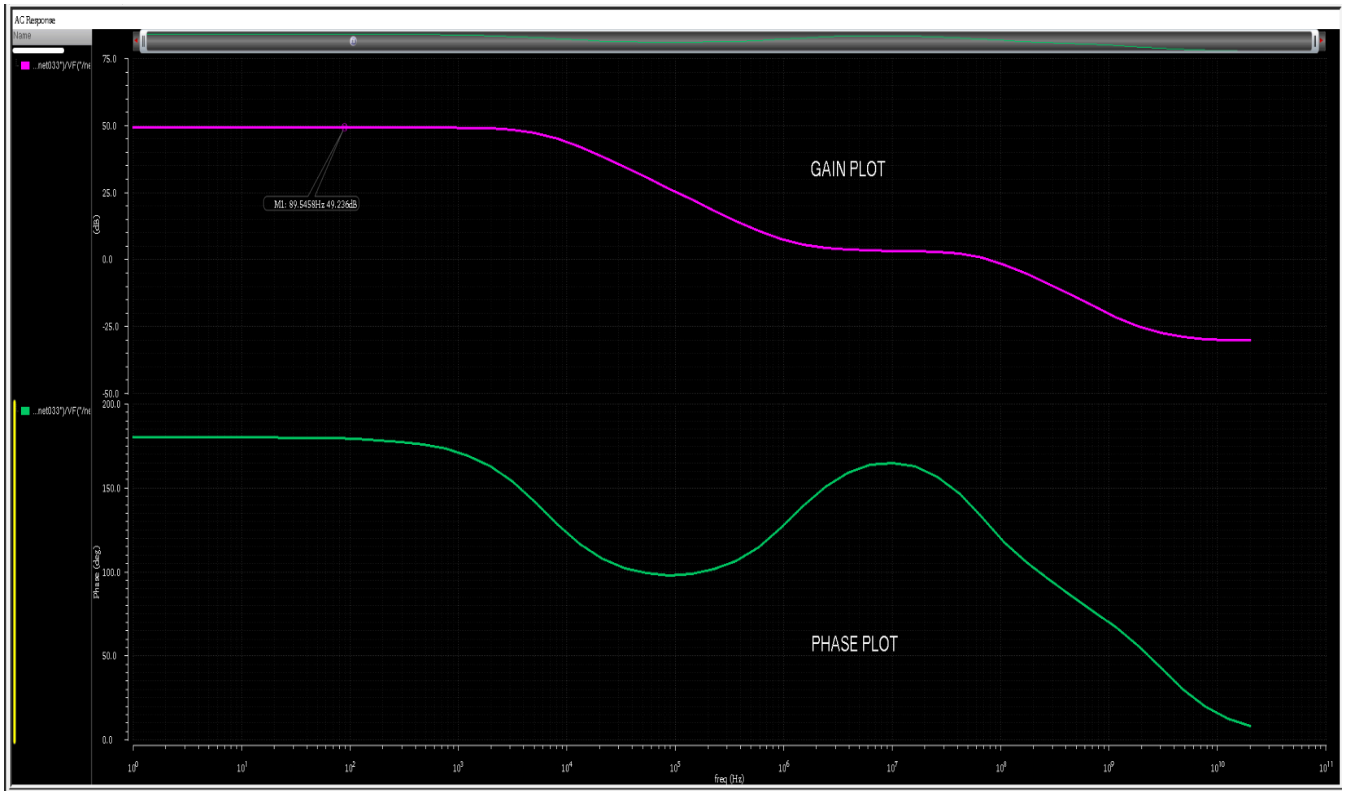

Figure 7: Gain and Phase plot of Differential Amplifier Stage

- **AC Response of Differential Amplifier (First Stage):**

  The above figure shows the **AC gain (in dB)** and **phase response (in degrees)** of the **first stage differential amplifier**. This analysis is performed to evaluate the small-signal frequency response of the stage and to verify its suitability as the input stage of the three-stage amplifier.

- **Gain Plot:**

  The gain remains nearly constant at **49.23 dB** up to a certain frequency (~89.5 Hz), as indicated by the marker.

- **CS amplifier Gain and phase plot (2nd stage):**

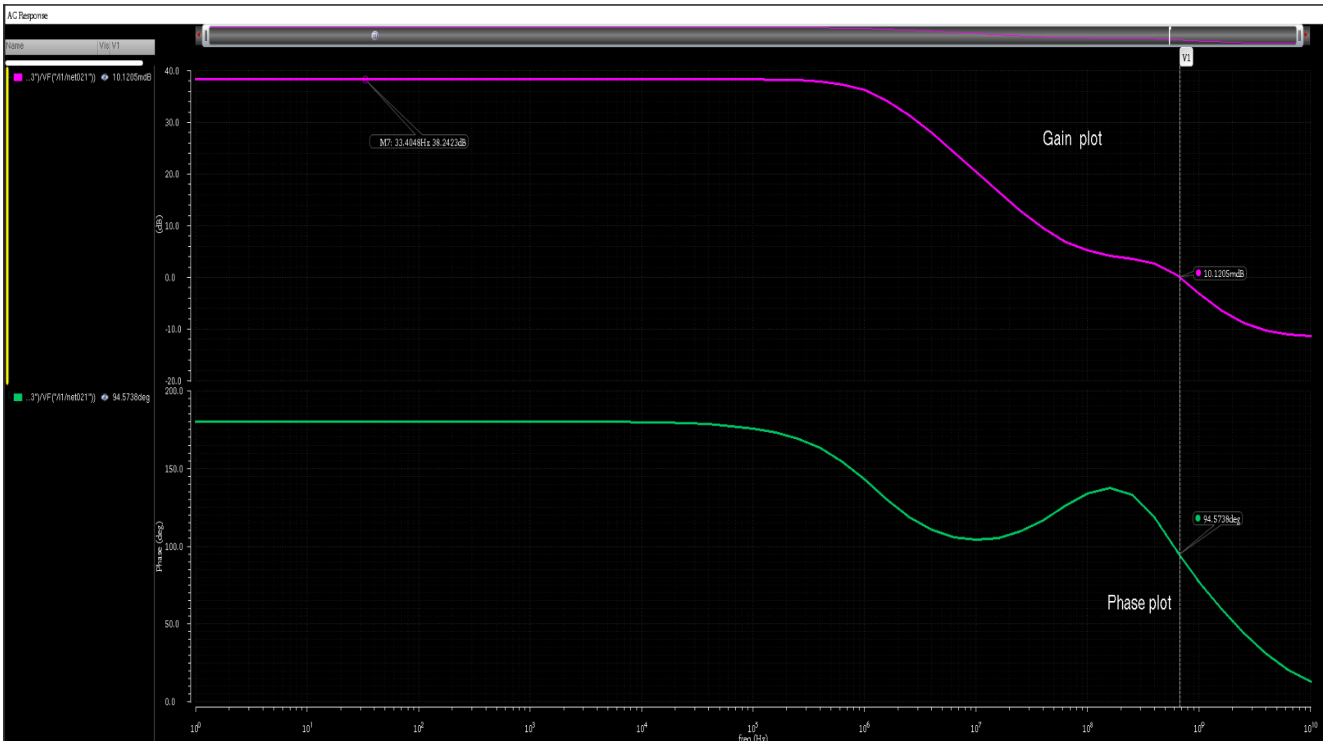

Figure 8: Gain and Phase plot of CS Amplifier Stage

- **AC Response of Common-Source Amplifier (Second Stage)**

  The above figure presents the **gain (dB)** and **phase (degrees)** response of the **second stage common-source amplifier**, which follows the differential input stage in the three-stage amplifier architecture. This analysis highlights the amplifier's frequency behavior, gain contribution.

- The gain of **~39 dB** ensures the stage significantly contributes to the overall high gain of the three-stage amplifier.

- **CD amplifier Gain and phase plot (3rd stage):**

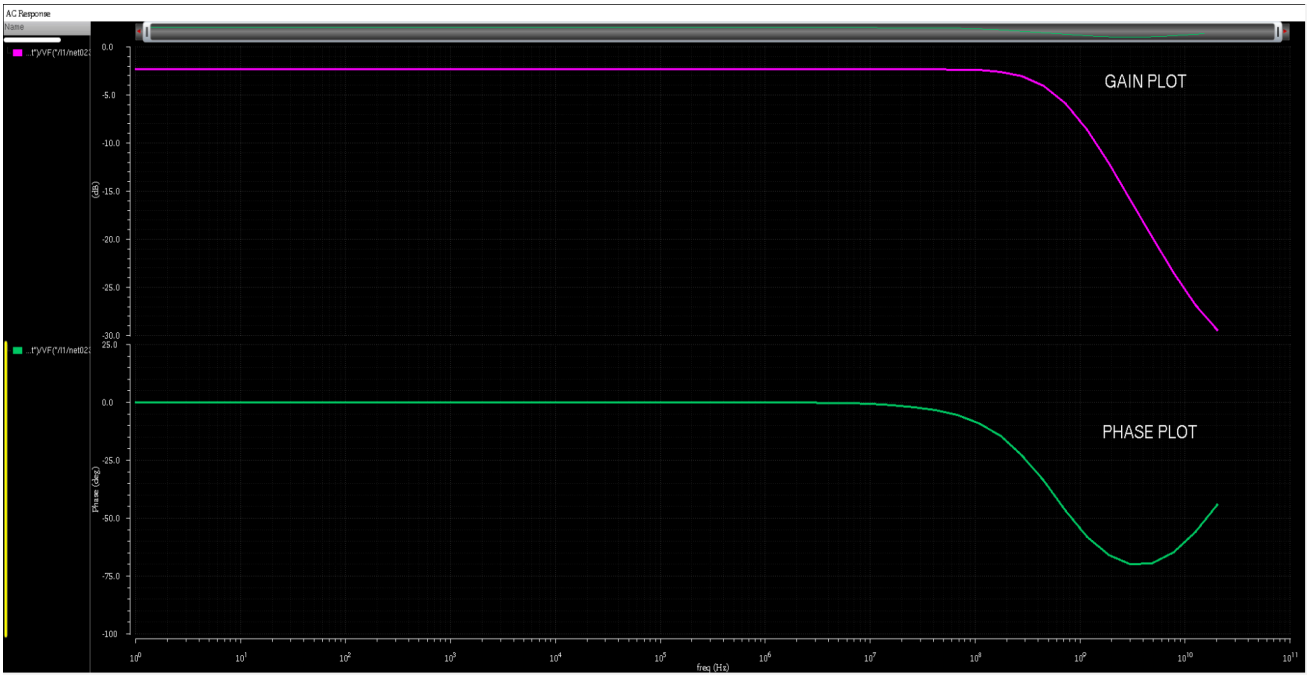

Figure 9: Gain and Phase plot of CD Amplifier

- **AC Response of Common-Drain (Source Follower) Amplifier – Third Stage**

➔ The figure above shows the **gain (magenta curve)** and **phase (green curve)** response of the **third stage** in your three-stage amplifier, which is implemented as a **common-drain (CD) amplifier**, also known as a **source follower**. This stage is primarily responsible for **output buffering** and ensuring **low output impedance**.

- The gain is slightly below **0 dB**, as expected from a **source follower**, which provides **voltage gain < 1**.

- **Multistage amplifier Gain and phase plot (without NMC):**

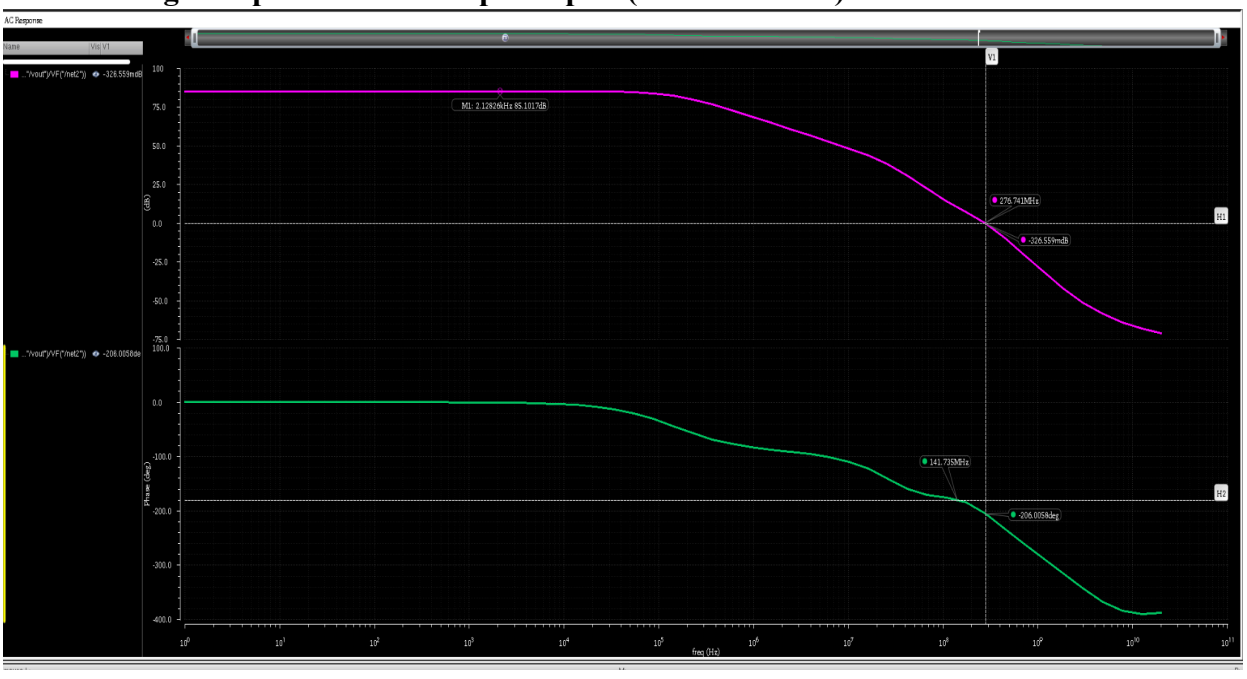

Figure 10: Gain and Phase plot of Three Stage Amplifier Without NMC

- **AC Response of Multistage Amplifier Without Nested Miller Compensation**

➔ The figure displays the **gain (magenta)** and **phase (green)** response of the full **three-stage amplifier**—differential amplifier (1st), common-source amplifier (2nd), and source follower (3rd)—**without any compensation technique** like Miller or Nested Miller Compensation (NMC). This plot evaluates the **uncompensated system's open-loop performance**.

- **Gain Plot (Magenta Curve):**

➔ The **midband gain** is observed to be around **85.10 dB** at low frequencies (~2.12 Hz), which confirms the **combined gain contribution** from all three stages.

➔ The **unity-gain frequency** is marked around **276.7 MHz**, beyond which the gain falls below 0 dB.

- **Phase Plot (Green Curve):**

➔ The phase initially stays close to **0°**, but starts to **decline gradually** as frequency increases.

➔ At the unity gain frequency, the phase drops to around **−206°**, which is a **critical stability issue**, indicating a **negative phase margin** (PM ≈ 180° − 206° = **−26°**).

- **Multistage amplifier Gain and phase plot (with NMC):**

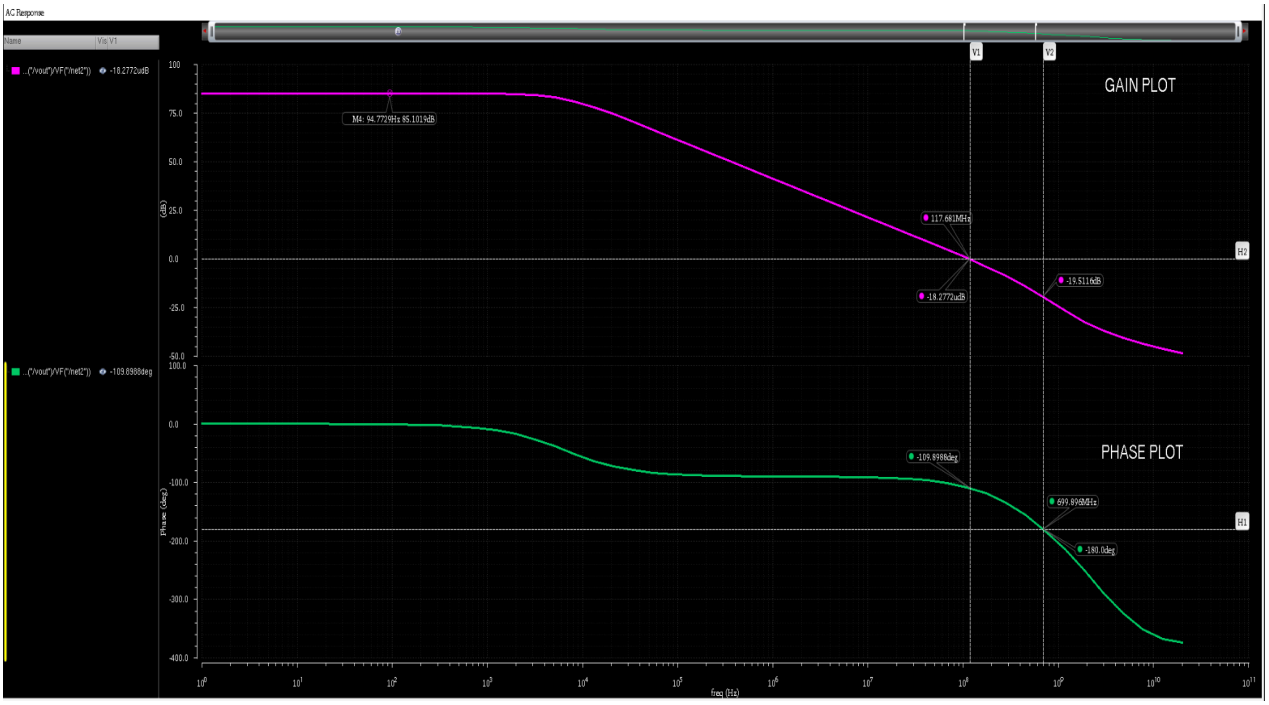

Figure 11: Gain and Phase plot of Three Stage Amplifier With NMC

- **AC Response of Multistage Amplifier with Nested Miller Compensation (NMC)**

➔ The above figure illustrates the **gain (magenta)** and **phase (green)** plots for the complete **three-stage amplifier** after applying **Nested Miller Compensation (NMC)** between the first and second stages. This analysis demonstrates the improvement in amplifier **stability**, **bandwidth**, and **phase margin** compared to the uncompensated version.

- **Gain Plot (Magenta Curve):**

➔ The amplifier achieves a high **low-frequency gain of ~85.1 dB** at around **94.77 Hz**, confirming effective amplification across the three stages.

➔ The **unity-gain bandwidth** (0 dB crossing) is observed at approximately **117.68 MHz**, indicating a good speed-power trade-off.

- **Phase Plot (Green Curve):**

➔ The phase drops smoothly from 0°, showing **no abrupt transitions** or instability dips.

➔ At the unity gain frequency (~117.68 MHz), the phase is about **−109.89°**, which corresponds to a **phase margin of ~70.1°**, calculated as:
PM=180 deg−∣Phase at Unity Gain∣=180 deg−109.89 deg=70.1degree

- **Closed loop stability analysis:**

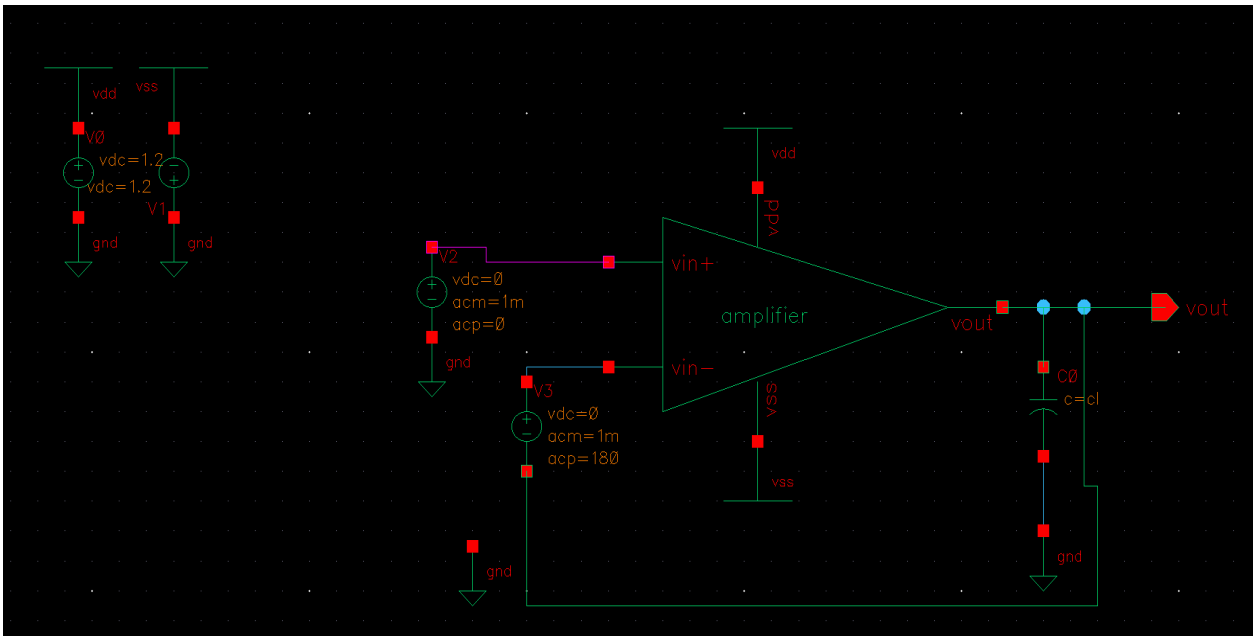

Figure 12: Closed loop Stability analysis

- **Amplifier Block:**

➔ Represents a differential Three Stage amplifier whose closed-loop stability is being tested.

- **Closed-Loop Configuration:**

➔ Output is connected back to the negative input terminal (vin−) through a feedback path.

➔ This forms a **closed-loop system** suitable for stability analysis.

- **Closed loop Phase Margin vs Load Capacitance**

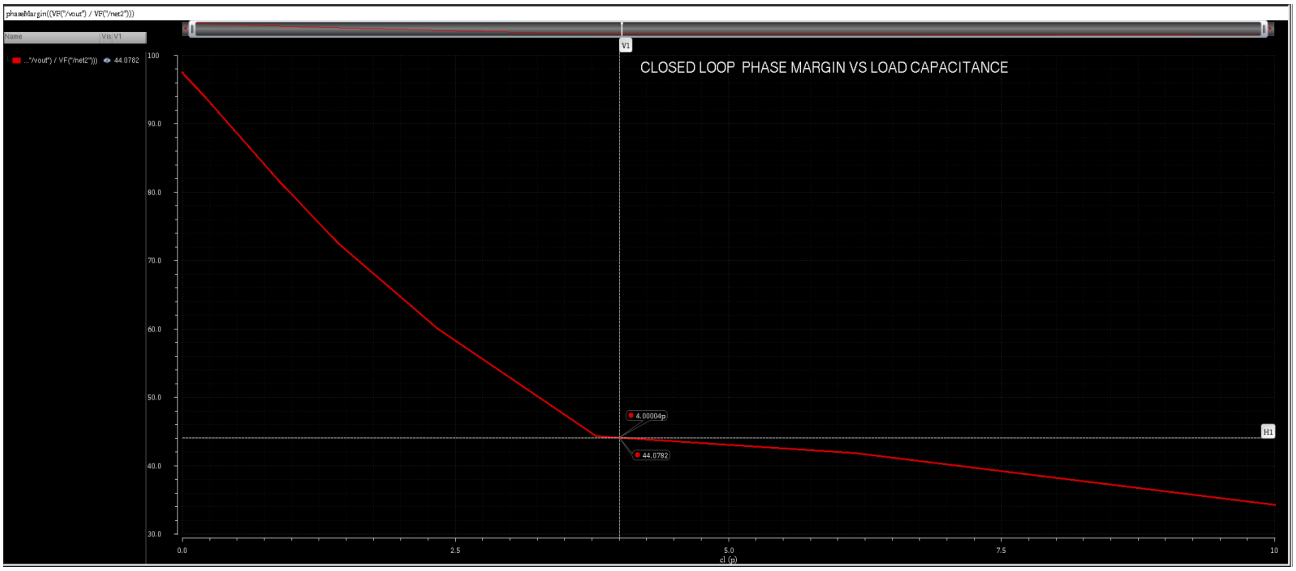

Figure 13: Closed loop Phase Margin vs Load Capacitance

- **Objective:**

➔ To analyze how the **closed-loop phase margin** varies with increasing **load capacitance**, thereby determining the amplifier's stability margin under different output loading conditions.

- **Phase Margin Decreases with Increasing Load Capacitance:**

➔ At lower Cl values (~0 pF), phase margin is high (~98°), indicating strong stability.

➔ As Cl increases, the phase margin drops monotonically.

➔ At Cl ≈ 4 pF, phase margin ≈ 44°, approaching the critical threshold for stability.

- **Open loop stability analysis:**

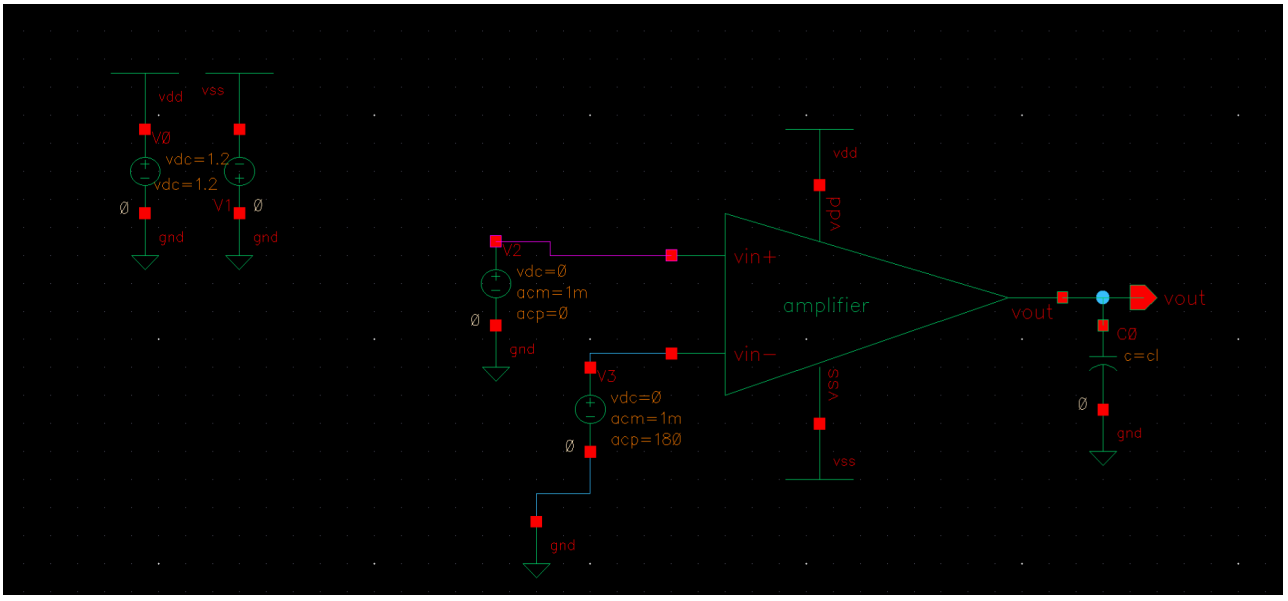

Figure 14: Open loop Stability analysis

- **Amplifier Block:**

➔ Represents a differential Three Stage amplifier whose open-loop stability is being tested.

- **Open loop Phase Margin vs Load Capacitance:**

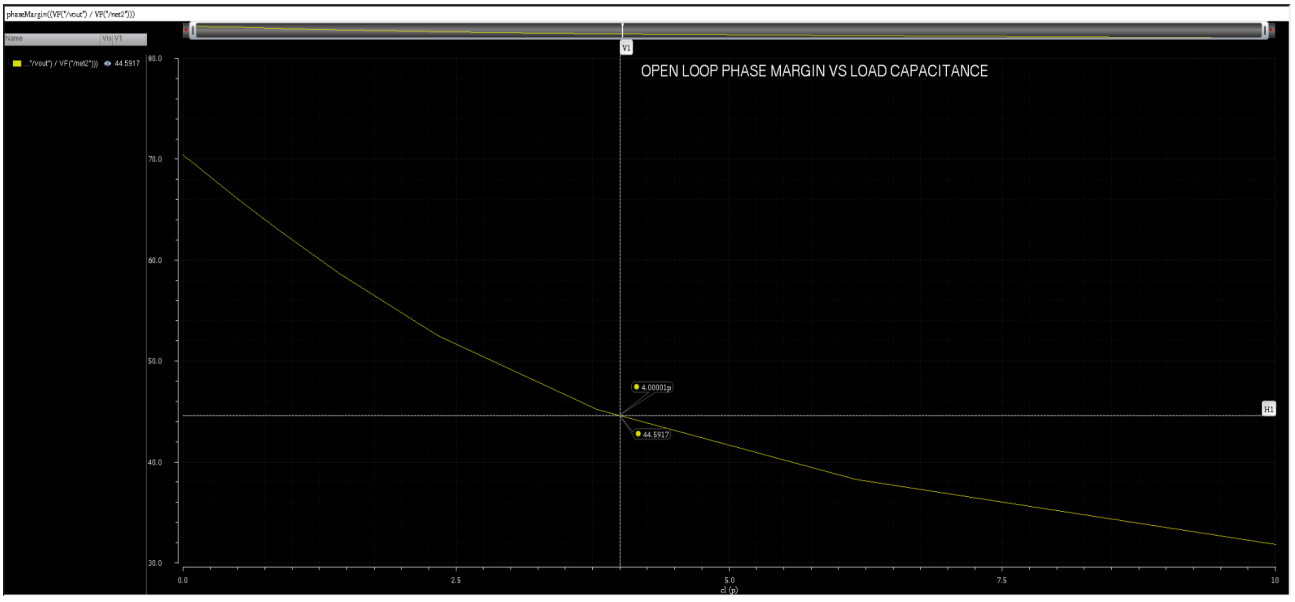

Figure 15: Open loop Phase Margin vs Load Capacitance

- **Objective:**

➔ To analyze how the **open-loop phase margin** varies with increasing **load capacitance**, thereby determining the amplifier's stability margin under different output loading conditions.

- **Phase Margin Decreases with Increasing Load Capacitance:**

➔ At lower Cl values (~0 pF), phase margin is high (~98°), indicating strong stability.

➔ As Cl increases, the phase margin drops monotonically.

➔ At Cl ≈ 4 pF, phase margin ≈ 44°, approaching the critical threshold for stability.

- **Transient Analysis of Three Stage Amplifier:**

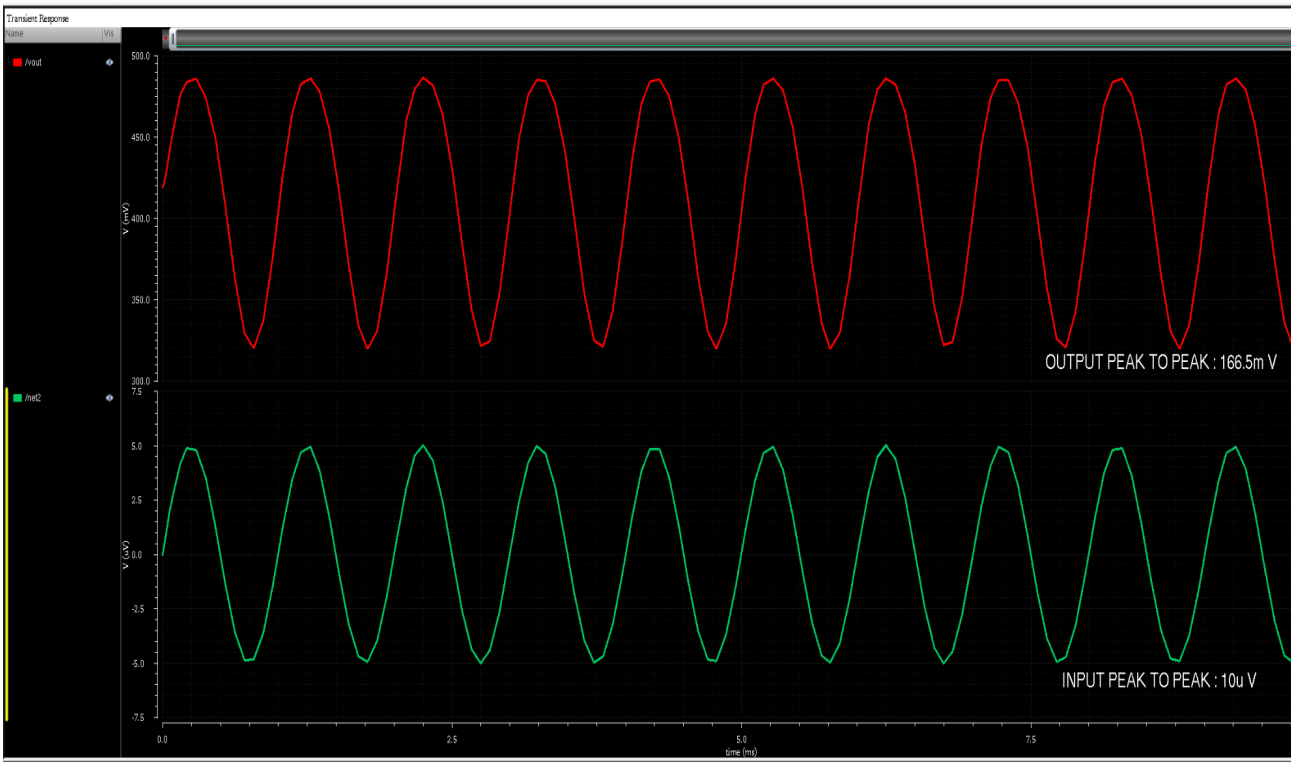

Figure 16: Transient Analysis of Three Stage Amplifier

- **The above Graph Representing the Time-Domain (Transient) Response of the Three-Stage Amplifier:**

➔ The transient analysis confirms the **functional amplification** of the designed three-stage amplifier.

➔ A small sinusoidal input of **10 µV peak-to-peak** is applied.

➔ The corresponding output reaches **166.5 mV peak-to-peak**, indicating significant voltage gain.

➔ The observed gain from the graph is:
Gain=166.5 mV/10uV =16,650 (≈84.4dB)

- **Analysis Conducted:**

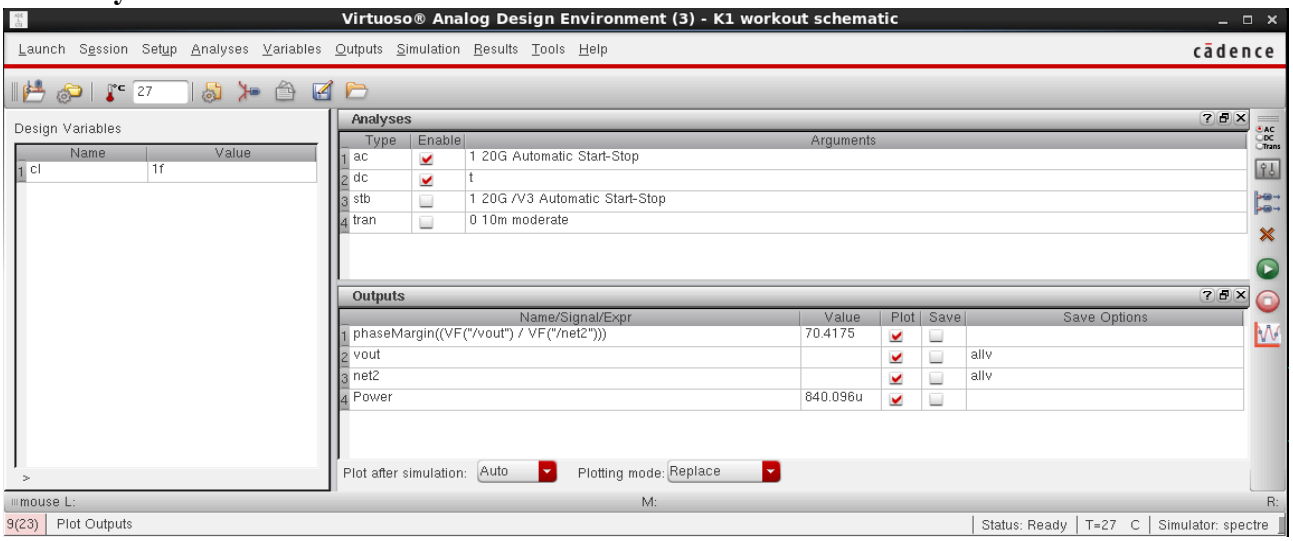

Figure 17: Analysis Conducted

- **This figure represents the simulation setup and analysis results for the Three-Stage Amplifier in Cadence Virtuoso's Analog Design Environment (ADE):**

➔ The **AC analysis** helps extract gain and bandwidth information.
➔ The **stability analysis** computes the **phase margin**, confirming that the design is stable (as a margin > 45° is generally considered stable).
➔ The **transient analysis** is essential for validating the amplifier's dynamic behavior and gain.
➔ The **DC analysis** provides the necessary operating point (biasing) for the circuit to ensure all MOSFETs are in the correct region.
➔ The **power consumption** of **840.096 µW** demonstrates that the amplifier is energy-efficient and suitable for low-power analog applications.

- **Obtained Results:**

Table 3: Output Results

Technology	90nm
Power	840.096u W
Gain	85.1019db
Phase margin	70.4175 degree
Peak to Peak input	10uv
Peak to Peak Output	166.5mv
GBWP	116.9MHz
Gain margin	19.44 db

CHAPTER 6

CONCLUSION

- In this project, a three-stage CMOS amplifier was successfully designed, optimized, and simulated using 90nm CMOS technology. The amplifier architecture — comprising a differential input stage, a common-source gain stage, and a source follower output buffer — was selected to achieve high voltage gain, stable frequency response, and efficient output drive capability.
- Through careful biasing, transistor sizing, and compensation using the Nested Miller approach, the design achieved a **voltage gain of 85.10 dB**, a **phase margin of 70.42°**, and a **gain-bandwidth product of 116.9 MHz**, while maintaining **low power consumption at just 840.096 µW**. The amplifier demonstrated good linearity and signal swing with a **10 µV peak-to-peak input** and **166.5 mV peak-to-peak output**.
- These results confirm that the amplifier meets key design targets for stability, gain, and power efficiency. The performance validates its suitability for low-frequency, low-signal analog applications such as **sensor front-ends, biomedical signal processing, and other mixed-signal systems** requiring moderate speed and strong gain characteristics.
- This project not only met its stated objectives but also built foundational skills in analog circuit design, biasing strategies, compensation techniques, and transistor-level simulation workflows using Cadence Virtuoso. It can be further extended to layout-level implementation, post-layout simulations, and real-world application integration in future work.

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