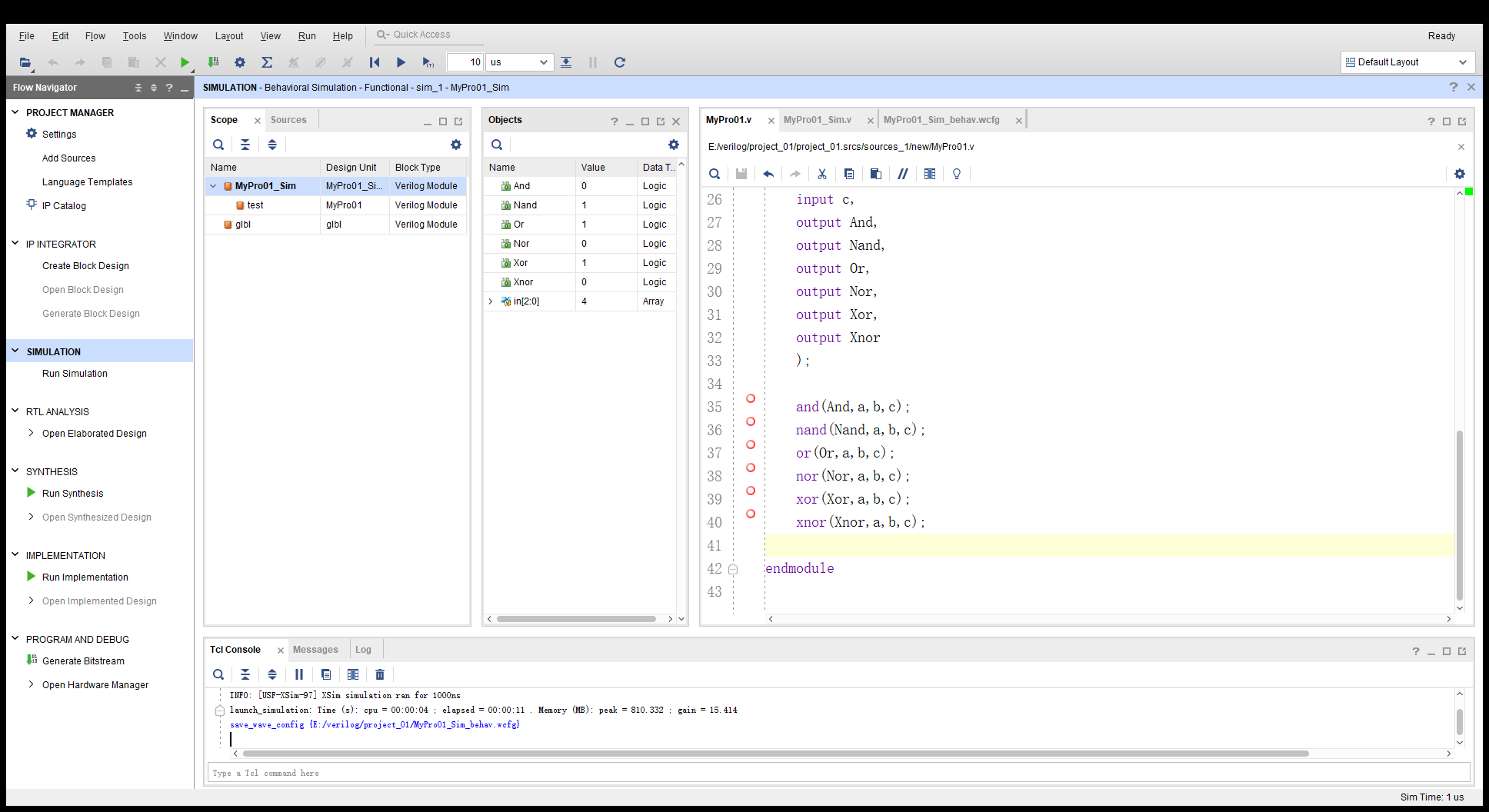
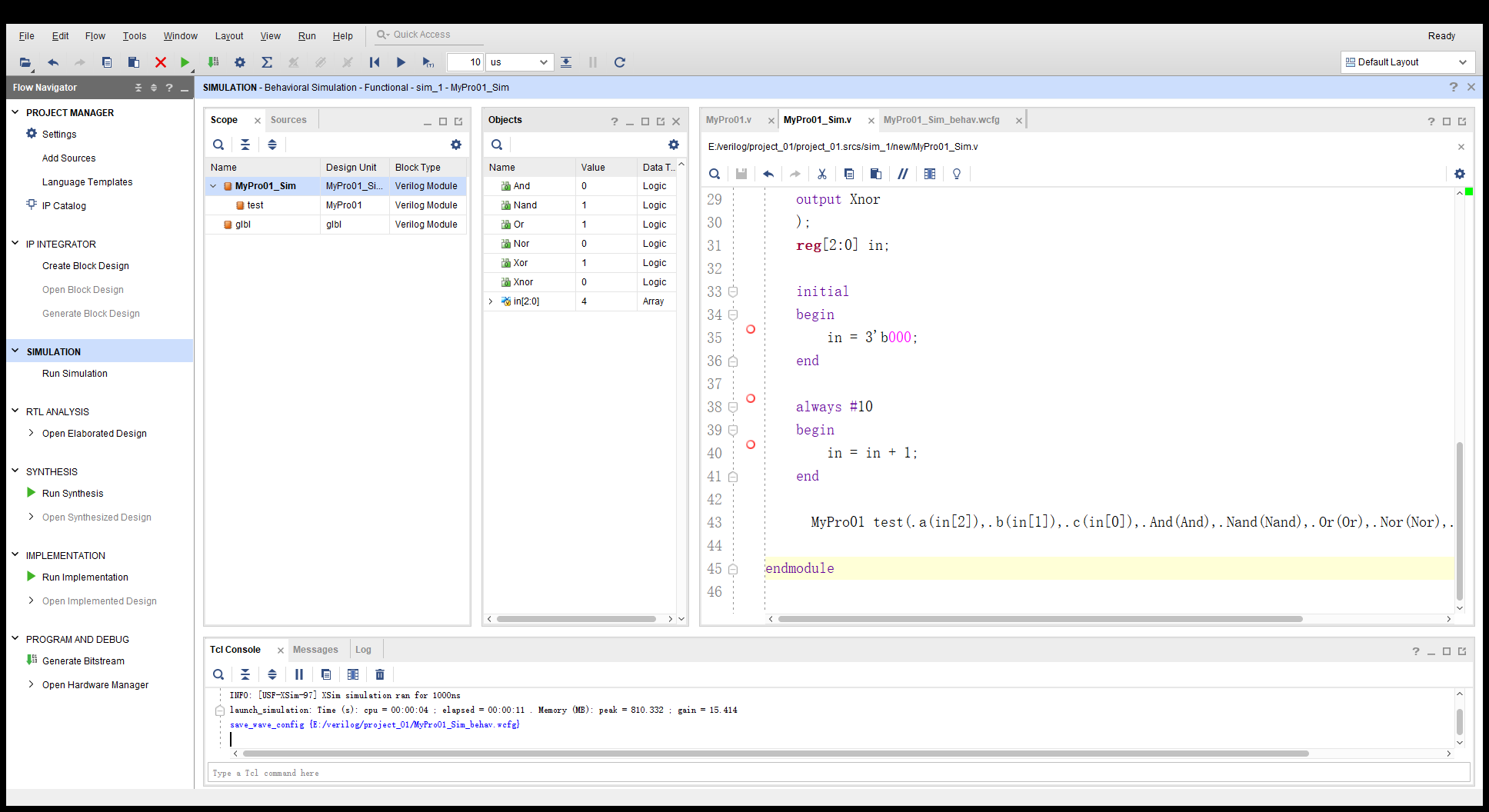
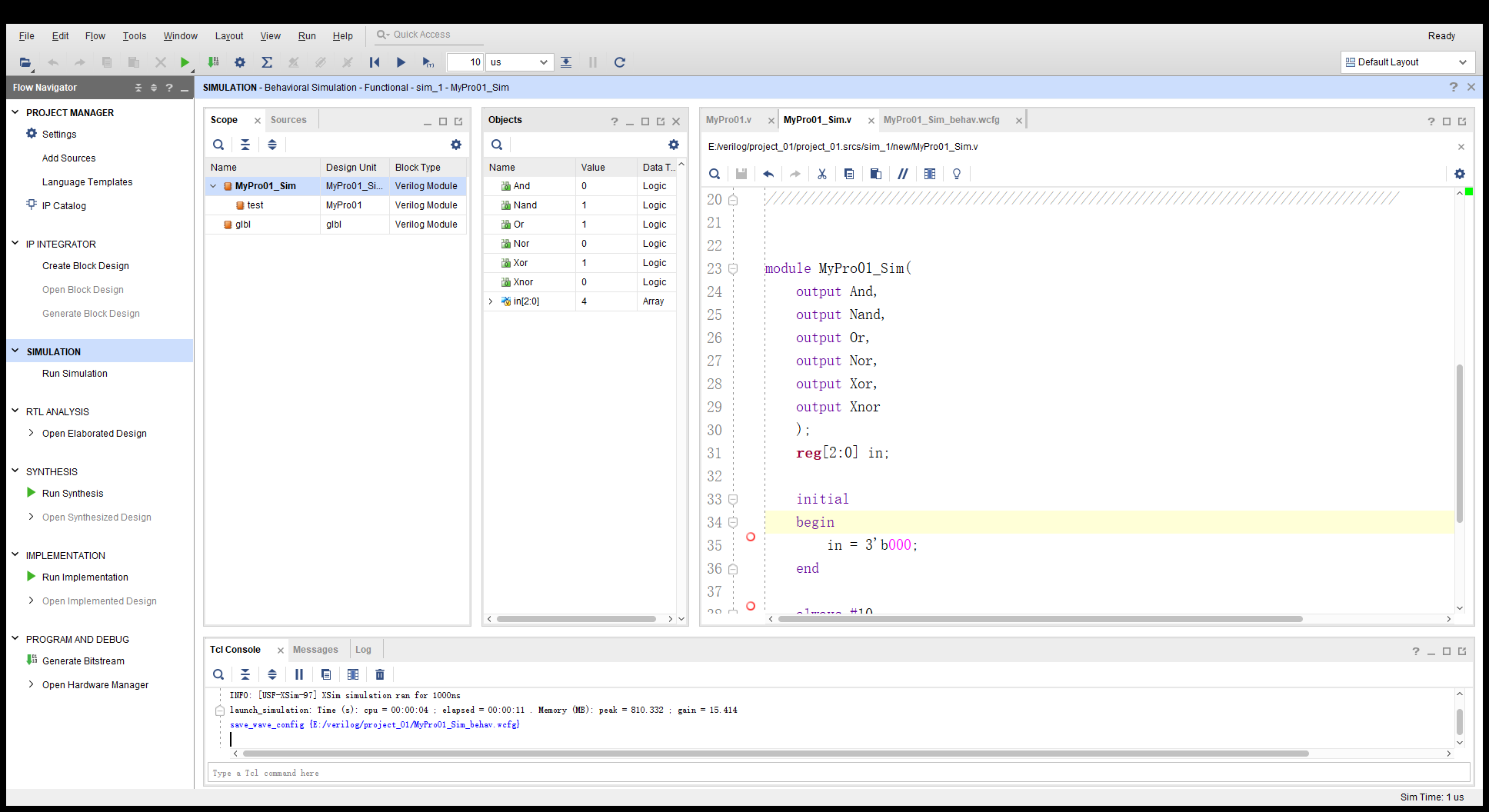
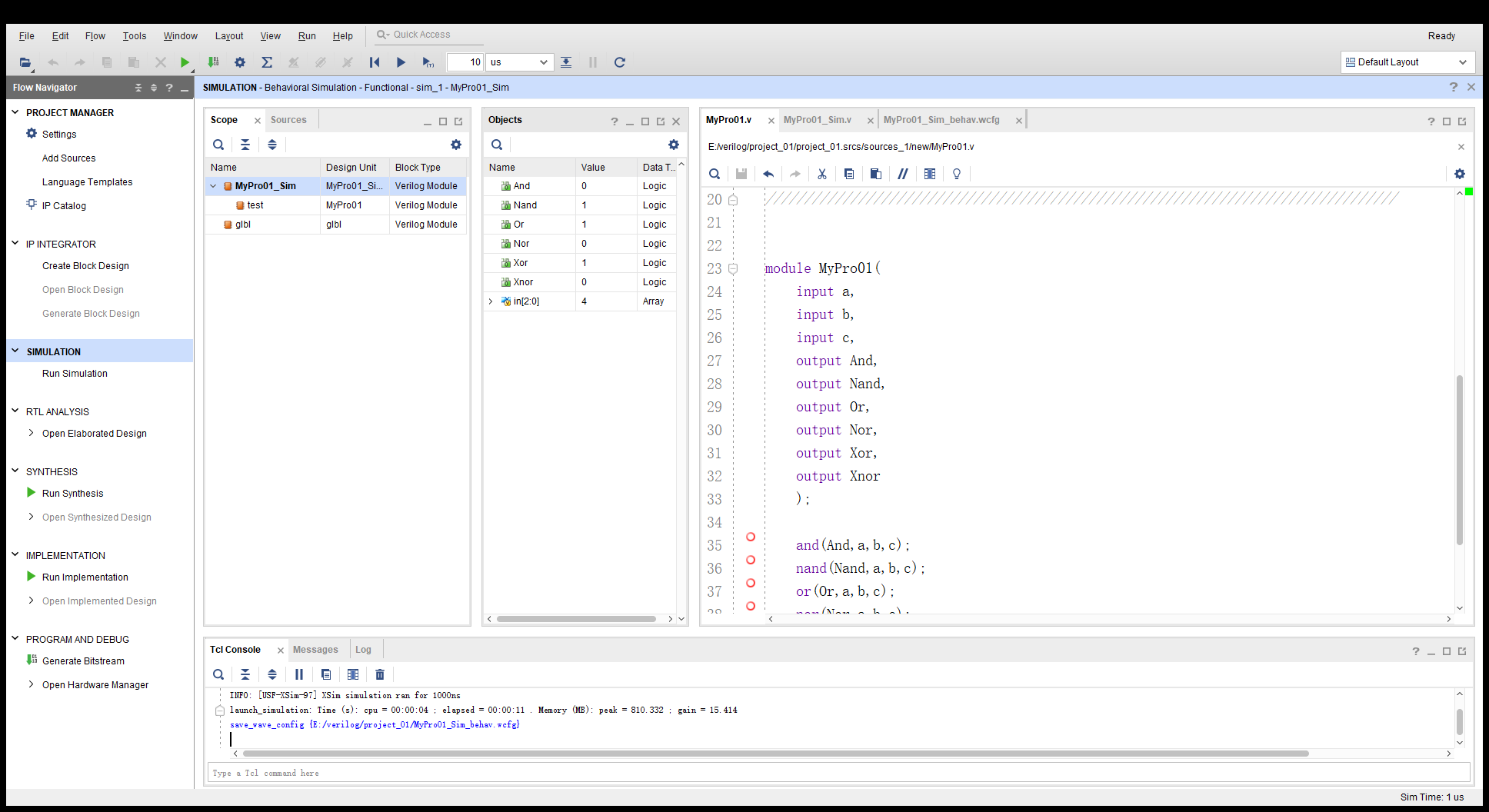
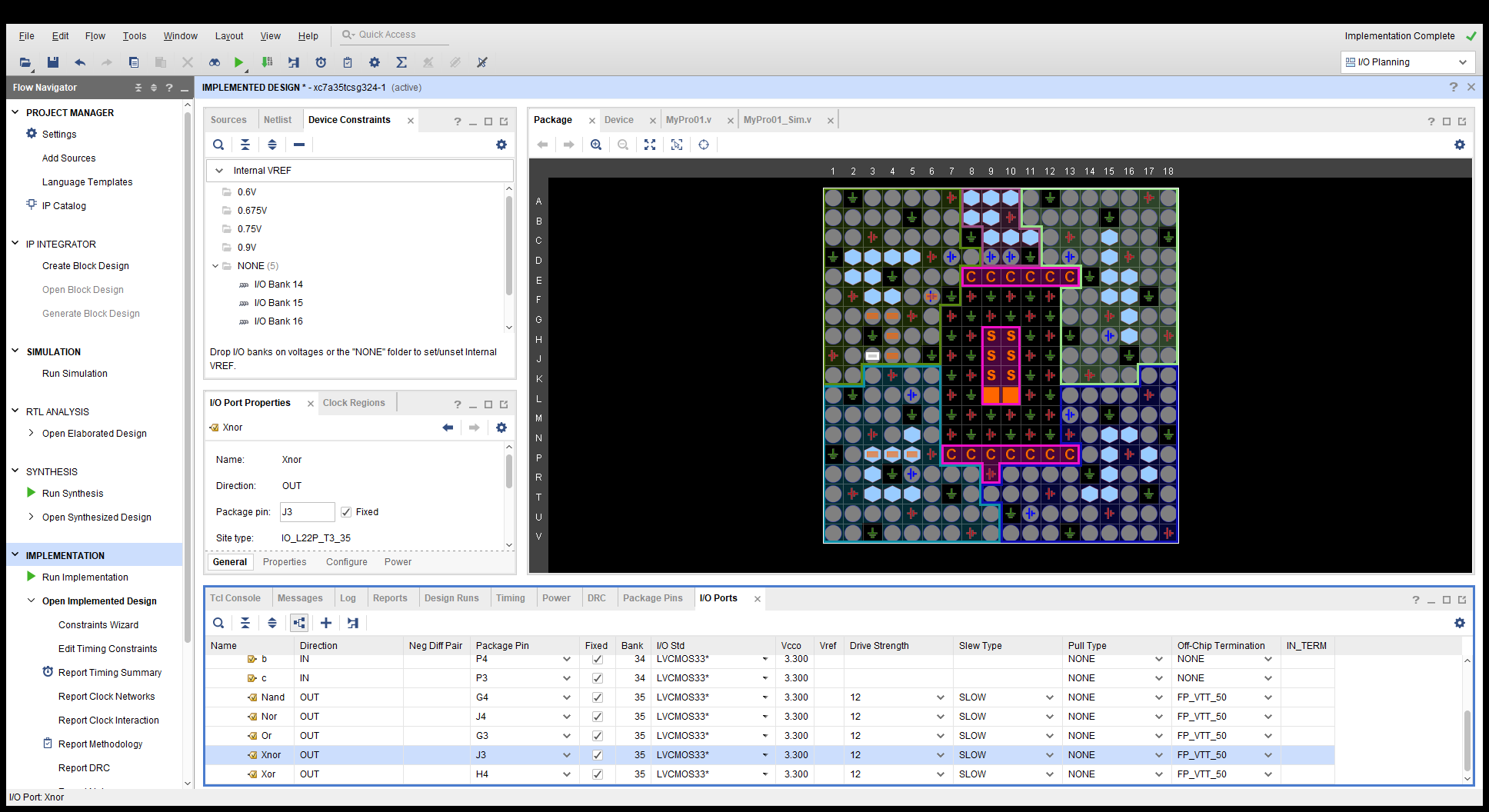
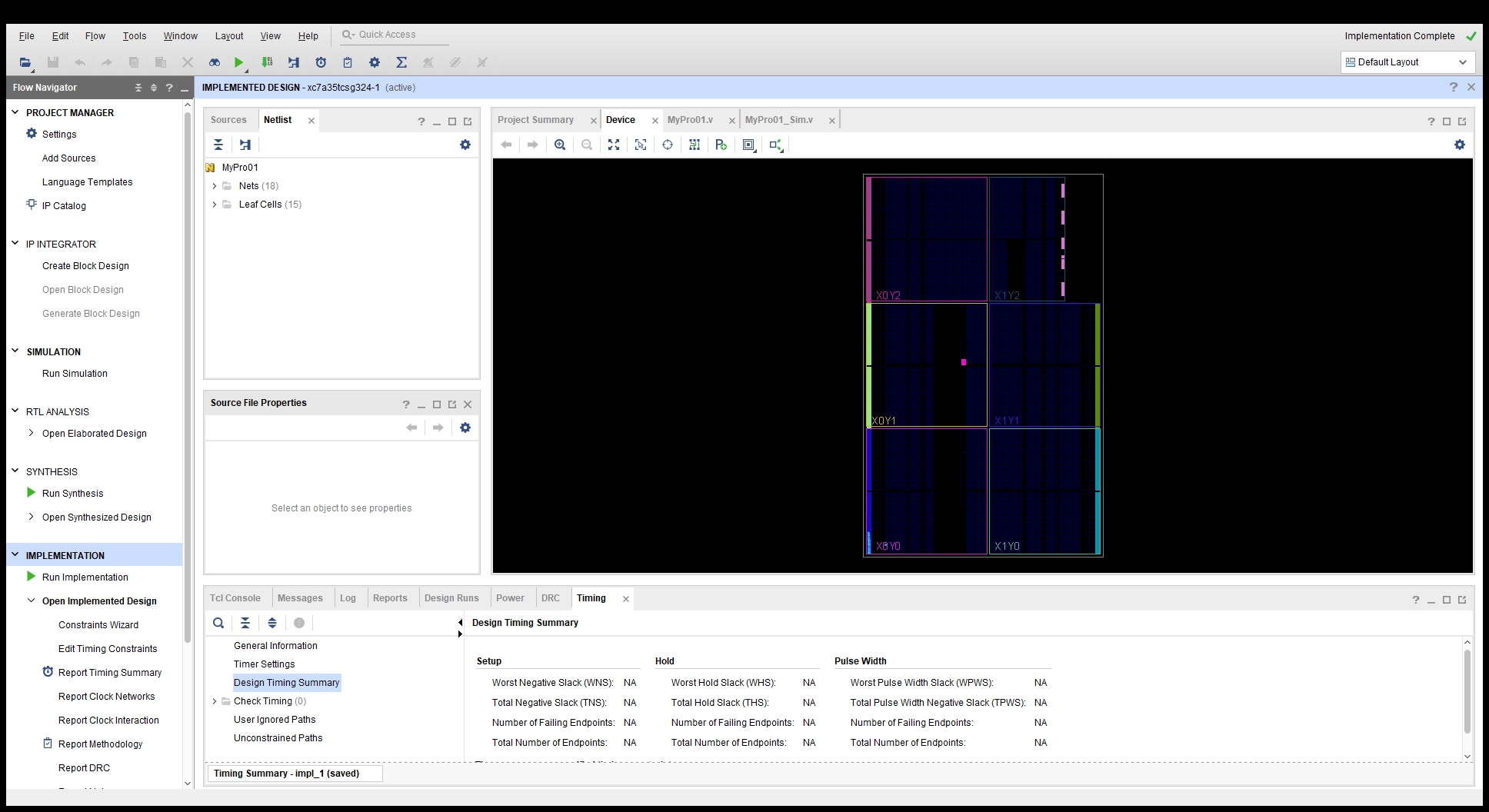
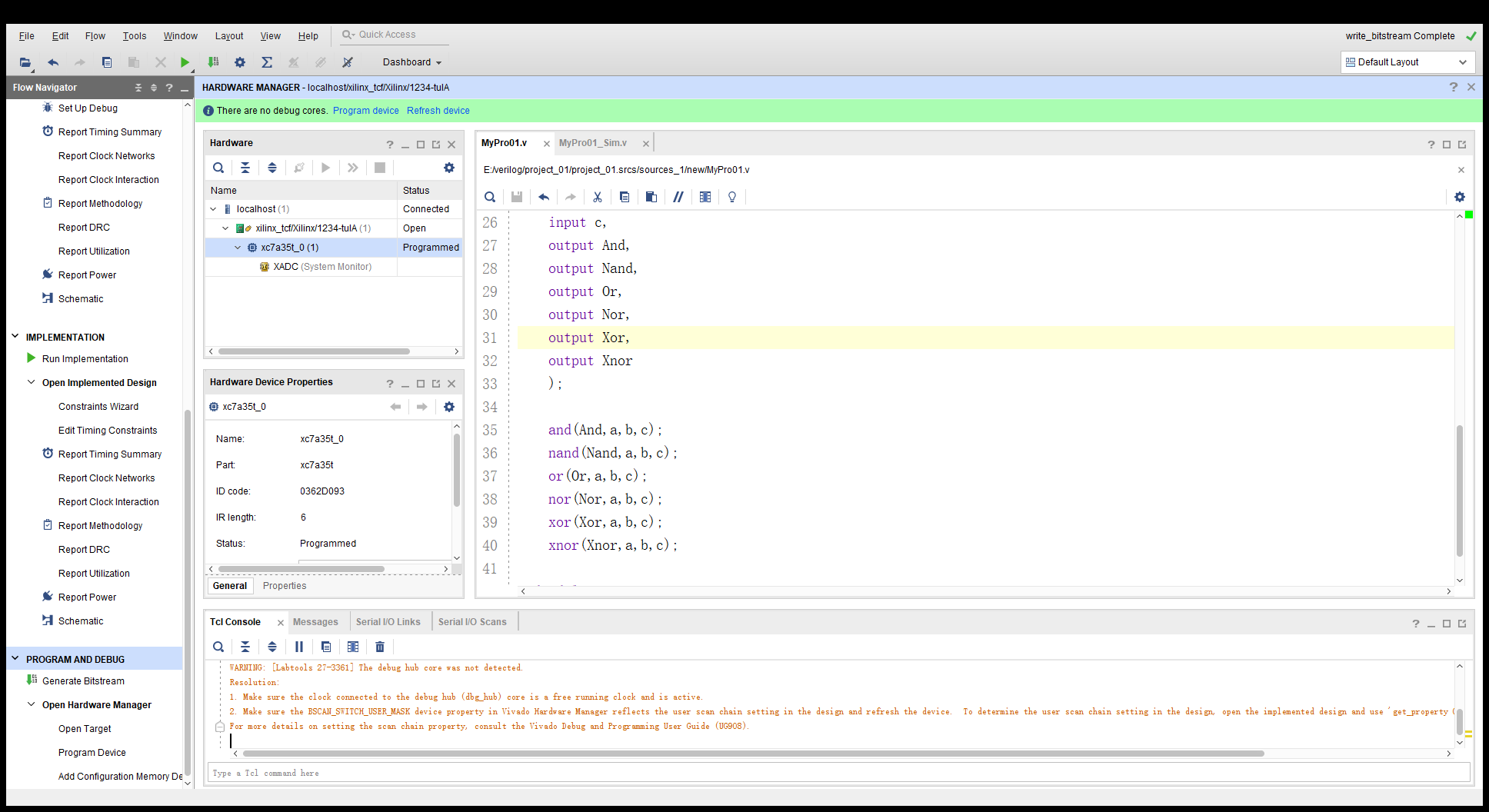


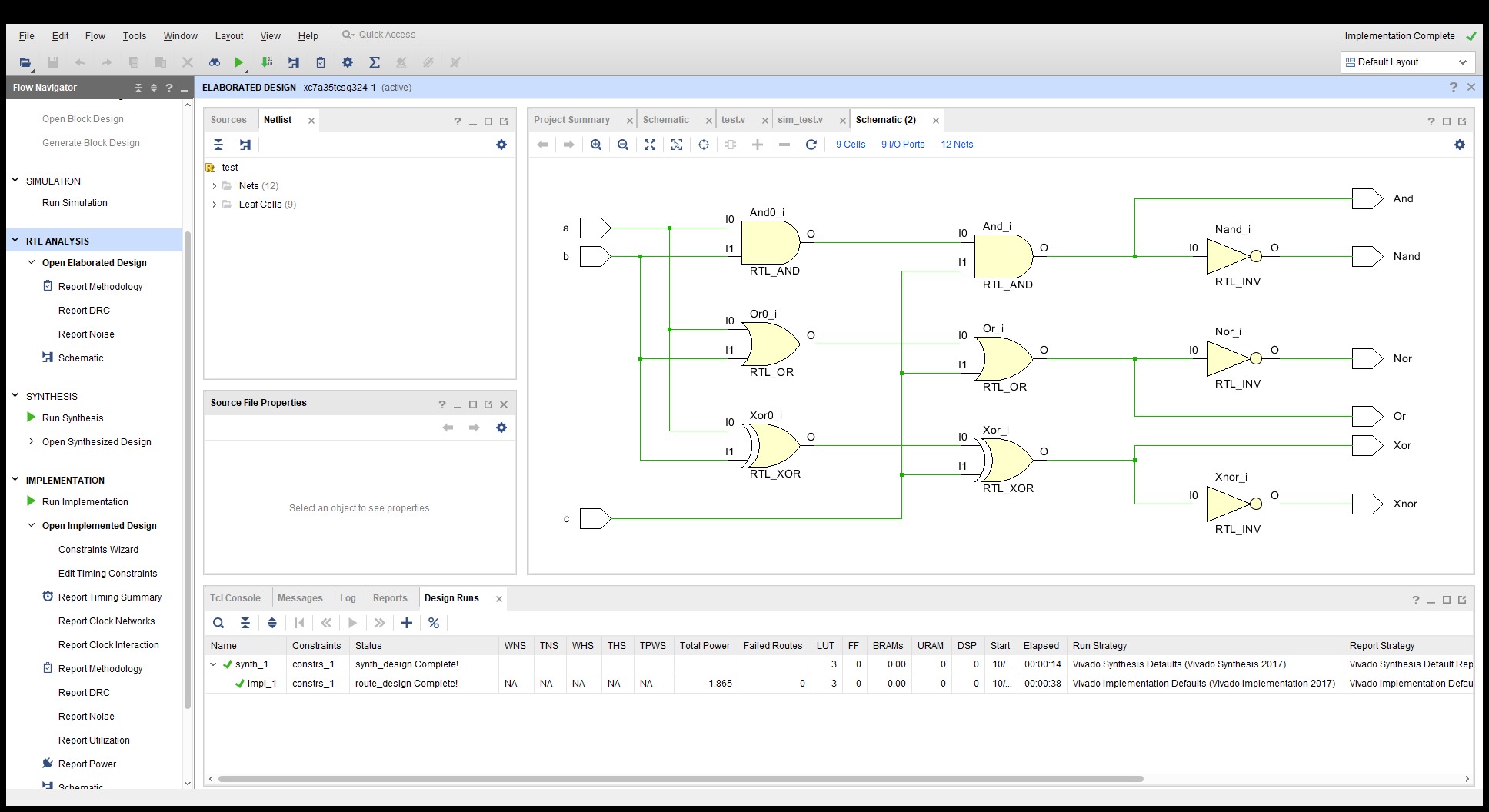
RUNSIM程序编码

仿真编码

RUNIMP,修改接口

创建比特流





原程序`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 2019/09/30 11:31:22

// Design Name:

// Module Name: MyPro01

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module MyPro01(

input a,

input b,

input c,

output And,

output Nand,

output Or,

output Nor,

output Xor,

output Xnor

);

and(And,a,b,c);

nand(Nand,a,b,c);

or(Or,a,b,c);

nor(Nor,a,b,c);

xor(Xor,a,b,c);

xnor(Xnor,a,b,c);

endmodule

仿真

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 2019/09/30 11:32:38

// Design Name:

// Module Name: MyPro01\_Sim

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module MyPro01\_Sim(

output And,

output Nand,

output Or,

output Nor,

output Xor,

output Xnor

);

reg[2:0] in;

initial

begin

in = 3'b000;

end

always #10

begin

in = in + 1;

end

MyPro01 test(.a(in[2]),.b(in[1]),.c(in[0]),.And(And),.Nand(Nand),.Or(Or),.Nor(Nor),.Xor(Xor),.Xnor(Xnor));

endmodule