程序代码：

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 2019/10/21 11:44:09

// Design Name:

// Module Name: experiment\_3

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module experiment\_3(

input [2:0] a,

input [2:0] b,

input c0,

output [2:0] sum,

output c3

);

wire [2:0]g;

wire [2:0]p;

wire [1:0]c;

assign g=a&b;

assign p=a^b;

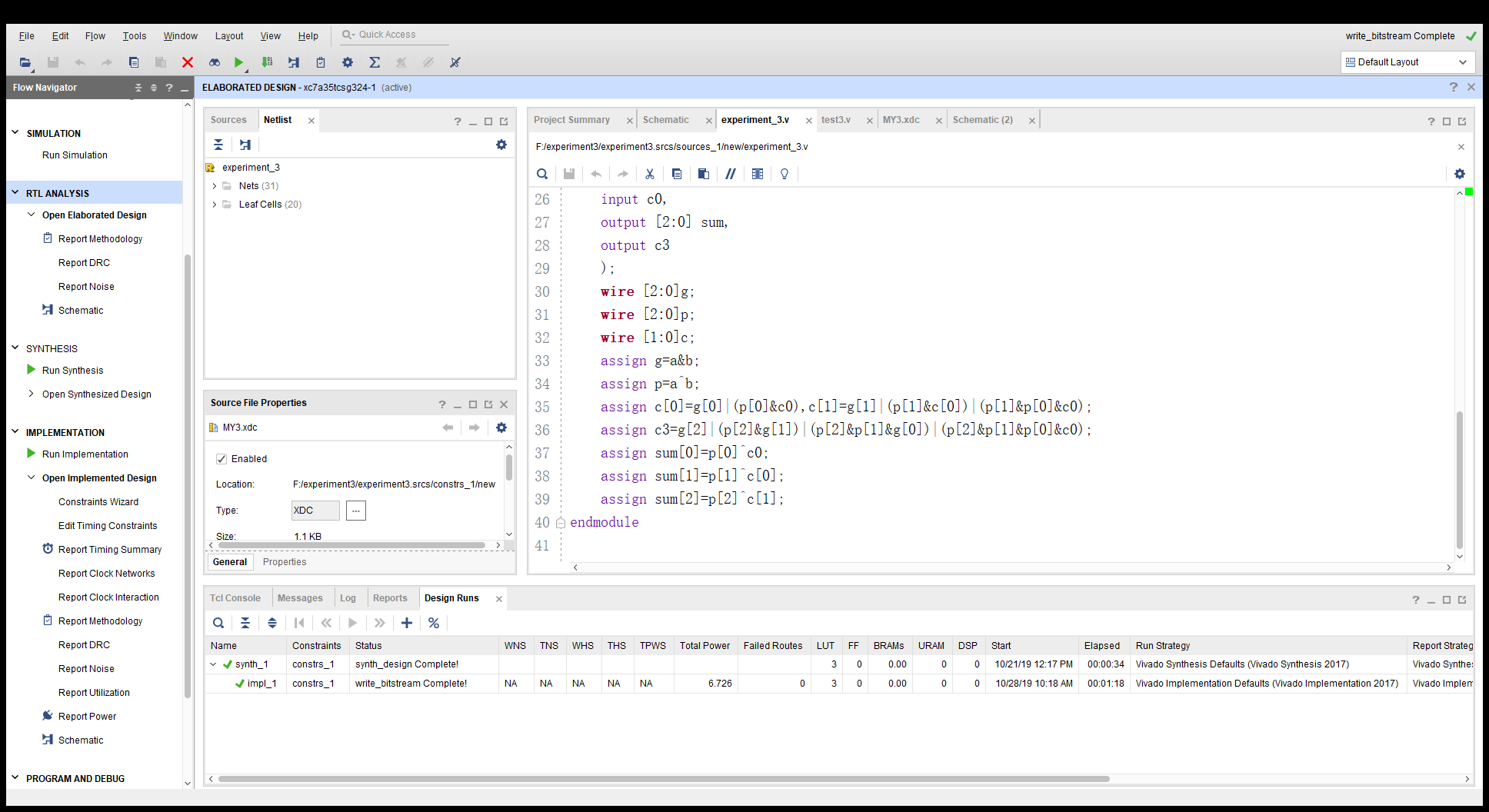
assign c[0]=g[0]|(p[0]&c0),c[1]=g[1]|(p[1]&c[0])|(p[1]&p[0]&c0);

assign c3=g[2]|(p[2]&g[1])|(p[2]&p[1]&g[0])|(p[2]&p[1]&p[0]&c0);

assign sum[0]=p[0]^c0;

assign sum[1]=p[1]^c[0];

assign sum[2]=p[2]^c[1];

endmodule

**仿真：**

**`timescale 1ns / 1ps**

**//////////////////////////////////////////////////////////////////////////////////**

**// Company:**

**// Engineer:**

**//**

**// Create Date: 2019/10/21 11:55:33**

**// Design Name:**

**// Module Name: test3**

**// Project Name:**

**// Target Devices:**

**// Tool Versions:**

**// Description:**

**//**

**// Dependencies:**

**//**

**// Revision:**

**// Revision 0.01 - File Created**

**// Additional Comments:**

**//**

**//////////////////////////////////////////////////////////////////////////////////**

**module test3(**

**output [2:0] sum,**

**output c3**

**);**

**reg[2:0] in1;**

**reg[2:0] in2;**

**reg c0;**

**initial**

**begin**

**in1=3'b000;**

**in2=3'b000;**

**c0=1'b0;**

**end**

**always #10**

**begin**

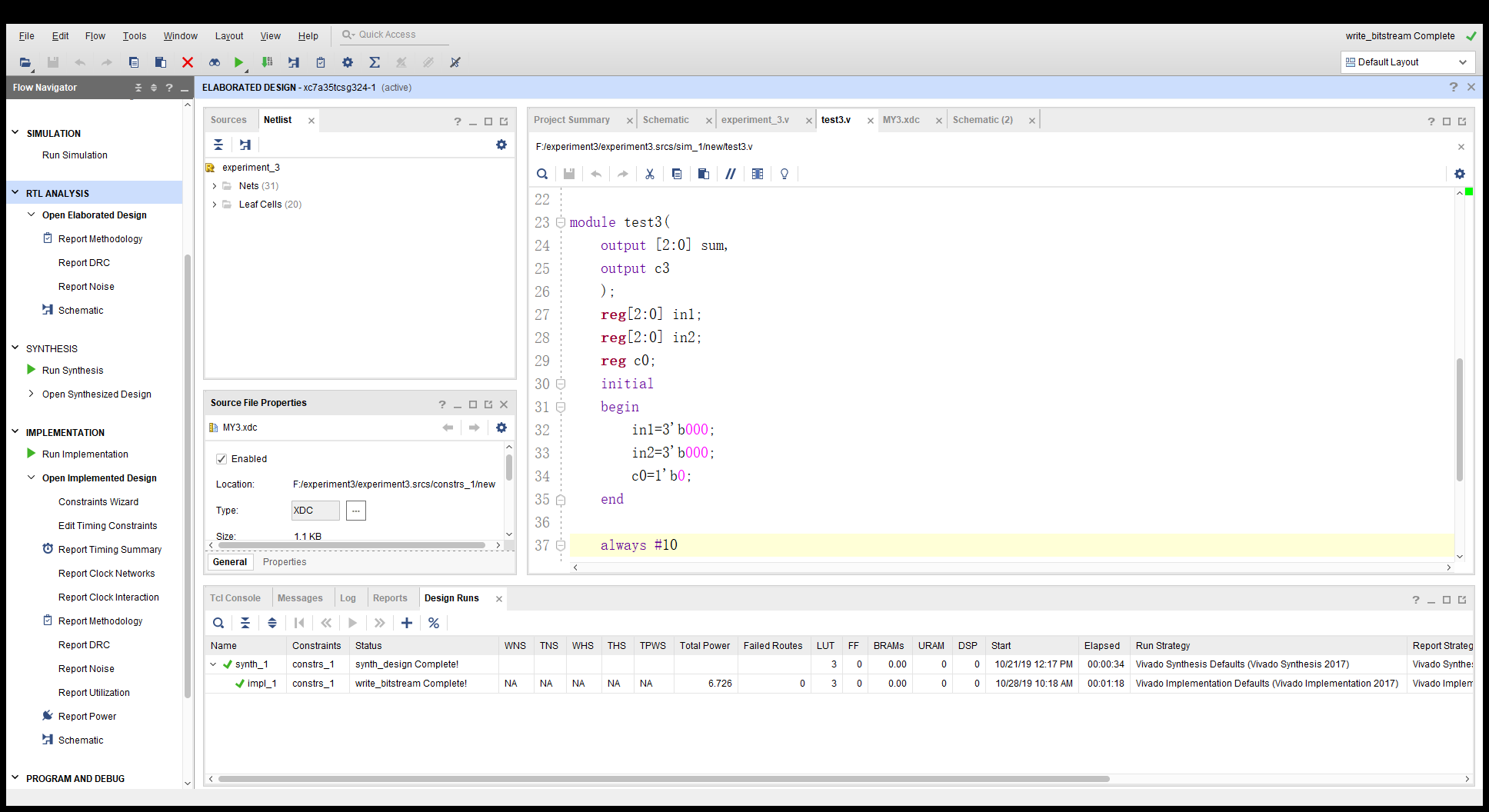
**in1=in1+1;**

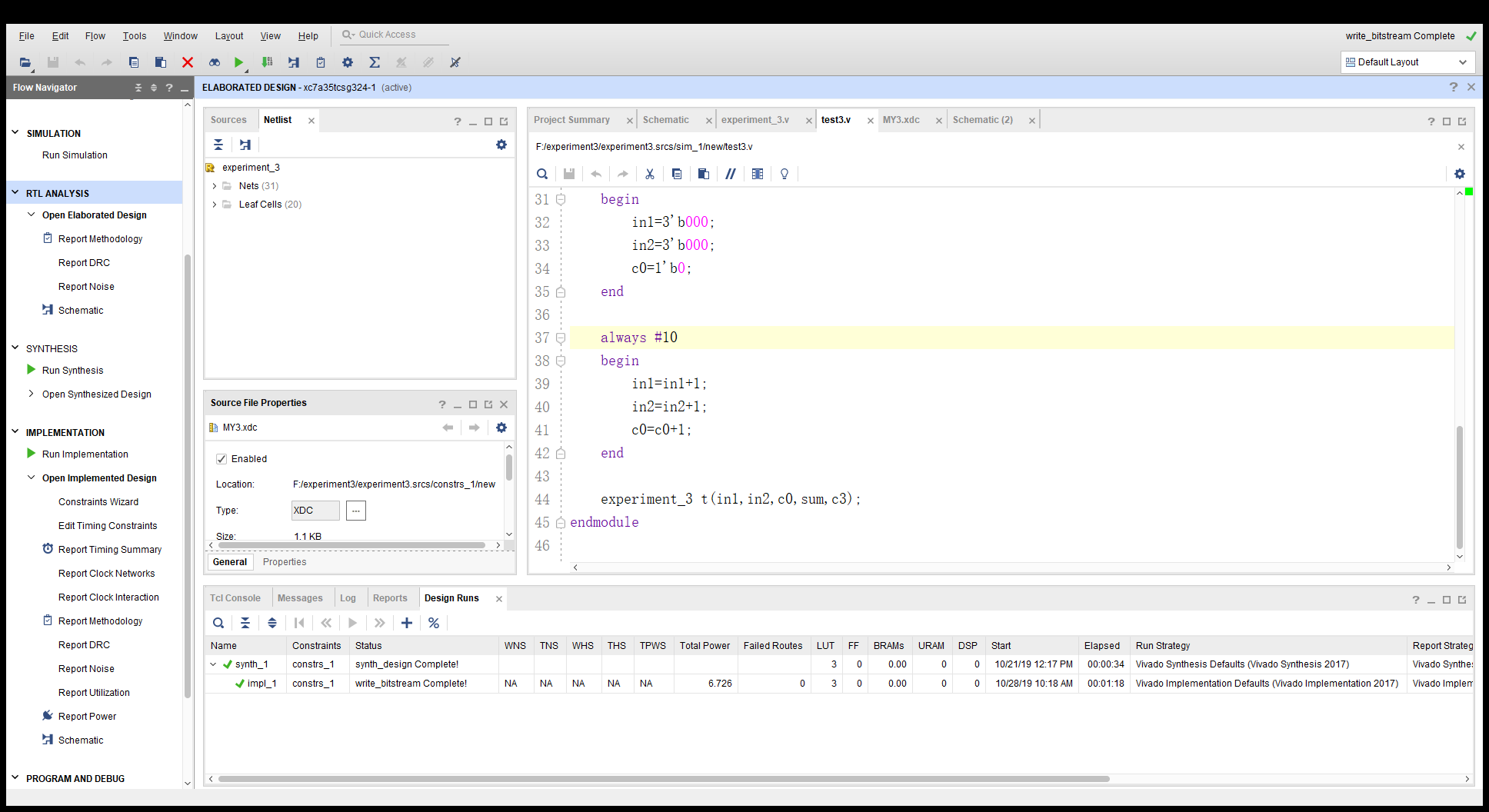
**in2=in2+1;**

**c0=c0+1;**

**end**

**experiment\_3 t(in1,in2,c0,sum,c3);**

**endmodule**

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**约束：**

**set\_property IOSTANDARD LVCMOS33 [get\_ports {a[2]}]**

**set\_property IOSTANDARD LVCMOS33 [get\_ports {a[1]}]**

**set\_property IOSTANDARD LVCMOS33 [get\_ports {a[0]}]**

**set\_property IOSTANDARD LVCMOS33 [get\_ports {b[2]}]**

**set\_property IOSTANDARD LVCMOS33 [get\_ports {b[1]}]**

**set\_property IOSTANDARD LVCMOS33 [get\_ports {b[0]}]**

**set\_property IOSTANDARD LVCMOS33 [get\_ports {sum[2]}]**

**set\_property IOSTANDARD LVCMOS33 [get\_ports {sum[1]}]**

**set\_property IOSTANDARD LVCMOS33 [get\_ports {sum[0]}]**

**set\_property PACKAGE\_PIN P5 [get\_ports {a[2]}]**

**set\_property PACKAGE\_PIN P4 [get\_ports {a[1]}]**

**set\_property PACKAGE\_PIN P3 [get\_ports {a[0]}]**

**set\_property PACKAGE\_PIN P2 [get\_ports {b[2]}]**

**set\_property PACKAGE\_PIN R2 [get\_ports {b[1]}]**

**set\_property PACKAGE\_PIN M4 [get\_ports {b[0]}]**

**set\_property IOSTANDARD LVCMOS33 [get\_ports c0]**

**set\_property PACKAGE\_PIN N4 [get\_ports c0]**

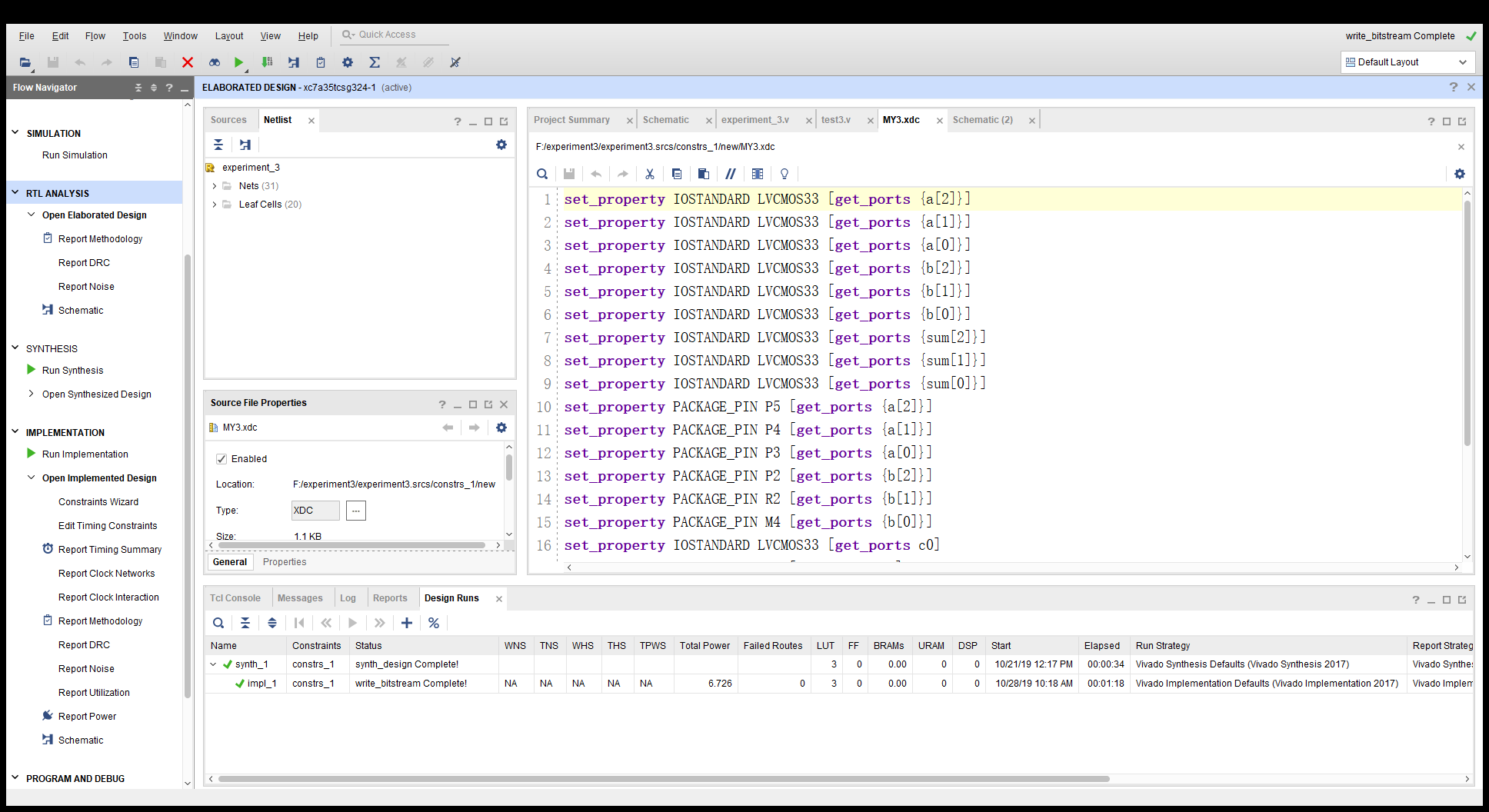
**set\_property PACKAGE\_PIN F6 [get\_ports c3]**

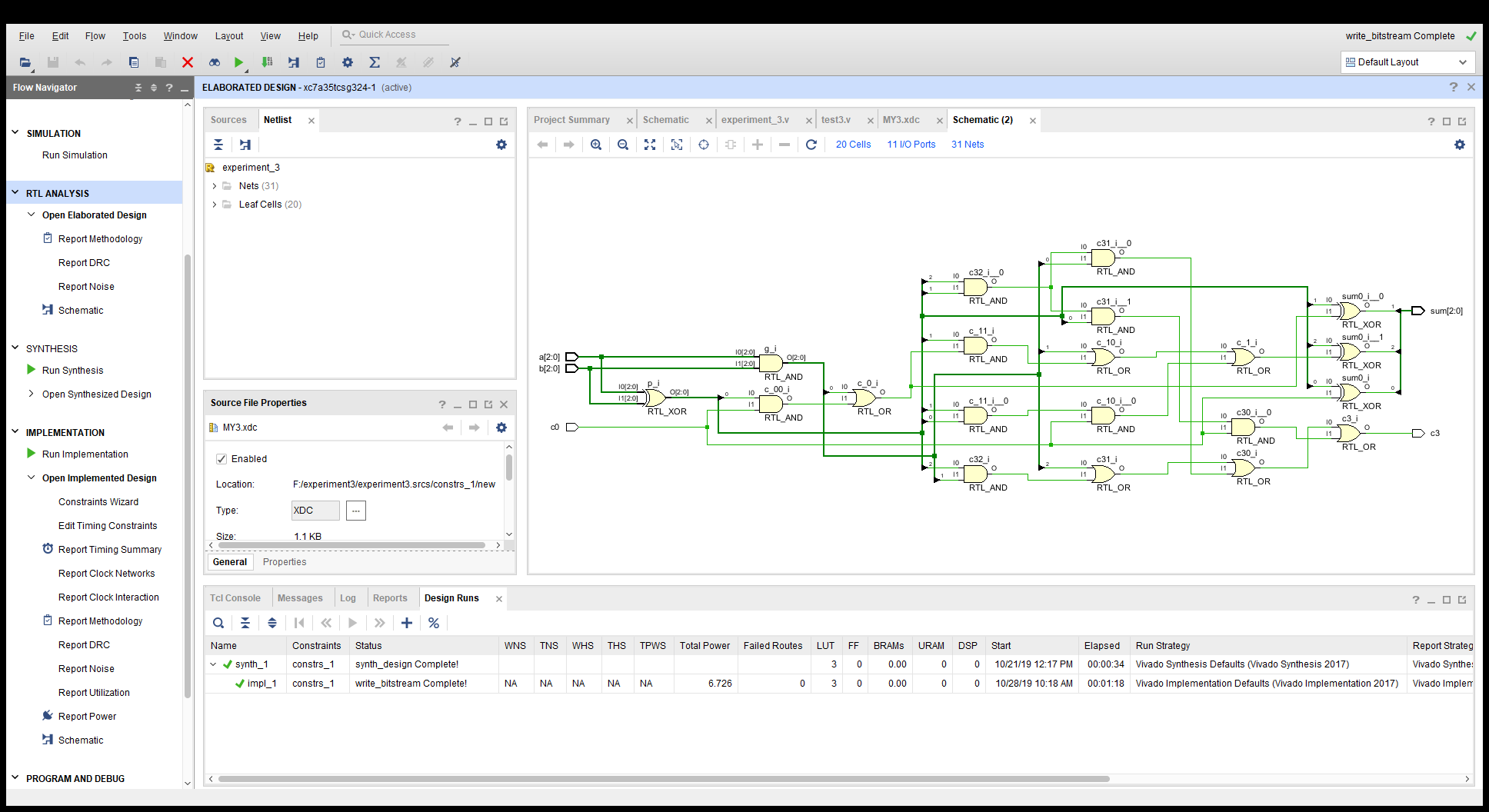
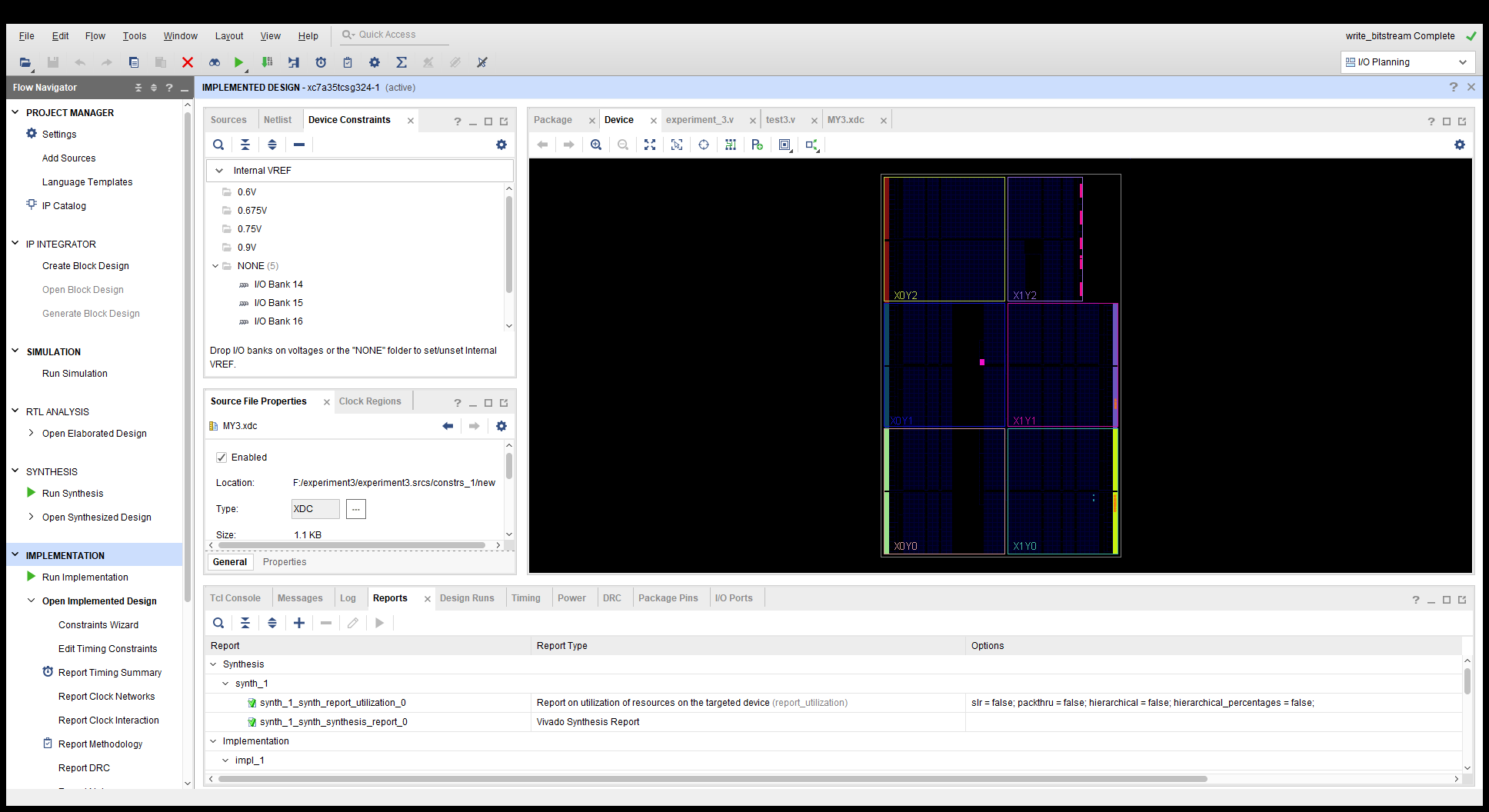
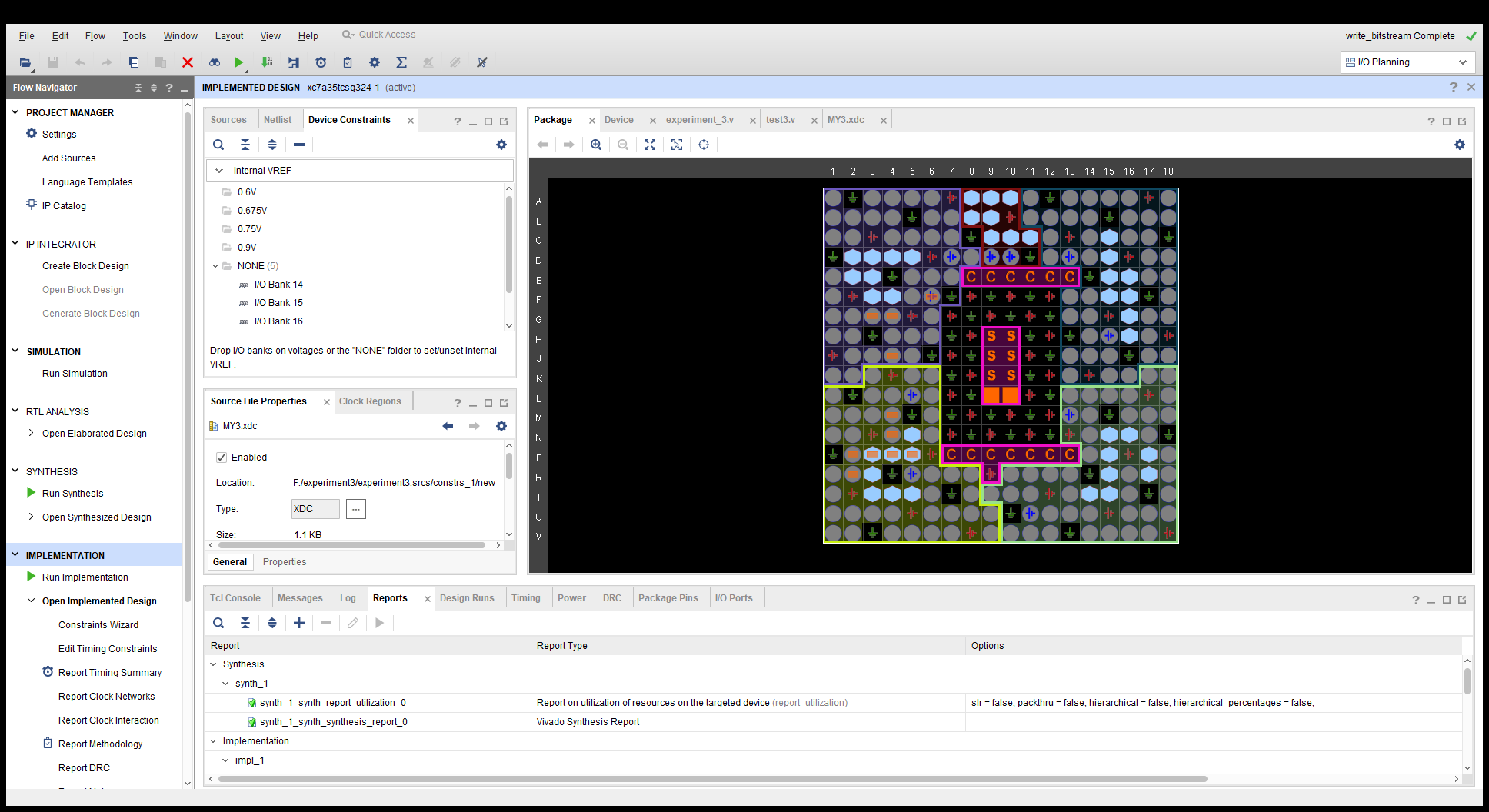
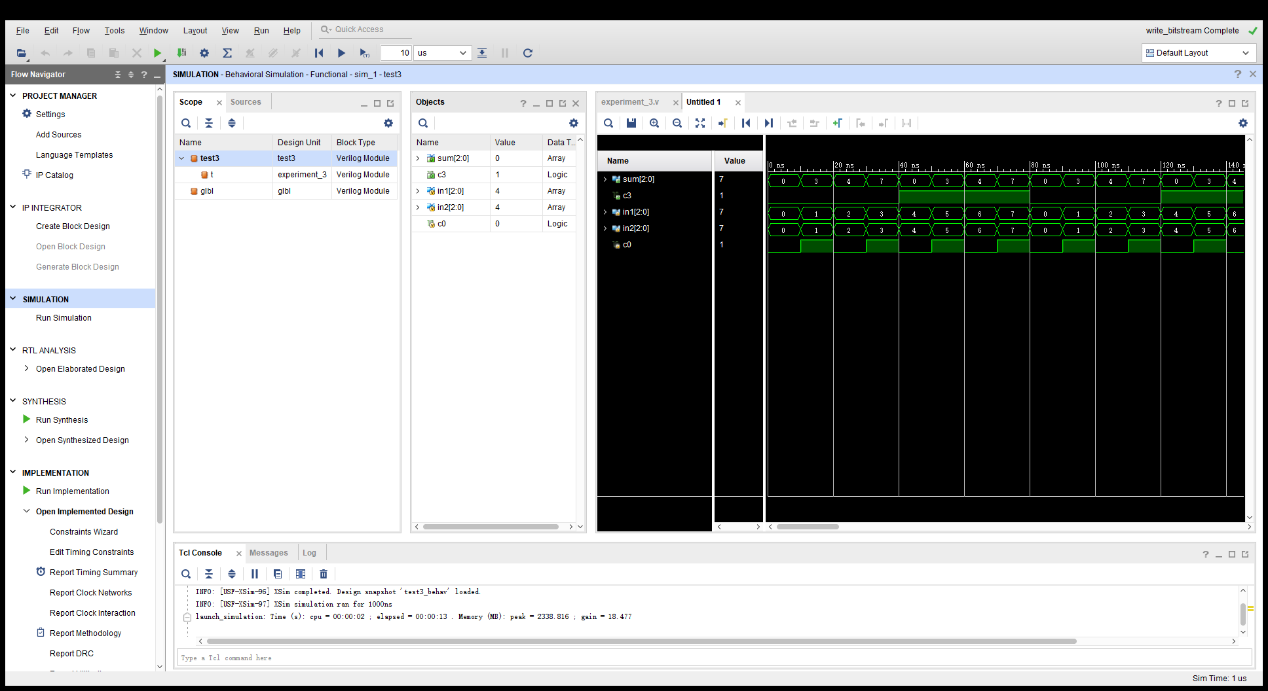
**set\_property PACKAGE\_PIN G4 [get\_ports {sum[2]}]**

**set\_property PACKAGE\_PIN G3 [get\_ports {sum[1]}]**

**set\_property IOSTANDARD LVCMOS33 [get\_ports c3]**

**set\_property PACKAGE\_PIN J4 [get\_ports {sum[0]}]**

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