实验代码：

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 2019/10/14 11:03:51

// Design Name:

// Module Name: project\_2

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module project\_2(

input A,

input B,

output OUT

);

wire temp1,temp2,temp3;

nand(temp1,A,B);

nand(temp2,A,temp1);

nand(temp3,B,temp1);

nand(OUT,temp2,temp3);

endmodule

仿真代码：

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 2019/10/14 11:09:32

// Design Name:

// Module Name: pro2\_test

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module pro2\_test(

output OUT

);

reg[1:0] in;

initial

begin

in=2'b00;

end

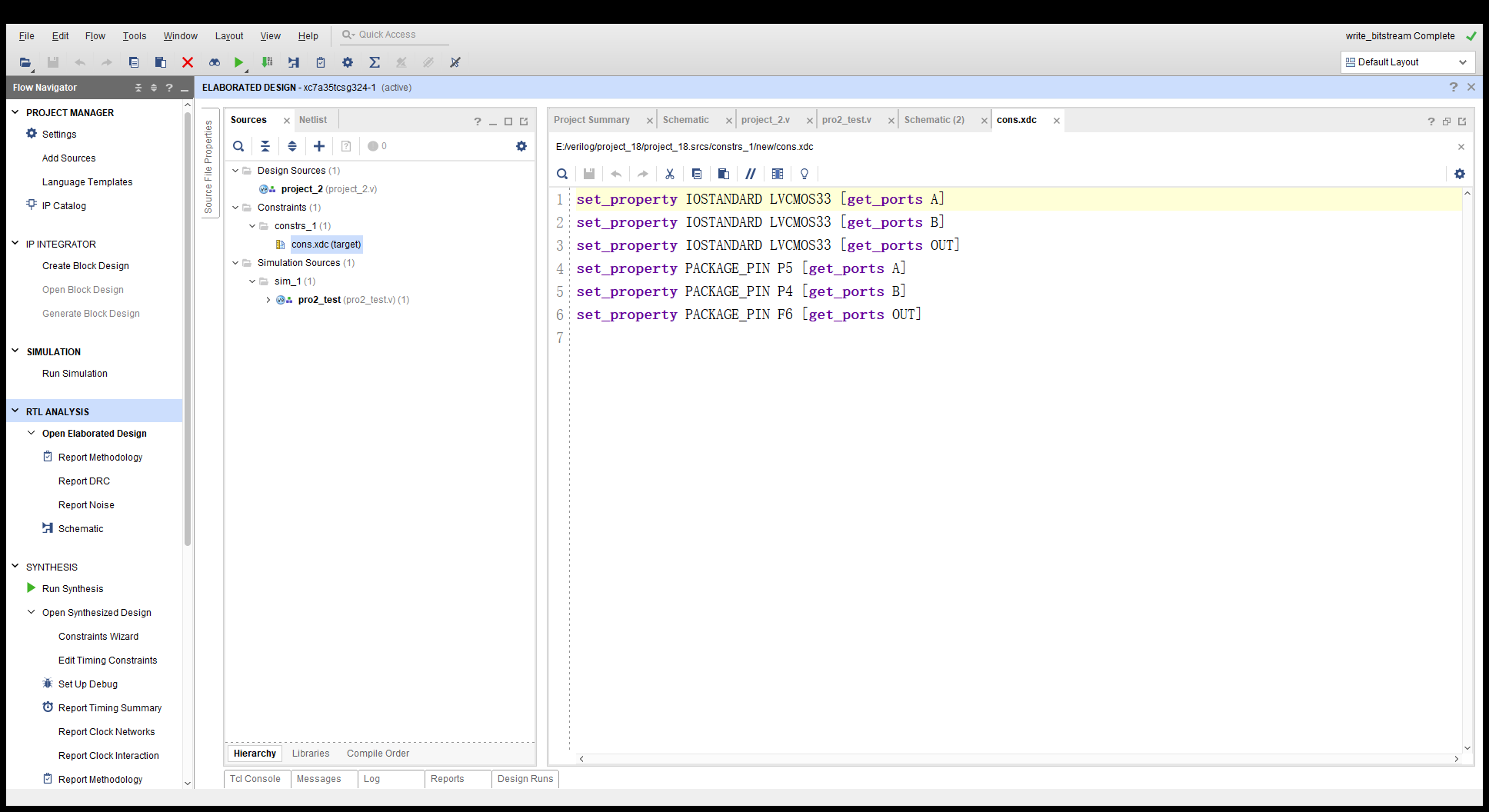
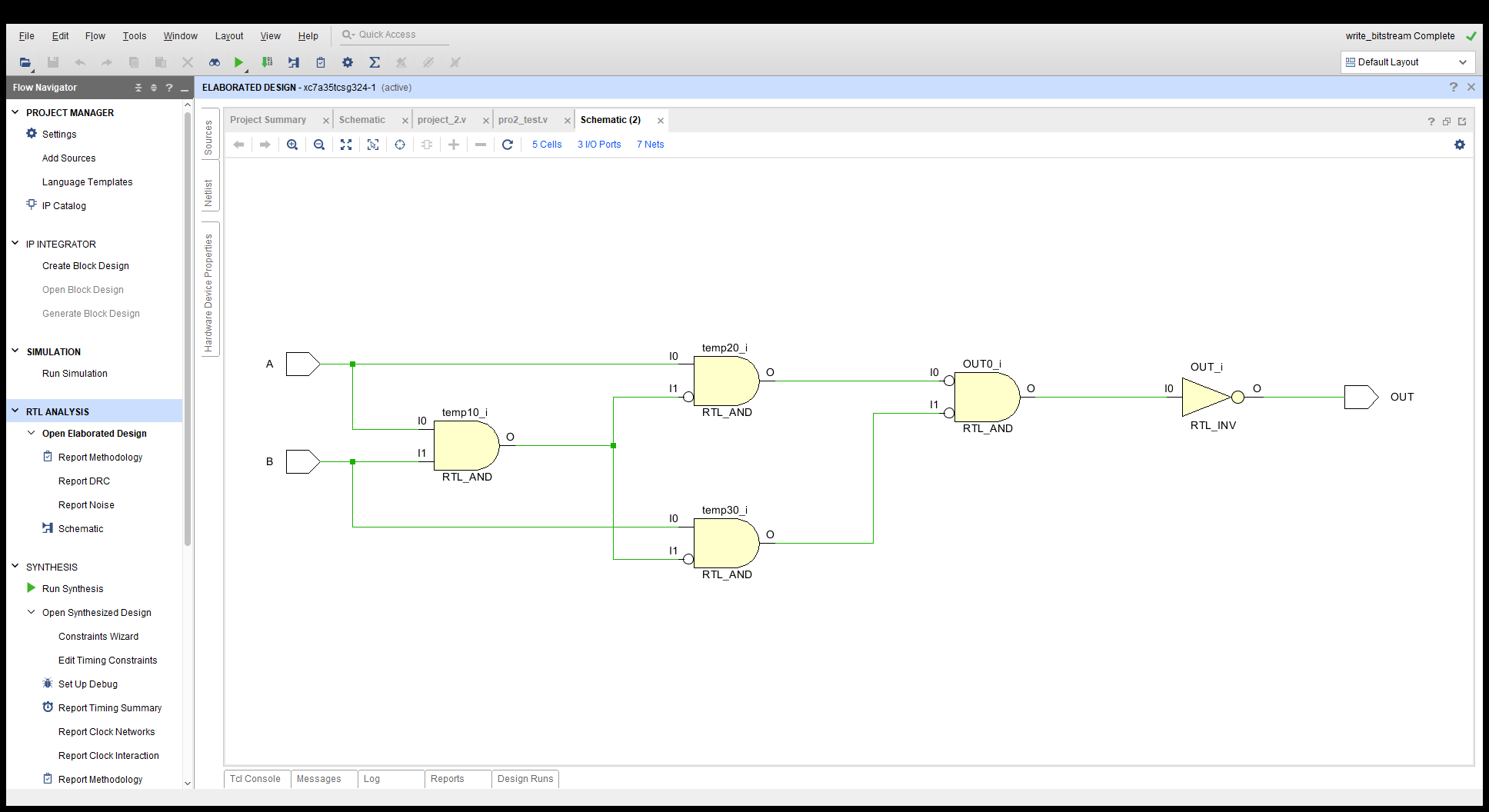
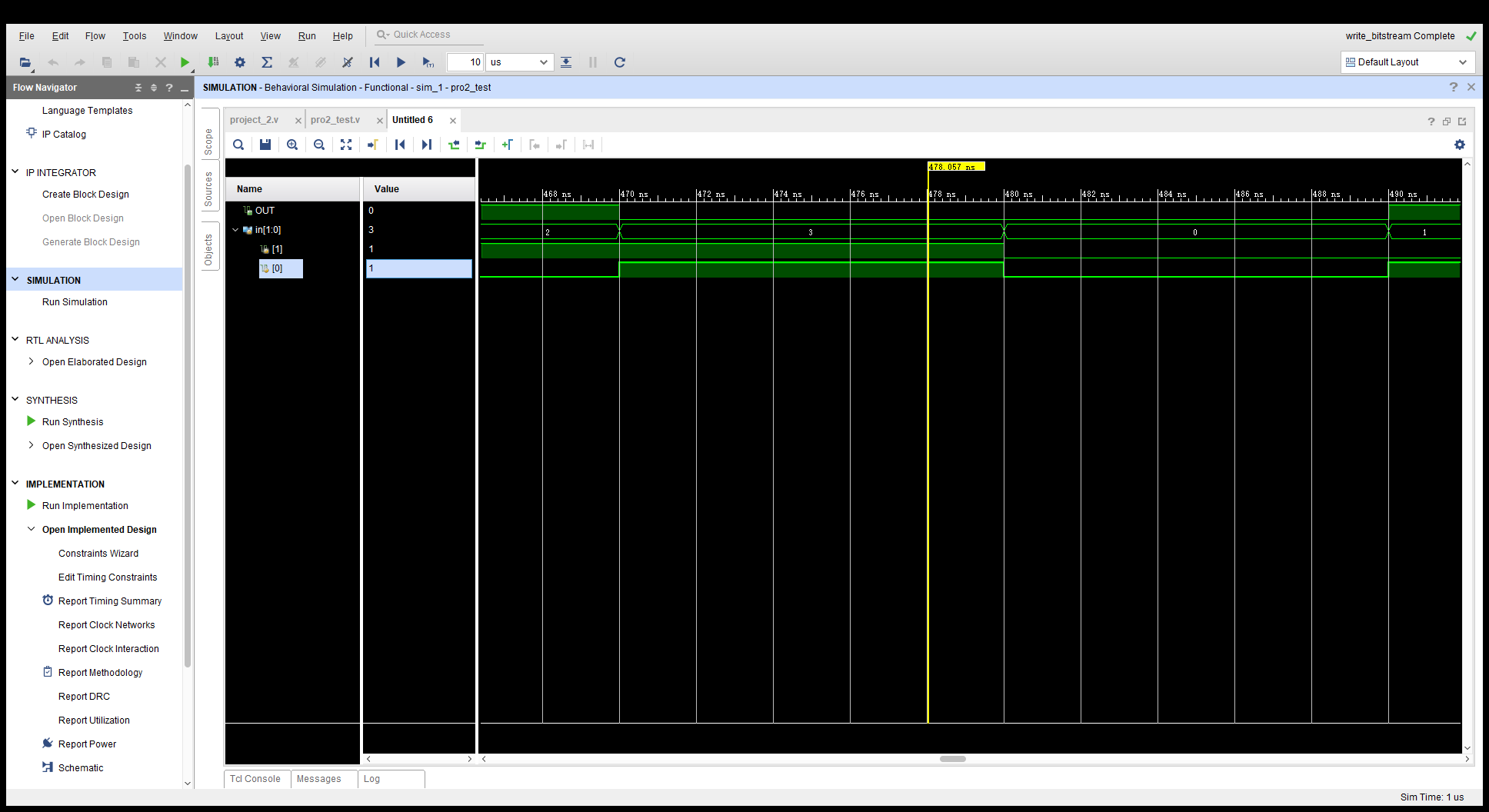
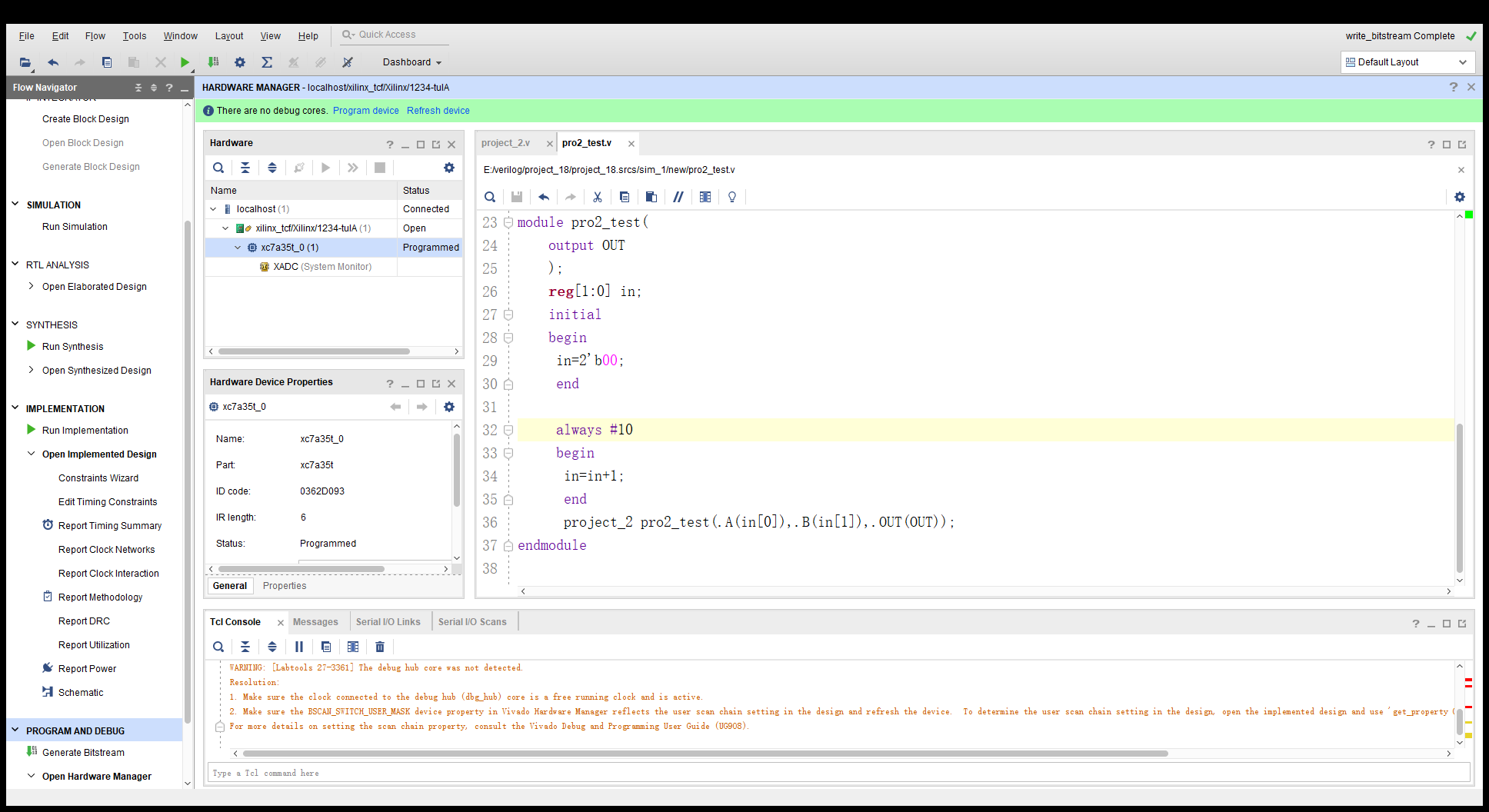
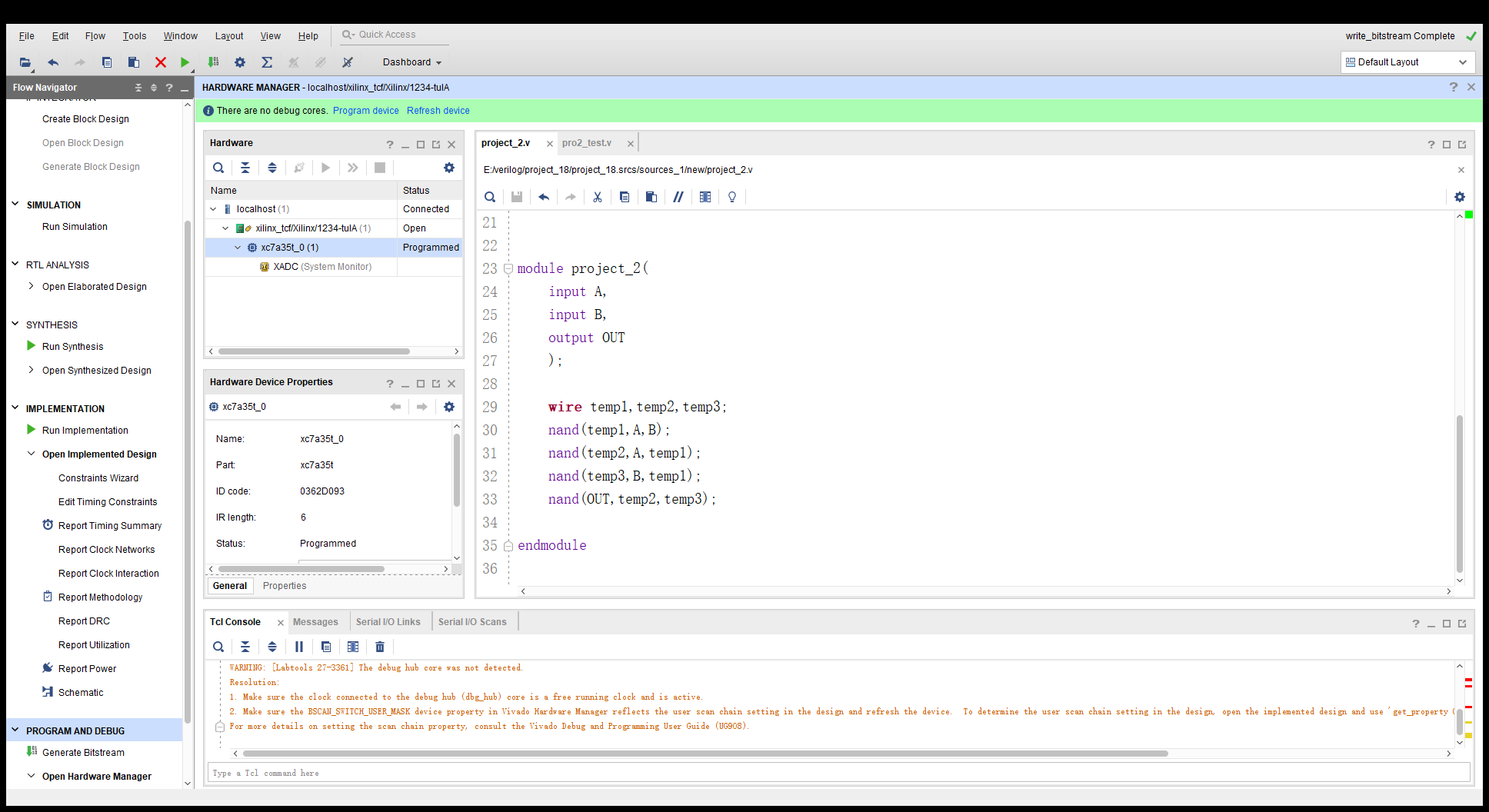
always #10

begin

in=in+1;

end

project\_2 pro2\_test(.A(in[0]),.B(in[1]),.OUT(OUT));



set\_property IOSTANDARD LVCMOS33 [get\_ports A]

set\_property IOSTANDARD LVCMOS33 [get\_ports B]

set\_property IOSTANDARD LVCMOS33 [get\_ports OUT]

set\_property PACKAGE\_PIN P5 [get\_ports A]

set\_property PACKAGE\_PIN P4 [get\_ports B]

set\_property PACKAGE\_PIN F6 [get\_ports OUT]