程序代码

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 2019/11/04 10:39:28

// Design Name:

// Module Name: Compare

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module Compare(

input [1:0] A,

input [1:0] B,

input [2:0] I,

output [2:0] F

);

wire t=((A==B)? 1:0);//确保temp在t为1时生效

wire temp2=t&I[2]&~I[1]&~I[0];

wire temp1=t&~I[2]&I[1]&~I[0];

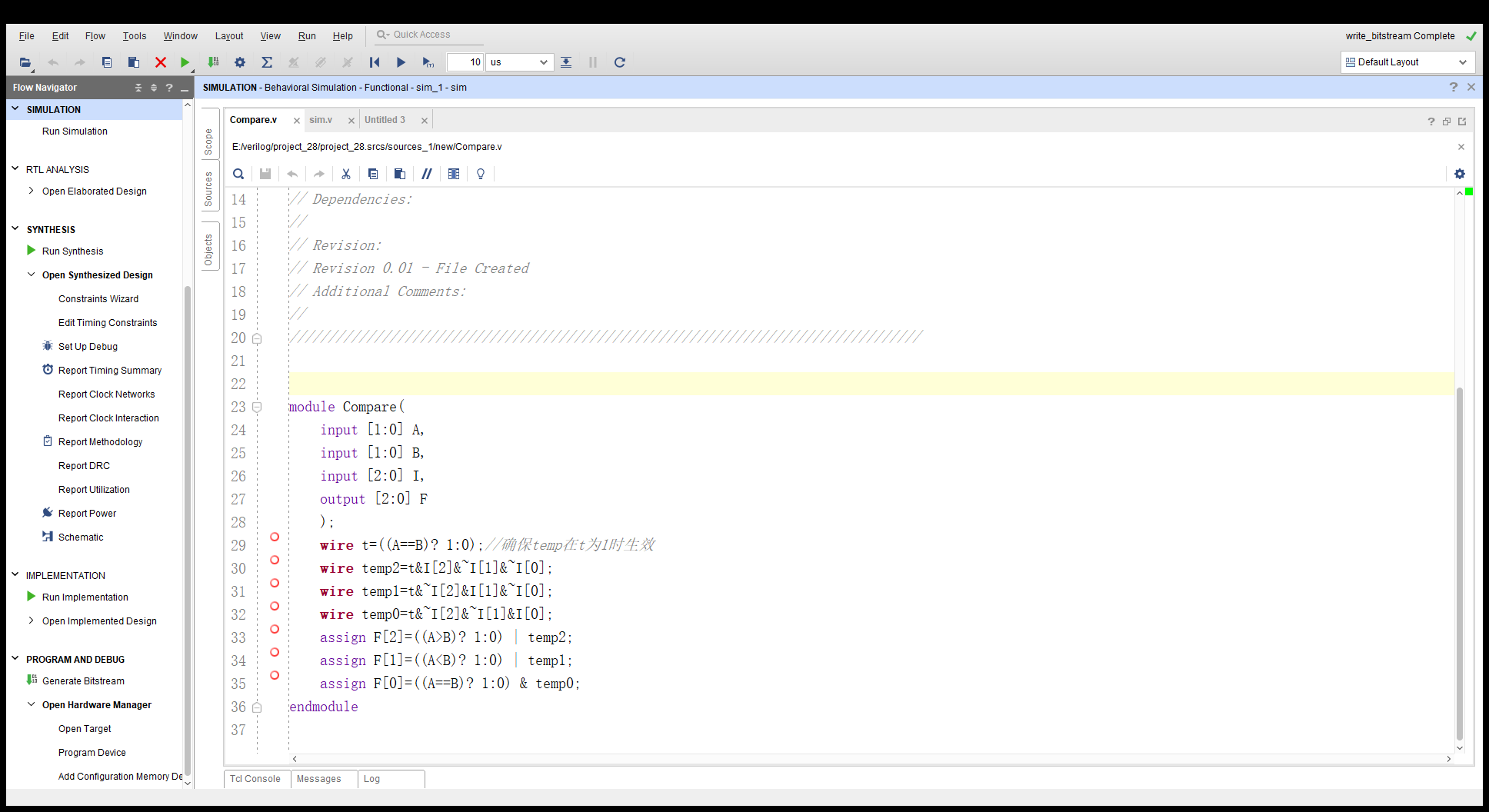
wire temp0=t&~I[2]&~I[1]&I[0];

assign F[2]=((A>B)? 1:0) | temp2;

assign F[1]=((A<B)? 1:0) | temp1;

assign F[0]=((A==B)? 1:0) & temp0;

endmodule



仿真代码

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 2019/11/04 11:06:19

// Design Name:

// Module Name: sim

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module sim(

output [2:0] F

);

reg[1:0] B,A;

reg[2:0] I;

initial

begin

A=2'b00;

B=2'b00;

I=3'b000;

end

always #10

begin

A=A+1;

end

always #40

begin

B=B+1;

end

always #160

begin

I=I+1;

end

Compare sim(B,A,I,F);

Endmodule

约束文件

set\_property IOSTANDARD LVCMOS33 [get\_ports {A[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {A[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {B[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {B[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {F[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {F[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {F[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {I[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {I[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {I[0]}]

set\_property PACKAGE\_PIN P5 [get\_ports {A[1]}]

set\_property PACKAGE\_PIN P4 [get\_ports {A[0]}]

set\_property PACKAGE\_PIN P3 [get\_ports {B[1]}]

set\_property PACKAGE\_PIN P2 [get\_ports {B[0]}]

set\_property PACKAGE\_PIN N4 [get\_ports {I[0]}]

set\_property PACKAGE\_PIN M4 [get\_ports {I[1]}]

set\_property PACKAGE\_PIN R2 [get\_ports {I[2]}]

set\_property PACKAGE\_PIN F6 [get\_ports {F[2]}]

set\_property PACKAGE\_PIN G4 [get\_ports {F[1]}]

set\_property PACKAGE\_PIN G3 [get\_ports {F[0]}]

