源：“

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 2019/11/11 11:38:26

// Design Name:

// Module Name: SevenSegment

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module SevenSegment(

input [3:0] in,

output reg [6:0] out,

output z

);

assign z=1;

always@(in)

case(in)

4'b0000 : out=7'b1111110;

4'b0001 : out=7'b0110000;

4'b0010 : out=7'b1101101;

4'b0011 : out=7'b1111001;

4'b0100 : out=7'b0110011;

4'b0101 : out=7'b1011011;

4'b0110 : out=7'b1011111;

4'b0111 : out=7'b1110000;

4'b1000 : out=7'b1111111;

4'b1001 : out=7'b1111011;

4'b1010 : out=7'b1110111;

4'b1011 : out=7'b0011111;

4'b1100 : out=7'b1001110;

4'b1101 : out=7'b0111101;

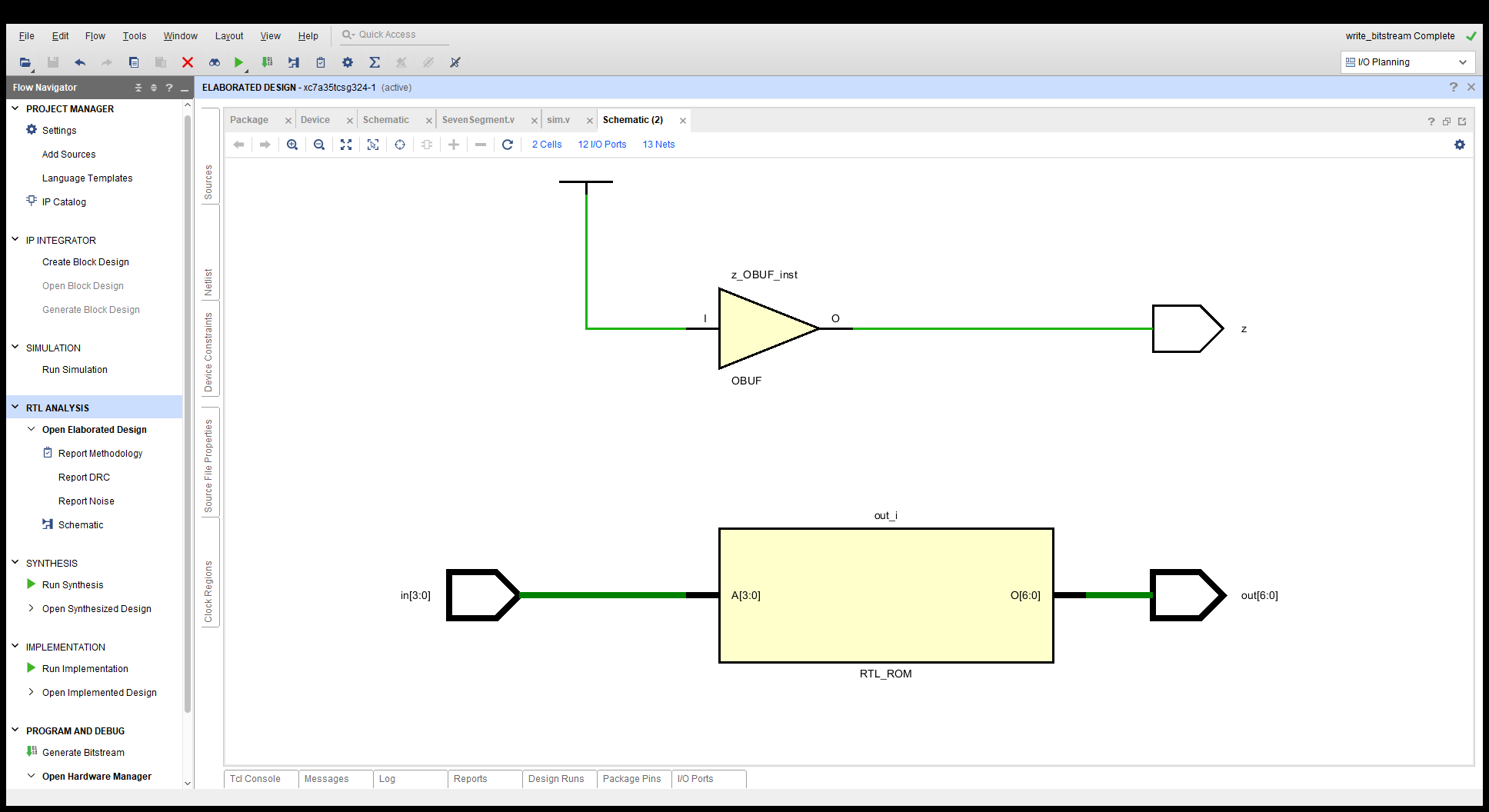
4'b1110 : out=7'b1001111;

4'b1111 : out=7'b1000111;

default : out=7'b1111110;

endcase

endmodule



约束：

set\_property IOSTANDARD LVCMOS33 [get\_ports {in[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {in[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {in[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {in[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {out[6]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {out[5]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {out[4]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {out[3]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {out[2]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {out[1]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports {out[0]}]

set\_property PACKAGE\_PIN R2 [get\_ports {in[3]}]

set\_property PACKAGE\_PIN M4 [get\_ports {in[2]}]

set\_property PACKAGE\_PIN N4 [get\_ports {in[1]}]

set\_property PACKAGE\_PIN R1 [get\_ports {in[0]}]

set\_property PACKAGE\_PIN D4 [get\_ports {out[6]}]

set\_property PACKAGE\_PIN E3 [get\_ports {out[5]}]

set\_property PACKAGE\_PIN D3 [get\_ports {out[4]}]

set\_property PACKAGE\_PIN F4 [get\_ports {out[3]}]

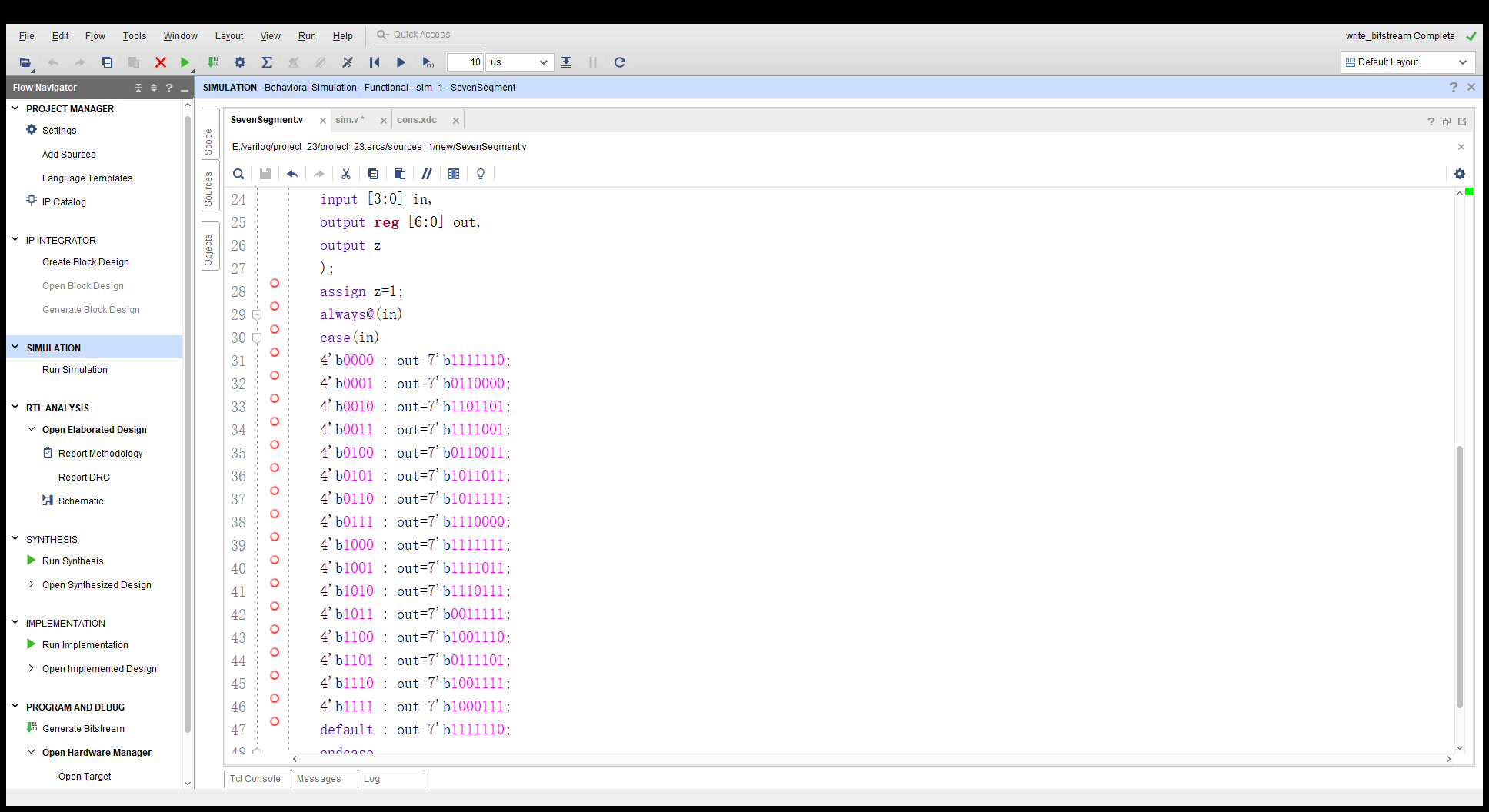
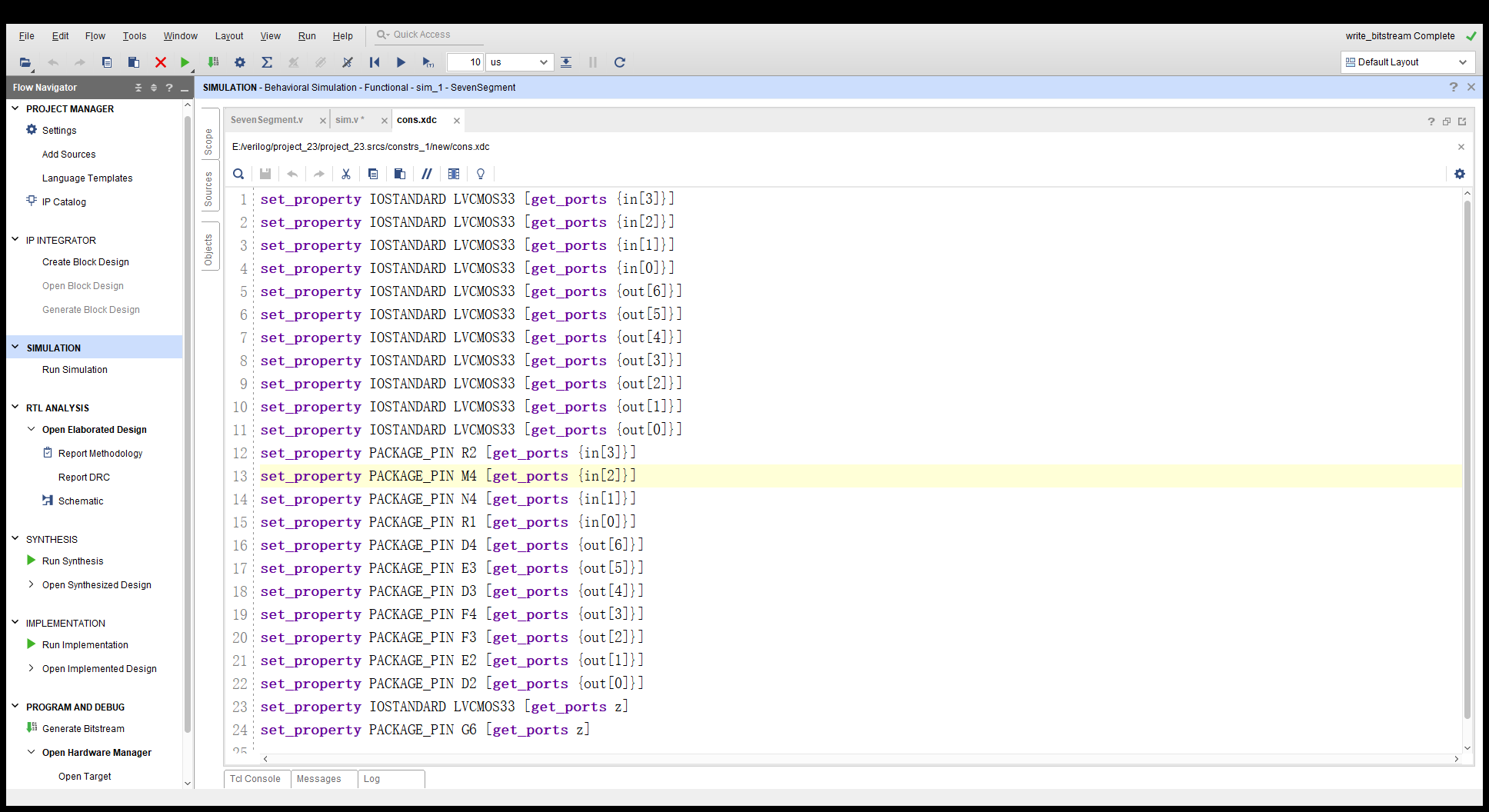
set\_property PACKAGE\_PIN F3 [get\_ports {out[2]}]

set\_property PACKAGE\_PIN E2 [get\_ports {out[1]}]

set\_property PACKAGE\_PIN D2 [get\_ports {out[0]}]

set\_property IOSTANDARD LVCMOS33 [get\_ports z]

set\_property PACKAGE\_PIN G6 [get\_ports z]



仿真：

`timescale 1ns / 1ps

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// Company:

// Engineer:

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// Create Date: 2019/11/18 10:20:14

// Design Name:

// Module Name: sim

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module sim(

output [6:0] out

);

reg [3:0] in;

initial

begin

in=4'b0000;

end

always #10

begin

in=in+1;

end

SevenSegment sim(.in(in),.out(out),.z(z));

endmodule

